A Si/SiC Hybrid Five-Level Active NPC Inverter With Improved Modulation Scheme

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***Abstract*—Compared with full-silicon-carbide (SiC) MOSFET converters, the hybrid utilization of Si/SiC converters is an alternative approach to achieve the tradeoff between performance and cost. In this article, a 2-SiC hybrid five-level active neutral-point-clamped (5L-ANPC) full-bridge inverter is proposed. The proposed inverter is constructed by combining a 2-SiC hybrid 3L-ANPC half-bridge inverter and a two-level half-bridge arm. The operation principle of the proposed inverter by using the conventional modulation scheme is analyzed in detail. Furthermore, a dedicated modulation scheme is proposed to lower the conduction losses. The calculated power losses of the 2-SiC hybrid 5L-ANPC full-bridge inverter with the conventional modulation scheme and the proposed modulation scheme are addressed and compared. The proposed modulation scheme exhibits higher efficiencies under high-power conditions. But the conventional modulation scheme shows efficiency superiority under low-power conditions. Therefore, a hybrid modulation scheme is also proposed to achieve an overall high efficiency performance. A 4-kW prototype is built to evaluate the proposed topology and its modulation scheme at conversion efficiency. Experimental results and analysis show that comparing to the conventional modulation scheme, the hybrid modulation scheme can reduce power loss without increasing the hardware cost.**

***Index Terms*—Five-level active neutral-point-clamped (5L-ANPC), inverter, multilevel inverter, SiC MOSFET, wide-bandgap devices.**

I. Introduction

THE requirements of the future power conversion systems, such as grid-tied inverters for photovoltaic systems, battery chargers for electric vehicles, uninterrupted power supplies for modern data centers, and hybrid-electric propulsion for more electric aircrafts, are high power density and high efficiency [1]–[5]. Therefore, the recent emerging wide bandgap switching devices, such as silicon carbide (SiC), provide an attractive solution to improve conversion efficiency as well as power density, since they feature higher switching speed capability and increased junction operating temperature [6]–[11]. Nevertheless, the price of SiC MOSFET, is still much higher than that of its silicon (Si) counterparts. The price of SiC MOSFET is two times higher than that of Si insulated gate bipolar translator (IGBT) in lower current rating, but it will increase to eight times in a higher current rating [12]. Therefore, the cost performance of full-SiC MOSFET converters, especially for the full-SiC MOSFET multilevel converters, is not excellent. Explorations on leveraging the superior advantages of the SiC MOSFETs while reducing the quantity of SiC MOSFETs to be used in multilevel converters will be of great necessity to lower the hardware cost [13].

A hybrid switch with a high-current main Si IGBT and a low-current auxiliary SiC MOSFET connected in parallel was proposed in recent literatures [14]–[16]. It lowers the switching device cost and overcomes the low power rating limitation of SiC MOSFETs. Unfortunately, there are few of mass-productive Si/SiC hybrid switches in the present market. Circuit-level hybrid utilization of Si and SiC switching devices is attracting increasing attention in both industry and academic area [9], [17]–[22]. A three-level (3L) active neutral-point-clamped (ANPC) rectifier based on a hybrid utilization of SiC MOSFETs and Si active switches was proposed in [9]. Only two SiC MOSFETs (S_5 and S_6) are used in the 3L-ANPC converter, and the remained active switches are still Si MOSFET, as shown in Fig. 1(a). By employing a dedicated modulation scheme, all the high-frequency switching events are moved to the SiC MOSFETs, and the Si active switches are operated at low switching frequency. The maximum efficiency of the 2-SiC hybrid 3L-ANPC rectifier can reach 99% at the switching frequency of 45 kHz. A 4-SiC hybrid 3L-ANPC inverter for aircraft hybrid-electric propulsion systems was developed by General Electric Corporation [17], [18]. It consists of two Si active switches and four SiC MOSFETs, as shown in Fig. 1(b). The maximum efficiency of the 4-SiC hybrid 3L-ANPC inverter can reach 99% at the switching frequency of 20 kHz. Since the power rating of the 4-SiC hybrid 3L-ANPC inverter is megawatt-scale, a modulation strategy with small commutation loops was proposed to avoid large commutation loops [18]. As a result, the voltage overshoot caused by the parasitic inductance of the commutation loops can be reduced.

Manuscript received March 30, 2019; revised July 17, 2019 and September 2, 2019; accepted September 26, 2019. Date of publication September 29, 2019; date of current version February 11, 2020. This work was supported in part by the National Natural Science Foundation of China under Grants 51677054 and 51807176, in part by the 13th Six Talent Peaks Project in Jiangsu Province under Grant XNY-008, and in part by the 111 project under Grant B14022. Recommended for publication by Associate Editor P. Barbosa. (*Corresponding author: Li Zhang.*)

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Digital Object Identifier 10.1109/TPEL.2019.2944688

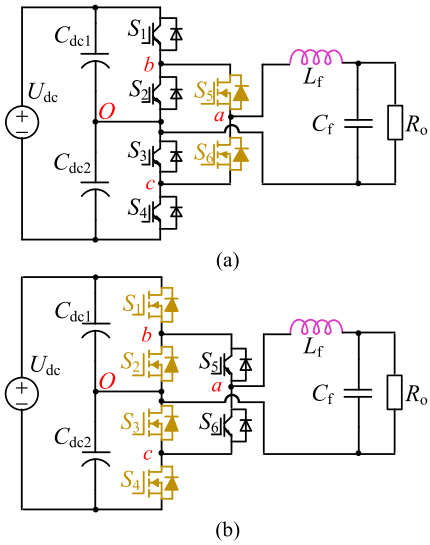

Fig. 1. 3L-ANPC inverters with hybrid Si/SiC switching devices. (a). 2-SiC hybrid 3L-ANPC topology. (b) 4-SiC hybrid 3L-ANPC topology.

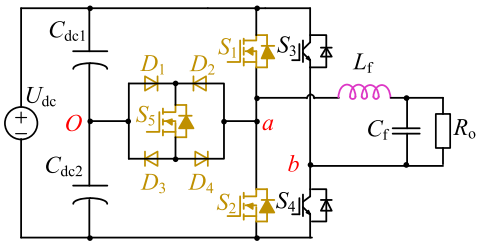

Fig. 2. Simplified 5L-ANPC full-bridge inverter topology.

A transistor clamped five-level (5L) full-bridge inverter was proposed in [23] and [24], which constituted by a neutral-point-clamped bidirectional switch (NPC branch) and an H-bridge inverter. Compared with conventional 5L half-bridge inverter topologies, such as the diode neutral-point-clamped topology and the flying-capacitor-clamped topology, the number of required switching devices is significant reduced with the same output voltage levels. Therefore, the 5L full-bridge inverter has been considered as one of the best solutions for grid-tied inverters [25]–[27]. To improve the efficiency of the 5L full-bridge inverter, SiC MOSFETs and SiC Schottky barrier diodes (SBD) are used in the NPC branch [19], as shown in Fig. 2. Nevertheless, it is well known that the SiC SBD exhibits a high voltage drop, and it leads to a high conduction loss of the freewheeling path from the neutral point (O) to the phase leg midpoint (A). On the other hand, the Si/SiC hybrid 5L full-bridge inverter has three SiC MOSFETs and four SiC SBDs, which also leads to a high hardware cost.

The article is organized as follows. In Section II, a 2-SiC hybrid 5L-ANPC full-bridge inverter is proposed. It is constructed by combining the 2-SiC hybrid 3L-ANPC half-bridge inverter proposed in [9] and a two-level half-bridge arm. The operation principle of the proposed 2-SiC hybrid 5L-ANPC full-bridge inverter with the conventional modulation scheme is analyzed in detail. A modulation scheme is proposed to lower the conduction losses in Section III. In Section IV, the calculated power losses of the 2-SiC hybrid 5L-ANPC full-bridge inverter with the conventional modulation scheme and the proposed modulation scheme are addressed and compared. In Section V, experimental results are presented, and Section VI concludes this article.

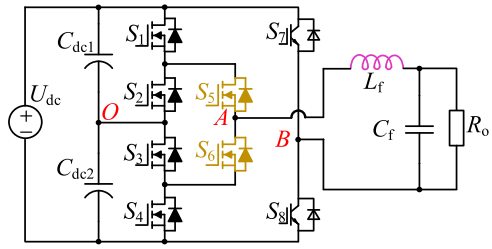

Fig. 3. Topology of the 2-SiC hybrid 5L-ANPC full-bridge inverter.

TABLE I
SWITCHING PATTERNS OF THE SI/SIC HYBRID 5L-ANPC FULL-BRIDGE INVERTER

States	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	u_{AB}
$P2$	1	0	1	0	1	0	0	1	$2E$
$P1a$	1	0	1	0	0	1	0	1	$+E$
$P1b$	0	1	0	1	1	0	0	1	$+E$
$P1c$	0	1	1	0	1	1	0	1	$+E$
$O+$	0	1	0	1	0	1	0	1	0
$O-$	1	0	1	0	1	0	1	0	0
$N1a$	1	0	1	0	0	1	1	0	$-E$
$N1b$	0	1	0	1	1	0	1	0	$-E$
$N1c$	0	1	1	0	1	1	1	0	$-E$
$N2$	0	1	0	1	0	1	1	0	$-2E$

II. TOPOLOGY AND ANALYSIS OF THE 2-SIC HYBRID 5L-ANPC FULL-BRIDGE INVERTERS

A. Topology of the 2-SiC Hybrid 5L-ANPC Full-Bridge Inverter

The topology of the 2-SiC hybrid 5L-ANPC inverter is shown in Fig. 3. The 2-SiC hybrid 5L-ANPC full-bridge inverter is constituted by the 2-SiC hybrid 3L-ANPC half-bridge inverter and a two-level half-bridge arm (S_7 and S_8). Switching patterns of the proposed inverter at each output level are listed in Table I. It can be seen that the output voltage level "E" has three redundant switching states ($P1$a, $P1$b, and $P1$c), and the output voltage level "$-E$" has three redundant switching states ($N1$a, $N1$b, and $N1$c) as well. Therefore, various modulation schemes can be used in the proposed inverter by using different switching states.

B. Switching State Analysis

Based on the modulation scheme presented in [9], the states $P2$, $P1$a, $P1$b, $O+$, $O-$, $N1$a, $N1$b, and $N2$ presented in Table I are used. The conventional modulation waveforms are illustrated in Fig. 4. u_{st} is the carrier signal. u_b represents the peak value of the carrier signal. u_e is the modulation signal. u_{gs1}–u_{gs8} represent

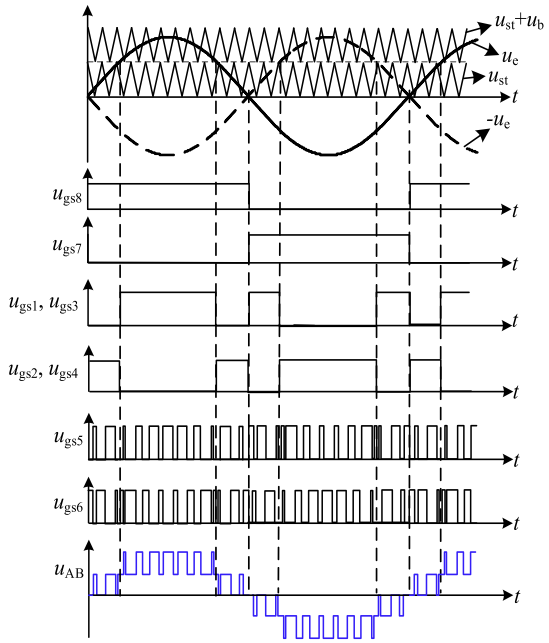

Fig. 4. Waveforms of the conventional modulation schemes.

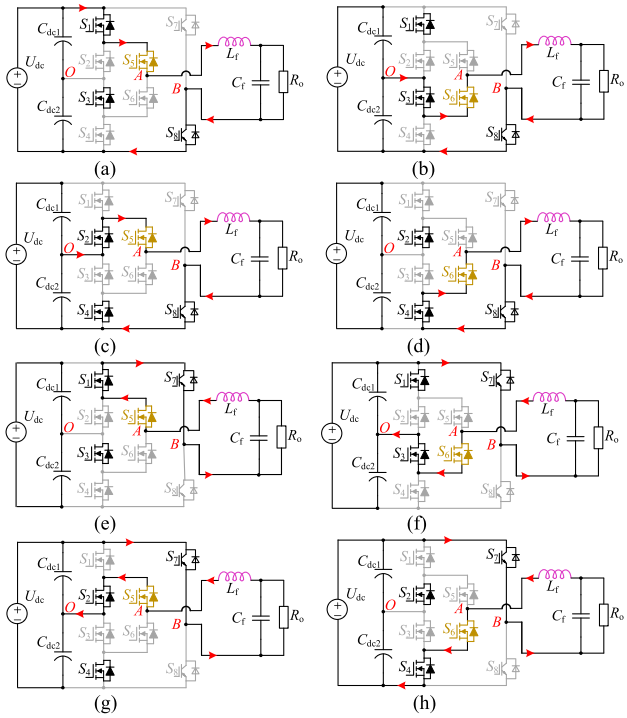

Fig. 5. Equivalent circuits of each switching states. (a) *P*2 state. (b) *P*1a state. (c) *P*1b state. (d) *O*+ state. (e) *O*− state. (f) *N*1b state. (g) *N*1a state. (h) *N*2 state.

the gating signals of the switches S_1–S_8. u_{AB} represents the voltage between terminal *A* and terminal *B*.

It can be seen that IGBT pairs S_7–S_8 are complementarily switching with the fundamental frequency of the ac voltage. Si MOSFET pairs S_1–S_3 and S_2–S_4 always share the same gating signals, respectively. Also, these two Si MOSFET pairs are complementarily switching with the double fundamental frequency. SiC MOSFETs S_5 and S_6 are complementary pairs with the switching frequency. The deadtime should be set between complementary gating signals to avoid the shoot-through issue. With this conventional modulation scheme, the equivalent circuits of each switching state are shown in Fig. 5.

From Fig. 5, it can be seen that all the high-frequency switching events are moved to the SiC MOSFETs S_5 and S_6. Therefore, the switching losses of the 2-SiC hybrid 5L-ANPC full-bridge inverter can be reduced. Since the Si active switches are operated with low frequencies, they only have conduction losses. According to Table I, both the states *P*1c and *N*1c are unused in the conventional modulation scheme. By using the states *P*1c and *N*1c, all the middle active switches (S_2, S_3, S_5, and S_6) are turned on. Therefore, there are two paths for conducting the inductor current, either through S_2 and S_5 or through S_3 and S_6. As a result, the conduction losses can be further reduced.

III. Novel Modulation Strategy With Conduction Loss Optimization

A. Proposed Modulation Scheme

By utilizing all the switching patterns listed in Table I, a modulation scheme for the 2-SiC hybrid 5L-ANPC full-bridge is proposed to lower the conduction losses. The waveforms of the proposed modulation scheme are illustrated in Fig. 6.

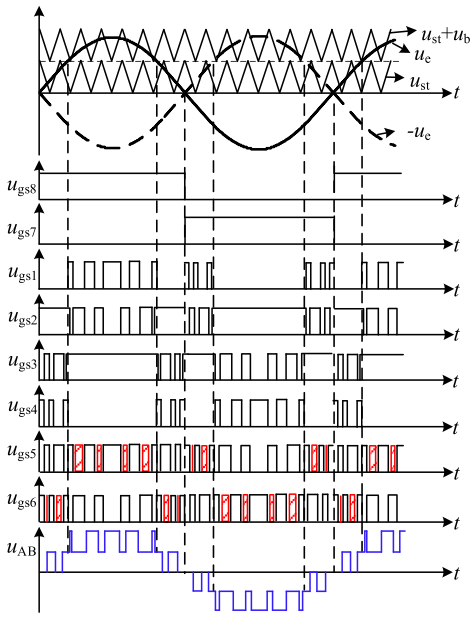

Fig. 6. Waveforms of the proposed modulation strategy.

The positive half-cycle is taken as an example for analysis. During the modulation signal, u_e is lower than the peak value of carrier signal u_b, and the *P*1b state, the *P*1c state, and the *O*+ state are used. Consequently, SiC MOSFET S_6 is operating with twice of the switching frequency. Si MOSFET pairs S_3–S_4 are high-frequency switching complementarity. Si MOSFET S_3

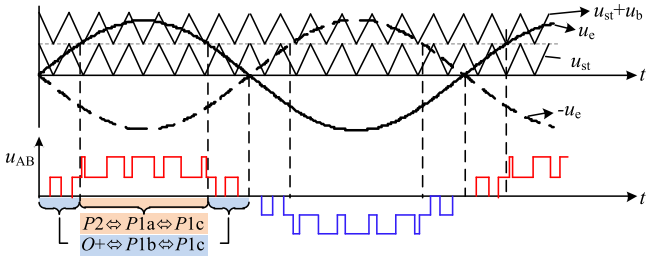

Fig. 7. Switching states sequence at the positive half-cycle.

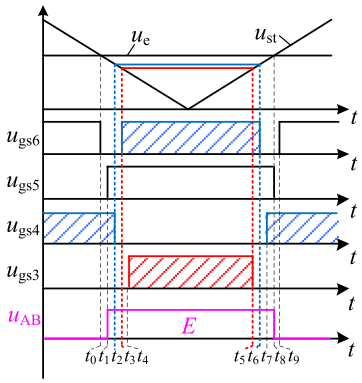

Fig. 8. Detailed waveforms of commutation process between the $O+$ state, the $P1$b state, and the $P1$c state.

and SiC MOSFET S_5 share the same gating signals. During the modulation signal, u_e is higher than the peak value of carrier signal u_b, and the $P1$b state, the $P1$c state, and the $P2$ state are used. Thus, SiC MOSFET S_5 is operating with twice of the switching frequency. Si MOSFET pairs S_1–S_2 are high-frequency switching complementarity. Si MOSFET S_2 and SiC MOSFET S_6 share the same gating signals. The deadtime should be set between complementary gating signals to avoid the shoot-through issue.

The diagram of switching states sequence at the positive half-cycle is shown in Fig. 7. From Fig. 7, it can be seen that the $P1$c state is enabled by employing the proposed modulation scheme. When u_e is lower than u_b, shown as blue shadow, the switching states include the $O+$ state, the $P1$b state, and the $P1$c state. When the u_e is higher than u_b, shown as orange shadow, the switching states include the $P2$ state, the $P1$a state, and the $P1$c state.

B. Switching State and Commutation Analysis Under the Resistive Load Condition

The detailed commutation process waveforms of the $P1$b state, the $P1$c state, and the $O+$ state are shown in Fig. 8. In this duration, S_1 is always OFF, and S_2 is always ON. Therefore, both of them are not depicted in Fig. 8.

The transitions between the $O+$ state and the $P1$b state by using the proposed modulation scheme are the same as the conventional scheme. The inductor current is flowing through S_4, S_6, and S_8 before t_0, as shown in Fig. 9(a). SiC MOSFET S_6 is

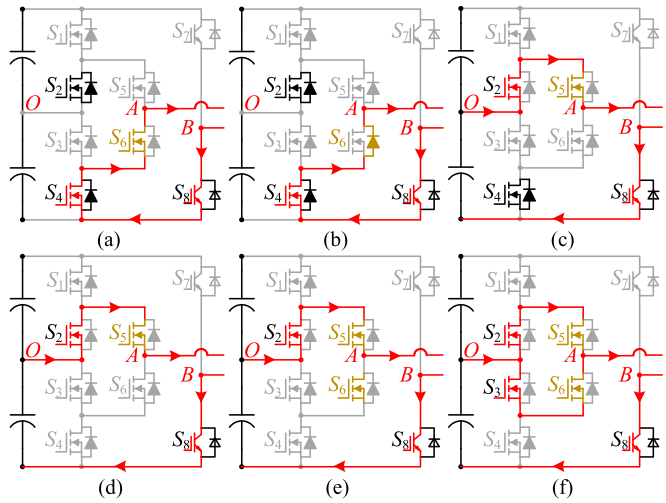

Fig. 9. Demonstration of commutation process among the $P1$b state, the $P1$c state, and the $O+$ state under positive output current condition. (a) Before t_0 and after t_9. (b) Deadtime. (c) t_1–t_2 and t_7–t_8. (d) t_2–t_3 and t_6–t_7. (e) t_3–t_4 and t_5–t_6. (f) t_4–t_5.

turned off at t_0. The turning off of S_6 will force the inductor current to commutate from S_6 channel to its body diode, as displayed in Fig. 9(b). From Fig. 8, SiC MOSFET S_5 is turned on at t_1, and the turning on of S_5 will force the inductor current to commutate from S_4 and the body diode of S_6 to S_2 and S_5, as displayed in Fig. 9(c). Therefore, it creates reverse recovery issues on the body diodes of S_6. However, thanks to the SiC material, the reverse recovery loss is very low. u_{AB} outputs the "E" level, and the off-state voltages of S_3 and S_6 are equal to 0.5 U_{dc}. To further lower the conduction loss, S_3 and S_6 should be turned on. Then, S_4 is turned off at t_2. The equivalent circuit of this switching state is shown in Fig. 9(d). It is worth to mention that the turn-OFF of S_4 is a zero-current switching (ZCS), since there is no current flowing through S_4. SiC MOSFET S_6 is turned on at t_3, as shown in Fig. 9(e). According to the KVL law, the off-state voltage of S_3 is changed from 0.5 U_{dc} to 0, and the off-state voltage of S_4 is changed from 0 to 0.5 U_{dc}. Therefore, it will create turn-ON loss on S_6. Then, S_3 is turned on at t_4, and it is apparently that the turn-ON of S_3 is a zero-voltage switching (ZVS), as shown in Fig. 9(f). As a result, the transition from the $P1$b state to the $P1$c state only creates turn-ON loss on S_6. The turn-ON loss on S_6 consists of the junction capacitor discharging losses of S_3 and S_6 and the junction capacitor charging loss of S_4.

From Fig. 8, S_3 is turned off at t_5. Since S_2, S_5, and S_6 are still turn-ON status, the off-state voltage of S_3 is zero. Thus, the turn-OFF of S_3 is a ZVS. Then, SiC MOSFET S_6 is turned off at t_6, and it is apparently that the turn-OFF of S_6 is a ZCS. S_4 is turned on at t_7. According to the KVL law, both the off-state voltages of S_3 and S_6 are changed from 0 to 0.5 U_{dc}. Therefore, the transition from the $P1$c state to the $P1$b state creates turn-ON loss on S_4. The turn-ON loss on S_4 consists of the junction capacitor charging losses of S_3 and S_6 and the junction capacitor discharging losses of S_4.

From Fig. 8, S_5 is turned off at t_8. The turning off of S_5 will force the inductor current to commutate from S_2 and S_5 to

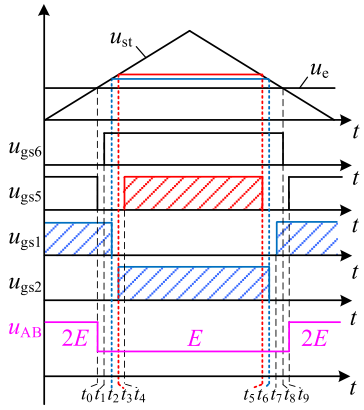

Fig. 10. Detailed waveforms of commutation process between the $P2$ state, the $P1$a state, and the $P1$c state.

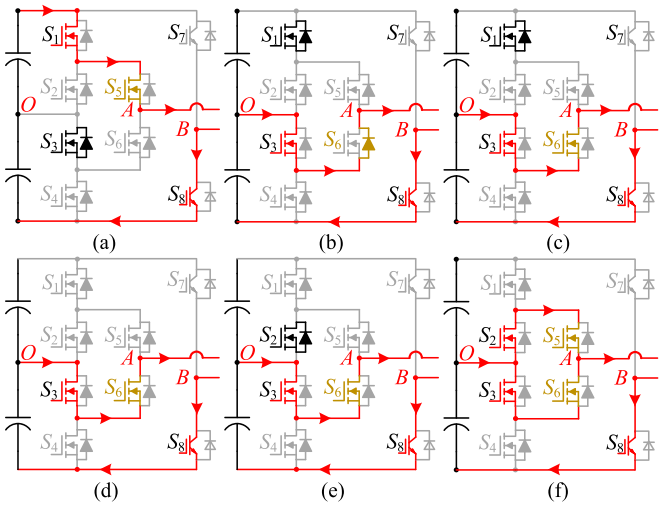

Fig. 11. Demonstration of commutation process among the $P2$ state, the $P1$a state, and the $P1$c state under positive output current condition. (a) Before t_0 and after t_9. (b) Deadtime. (c) t_1–t_2 and t_7–t_8. (d) t_2–t_3 and t_6–t_7. (e) t_3–t_4 and t_5–t_6. (f) t_4–t_5.

S_3 and the body diode of S_6 during the deadtime, as displayed in Fig. 9(b). After the deadtime, S_6 is turned on at t_9, and the turn-ON of S_6 is a ZVS. Therefore, the transition from the $P1$b state to the $O+$ state only creates the turn-OFF loss on S_5.

The detailed commutation process waveforms of the $P1$a state, the $P1$c state, and the $P2$ state are shown in Fig. 10. In this duration, S_4 is always OFF, and S_3 is always ON.

Therefore, both of them are not drawn in Fig. 10. The detailed switching states of commutation process among the $P2$ state, the $P1$a state, and the $P1$c state under resistive load condition are shown in Fig. 11.

From Fig. 11(a), the inductor current is flowing through S_1, S_5, and S_8 before t_0. SiC MOSFET S_5 is turned off at t_1, the turning off of S_5 will force the inductor current to commutate from S_1 and S_5 to S_3 and the body diode of S_6, as displayed in Fig. 11(b). SiC MOSFET S_6 is turned on at t_1, and it is apparently that the turn-ON of S_6 is a ZVS. The equivalent circuit of this switching state is shown in Fig. 11(a). u_{AB} outputs the "E" level, and the off-state voltages of S_2 and S_5 are equal to 0.5 U_{dc}. To further lower the conduction loss, S_2 and S_5 should be turned on. Then, S_1 is turned off at t_2. The equivalent circuit of this switching state is shown in Fig. 11(b). It is worth to mention that the turn-OFF of S_1 is a ZCS, since there is no current flowing through S_1. S_2 is turned on at t_3. The equivalent circuit of this switching state is shown in Fig. 11(c). According to the KVL law, the off-state voltage of S_5 is changed from 0.5 U_{dc} to 0, and the off-state voltage of S_1 is changed from 0 to 0.5 U_{dc}. Therefore, the turn-ON loss on S_2 occurs at t_3. Then, SiC MOSFET S_5 is turned on at t_4, and it is apparently that the turn-ON of S_5 is a ZVS, as shown in Fig. 9(d). As a result, the transition from the $P1$a state to the $P1$c state only creates turn-ON loss on S_2. The turn-ON loss on S_2 consists of the junction capacitor discharging losses of S_2 and S_5 and the junction capacitor charging loss of S_1.

From Fig. 10, SiC MOSFET S_5 is turned off at t_5. Since S_2, S_3, and S_6 are still turn-ON status, the off-state voltage of S_5 is zero. Thus, the turn-OFF of the switch S_5 is a ZVS. Then, S_2 is turned off at t_6, and it is apparently that the turn-OFF of the switch S_2 is a ZCS. S_1 is turned on at t_7. According to the KVL law, both the off-state voltages of S_2 and S_5 are changed from 0 to 0.5 U_{dc}. Therefore, the transition from the $P1$c state to the $P1$a state creates turn-ON loss on S_1. The turn-ON loss on S_1 consists of the junction capacitor charging losses of S_2 and S_5, the junction capacitor discharging loss of S_1.

From Fig. 10, S_6 is turned off at t_8. The turning off of S_6 will force the inductor current to commutate from S_6 channel to its body diode, as displayed in Fig. 11(b). After the deadtime, S_5 is turned on at t_9, and it will create reverse recovery issues on the body diodes of S_6. However, thanks to the SiC material, the reverse recovery loss is very low.

Based on the analysis mentioned above, there are no reverse recovery issues of S_1–S_4 during the deadtime under the resistive load condition. Most of the switching events are moved to SiC MOSFETs.

C. Switching State and Commutation Analysis Under the Inductive Load Condition

The commutation process of the $P1$b state, the $P1$c state, and the $O+$ state under the inductive load condition is shown in Fig. 12. The commutation process of the $P2$ state, the $P1$a state, and the $P1$c state under inductive load condition is shown in Fig. 13.

The detailed analysis under the inductive load condition is almost the same as that presented in Section III.B, which is not described here. However, from Figs. 12 and 13, it can be seen that there are no reverse recovery issues of S_1 to S_4 during the deadtime under the inductive load condition as well.

From the abovementioned analysis, it can be concluded that when u_{AB} outputs the "E" level and the "$-E$" level, all the middle switches are turned on by using the proposed modulation scheme, and the conduction losses can be reduced. However, the switching losses of the transition between the $P1$a state and the $P1$c state, as well as the switching losses of the transition between the $P1$b state and the $P1$c state, are increased. To achieve

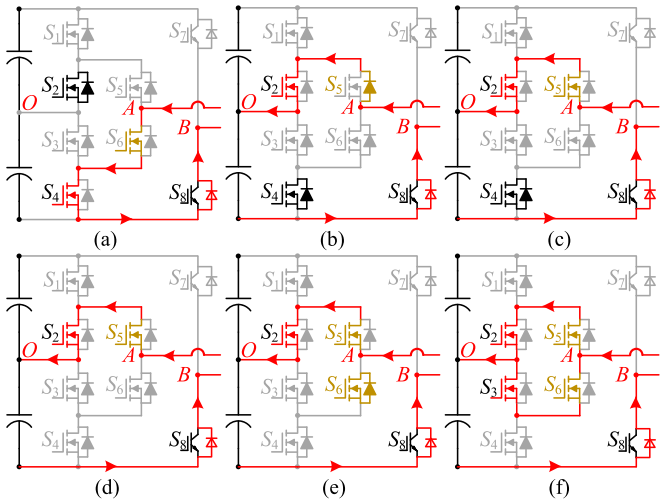

Fig. 12. Demonstration of commutation process among the $P1$b state, the $P1$c state, and the O+ state under negative output current condition. (a) Before t_0 and after t_9. (b) Deadtime. (c) t_1–t_2 and t_7–t_8. (d) t_2–t_3 and t_6–t_7. (e) t_3–t_4 and t_5–t_6. (f) t_4–t_5.

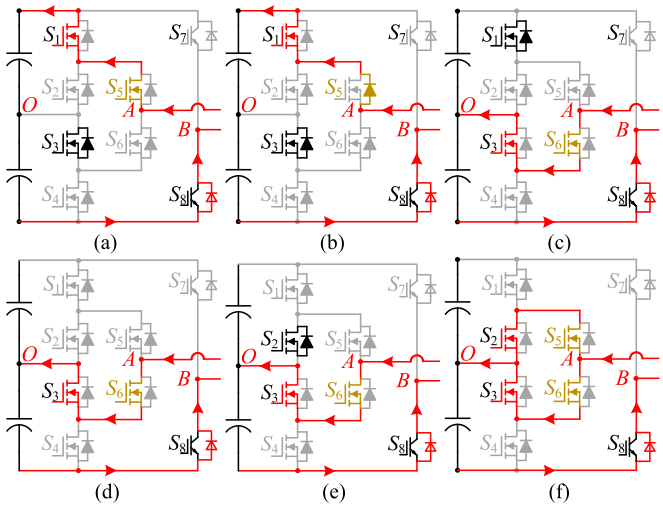

Fig. 13. Demonstration of commutation process among the $P2$ state, the $P1$a state, and the $P1$c state under negative output current condition. (a) Before t_0 and after t_9. (b) Deadtime. (c). t_1–t_2 and t_7–t_8. (d) t_2–t_3 and t_6–t_7. (e) t_3–t_4 and t_5–t_6. (f) t_4–t_5.

the efficiency improvement, the decreased conduction losses should be higher than the increased switching losses.

IV. Loss Analysis of the Novel Modulation Scheme

The conduction energy loss expressions of Si MOSFET and SiC MOSFET are the same. For each switching cycle, it can be described as follows:

$$W_{\text{on-state}}(t) = i^2(t) R_{\text{DS(on)}} t_{\text{on}}(t) \tag{1}$$

where $R_{\text{DS(on)}}$ represents the ON-state resistance, which can be extracted from Si MOSFET and SiC MOSFET datasheets, respectively. $t_{\text{on}}(t)$ represents the ON-state time.

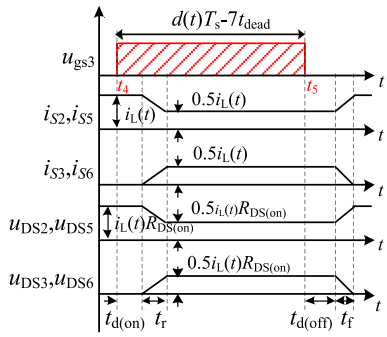

Fig. 14. Switching process of S_3.

The transition between the $P1$b state and the $P1$c state is taken as an example for analysis. From the analysis presented in Section III, the conduction losses can be reduced by the proposed modulation scheme during the ON-state time of S_3. The switching process of S_3 and the inductor current waveforms are illustrated in Fig. 14, where $d(t)$ represents the duty cycle, T_s represents the switching period. t_{dead} represents the deadtime that is set to ensure the reliable actions of active switches. Moreover, $t_{d(\text{on})}$, t_r, $t_{d(\text{off})}$, and t_f represent the turn-ON delay time, the rise time, the turn-OFF delay time, and the fall time, respectively. All of these parameters can be extracted from the switching device datasheet.

From Fig. 14, it can be seen that the duration of the gating signal of S_3 is equal to $(d(t)T_s - 7t_{\text{dead}})$. The total of deadtime includes one transition from the $O+$ state to the $P1$b state, three transitions from the $P1$b state to the $P1$c state, and three transitions from the $P1$c state to the $P1$b state. Consequently, the ON-state time of S_3 is expressed as follows:

$$t_{S3(\text{on})} = d(t)T_s - 7t_{\text{dead}} - t_{d(\text{on})} + t_{d(\text{off})} + t_f. \tag{2}$$

It is worth to mention that $t_{\text{S3(on)}}$ should be larger than zero. In other words, the proposed modulation scheme is not available when the ON-state time of S_3 is shorter than the total deadtime. The conduction energy loss can be calculated as follows:

$$W_{\text{on-state(new)}}(t) = 0.5 i_L^2(t) \left(R_{\text{Si.DS(on)}} + R_{\text{SiC.DS(on)}}\right) \times \left(d(t)T_s - 7t_{\text{dead}} - t_{d(\text{on})} + \frac{1}{3}t_r + t_{d(\text{off})} + \frac{4}{3}t_f\right). \tag{3}$$

The detailed derivation of (3) is shown in (4) as shown at the bottom of next page. The conduction energy loss during this switching process by using the conventional modulation scheme is calculated as follows:

$$W_{\text{on-state(old)}}(t) = i_L^2(t) \left(R_{\text{Si.DS(on)}} + R_{\text{SiC.DS(on)}}\right) \times \left(d(t)T_s - 7t_{\text{dead}} - t_{d(\text{on})} + t_{d(\text{off})} + t_f\right). \tag{5}$$

In the same way, the decreased conduction energy losses of $P1$a and $P1$c in one switching period can be deduced. Based on the analysis mentioned in Section III, the switching energy losses are increased by the proposed modulation scheme. The

transition between the $P1$b state and the $P1$c state is still taken as an example for analysis. The turn-ON loss on S_6 consists of the junction capacitor discharging losses of S_3 and S_6 and the junction capacitor charging loss of S_4. The turn-ON loss on S_4 consists of the junction capacitor charging losses of S_3 and S_6 and the junction capacitor discharging losses of S_4. Therefore, in one switching period, two Si MOFSETs and one SiC MOSFET have charging and discharging energy losses of junction capacitors. The increased energy losses in one switching period can be calculated as follows:

$$W_{C\text{oss}}(t) = 2 \times (2E_{\text{Si.oss}} + E_{\text{SiC.oss}}) \tag{6}$$

where $E_{\text{Si.oss}}$ and $E_{\text{SiC.oss}}$ represent the junction capacitor energy losses of Si MOSFET and SiC MOSFET, respectively, which can be extracted from their datasheets as well.

Compared with the conventional modulation scheme, the decreased conduction energy losses and the increased switching energy losses by the proposed modulation scheme during the positive half-cycle are depicted in Fig. 15, where $W_{\text{i}}(t)$ represents the decreased conduction energy losses and is equal to $(W_{\text{on-state(old)}}(t) - W_{\text{on-state(new)}}(t))$. The conditions used for analysis and calculations are the same as the parameters listed in Table II.

The junction capacitor energy losses depend on their drain–source voltages. Therefore, the values of $W_{C\text{oss}}$ with different drain–source voltages can be extracted from Si MOSFET and SiC MOSFET datasheets. In Fig. 15(a), $W_{C\text{oss}}$ shows a constant value with a fixed dc-link voltage. It is clear that when the output power is 1 kW, the reduced conduction energy losses are not significant. After the inverter outputs higher power, the reduced conduction energy losses become larger. It indicates that compared with the conventional modulation scheme, the proposed modulation scheme exhibits better efficiencies under high power conditions.

In Fig. 15(b), $W_{C\text{oss}}$ shows different values with different dc-link voltages at the fixed output power. It can be seen that the conduction energy losses in one switching period are definitely reduced with different dc-link voltages at the 4 kW output power. The reduced conduction energy losses reach the maximum value at the 580 V dc-link voltage. When the dc-link voltage is higher, such as 700 V, the durations of the "E" level and the "$-E$" level are shorter. Thus, the reduced conduction energy losses become smaller. It indicates that compared with the conventional control scheme, the proposed modulation scheme can achieve better efficiencies under high modulation indices. Furthermore, the durations of the "E" level (as well as the "$-E$" level) has a relationship with the inductor current, which is illustrated in Fig. 16. It is clear that part of duty cycles are positive proportional to the inductor current, and the duty cycle is larger than 0.5 at the high inductor current. As a result, the proposed scheme can be used to achieve better efficiencies for most of switching cycles.

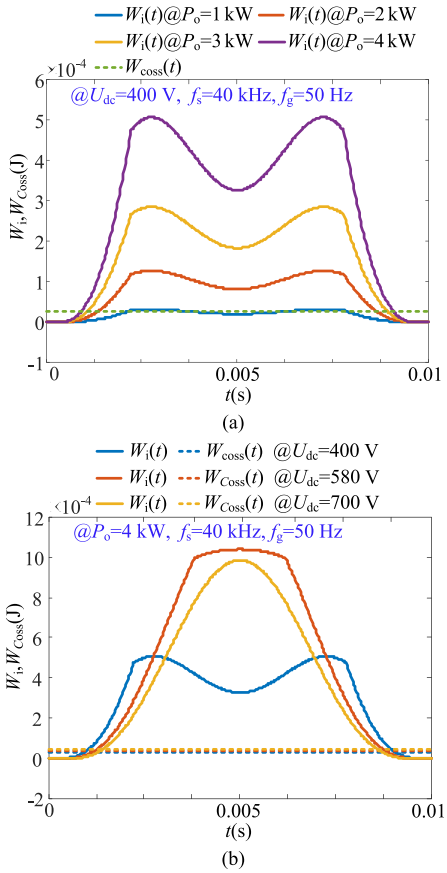

Fig. 15. Calculated energy losses in one switching period during the positive half-cycle. (a) Calculation results associated with different output power rates at the 400 V dc-link voltage. (b) Calculation results associated with different dc-link voltages at the 4 kW output power.

$$\begin{aligned}
W_{\text{on-state(new)}}(t) &= 0.5i_L^2(t)\left(R_{\text{Si.DS(on)}} + R_{\text{SiC.DS(on)}}\right)\left(d(t)T_s - 7t_{\text{dead}} - t_{d(\text{on})} - t_r + t_{d(\text{off})}\right) \\
&+ \int_0^{t_r}\left[\left(0.5i_L(t) + 0.5i_L(t)\frac{t}{t_r}\right)^2 + \left(0.5i_L(t)\frac{t}{t_r}\right)^2\right]\left(R_{\text{Si.DS(on)}} + R_{\text{SiC.DS(on)}}\right)dt \\
&+ \int_0^{t_f}\left[\left(0.5i_L(t) + 0.5i_L(t)\frac{t}{t_f}\right)^2 + \left(0.5i_L(t)\frac{t}{t_f}\right)^2\right]\left(R_{\text{Si.DS(on)}} + R_{\text{SiC.DS(on)}}\right)\text{d}t \\
&= i_L^2(t)\left(R_{\text{Si.DS(on)}} + R_{\text{SiC.DS(on)}}\right)\left(\frac{1}{2}d(t)T_s - \frac{7}{2}t_{\text{dead}} - \frac{1}{2}t_{d(\text{on})} + \frac{1}{6}t_r + \frac{1}{2}t_{d(\text{off})} + \frac{2}{3}t_f\right) \\
&= 0.5i_L^2(t)\left(R_{\text{Si.DS(on)}} + R_{\text{SiC.DS(on)}}\right)\left(d(t)T_s - 7t_{\text{dead}} - td_{(\text{on})} + t_{d(\text{off})} + \frac{1}{3}t_r + \frac{4}{3}t_f\right)
\end{aligned} \tag{4}$$

TABLE II
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameter	Value
DC-link voltage	400~700 V
Output voltage/ frequency	220 V/ 50 Hz
Rated power	4 kW
Switching frequency	40 kHz
Filter inductor L_f	1.4 mH
Filter capacitor C_f	4.7 uF
Si IGBT (S_7, S_8)	IRG4PH40UD2-E U_{ce}=2.4V(@T_j=150℃, I_C=20 A)
Si MOSFET (S_1 to S_4)	IPW60R099C6 $R_{ds(on)}$=160 mΩ (@T_j=125℃, I_D=20 A)
SiC MOSFET (S_5, S_6)	ROHM-SCT3080AL $R_{ds(on)}$=105 mΩ (@T_j=125℃, I_D=20 A)

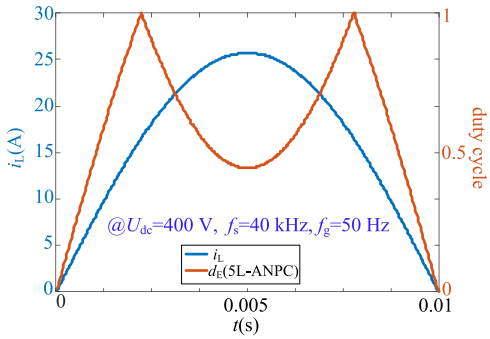

Fig. 16. Relationship between the duty cycle and the inductor current.

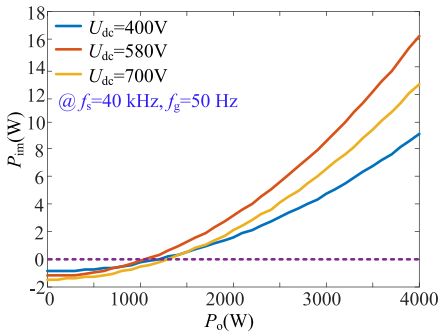

Fig. 17. Theoretical calculation results of the power loss optimization by using the proposed scheme.

The theoretical calculation results of the power loss optimization with different dc-link voltages and different output powers are shown in Fig. 17, where $P_{\rm im}$ represents the reduced power loss, and $P_{\rm im}$ is calculated as follows, (7) as shown at the bottom of this page, where T_g represents the fundamental period. $W_{\rm im}(t)$ represents the optimized energy loss in one switching cycle and is calculated as follows:

$$W_{\rm im}(t) = W_{\rm on-state(old)}(t) - W_{\rm on-state(new)}(t) - W_{Coss}(t). \tag{8}$$

It indicates that when $P_{\rm im}$ is higher than zero, the efficiency of the proposed inverter can be enhanced by the proposed modulation scheme. On the contrary, the efficiency of the conventional modulation scheme is higher than that of the proposed modulation scheme. Thus, there is a tradeoff between the reduced conduction losses and the increased switching losses. Thus, when the output power is lower than the half rated power, the conventional modulation scheme is still enabled. When the output power is higher than the half rated power, the proposed modulation scheme is used. As a result, a hybrid modulation scheme is proposed to enhance the overall efficiency.

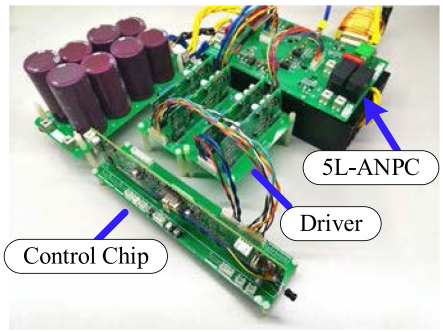

Fig. 18. Prototype of the 2-SiC hybrid 5L-ANPC full-bridge inverter.

V. EXPERIMENTAL RESULTS

A 4-kW 2-SiC hybrid 5L-ANPC full-bridge inverter prototype was built to verify the validity of the proposed topology and the modulation scheme. The experimental prototype is shown in Fig. 18. The specifications of the prototype are listed in Table II. A power analyzer WT1800 was used to test the efficiency. The deadtime between complementary gating signals is set as 0.6 μs. On the other hand, the total prices of the Si/SiC hybrid 5L T-type full-bridge inverter (shown in Fig. 2) and the proposed 2-SiC hybrid 5L-ANPC full-bridge inverter are given. The detailed prices of switching devices are listed in Table III.

According to Table III, it is clear that the Si/SiC hybrid 5L-T-type full-bridge is the expensive one. The total price of the proposed 2-SiC hybrid 5L-ANPC full-bridge inverter has been decreased by 50%.

The detailed switching process of the novel modulation scheme, when u_{AB} outputs between the "E" level and the "0" level, is shown in Fig. 19. Where $u_{\rm gs1}$–$u_{\rm gs6}$ represent the

$$P_{\rm im} = \frac{4\left[\sum_{t=1}^{\arcsin\left(\frac{1}{2\sqrt{2}m}\right)\frac{2f_s}{\pi f_g}} W_{\rm im}(t) + \sum_{t=\arcsin\left(\frac{1}{2\sqrt{2}m}\right)\frac{2f_s}{\pi f_g}+1}^{\frac{f_s}{f_g}} W_{\rm im}(t)\right]}{T_{\rm g}} \tag{7}$$

TABLE III
SELECTED SWITCHING DEVICES FOR COMPARISON AND TOTAL PRICE OF INVERTERS

Items	5L-T-type [19] (USD)*(@www.digikey.com)*	5L-ANPC
SiC MOSFET	3×16.75 (ROHM-SCT3080KLGC11)	2×8.92
SiC diode	4×10.62 (ROHM-SCS230AE2HRC)	0
Si MOSFET	0	4×5.81
Si IGBT	2×4.64 (same as 5L-ANPC)	2×4.64
Total Cost (USD)	102.01	50.36

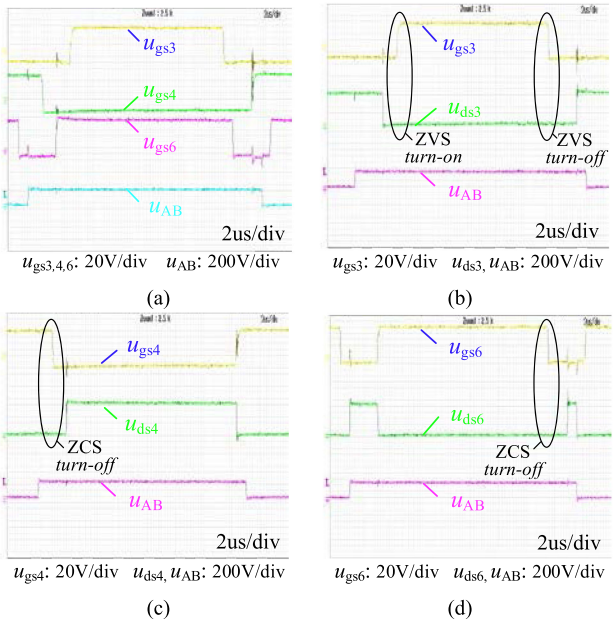

Fig. 19. Detailed waveforms of switching process between "*E*" level and "0" level. (a) Gating signals of S_3, S_4, and S_6. (b) Turn-ON/turn-OFF waveforms of S_3. (c) Turn-ON/turn-OFF waveforms of S_4. (d) Turn-ON/turn-OFF waveforms of S_6.

gating signals of S_1–S_6, respectively. u_{ds1}–u_{ds6} represent the drain–source voltages of S_1–S_6, respectively.

From Fig. 19(a), it can be seen that, u_{AB} outputs between the "*E*" level and the "0" level. Si MOSFET pairs S_3–S_4 are complementarily switching, and the deadtime is set between them to avoid the shoot-through issue. From Fig. 19(b), it is obviously that turn-ON and turn-OFF of S_3 are soft switching during the switching process of the *P*1b state and the *P*1c state. From Fig. 19(c), it can be seen that the turn-OFF of S_4 is a soft switching, but the turn-ON of S_4 is a hard switching. Because when S_4 is turned on, the drain–source voltages of S_3 and S_6 are changed from 0 to 0.5 U_{dc}, and the drain–source voltage of S_4 is changed from 0.5 U_{dc} to 0. Therefore, the turn-ON loss of S_4 involves the charging and discharging losses of junction capacitors of S_3, S_4, and S_6. From Fig. 19(d), it can be seen that the turn-OFF of S_6 is a soft switching, but the turn-ON of S_6 is a hard switching. Because when S_6 is turned on, the drain–source voltages of S_3 and S_6 are changed from 0.5 U_{dc} to 0, and the drain–source voltage of S_4 is changed from 0 to 0.5 U_{dc}. It indicates that the turn-ON loss of S_6 involves the charging and discharging losses of junction capacitors of S_3, S_4, and S_6.

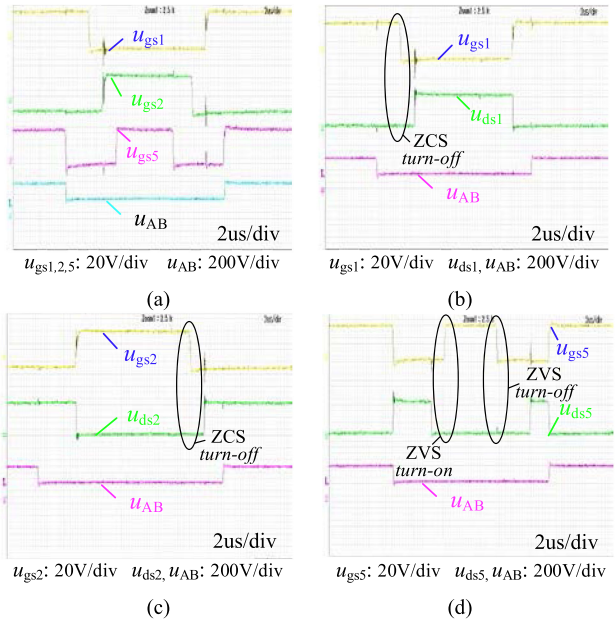

Fig. 20. Detailed waveforms of switching process between "2*E*" level and "*E*" level. (a) Gating signals of S_1, S_2, and S_5. (b) Turn-ON/turn-OFF waveforms of S_1. (c) Turn-ON/turn-OFF waveforms of S_2. (d) Turn-ON/turn-OFF waveforms of S_5.

From Fig. 19(c), it can be seen that the turn-OFF of S_4 is a soft switching, but the turn-ON of S_4 is a hard switching. Because when S_4 is turned on, the drain–source voltages of S_3 and S_6 are changed from 0 to 0.5 U_{dc}, and the drain–source voltage of S_4 is changed from 0.5 U_{dc} to 0. Therefore, the turn-ON loss of S_4 involves the charging and discharging losses of junction capacitors of S_3, S_4, and S_6. From Fig. 19(d), it can be seen that the turn-OFF of S_6 is a soft switching, but the turn-ON of S_6 is a hard switching. Because when S_6 is turned on, the drain–source voltages of S_3 and S_6 are changed from 0.5 U_{dc} to 0, and the drain–source voltage of S_4 is changed from 0 to 0.5 U_{dc}. It indicates that the turn-ON loss of S_6 involves the charging and discharging losses of junction capacitors of S_3, S_4, and S_6.

The detailed switching process of the improved modulation scheme, when u_{AB} outputs between the "2*E*" level and the "*E*" level at the positive half-cycle, is shown in Fig. 20.

From Fig. 20(a), it can be seen that, u_{AB} outputs between the "2*E*" level and the "*E*" level. Si MOSFET pairs S_1–S_2 are complementarily switching, and the deadtime is set between them to avoid the shoot-through issue. From Fig. 20(b), it is obviously that the turn-OFF of S_1 is a soft switching, but the turn-ON of S_1 is a hard switching. Because when S_1 is turned on, the drain–source voltages of S_2 and S_5 are changed from 0 to 0.5 U_{dc}, and the drain–source voltage of S_1 is changed from 0.5 U_{dc} to 0. It indicates that the turn-ON loss of S_1 involves the charging and discharging losses of junction capacitors of S_1, S_2, and S_5. From Fig. 20(c), it can be seen that the turn-OFF of S_2 is a soft switching, but the turn-ON of S_2 is a hard switching. Because when S_2 is turned on, the drain–source voltages of S_2 and S_5 are changed from 0.5 U_{dc} to 0, and the drain–source voltage of S_1 is changed from 0 to 0.5 U_{dc}. It indicates that the turn-ON loss of S_2 involves the charging and discharging losses of junction capacitors of S_1, S_2, and S_5. From Fig. 20(d), it is obviously that the turn-ON and turn-OFF of S_6 are soft switching during the switching process of the *P*1a state and the *P*1c state.

The proposed hybrid modulation can enable different modulation schemes according to the output power. The dynamic waveforms are shown in Fig. 21. It can be seen that a flexible transition between the conventional modulation scheme and the proposed modulation scheme is achieved.

At the time of the red solid line, the output power is changed from 1.2 to 2.1 kW. From the waveform of u_{ds2}, it can be seen

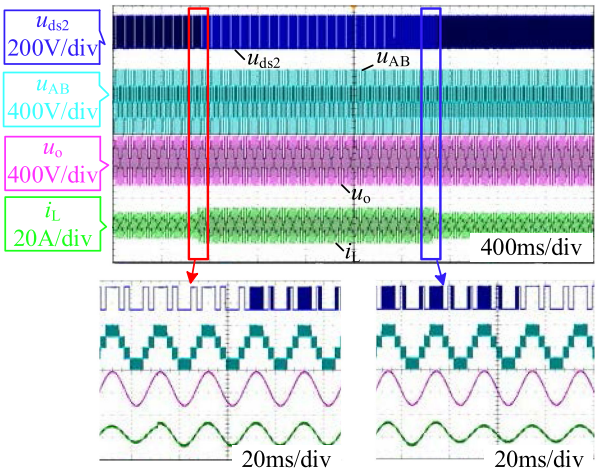

Fig. 21. Dynamic waveforms of the transition between the conventional modulation scheme and the proposed scheme.

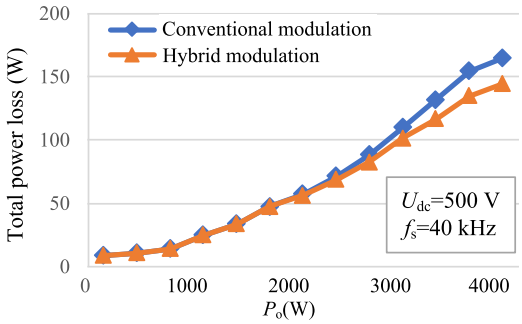

Fig. 22. Experimental power loss comparison between the hybrid modulation scheme and the conventional scheme.

that the modulation scheme is switched from the conventional scheme to the proposed scheme. At the time of the blue solid line, the output power is changed from 2.1 to 1.2 kW. It is obviously that the modulation can be switched from the proposed scheme to the conventional scheme. Therefore, a flexible modulation transition is achieved by employing the hybrid modulation scheme.

The experimental loss comparison between the improved modulation scheme and the conventional one with 500 V dc-link voltage at the switching frequency 40 kHz is shown in Fig. 22. It is clear that the total power loss can be reduced by the proposed hybrid scheme under higher power conditions. Thus, the efficiency can be optimized by the proposed hybrid modulation scheme without increasing the hardware cost.

Experimental efficiencies of the 2-SiC hybrid 3L-ANPC inverter shown in Fig. 1(a) are measured. To fairly compare the efficiencies of 3L-ANPC and 5L-ANPC, both of the modulation indices are set as 0.78. Thus, the dc-link voltage of 3L-ANPC is equal to 800 V, whereas the dc-link voltage of 5L-ANPC is equal to 400 V. Both of the switching frequencies are 40 kHz. The efficiency comparison between 3L-ANPC and 5L-ANPC is shown in Fig. 23.

From Fig. 23, it can be seen that the efficiency of 5L-ANPC with the proposed modulation scheme is higher than that of

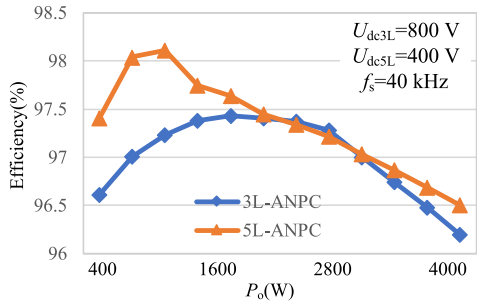

Fig. 23. Experimental efficiency comparison between 3L-ANPC and 5L-ANPC.

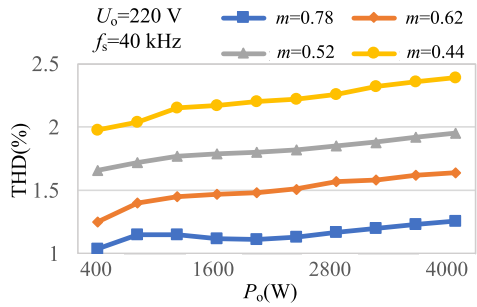

Fig. 24. THD performance with the proposed modulation scheme.

3L-ANPC. It is because that the drain–source voltages of the switches in the 3L-ANPC are higher than that of 5L-ANPC with the same modulation index. Therefore, the switching losses of 3L-ANPC are higher than that of the 5L-ANPC, especially under high-frequency switching conditions.

Experimental results of total harmonic distortion (THD) performance for the 2-SiC hybrid 5L-ANPC inverter with different modulation indices and output power are depicted in Fig. 24. The switching frequency is 40 kHz, and the input voltage is 400 V.

From Fig. 24, it can be concluded that the output voltage THD is proportional to the output power and inversely proportional to modulation indices. Furthermore, the output voltage THD is always lower than 2.5% with different modulation indices and output powers. Therefore, the quality of the output voltage is great.

VI. Conclusion

In this article, a 2-SiC hybrid 5L-ANPC full-bridge inverter is proposed. A hybrid modulation scheme is also proposed to lower the conduction losses both in the $P1$ state and the $N1$ state, and the overall efficiency improvement is enhanced. The power losses of the 2-SiC 5L-ANPC full-bridge inverter with different modulation schemes are calculated and compared. Analysis and experimental results demonstrate the following features of the proposed inverter and modulation strategy.

1) Compared with the conventional modulation scheme, the proposed modulation scheme can improve the conversion efficiency of the 2-SiC hybrid 5L-ANPC full-bridge

inverter under high-power conditions. Under low-power conditions, the efficiency of the proposed modulation is lower than that of the conventional modulation.

2) To further optimize efficiencies over the whole power conditions, a hybrid modulation scheme is proposed to enable the novel scheme or the conventional scheme depending on the output power. Experimental results show that a flexible modulation transition is achieved by employing the hybrid modulation scheme, and the overall efficiency improvement is achieved as well.

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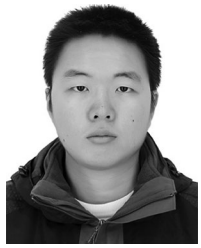

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