Letters

A New Primary PWM Control Strategy for CCM Synchronous Rectification Flyback Converter

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***Abstract*—A new primary PWM (pulsewidth modulation) control strategy for continuous conduction mode (CCM) synchronous rectification (SR) flyback converter is proposed in this letter. The PWM signal for the primary switch has been divided into two pulses in a switching period (dual-pulse PWM, DP-PWM). The first pulse is a fixed narrow pulse, which is used to turn OFF the SR, whereas the second pulse is a regulated pulse for output voltage regulation. With the proposed DP-PWM control scheme, the shoot-through currents exist on both the primary side and secondary side of the CCM SR flyback converter can be effectively reduced. Meanwhile, the efficiency has been improved obviously. Detailed theoretical analysis has been presented and verified by a 12 V/2.5 A CCM flyback experimental prototype.**

***Index Terms*—Continuous conduction mode (CCM) flyback, dual pulse (DP) pulsewidth modulation (PWM) control, synchronous rectification (SR).**

I. Introduction

THE FLYBACK topology has been widely applied in portable devices as their chargers. To meet the requirement of fast charge technique, the charge power of the chargers should be increased, i.e., both of the output voltage and output current should be extended [1]. To achieve high efficiency, the synchronous rectification (SR) technique should be applied to replace the output diode in those chargers.

The variable frequency control is usually applied in low power flyback converter to realize boundary conduction mode so that the switching losses of the primary switch can be reduced [2]. However, the peak value of primary current is large under low input voltage, which increases the size of the transformer and also makes the converter difficult to pass the EMI limitation. When the flyback converter is designed to operate in continuous conduction mode (CCM) under low input voltage, the peak value of primary current can be reduced. Therefore, CCM/ discontinuous conduction mode (DCM) dual-mode flyback converter has drawn more and more attentions [3]–[5]. However, the driving scheme for SR becomes more complex especially when the converter operates in CCM. When the flyback converter operates in CCM with the most popular SR drain-source (DS) voltage detection (DSVD) based on SR driving method [6]–[8], there always exists a short overlapped period between the primary switch and SR due to the signal transfer time delay T_{d2} caused by the inner circuit of the SR controller [7], [8]. It results in large shoot-through currents on both the primary and secondary sides [4], [5]. These large shoot-through currents increase converter losses including conduction losses, secondary leakage inductor loss, and SR switch loss.

To resolve this problem, many new driving schemes for SR have been proposed [4], [5], [9]–[17]. However, some schemes cannot eliminate the overlap period totally [14], [15], whereas some schemes need a large dead time be left as a predefined condition for avoiding shoot-through problem during dynamic process, which deteriorates the converter efficiency [4], [9]–[13]. The external-driven methods using pulse transformer [16] or integrated fluxlink technique [17] are reliable with no cross conduction. However, they are usually complex and costly.

In [5], a transformer winding short method for CCM SR flyback converter is proposed. This method is simple and can eliminate the shoot-through problem totally. But it needs to add a combined switch in parallel with the auxiliary winding of the transformer, which increases the cost and size of the converter.

In this letter, a new control scheme for CCM SR flyback converter by simply modifying the structure of primary pulsewidth modulation (PWM) controller is proposed, as shown in Fig. 1. This control is realized by adding a dual pulse (DP) generator formed by simple logic circuits after a conventional PWM controller. In this way, the conventional DSVD SR controller [7], [8] can be applied. The main idea of the proposed control scheme is similar to that in [5], but the main structure is simpler and cheaper (about $0.092 cost saved in the same prototype in [5]), which is a good benefit for charger applications. Hence, the proposed control scheme is promising and more suitable for industrial applications.

II. Theoretical Analysis on SR Flyback Converter With Proposed DP-PWM Control

As shown in Fig. 1, the DP generator consists of two delay circuits and three logic components. Fig. 2(a) shows the key

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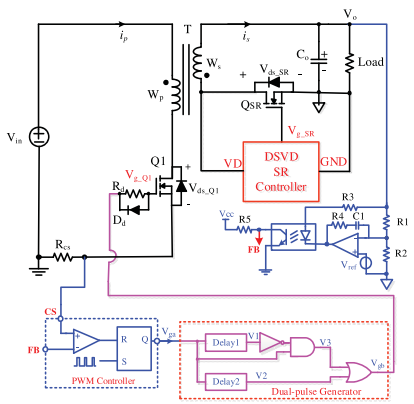

Fig. 1. Diagram of SR flyback converter with proposed primary PWM control.

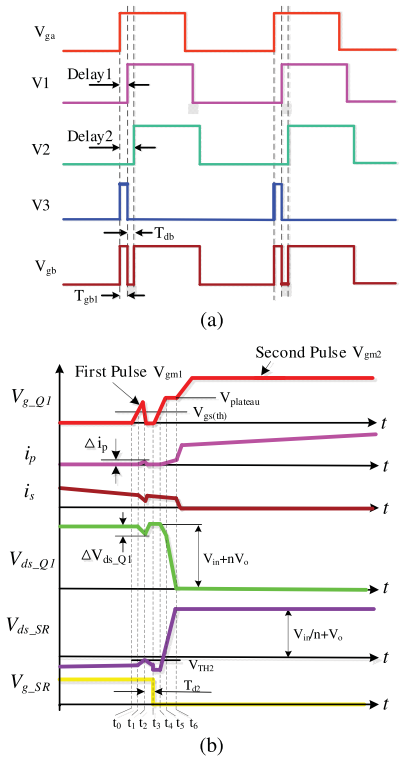

Fig. 2. Key waveforms of the SR flyback converter with the proposed DP-PWM control and conventional DSVD SR controller. (a) In DP generator. (b) During primary switch $Q1$ turn-ON process.

waveforms in the DP generator and Fig. 2(b) shows the key waveforms during primary switch $Q1$ turn-ON process.

With the proposed DP-PWM control, the conventional single pulse driving signal of primary switch has been split into two pulse signals in a switching cycle, as shown in Fig. 2(a). The first pulse is narrow and the second pulse is wide. The first narrow pulse is of fixed width and used to turn OFF the SR so that the overlapped period between the primary switch and SR can be almost eliminated and the severe shoot-through problem in CCM SR flyback converter can be alleviated, whereas the second wide pulse is used to regulate the output.

A. *Turn-ON Process of Q1 and Considerations on V_{gm1}*

During the switching processes, the primary equivalent model of the flyback converter can be regarded as an inductive load system with distributed inductor (considering the leakage inductor of transformer) [18]. The turn-ON process of $Q1$ under this condition is depicted as the following.

Referred to Figs. 1 and 2(b), the first pulse V_{gm1} increases with a slope determined by the driving resistor R_d, MOSFET gate resistor R_G, and input capacitance $C_{\rm iss}$ during period [t_0-t_2] as follows:

$$V_{gm1}(t) = V_{gam}\left(1 - e^{-\frac{t}{(R_d+R_G)C_{\rm iss}}}\right) \tag{1}$$

where V_{gam} is amplitude of the pulse signal V_{gb}. Once the first pulse V_{gm1} of V_{g_Q1} reaches the turn-ON threshold voltage $V_{gs(\rm th)}$ at time t_1, the primary current i_p starts to increase with a slope determined by the MOSFET transfer characteristic curve [19]. The expression of primary current i_p during period [t_1-t_2] is obtained

$$i_p(t) = G_m[V_{gm1}(t)][V_{gm1}(t) - V_{gs(\rm th)}] \tag{2}$$

where G_m is the transconductance of the primary MOSFET, which is a nonlinear function varied with gate voltage and can be deduced according to the MOSFET transfer characteristic curve.

As i_p increases, the DS voltage V_{ds_Q1} starts to drop due to the induced voltage across the leakage inductor of transformer. Correspondingly, the reflected voltage across of transformer increases and secondary current i_s decreases, which make V_{ds_SR} arises. When V_{ds_SR} reaches the threshold voltage $V_{\rm TH2}$ inside the SR controller at time t_2, the inner logic circuit is triggered. The turn-OFF trigger condition is shown as follows:

$$V_{ds\_SR} = -\left[i_s\left(t_1\right) - N_T i_p(t_2)\right] R_{SR\_\rm on} = V_{\rm TH2} \tag{3}$$

where N_T is the turns ratio of the transformer. $R_{SR\_\rm on}$ is the ON-resistance of SR. $i_s(t_1)$ can be calculated according to the main parameters and operation conditions of the converter.

At time t_3, after an inner time delay T_{d2}, Q_{SR} is turned off and i_s flows through the body diode of Q_{SR}. Although V_{ds_SR} is lower than $V_{\rm TH2}$ at this moment, Q_{SR} will not be turned on again due to the blank circuit integrated inside the controller [7], [8]. At time t_4, the second pulse V_{gm2} of V_{g_Q1} reaches the turn-ON threshold voltage $V_{gs(\rm th)}$. Because SR has been turned off already, $Q1$ is turned on normally and there is no shoot-through phenomenon.

Obviously, it is best to turn OFF the first pulse V_{gm1} right after time t_2. Otherwise, i_p will continue to increase and V_{ds_Q1} will continue to drop. Therefore, the period [t_0-t_2] is the required minimal first driving pulsewidth T_{gb1} to trigger the turn-OFF condition of SR, which can be derived with (1)–(3). The calculated period [t_0-t_2] is about 30 ns under 90 $\rm V_{ac}$ input voltage and full load using the specific prototype parameters in Section III.

The amplitude of V_{gm1} should be lower than the miller plateau voltage $V_{plateau}$. If not, the drop speed of V_{ds_Q1} will be very fast, which also causes fast falling speed of i_s and arising speed of i_p. Large shoot-through currents may occur and benefit of the proposed control is weakened. Therefore, it is better to select the

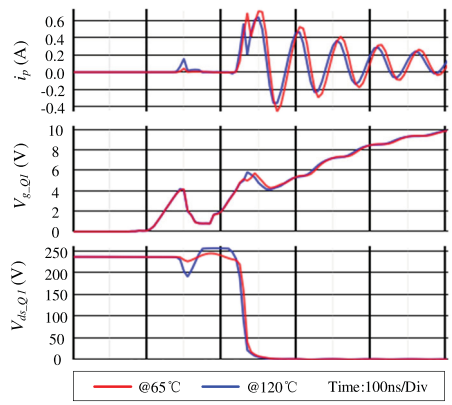

Fig. 3. Simulation waveforms of i_p, V_{g_Q1}, and V_{ds_Q1}.

amplitude of the first pulse V_{gm1} between $V_{gs(\mathrm{th})}$ and $V_{plateau}$ of $Q1$.

The dead time T_{db} between the first pulse V_{gm1} and second pulse V_{gm2} is used to prevent cross conducting between $Q1$ and SR. Referred to Fig. 2, the value of T_{d2} is enough for T_{db}.

MOSFET junction temperature also has effects on the gate threshold voltage and transfer characteristic [19]. A simulation circuit of the SR flyback converter with proposed control is built up based on SIMetrix/SIMPLIS software, in which the Infineon MOSFET IPP65R225C7 model possessing temperature characteristic [20] is adopted for $Q1$. Fig. 3 shows the simulation results when MOSFET junction temperature is set to 65 and 120 °C, respectively. It can be seen that both the raising amplitude of primary current i_p and the drop amplitude of V_{ds_Q1} caused by the first pulse V_{gm1} have increased some limited values under higher MOSFET temperature. The main factors causing the variations on i_p and V_{ds_Q1} are that $V_{gs(\mathrm{th})}$ decreases and G_m increases as MOSFET junction temperature increases [19].

The turn-OFF process of $Q1$ and turn-ON process of SR of the CCM SR flyback converter with proposed DP-PWM control are similar to the conventional SR flyback converter and are not discussed in detail in this letter.

B. Losses Analysis

The large shoot-through currents existed in conventional CCM SR flyback converter bring two main losses: the secondary leakage inductor *loss* P_{lk_s} and the turn-OFF loss of SR P_{off_SR} [5]. The shoot-through currents also increase some other losses such as conduction losses, which are very small.

According to the parameters of prototype as shown in Table I, calculated P_{lk_s} and P_{off_SR} in conventional CCM SR flyback are presented in Fig. 4, respectively. As input voltage increases, the power losses increase obviously due to the increased negative secondary current spike I_{s_spike}. Similar to the SR flyback converter shown in [5], these two losses in the CCM SR flyback converter with the proposed DP-PWM control are almost zero because there is almost no negative shoot-through current on the secondary side. The increased losses with the proposed control are mainly the capacitor loss of $Q1$ and the conduction loss on the primary side brought by the first pulse of V_{g_Q1}. However, these two losses can be very small with appropriate amplitude and width of V_{gm1}. The analysis abovementioned has explained why the proposed DP-PWM control can improve the converter efficiency. Compared with the scheme shown in [5], the SR flyback converter with proposed control can achieve slightly efficiency improvement because of the elimination of auxiliary switches losses.

TABLE I
COMPONENTS PARAMETERS OF PROTOTYPE

Components	Parameters
Input Capacitor C_{in}	2×22μF/400V
Rectifier Bridge DB	4×1N4004, 1A/400V
Output Capacitor C_o	2×100μF/50V
Primary Switch $Q1$	IPP65R225C7,11A/650V
SR Q_{SR}	IRLR3110, 14mΩ/100V
Transformer T	Core:RM8, L_p=700μH, L_{lkp}=15.8μH, L_{lks}=0.4μH W_p:W_s =54:8
Gate Resistor R_d	51Ω

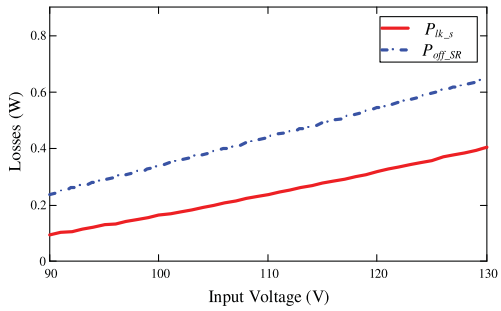

Fig. 4. Calculated secondary leakage loss and turn-OFF loss of SR with 90∼130 V_{ac} input in conventional CCM SR flyback converter.

III. EXPERIMENTAL RESULTS

A 12 V/2.5 A experimental prototype with 90∼130 V_{ac} input has been built up to verify the theoretical analysis. The prototype is designed to operate in CCM at rated output power. Key components parameters of the prototype are listed in Table I. UCC3845 from TI is used as PWM controller and the frequency of converter is set to 95 kHz. A conventional DSVD SR controller IR1167 from Infineon is applied as SR controller. The SR flyback converter with scheme shown in [5], together with two conventional PWM controlled SR flyback converters with IR1167 and a demagnetization period calculation method based SR controller FAN6204A [10] have been built up and tested for comparison.

Measured waveforms of SR flyback converter in CCM with conventional PWM control and IR1167 are shown in Fig. 5. It can be seen that there exist large shoot-through spikes in the primary current i_p and secondary current i_s due to the cross conduction between the primary switch and SR.

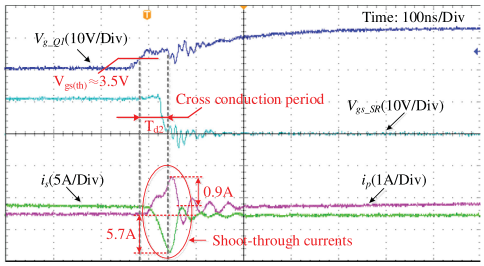

Fig. 5. Measured waveforms of SR flyback converter with conventional PWM control and IR1167 at 110V_{ac} and full load.

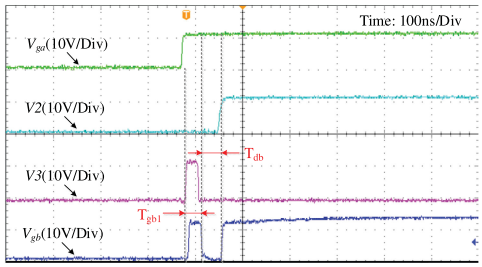

Fig. 6. Measured waveforms of V_{ga}, $V2$, $V3$, and V_{gb} in DP generator.

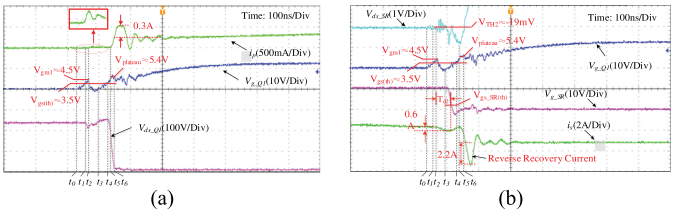

Fig. 7. Measured waveforms of SR flyback converter with proposed DP-PWM control at 110 V_{ac} and full load. (a) Waveforms of V_{g_Q1}, V_{ds_Q1}, and i_p. (b) Waveforms of V_{ds_SR}, V_{g_Q1}, V_{g_SR}, and i_s.

Fig. 6 shows the main pulse signals in DP generator. The first pulsewidth of V_{g_Q1} is set to 35 ns and the dead time T_{db} between the first pulse and second pulse is set to 50 ns, which is approximately equal to the delay time T_{d2}.

Fig. 7 shows the measured waveforms of prototype with proposed DP-PWM control in CCM. The amplitude of V_{gm1} is set to 4.5 V, which is higher than the threshold voltage 3.5 V but below the gate plateau voltage 5.4 V of the primary switch. As shown in Fig. 7(a), V_{ds_Q1} drops a little and i_p can be almost neglected during the conduction period of the first pulse of V_{g_Q1}. Fig. 7(b) shows that Q_{SR} is turned off by voltage variation on V_{ds_SR} induced by the first pulse of V_{g_Q1}. The falling value of i_s is small during the turn-OFF process of SR. In Fig. 7(a) and (b), it can still be observed current spikes during the turn ON process of the second driving pulse of $Q1$. The spikes are mainly caused by the parasitic parameter of switches and transformer, which is much smaller than the shoot-through spikes shown in Fig. 5.

Fig. 8(a) shows the measured full load efficiency curves of the prototypes with proposed DP-PWM control scheme in [5], and conventional PWM control based on two different SR controllers. Both the efficiencies of the prototypes with proposed

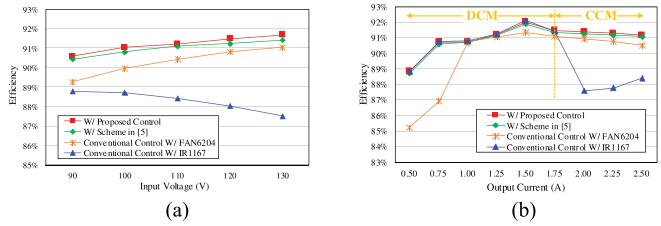

Fig. 8. Measured efficiency curves. (a) With input voltage variations at full load. (b) With load variations at 110 V_{ac}.

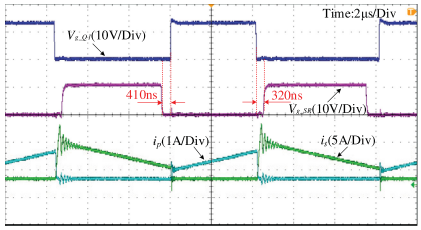

Fig. 9. Waveforms of V_{g_Q1}, V_{g_SR}, i_p, and i_s in prototype with conventional PWM control and FAN6204A @90V_{ac} and full load.

DP-PWM control and the control scheme in [5] have been improved obviously in CCM because of the shoot-through currents reduction. The former is slightly higher than the latter in all the input voltage range and load range due to the elimination of combined switch. The full load efficiency of the prototype with conventional PWM control and FAN6204A is obviously lower than the prototypes with proposed DP-PWM control and scheme in [5]. The main reason is that enough dead times between the primary driving signal and SR driving signal should be left with FAN6204A to prevent cross conduction under different conditions [10], as shown in Fig. 9. Otherwise, shoot-through problem may occur especially under low input voltage and FAN6204A will work intermittently under this condition, which causes even worse efficiency. A Schottky diode SR5100 has been in parallel with SR in this prototype to carry the secondary current during the dead times, but the efficiency improvement is minor. As shown in Fig. 8(b), the prototype with conventional PWM control and FAN6204A is of lower efficiency under light load condition. The reason is that FAN6204A enters "green mode" and SR stops switching as the output current is lower than 1 A in this prototype [10]. The other three prototypes have almost the same efficiency in DCM because there is no cross-conduction problem under this mode.

IV. Conclusion

A DP-PWM control strategy for CCM SR flyback converter has been proposed in this letter, which can effectively resolve the shoot-through problem in conventional PWM control so that the efficiency has been improved obviously. The first pulse of the primary driving pulse is designed according to the MOSFET transfer characteristic to avoid introducing additional losses. The proposed scheme is realized only with some added logic circuits, which can be further integrated with the conventional PWM controller. The cost and size are reduced compared with

the scheme in [5]. The proposed control method can also be applied to LLC resonant converter with SRs for achieving better features.

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