A Modified Asymmetrical Half-Bridge Flyback Converter for Step-Down AC–DC Applications

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***Abstract*—This article presents a modified asymmetrical half-bridge flyback converter (AHBFC) to fulfill the single-stage step-down ac–dc universal input voltage application. This topology is obtained from the integration of a buck-type power factor correction, an auxiliary energy buffer, and a conventional AHBFC. By sharing common switches and utilizing transformer's leakage inductor, the single-stage circuit can achieve both high power factor (PF) and low total harmonic distortion with the simple constant on-time control while regulating the dc output voltage. In addition, it is able to operate in universal input voltage with low dc link voltage and low output voltage. Moreover, the zero voltage switching and the zero current switching features of the power switches can also be achieved. Detailed analyses and design procedures of the proposed converter are given and verified by the experimental results. Finally, the comparison with reported circuit topologies and power loss analyses verified by experimental results are presented to provide the insight of practical design.**

***Index Terms*—Power factor correction (PFC), step-down ac–dc converter, zero current switching (ZCS), zero voltage switching (ZVS).**

I. Introduction

THE ac–dc voltage conversion can be easily achieved by using a full-bridge rectifier and a large output dc capacitor. However, this approach has the drawbacks of large output voltage variation, low power factor (PF), and high total harmonic distortion (THD), which will pollute the ac power system and interfere with other electronic equipment. Therefore, the ac–dc adapter with input power exceeding 75 W should be capable of high PF and low THD, which is the feature specified by international regulations such as EN/IEC 61000-3-2 Class D [1].

Due to the output voltage regulation for ac–dc adapter, an additional dc–dc converter is in series with the power factor correction (PFC) stage, which will reduce the efficiency because of the two-stage power-processing. Besides, an additional circuit stage requires extra components and will increase the circuit complexity. To improve the efficiency and reduce the overall size and cost, a number of single-stage PFC circuits have been presented and discussed [2]–[12].

To achieve higher efficiency, soft switching characteristics have gained lots of attention for high switching frequency applications. The active-clamp flyback converter can achieve zero voltage switching (ZVS), but it has diode reverse recovery issue and high voltage stress on the switch [13], [14]. The asymmetrical half-bridge flyback converter (AHBFC) has the ZVS features by utilizing the resonance of parasitic components. Therefore, there is no need to add extra components. Moreover, the voltage stress on the switch is confined to the input voltage, making it suitable for high power applications. Besides, the reverse recovery loss of the output diode can be minimized due to its zero current switching (ZCS) [15], [16]. For reasons outlined above, the AHBFC is commonly used for dc input applications [17]–[19]. Nevertheless, the use of AHBFC for the ac input application can only be found in [20]. However, due to the step-down ac–dc conversion, the inherent dead-zone feature will cause low PF and high THD problems. To solve this dead-zone issue, an energy buffer can be adopted [21].

Therefore, a modified AHBFC, which is the fusion of a buck-type PFC, an energy buffer, and a conventional AHBFC, is proposed in this article. To accommodate the universal input voltage range, the ZVS and ZCS operation of the power switches with the asymmetrical pulsewidth-modulation (APWM) along with the constant on-time control should be analyzed. Also, the design procedure and power budget should be established for practical engineering design. Thus, the proposed converter is able to achieve universal input voltage with low dc link voltage and low output voltage, and both high PF and low THD.

In this article, the circuit configuration and operation modes of the proposed modified AHBFC will be introduced, followed by the thorough circuit analyses. Then, based on the derived mathematical equations, a practical design procedure can be obtained. The experimental results of a prototype circuit are presented to verify the performance of the proposed modified AHBFC with desired features. Finally, the comparisons with different circuit topologies and the power loss analyses verified by experimental results are presented to provide the insight of practical design.

II. Circuit Configuration and Operation Mode

Fig. 1 shows a two-stage circuit topology of the buck-type ac–dc adapter. The first stage is a buck-type PFC and the second stage is an AHBFC. A low pass filter L_f and C_f is used to smooth

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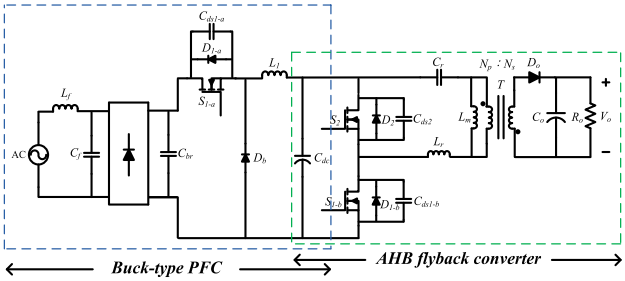


Fig. 1. Two-stage circuit topology of the buck-type ac–dc adapter.

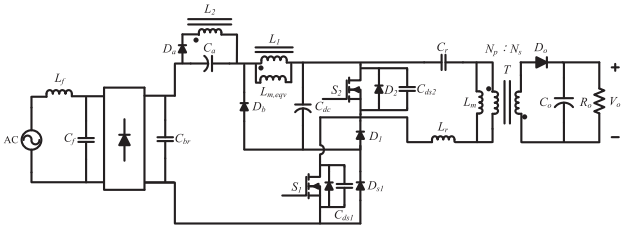


Fig. 2. Single-stage circuit topology of the proposed modified AHBFC.

out the high switching frequency current at the input line. The ac line voltage is rectified by the bridge diodes followed by a buck-type PFC. The switch S_{1-a} controls the energy delivering to the dc link capacitor $C_{\rm dc}$. The buck diode D_b provides the freewheeling current path for the buck inductor L_1, which operates in the discontinuous conduction mode (DCM). The two switches S_{1-b} and S_2 are operated asymmetrically with a short dead-time to achieve ZVS and the duty cycle d is referred to S_{1-b}. Each switch is composed of an active switch, an intrinsic antiparallel diode, and a parasitic capacitor. The transformer T is modeled as the magnetizing inductor L_m, the leakage inductor L_r, and an ideal transformer with turns ratio of N_p:N_s. The leakage inductor is used as the resonant inductor and is much smaller than the magnetizing one. The resonance between L_r and C_r allows the output diode D_o to achieve ZCS. The output capacitor C_o is large enough that the output voltage V_o is constant.

To improve the efficiency and reduce the overall size and cost, a single-stage modified AHBFC is proposed and illustrated in Fig. 2. Based on the operation principles and gating signals of switches S_{1-a} and S_{1-b} in Fig. 1, one of them can be eliminated by adding two extra diodes D_1 and D_{S1} at the appropriate nodes. The two switches S_1 and S_2 are operated asymmetrically with a short dead-time to achieve ZVS while the duty cycle d is referred to S_1. To solve the dead-zone problem for the buck-type PFC, an energy buffer should be adopted. For the modified AHBFC, the energy buffer which consists of a buffer capacitor C_a, a freewheeling diode D_a, and a coupled inductor L_2 is utilized. The L_2 is designed to be equal to the buck inductor L_1, so the voltage of C_a is equal to the voltage of dc link capacitor $C_{\rm dc}$. Therefore, the energy buffer can boost the rectified voltage so the input current can flow continuously from the ac source within a line period. Eventually, the proposed modified AHBFC can achieve high PF and low current THD.

As shown in Fig. 3(a)–(g), the steady state operation of the modified AHBFC can be divided into seven modes within

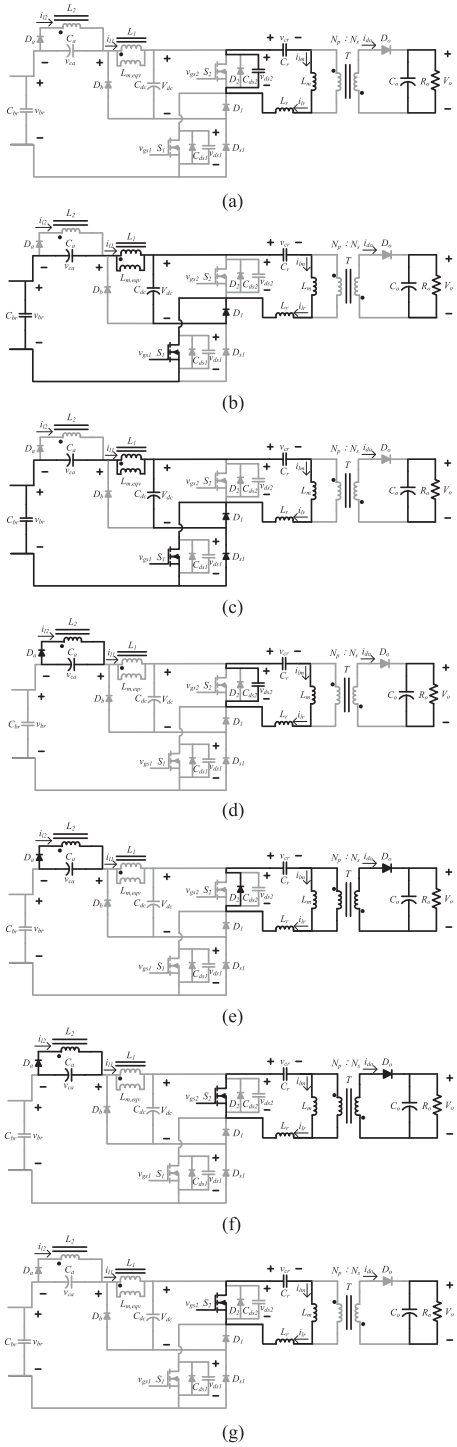


Fig. 3. Operation modes of the proposed modified AHBFC. (a) Mode I ($t_0 \sim t_1$). (b) Mode II ($t_1 \sim t_2$). (c) Mode III ($t_2 \sim t_3$). (d) Mode IV ($t_3 \sim t_4$). (e) Mode V ($t_4 \sim t_5$). (f) Mode VI ($t_5 \sim t_6$). (g) Mode VII ($t_6 \sim t_7$).

a switching period T_s. Fig. 4 shows the corresponding key waveforms. To achieve a high PF with a simple control method, the buck inductor L_1 is operated in DCM. The two switches S_1 and S_2 are operated complementarily with a short dead-time. The dc link capacitor $C_{\rm dc}$ is large enough, so the dc link voltage $V_{\rm dc}$ is almost constant in a switching period. Prior to *Mode I*, the energy stored in the coupled inductor L_2 is released

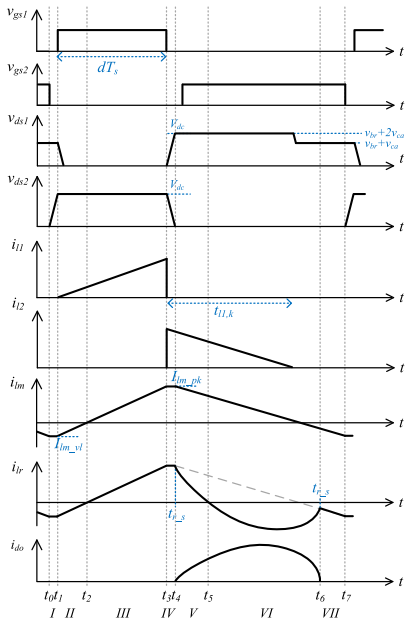


Fig. 4. Key waveforms of the modified AHBFC.

completely, both the magnetizing inductor current i_{lm} and resonant inductor current i_{lr} are negative, and the output diode current i_{do} is zero. The details of each mode are described as follows.

Mode I ($t_0 \sim t_1$): This is a dead-time interval since both S_1 and S_2 are off. Both i_{lm} and i_{lr} are negative in the previous mode due to the resonant behavior of the inductor current. The i_{lm} will first flow through C_{ds2}. After C_{ds2} is charged to $V_{\rm dc}$, the i_{lm} will flow through $C_{\rm dc}$ and D_1. The output diode D_o is reverse biased and the output capacitor C_o provides power to the load.

Mode II ($t_1 \sim t_2$): This mode begins when a turn-on signal v_{gs1} is applied to the gate of S_1 while i_{lr} is still negative. After S_1 is turned on, both D_a and D_b are reverse biased. The buck inductor L_1 starts to be charged through the rectified input voltage in series with the buffer capacitor C_a, where the capacitor voltage is decreased. Since v_{ca} can be approximated to $V_{\rm dc}$ in steady state, the voltage across L_1 is equal to the input voltage. This mode ends when i_{lr} reaches zero.

Mode III ($t_2 \sim t_3$): This mode begins when i_{lr} becomes positive. At the beginning of *Mode III*, both L_m and L_r start to be charged through S_1, D_{s1}, $C_{\rm dc}$, and C_r. Both i_{lm} and i_{lr} are increased linearly. The D_o is still reverse biased so C_o keeps providing power to the load. The L_1 is still to be charged through the rectified input voltage. This mode ends when S_1 is turned off.

Mode IV ($t_3 \sim t_4$): This mode is another dead-time interval since both S_1 and S_2 are off. The i_{lm} will flow through C_{ds2} and quickly discharge it completely. Because of the short dead-time interval, the changes of i_{lm} and i_{lr} are very small. When S_1 is off, the D_b is still reverse biased. The voltage on S_1 is equal to $v_{br} + 2v_{ca}$ and that on D_b is equal to $V_{\rm dc} - v_{ca}$. The energy stored in L_1 is recycled to C_a through L_2 and D_a. The voltages of L_1 and L_2 are clamped at v_{ca} with a turn ratio.

Mode V ($t_4 \sim t_5$): This mode begins when C_{ds2} is discharged to zero. The i_{lm} will continue to flow through D_2 and create a zero voltage upon the switch S_2. Within this mode, the S_2 is turned on before i_{lr} becomes negative. Then, the ZVS feature can be achieved. The stored energy in L_m is released to the load through the transformer, forward bias D_o and delivers energy to the secondary side. Because of the conduction of D_o, the voltage across L_m is clamped by the reflected output voltage. The i_{lm} will decrease linearly. On the other hand, the C_r and L_r will begin to resonant and i_{lr} will be deviated from i_{lm}. The energy stored in L_1 is still recycled to C_a through L_2 and D_a. This mode ends when i_{lr} drops to zero.

Mode VI ($t_5 \sim t_6$): This mode begins when i_{lr} changes its direction due to the resonance. The operations of all components are similar as *Mode V*. When i_{lr} resonates to i_{lm} before S_2 is turned off, the i_{do} drops to zero and the ZCS feature for D_o can be achieved. It should be mentioned that both i_{lm} and i_{lr} can be positive or negative when i_{lr} resonates to i_{lm}. The energy stored in L_2 is released completely, so the voltage across S_1 is equal to $v_{br} + v_{ca}$.

Mode VII ($t_6 \sim t_7$): The mode begins when $i_{lr} = i_{lm}$ and i_{do} drops to zero. A negative resonant current will flow through S_2 and there is no energy transferred through the transformer to the load. The C_o provides power to the load. When S_2 is turned off, the operation mode goes back to in *Mode I* and the next switching period begins.

III. Circuit Analysis and Design Example

To simplify the steady-state analysis, several assumptions are made: 1) The two switches S_1 and S_2 consist of MOSFET channels, body diodes and parasitic capacitors. 2) The transformer T is modeled as the magnetizing inductor L_m, the leakage inductor L_r, and an ideal transformer with turns ratio of N_p:N_s. 3) The dc link capacitor $C_{\rm dc}$ and buffer capacitor C_a are large enough, so the voltages on these two capacitors are almost constant within a switching period. 4) The buck inductor L_1 and the coupled inductor L_2 are tightly coupled, so the leakage inductor can be neglected.

To achieve high PF, the buck-type PFC is operated in DCM over an entire line period. Due to the DCM operation and the additional capacitor voltage provided by the energy buffer, the input current $i_{\rm in}$ with an additional input low pass filter can be derived and expressed as

$$i_{\rm in} = \frac{v_{\rm in}}{2L_1} d^2 T_s \tag{1}$$

where d is the duty cycle of S_1 and T_s is the switching period. It should be mentioned that the operation of S_2 will not affect the buck-type PFC because of the current blocking diode D_1. From (1), it can be seen that $i_{\rm in}$ is proportional to the sinusoidal input voltage $v_{\rm in}$ with a constant d operation.

The input power $P_{\rm in}$ can be obtained by taking the average of the instantaneous line power over one line period by using (1)

$$P_{\rm in} = \frac{1}{2\pi} \int_0^{2\pi} [v_{\rm in} \times i_{\rm in}]\, dt = \frac{{V_m}^2 d^2 T_s}{4L_1} \tag{2}$$

where V_m is the peak value of the input voltage. The L_1 can be selected in accordance with the rated input power by (2)

$$L_1 = \frac{(V_m d)^2 T_s}{4P_{\text{in}}}. \tag{3}$$

The voltage transfer function of the buck-type PFC can be obtained by applying the voltage-second balance theorem to L_1. When S_1 is turned on, the voltage across L_1 is V_m. When S_1 is turned off, the voltage across L_1 is V_{dc}. To ensure that the buck inductor current i_{l1} can be operated in DCM, the following voltage transfer function should be satisfied

$$\frac{V_{\text{dc}}}{V_m} \geq \frac{d}{1-d}. \tag{4}$$

Besides the desired buck-type PFC feature, the output voltage is regulated by S_1 and S_2 with an appropriate d. It is assumed that C_{dc} is large enough, so the dc link voltage V_{dc} is almost constant. The average voltage, V_{cr}, of the resonant capacitor C_r, is related to V_{dc}, d, L_m, and L_r by applying the voltage-second balance theorem to L_m

$$(V_{\text{dc}} - V_{cr}) \frac{L_m}{L_m + L_r} d = V_{cr}(1-d). \tag{5}$$

From (5), the L_r which is much smaller than L_m can be eliminated, so the V_{cr} can be obtained

$$V_{cr} \approx dV_{\text{dc}}. \tag{6}$$

When S_1 is turned on and S_2 is turned off, as shown in Fig. 3(b) and (c), the voltage across L_m can be expressed as (1-d)V_{dc}. It should be mentioned that L_r is much smaller than L_m, so L_r can be neglected. When S_1 is turned off and V_{ds2} becomes zero, as shown in Fig. 3(e)–(g), the voltage across L_m is $V_o \cdot (N_p/N_s)$. By applying the voltage-second balance theorem to L_m, the voltage transfer function of the AHBFC can be determined as

$$\frac{V_o}{V_{\text{dc}}} = n \times d \tag{7}$$

where $n = N_s/N_p$ is the turns ratio of transformer.

The CCM operation of L_m is preferred in order to increase the utilization of transformer. As shown in Fig. 4, the difference between i_{lm} and i_{lr} will flow through the output diode D_o via the transformer. Thus, the average magnetizing inductor current I_{lm} is related to the turns ratio n and the output current I_o as shown in (8)

$$I_{lm} = nI_o. \tag{8}$$

The peak current I_{lm_pk} and valley current I_{lm_vl} of L_m can be obtained by using (8) which should be plus and minus with a half of current ripple on L_m, respectively

$$I_{lm\_pk} = nI_o + \frac{V_o(1-d)T_s}{2nL_m} \tag{9}$$

$$I_{lm\_vl} = nI_o - \frac{V_o(1-d)T_s}{2nL_m}. \tag{10}$$

During the resonant period, the voltage on L_m is clamped by the reflected output voltage while L_r and C_r form a resonant path. The instantaneous current of L_m, i_{lm}, during the resonant period can be derived as

$$i_{lm} = I_{lm\_pk} - \frac{V_o}{nL_m}(t - dT_s). \tag{11}$$

By using the current–voltage relationship for L_r, the resonant inductor current i_{lr} can be written as a second-order differential equation, which is shown in (12)

$$i_{lr} = -L_r C_r \frac{di_{lr}(t)^2}{dt^2}. \tag{12}$$

By using Laplace transform to solving the second-order differential equation shown in (12), the instantaneous current of L_r, i_{lr}, can be derived as

$$i_{lr} = I_{lm\_pk} \cos[\omega_r (t - dT_s)] - \frac{V_o}{n\omega_r L_m} \sin[\omega_r (t - dT_s)] \tag{13}$$

where the resonant angular frequency ω_r is

$$\omega_r = \frac{1}{\sqrt{L_r C_r}}. \tag{14}$$

The ZVS operation of the switch can be achieved when the energy stored in L_m is greater than that of the parasitic capacitors of the two switches. In addition, a sufficient time segment for the switching dead-time should be established for the resonance. After a series of mathematical equation derivation, the L_m and the minimum dead-time t_d for the ZVS condition can be derived as

$$L_m < \frac{(1-d)T_s}{2} \times \frac{R_o}{n^2} \tag{15}$$

$$t_d > \max\left[\frac{C_{ds1} \times V_{\text{dc}}}{|i_{lm\_vl}|}, \quad \frac{C_{ds2} \times V_{\text{dc}}}{i_{lm\_pk}}\right] \tag{16}$$

where C_{ds1} and C_{ds2} are the parasitic capacitors of switches S_1 and S_2, respectively.

For the ZCS operation of the output diode D_o, the i_{lr} should reach the same amount of i_{lm} within the resonant period before the next switching cycle begins. Thus, the interval of *Mode VI* of the modified AHBFC is determined by the resonant angular frequency ω_r, and the boundary conditions are $d = d_{\max}$ and $i_{lm}(T_s) = i_{lr}(T_s)$. By combining (9), (11), and (13) with the boundary conditions, the following equation can be obtained

$$\left[\frac{n^2 L_m}{R_o} + \frac{(1-d_{\max})T_s}{2}\right] \cos[\omega_{br} \times (1-d_{\max})T_s] - \frac{1}{\omega_{br}} \sin[\omega_{br} \times (1-d_{\max})T_s] = \frac{n^2 L_m}{R_o} - \frac{(1-d_{\max})T_s}{2} \tag{17}$$

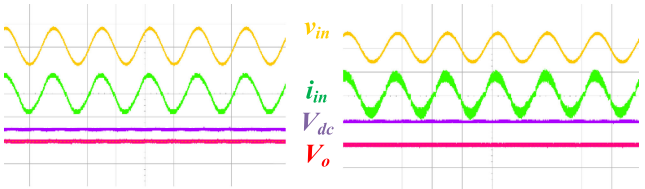
where ω_{br} is the boundary resonant angular frequency. It is very difficult to obtain the value of ω_{br} from (17), directly. However, by using numerical calculation, such as Bolzano's Theorem, the ω_{br} can be calculated. Moreover, the resonant capacitor must satisfy the following constrain

$$C_r < \frac{1}{{\omega_{br}}^2 \times L_r}. \tag{18}$$

Based on the operation modes and the derived equations, the design of the proposed single-stage AHBFC with PFC feature

TABLE I
SPECIFICATIONS OF THE MODIFIED AHBFC

Parameters	Value
Input Voltage $v_{in,rms}$	90 V_{ac} ~ 264 V_{ac}
Output Voltage V_o	19 V_{dc}
Output Power $P_{o,max}$	100 W
Switching Frequency f_s	100 kHz



(V_{dc}:200V/div; V_o:20V/div; t:10ms/div).
(v_{in}:200V/div; i_{in}:2A/div) (v_{in}:500V/div; i_{in}:1A/div)

(a) (b)

Fig. 5. Measured waveforms of input voltage $v_{\rm in}$, input current $i_{\rm in}$, dc link voltage $V_{\rm dc}$, and output voltage V_o. (a) $V_{in}=110V_{\rm ac}$. (b) $V_{in}=220V_{\rm ac}$.

can be accomplished. The specifications shown in Table I is built and tested. The designed procedure is described as follows.

Step 1) Determine n, d, and L_1 at steady state. From (7), it can be found that $V_{\rm dc}$ is related to n. To avoid high voltage on $C_{\rm dc}$, resulting in high voltage stress on other components, the n is selected as 0.6. To fulfill the boundary condition of buck-type PFC and the voltage transfer function of the AHBFC, the d can be obtained by combing (4) and (7)

$$d \le \frac{-V_o \pm \sqrt{(V_o)^2 - 4V_m n\,(-V_o)}}{2V_m n}. \tag{19}$$

To ensure that L_1 can be operated in DCM at 90$V_{\rm ac}$ input voltage under full load condition, the maximum duty cycle $d_{\max}$ is selected as 0.36 which is smaller than the theoretical calculation from (19). The minimum duty cycle $d_{\min}$ is calculated as 0.12 at 264$V_{\rm ac}$ input voltage. From (3), the L_1 can be calculated as 52.5 μH due to the rated output power.

Step 2) Calculate L_m and L_r. According to (15), the maximum L_m is calculated as 32.08 μH, but a smaller 30 μH magnetizing inductor is selected in practical. The L_r should be much smaller than L_m so a 600 nH resonant inductor, which is 2% of the magnetizing inductance, is selected.

Step 3) Calculate t_d, C_r, and f_r. To ensure the ZVS operation of S_2, the t_d should satisfy (16), thus t_d is designed as 300 ns which is larger than the minimum theoretical calculation. For the ZCS operation of the output diode D_o from (17), the boundary resonant frequency f_{br} is calculated as 160 kHz. Eventually, the C_r can be chosen from (18) as 1 μF and the resonant frequency f_r can be calculated as 205.5 kHz.

IV. EXPERIMENTAL RESULTS

A prototype circuit with the specification shown in Table I is build and tested. Fig. 5(a) and (b) show the waveforms of input voltage $v_{\rm in}$, input current $i_{\rm in}$, dc link voltage $V_{\rm dc}$, and output voltage V_o, for different line voltages. The vertical scales of $v_{\rm in}$ and $i_{\rm in}$ in Fig. 5 are different. The $i_{\rm in}$ is almost sinusoidal and in phase with $v_{\rm in}$. Unlike conventional buck-type PFC, there is no dead-zone appearing in the input current. Besides, the $V_{\rm dc}$ is almost constant where it is 94.8 V and 187 V for different input voltages. With the voltage feedback control by using Microchip dsPIC33FJ16GS502, the V_o can be fixed to 19 V.

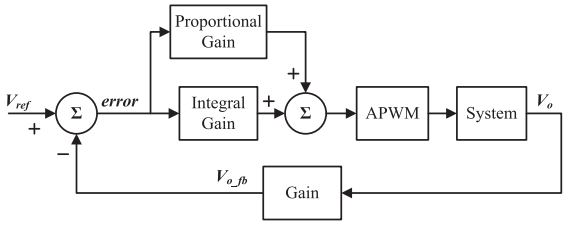
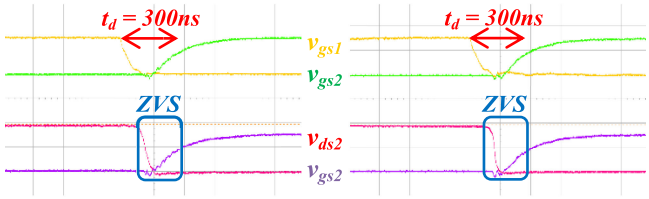


Fig. 6. Functional block diagram of the APWM constant switching frequency voltage-mode control.



(v_{gs1}:10V/div; v_{gs2}:10V/div; t:200ns/div).
(v_{ds2}:50V/div). (v_{ds2}:100V/div).

(a) (b)

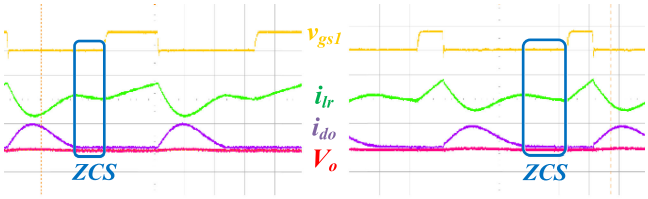
Fig. 7. ZVS operation of S_2. (a) $V_{in}=110V_{\rm ac}$. (b) $V_{in}=220V_{\rm ac}$.

The control strategy adopted in the proposed converter is the APWM constant switching frequency voltage-mode control. The microcontroller unit dsPIC33FJ16GS502 is chosen to implement the control strategy. The main concept for the APWM constant switching frequency voltage-mode control is briefly explained as follows.

The V_{o_fb} is the output voltage feedback signal, and the V_{ref} is a predetermined reference voltage. The voltage difference between V_{o_fb} and V_{ref}, *error*, is amplified by the proportional-integral controller. Then the amplified error is compared with a programmable build-in digital triangle ramp to generate a pair of APWM signals with complementary duty cycle and fixed switching frequency to control the two switches in the power stage. The functional block diagram of the APWM constant switching frequency voltage-mode control is shown in Fig. 6.

Fig. 7(a) and (b) show the turn-on transient of the gate signal and the drain-to-source voltage of S_2 under different ac mains voltages. The vertical scales of v_{ds2} in Fig. 7 are different. With sufficient dead-time $t_d = 300$ ns, before S_2 is turned on, its drain-to-source voltage v_{ds2} decreases to zero. Hence, the ZVS operation for S_2 can be achieved.

The measured waveforms of gate signal v_{gs1} for S_1, the resonant inductor current i_{lr}, the output diode current i_{do}, and the output voltage V_o, under different ac mains are shown in Fig. 8. The waveforms of i_{lr} and i_{do} agree with the simulated



(v_{gs1}:20V/div; i_{lr}:10A/div; i_{do}:20A/div; V_o:20V/div; t:2μs/div).

(a) (b)

Fig. 8. Measured waveforms of gate signal for S_1 v_{gs1}, resonant inductor current i_{lr}, output diode current i_{do}, and output voltage V_o. (a) V_{in}= 110V_{ac}. (b) V_{in}= 220V_{ac}.

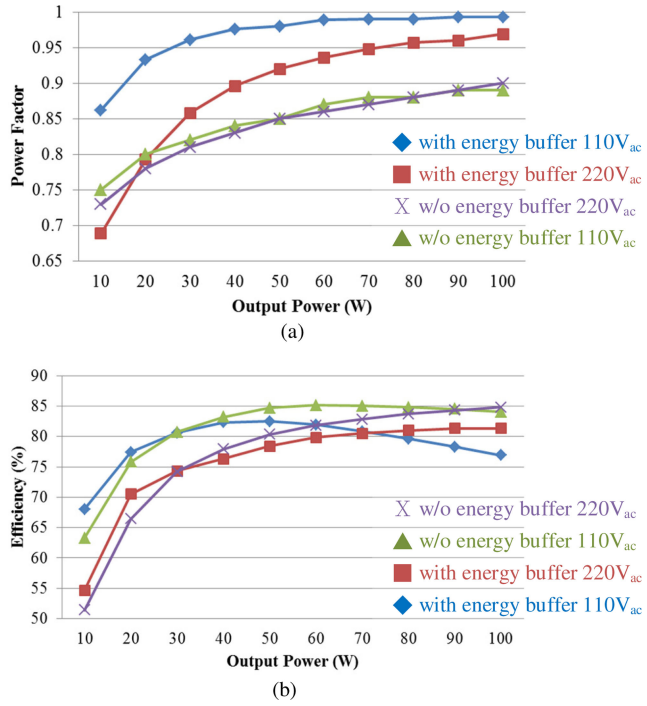


Fig. 9. PF and efficiency of the modified AHBFC. (a) PF curves. (b) Efficiency curves.

ones. Before S_1 is turned on, the i_{do} has dropped to zero. It can be seen that the diode current is zero at both the turn-on and turn-off transients so the ZCS feature for output diode is achieved.

Fig. 9 shows the PF and efficiency under different line input and output power conditions. The PF is nearly 0.99 at full load. However, the efficiency is relatively low due to the nonoptimal component selection and the extra energy buffer for solving the dead-zone problem. Nevertheless, it is very difficult to make a fair efficiency comparison among converters with different input voltage ranges, output voltages, or rated powers. The efficiency can be improved in the future if the power loss analyses are well established.

V. Discussion

The performance of a power converter can be evaluated by different features such as input/output voltage range, dc link voltage level, PF, THD, efficiency, dynamic response, and reliability. The designers need to decide the tradeoff between different performance requirements. For instance, it is very difficult to make a fair efficiency comparison among converters with different input voltage range or rated power. Nevertheless, the power loss analysis is still essential for every practical design. In this section, the key performance of the proposed converter is compared with different circuit topologies published in literature under similar operation conditions. In addition, the power loss analyses for the selected components under different operation conditions are evaluated. The measured converter efficiency agrees with presented power loss analyses which are beneficial to practical converter design.

TABLE II
Operating Voltage Level Comparisons With Reported Topologies

Reference	DC Link Voltage (V)	Input Voltage (V)	Output Condition
[22]	< 355	90 ~ 150	48 V/250 W
[23]	< 350	110	48 V/144 W
[24]	< 400	90 ~ 270	100 V/100 W
Proposed	< 260	90 ~ 264	19 V/100 W

TABLE III
PF and THD Comparisons With Reported Topologies

Reference	PF	The Harmonic Input Current	
		3rd (mA/W)	5th (mA/W)
[25]	0.96	1.4	0.40
[26]	0.97	1.5	0.81
[27]	0.90	2.2	0.30
[20]	0.90	2.4	0.07
Proposed	0.97	0.17	0.11

A. Reported Topologies Comparison

Different circuit topologies from literature with similar operation conditions are selected for key performance comparison. First of all, operating voltage level comparisons among different reported circuit topologies are shown in Table II. It should be noticed that all of them can achieve high PF and low THD. As shown in Table II, [22] and [23] can achieve low voltage output feature but cannot operate at high line condition. Although [24] can accomplish universal input voltage range, it cannot meet the low output voltage demand. Under the similar PF and THD performance, the proposed circuit topology can achieve the lowest output voltage level under the universal input voltage range operation. Besides, the proposed one has the lowest dc link voltage which implies that lower voltage-rating components can be adopted.

For those circuit topologies that can achieve the low output voltage with the universal input voltage range, their PF and THD should be taken into account. Table III shows the PF and the 3rd and 5th harmonics comparisons for different reported circuit topologies in major journals. It can be seen that the proposed

TABLE IV
POWER LOSS OF ACTIVE COMPONENTS

MOSFETs	$R_{ds(on)}$ (Ω)	Power Loss (W)
S_1: SPA17N80C3	0.25	2.87
S_2: STP14NK50Z	0.34	4.75

one can achieve the highest PF and lowest harmonics. Also, it should be mentioned that the measured current harmonics of the prototype can meet the IEC 61000-3-2 class D standard.

On the other hand, it is very difficult to make a fair efficiency comparison among different circuit topologies with different operation conditions. For instance, under the same rated power, the lower the output voltage, the lower the efficiency it will be due to the higher current conduction loss. However, the power loss analyses of the proposed converter are required to improve the efficiency.

B. Power Loss Calculation

Details of power loss calculation for the proposed converter with selected components are described as follows. The conduction loss $P_{\rm cond}$ of the MOSFETs, S_1 and S_2, can be expressed in (20), where $I_{ds\_\rm rms}$ is the root-mean-square (rms) value for drain-source current and $R_{ds(\rm on)}$ is the on-resistance. On the other hand, the turn-on and turn-off switching loss, $P_{sw\_\rm on}$ and $P_{sw\_\rm off}$, are affected by the duration of the switching transient and the time varying values of voltage and current on the MOSFET. Usually, the switching transient can be divided into different time segments, which are the delay time t_d, the rise time t_r, and the fall time t_f. Theoretically, the turn-on and turn-off switching loss, $P_{sw\_\rm on}$ and $P_{sw\_\rm off}$, can be expressed as (21) and (22), where v_{ds} and i_{ds} are the linearly approximated functions for voltage across and the current through the MOSFET during the switching transient. Variables V_{ds} is the turn-off blocking voltage, while I_{ds} is the turn-on conduction current.

Due to the ZVS features, the turn-on switching loss of S_2 can be ignored. Based on the above mentioned power loss calculations and the characteristics of the two MOSFETs, SPA17N80C3 and STP14NK50Z, the power losses for full load with input voltage $110\rm V_{ac}$ are shown in Table IV.

$$P_{\rm cond} = I^2_{ds\_\rm rms} \times R_{ds(\rm on)} \tag{20}$$

$$P_{sw\_\rm on} = \left(\int_0^{t_d(\rm on)} V_{ds} \times i_{ds} dt + \int_0^{t_r} v_{ds} \times I_{ds} dt \right) \times f_s \tag{21}$$

$$P_{sw\_\rm off} = \left(\int_0^{t_f} v_{ds} \times I_{ds} dt + \int_0^{t_d(\rm off)} V_{ds} \times i_{ds} dt \right) \times f_s \tag{22}$$

For the proposed converter, because the buck inductor L_1 is operated in DCM and the output diode D_o has ZCS feature, all diodes will be turned off at zero current. Therefore, the reverse recovery time t_{rr} can be neglected, and the power loss of the diode, P_d, can be calculated by using the forward voltage V_f and the average conducting current $I_{d\_\rm ave}$, as shown in (23)

$$P_d = V_f \times I_{d\_\rm ave}. \tag{23}$$

For the proposed converter, the L_1 is coupled to L_2, via a PQ3230 magnetic core, with DCM operation. The leakage inductance is much smaller than the magnetizing inductance. On the other hand, when S_1 is turned off, the energy stored in magnetizing inductance will be either transferred to L_2 via L_1 to charge C_a through D_a or to charge $C_{\rm dc}$ via D_b. Meanwhile, the energy stored in leakage inductance will quickly release to $C_{\rm dc}$ via D_b. Because the leakage inductance is very small with very limited stored energy by comparing to the large capacitance $C_{\rm dc}$, the discharging time will be very short. Eventually, the voltage variation on $C_{\rm dc}$ caused by the released energy from the leakage inductance can be neglected. In other words, the leakage inductance does not affect the operation of the proposed converter so the leakage inductance can be neglected in the operation mode analysis. The transformer *T* is modeled as the magnetizing inductor L_m, the leakage inductor L_r, and an ideal transformer with turn ratio of N_p:N_s. The filter inductor L_f is used to attenuate the high frequency current harmonics at the input terminal. The low permeability powder core CM358147 is selected.

The copper loss, $P_{\rm copper}$, of these magnetic components can be determined by their rms currents and wire resistances. For the transformer, both primary side and secondary side winding should be taken into account as shown in (24). The derivation of the rms current for each magnetic component of the modified AHBFC is highly related to its operation condition. On the other hand, both of the core loss and air gap loss of the magnetic components should be determined according to the datasheet provided by the manufacturing company.

$$P_{\rm copper} = I^2_{pri\_\rm rms} \times R_{dc\_pri} + I^2_{sec\_\rm rms} \times R_{dc\_\rm sec} \tag{24}$$

The capacitor's power loss is mainly caused by its equivalent series resistance (ESR) and the rms current flowing through, which can be expressed as (25). The capacitor's ESR value, as shown in (26), depends on the operating frequency *f*, capacitance *C*, and dissipation factor tan δ, provided by the manufacturing company.

$$P_{\rm cap} = I^2_{c\_\rm rms} \times ESR \tag{25}$$

$$ESR = \frac{\tan \delta}{2\pi f C} \tag{26}$$

Based on the datasheet of the selected components as well as the derived equations, the power losses of the modified AHBFC under full-load condition with input voltage $110\rm V_{ac}$ are shown in Table V.

From the power loss analyses of the selected components, the calculated power loss is 21.05 W which is close to the measured one, 23.1 W. It should be mentioned that the power losses of C_f, C_{br}, $C_{\rm dc}$, D_1, and D_{s1} are neglected because they are much smaller than others.

TABLE V
POWER LOSS OF PASSIVE COMPONENTS

Diodes, Inductors and Capacitors	V_f (V)	ESR (mΩ)	Power Loss (W)
D_{bridge}: ER304	0.78	-	1.27
D_b: STTH15R06FP	0.5	-	0.08
D_a: STTH15R06FP	0.5	-	0.81
D_o: STPS30150CT	0.57	-	3
L_1, L_2: PQ3230	-	155 (N_p), 176 (N_s)	3.37
T: PQ3230	-	26 (N_p), 14 (N_s)	2.13
L_f: CM358147	-	8	0.14
C_a: 110μ/450V	-	220	0.88
C_r: 1μ/420V	-	13	0.28
C_o: 940μ/35V	-	19	1.48

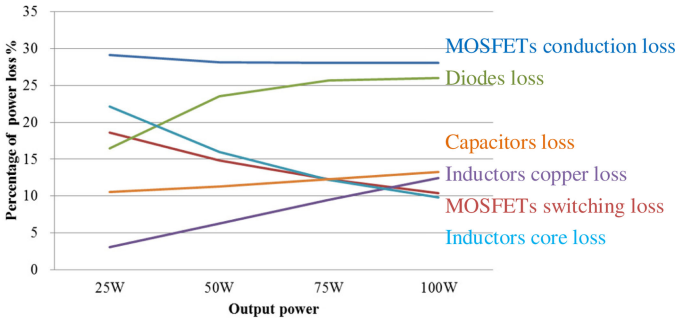


Fig. 10. Curves of power loss under different output power.

C. Component Parameters Evaluation

According to the power loss analyses listed above, it can be observed that each component has various power loss under different output power P_o and dc link voltages $V_{\rm dc}$. It also implies that under different operating condition the power loss of each component may vary. To achieve a better efficiency performance for the proposed converter, the power loss under different operation conditions for key components should be conducted.

Fig. 10 shows the percentage curves of power loss for key components when the input voltage is 110$V_{\rm ac}$. For low output power, the conduction and switching losses of MOSFETs as well as the core losses of inductors dominate the most of total power losses. On the other hand, for high output power, the MOSFET's conduction losses and the diode's losses occupy a large share of total power losses. The curves for the conduction loss of MOSFETs and the diode loss are relatedly flat for the medium and heavy output power loads. It reveals that selecting MOSFETs and diodes with smaller turn-on resistance can effectively improve the efficiency.

Fig. 11 shows the percentage curves of the power loss under different $V_{\rm dc}$. It can be seen that the conduction losses of MOSFETs have the largest power losses share under low $V_{\rm dc}$ condition. From the operation principle, it is understandable that higher peak current and rms current are generated when $V_{\rm dc}$ is relatively low. According to the derived power loss equations,

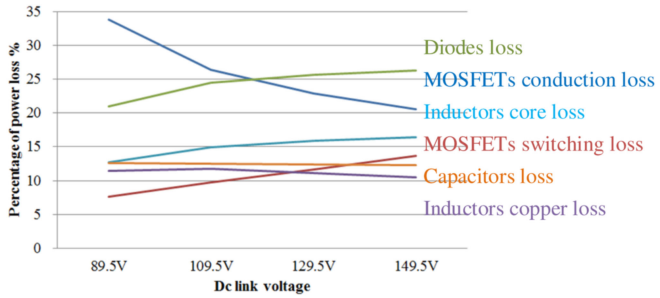


Fig. 11. Curves of power loss under different dc link voltage.

it leads to the higher conduction losses on MOSFETs. As $V_{\rm dc}$ increasing, the conduction losses of MOSFETs will be mitigated so their power losses share will be decreased. On the other hand, the percentage of the switching losses, diode losses, and inductor core losses are increased due to the higher $V_{\rm dc}$. Nevertheless, the percentage of capacitor losses and inductor copper losses are slightly reduced because of the reduced rms current caused by the higher $V_{\rm dc}$.

VI. CONCLUSION

A modified AHBFC to fulfill the single-stage step-down ac–dc universal input voltage application is proposed. Due to its single-stage structure, the simple constant on-time control can be adopted to achieve both high PF and low THD while regulating the dc output voltage. In addition, the proposed converter is able to operate in universal input voltage with low dc link voltage and low output voltage.

A 100 W prototype circuit is designed and implemented to verify the performance of the proposed converter, which features ZVS for the power switch and ZCS for the output diode. Also, the design procedure and the power loss analyses verified by experimental results are presented to provide the insight of practical design.

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