A Family of High Step-Up Cascade DC–DC Converters With Clamped Circuits

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***Abstract*—In this article, a novel passive lossless clamped circuit composed of two capacitors and one diode is proposed. One of the two capacitors is used to construct a flowing path for the energy of leakage inductor and the other is used to store the leakage energy. Compared with a classical passive lossless clamped circuit, the novel circuit structure is more flexible and versatile, and the number of the extra capacitor and diode is consistent to the classical circuit for recycling the energy. Moreover, an idea of using more capacitors in series instead of a single output capacitor to reduce voltage stress and volume is presented. In order to extend their application scope and demonstrate their practical value, the novel clamped circuits and the idea are integrated into a family of cascade dc–dc converters based on the popular boosting cell, such as voltage-lift cell, symmetric voltage multiplier cell and asymmetric voltage multiplier cell. As a representative, a novel cascade converter, which integrates the novel passive lossless clamped circuit and the idea is analyzed in detail. The proposed converter has a high voltage gain and low ripple input current. The voltage stresses of an output diode and output capacitor can be effectively reduced. Its output capacitor adopts a 20-uF polypropylene (CBB) capacitor rated at 250 V to replace the higher rated electrolytic capacitor. A prototype circuit in the laboratory is established to verify its performances.**

***Index Terms*—Clamped circuit, coupled inductor, dc–dc converters, voltage multiplier cell.**

I. Introduction

With the growing maturity of renewable energy technology in power generation, more and more environmentally friendly energy sources have been widely used in our daily life, such as solar energy and wind energy in [1]–[3]. Therefore, a lot of labor power and material resources are invested in the exploitation of renewable energy sources. Unfortunately, all of these applications are ultimately characterized by low voltage and high current. A typical renewable energy system is shown in Fig. 1. The low voltage of the photovoltaic power source can be converted into high voltage through the high step-up dc–dc converter, and then, the renewable energy can be directly transferred into load or dc microgrid or be indirectly transferred into utility or load through an inverter. The conventional boost converter can theoretically provide a high voltage gain with an extreme duty cycle, but with the increase of duty cycle, its voltage gain and efficiency are seriously limited by the parasitic parameters in fact.

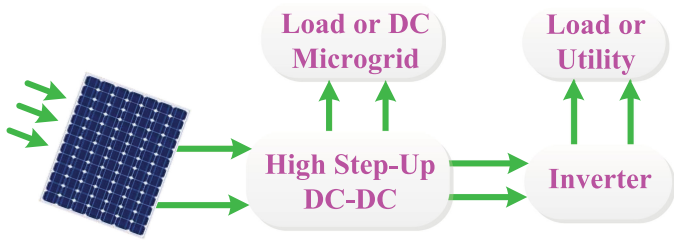

Fig. 1. Typical renewable energy system.

To obtain a high voltage gain and efficiency, a great number of converters are proposed in [4], [5], [7]–[9], and [23]. The boost converter can achieve a high voltage gain by applying switch capacitor cells in [4]. However, the active switch is attacked by surge current so that the loss is large. For the surge current can be limited by inductor, the switch inductor cell can be integrated into boost converter to achieve a high voltage conversion ratio in [5]. However, the switch inductor cell also adds the number of core, which results in a large space. A flyback converter can be expected to achieve a high voltage gain by adjusting the turns ration. Owing to the effect of the energy stored in leakage inductor, the active switch suffers from a high spike voltage. Therefore, there is a low efficiency in this converter.

For improving the voltage gain, voltage-lift cell (VLC) technology, which is composed of one inductor, one capacitor, and one diode, is integrated into the converter in [7]. In order to further improve voltage gain, the coupled inductor technology and VLC are integrated into [8] and [23]. Besides, the voltage stresses on semiconductor devices are reduced. However, the voltage and current of the semiconductor devices have a serious resonance in that the energy stored in leakage inductor cannot be effectively released when the power switch is turned off. By employing an active clamped circuit, the converter based on coupled inductor technology and two VLCs can realize high voltage conversion in [9]. The efficiency is improved for the energy stored in leakage inductor is effectively absorbed. However, the cost is increased, and the control becomes more complicated.

In [6], a cascade boost converter consists of two inductors, two capacitors, three diodes, and one active switch. By adding one

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capacitor and two diodes to the conventional boost converter, the voltage gain is twice that of conventional boost converter. Although the voltage stresses on active switch and output diode cannot be reduced in comparison with the boost converter and the efficiency is low, there is a low current ripple in a cascade boost converter. By imitating boost converter, cascade structure converters with VLC are proposed to achieve high voltage conversion in [14] and [24]. Their voltage gain has a quadratic feature so that it is easy for these converters to get a high voltage gain. By employing the passive lossless clamped circuit, these converters can not only effectively recycle leakage energy, but also effectively upgrade their efficiency. However, the voltage stresses of switch and output diode are still high, which results in low efficiency.

Myriads of converters with symmetric voltage multiplier cell (SVMC), consisting of one inductor, two capacitors, and two diodes, have been published because this cell is well placed to expand voltage gain in [10]–[12], [19]–[22]. In SVMC, two capacitors are charged in parallel and are discharged in series through an inductor. Compared with VLC, the voltage gain can be further increased for the introduction of SVMC in converter. Besides, voltage stresses of switch and output diode can be also reduced for the converter. The SVMC and passive clamped circuit are successfully integrated to achieve high efficiency and voltage gain in [12] and [16]. Moreover, the voltage stresses of active switch and output diode are effectively reduced. In [15], a cascade converter successfully integrates the coupled inductor technology and the cell. Although this converter obtains a high voltage conversion, the voltage stress on main switch is equal to $V_o/(1+ND)$. If $N=2$, $D=0.5$, and $V_o=380$ V, its value is equal to 190 V and is not quite low enough.

Compared with an active clamped circuit, the passive clamped circuit is simple and has almost no influence on control system. Therefore, the passive lossless clamped circuit has been widely used in the converters with coupled inductor to recycle the energy stored in the leakage inductor. On the one hand, the classical passive lossless clamped circuit is usually directly connected on both sides of main switch or primary winding of coupled inductor. In fact, it limits application of converters, which will be discussed in Section II-B. On the other hand, output capacitor is either connected in parallel with load or in series with a clamped capacitor. Thus, voltage of output capacitor usually equals to or gets close to output voltage of the converter, which results in a vulnerability that the output capacitor must select an electrolytic capacitor with large volume to fix the output voltage. As the output voltage increases, the volume of output capacitor is to severely reduce the power density of converter.

In this article, novel passive lossless clamped circuits composed of two capacitors and one diode are proposed. The most important feature is that one of the two capacitors is used to construct a flowing path for the energy of leakage inductor and the other is used to absorb the energy of the leakage inductor. Moreover, it is more flexible than the classical passive lossless clamped circuit, although both of them just add one capacitor and one diode in converter. An idea of using more capacitors in series instead of a single output capacitor to degrade the voltage stress and volume of output capacitor is presented. Therefore, based on VLC, SVMC, asymmetric voltage multiplier cell (AVMC), and these ideas, a family of cascade dc–dc converters is presented. In this family, the voltage stress of output capacitor is far lower than that of output voltage. Besides, the novel passive lossless clamped circuits can help converters to improve voltage gain and reduce the voltage stresses of output diode and switch. The relevant converters are shown in Section II.

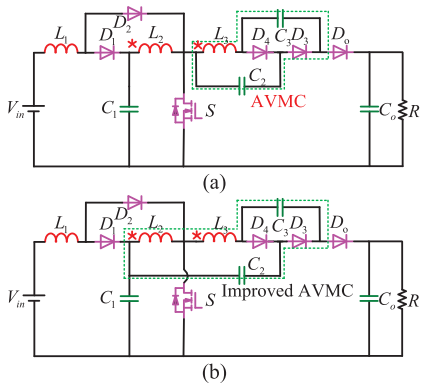


Fig. 2. Presented quadratic boost converters. (a) Converter based on AVMC. (b) Converter based on improved AVMC.

As a representative, one of the deduced converter topologies is selected and analyzed in detail in the following sections, which successfully integrates coupled inductor technology, two capacitors' passive lossless clamped circuit, and the idea is put forward above. To verify the performances of the proposed converter, a 300-W laboratory prototype circuit is implemented so that the intended results and practicability of the proposed converters can be validated by theoretical analyses.

II. Converters Stems and Operational Principle

A. Cascade Boost Converters With AVLC

The proposed converters, which can provide a high voltage gain, are presented as shown in Fig. 2. This converter in Fig. 2(a) successfully integrates coupled inductor technology and AVMC. Two capacitors in the cell are charged or discharged in an asynchronous operation mode. Its greatest attribute is that the energy of leakage inductor can be recycled without additional passive lossless clamped circuit. It means that the converter may be the best one to improve voltage gain now under the same number of devices and the same conditions. When switch is turned off, the energy stored in the leakage inductor is released into output capacitor and load through capacitor C_2 and diode D_o. Therefore, the voltage of the primary-side of the coupled inductor is equal to $V_o - V_{C_1} - V_{C_2}$. As the current of the secondary side of coupled inductor decreases to zero, then, the direction of the current flow changes. When the current flowing through the primary side is the same as that of the secondary side, diode D_4 is turned on and diode D_3 is turned off. Therefore, the voltage of the primary side of the coupled inductor is equal to $V_o - V_{C_1} - V_{C_2} - V_{C_3}$. As a result, inductor L_2 suffers from a high voltage spike because of the free-wheeling process of the

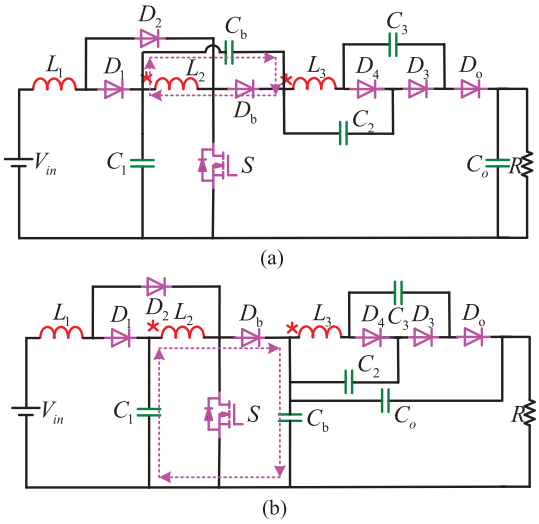


Fig. 3. Quadratic boost converters with the classical passive lossless clamped circuit and AVMC.

current flowing through the secondary side when switch is turned off. For this reason, the main switch also suffers from high voltage spike, thereby increasing switching losses. Moreover, based on the improved AVMC, the converter in Fig. 2(b) is proposed to further improve voltage conversion ratio. However, the two converters need to recycle the leakage energy to improve their efficiency.

B. Family of Cascade Boost Converters With the Passive Lossless Clamped Circuit Formed by Two Capacitors

According to the literature [18] and Fig. 2(a), the classical passive lossless clamped circuits are employed into the proposed converter with AVMC in order to eliminate voltage spike and upgrade efficiency as shown in Fig. 3. Based on Fig. 3, the classical clamped circuit is usually located directly on both sides of the main switch or the primary winding of coupled inductor. However, although the other proposed converter with improved AVMC in Fig. 2(b) can further increase voltage gain, it is difficult for the converter to employ the classical passive lossless clamped circuit to recycle the leakage energy. Therefore, the connection way of the classical passive lossless clamped circuit limits the application of the improved AVMC in various converters, as shown in Fig. 2(b).

As shown in Fig. 4(a), a novel passive lossless clamped circuit consisting of one diode and two capacitors is proposed and employed into the proposed converter with the improved AVMC. In order to expand its application scope and demonstrate the extendibility value in various converters, the converters with VLC or SMC adopt the novel clamp circuit to absorb the leakage energy, as shown in Fig. 4, for VLC and SMC have been extensively used to achieve high voltage gain in various converters. For the use of the novel clamp circuit, the problem, which needs to be overcome, is that the proposed converter with improved AVMC cannot employ the classical passive lossless clamped circuit to recycle the energy stored in the leakage inductor. The details will be shown in the Section II-C.

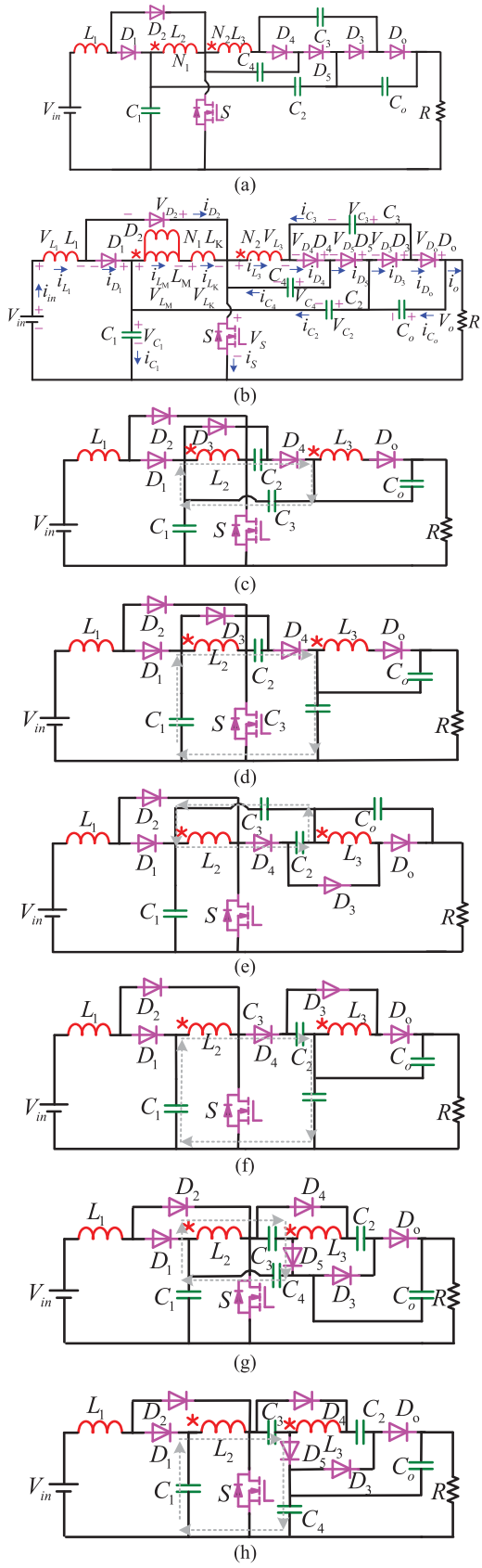


Fig. 4. Family of quadratic boost converters with passive lossless clamped circuit consisting of two capacitors. (a) Proposed converter based on AVMC. (b) Equivalent circuit of the proposed converter. (c)–(f) Converter based on VLC. (g) and (h) Converter based on SMC.

TABLE I
PERFORMANCE COMPARISON AMONG DIFFERENT CONVERTERS

Performances	Voltage stress of active switch	Voltage stress of output diode	Voltage stress of output capacitor	Voltage gain
Fig. 4(c)	$\frac{V_o}{2+ND-D}$	$\frac{NV_o}{2+ND-D}$	$\frac{NDV_o}{2+ND-D}$	$\frac{2+ND-D}{(1-D)^2}$
Fig. 4(e)	$\frac{V_o}{N+1}$	$\frac{NV_o}{N+1}$	$\frac{NDV_o}{N+1}$	$\frac{1+N}{(1-D)^2}$
Fig. 4(g)	$\frac{V_o}{1+2N-DN}$	$\frac{NV_o}{1+2N-DN}$	$\frac{NDV_o}{1+2N-DN}$	$\frac{1+2N-DN}{(1-D)^2}$
Fig. 4(a)	$\frac{V_o}{2+N+DN}$	$\frac{(N+1)V_o}{2+N+DN}$	$\frac{(N+1)V_o}{2+N+DN}$	$\frac{2+N+DN}{(1-D)^2}$

The novel passive lossless clamped circuit is composed of one diode D_5 and two capacitors C_2 and C_4 as shown in Fig. 4(a). Fortunately, capacitor C_2 is from the improved AVMC. Therefore, the novel clamped way only adds one capacitor and one diode. Compared with the traditional passive lossless clamped circuit, the number of the devices is the same. In Fig. 4(c), diode D_4 and capacitors C_2 and C_3 constitute the novel passive lossless clamped circuit of the converter. According to the looping direction of the leakage inductor, the novel passive lossless clamped circuit in other converters can be searched as shown in Fig. 4.

Generally speaking, the output capacitor voltage in the boost converter is equal to either the output voltage when the output capacitor is connected in parallel with the load as shown in Fig. 3(a) or equal to $(G + D - 1)V_o/G$ when the output capacitor is connected in series with the clamped capacitor as shown in Fig. 3(b). In the formula, G and D mean voltage gain and duty cycle, respectively. Therefore, electrolytic capacitor with high rated voltage and large volume is usually selected to fix the output voltage because of large G.

A novel idea is to let the voltage on the clamped capacitor increase and, then, connect the output capacitor in series with the clamped capacitor, which can effectively reduce the voltage stress and the volume of the output capacitor, as shown in Fig. 4. According to Table I and Fig. 5, the output capacitor of the converters in Fig. 4 has lower voltage stress in comparison with that in Fig. 3. Even when $G > 10$ under $0.3 < D < 0.68$, the output capacitor voltage of the converters with VLC or SMC is less than half of its own output voltage. The output capacitor voltage of the converter in Fig. 4(g) is only about 0.17 V_o when $D = 0.3$ and $N = 2$. It means that the electrolytic capacitor under rated output voltage $V_o = 400$ V can be replaced by polypropylene (CBB) capacitor so that the reliability of the converter can be improved and the volume of the converter can be reduced effectively.

Based on Fig. 5 and Table I, some main conclusions can be drawn as follows: compared with the classical passive lossless clamped circuit, the circuit structure is more flexible and can almost meet the needs of all converters for recycling the leakage inductor energy. Moreover, one of the two capacitors in this circuit structure is used to construct a flowing path for the energy stored in the leakage inductor and the other is used to absorb the energy. Furthermore, one of the capacitors comes from the existing converters, so only one additional capacitor is needed without an additional cost. Meanwhile, the voltage and volume of output capacitor in the converters can be effectively decreased by using the clamped capacitor in series with the output capacitor. This new clamped circuit can be used to reduce the voltage and volume of output capacitor of all kinds of converters with coupled inductor, such as boost converter based on coupled inductor, buck-boost converter, flyback converter, forward converter, interleaved converter, and so on. Finally,

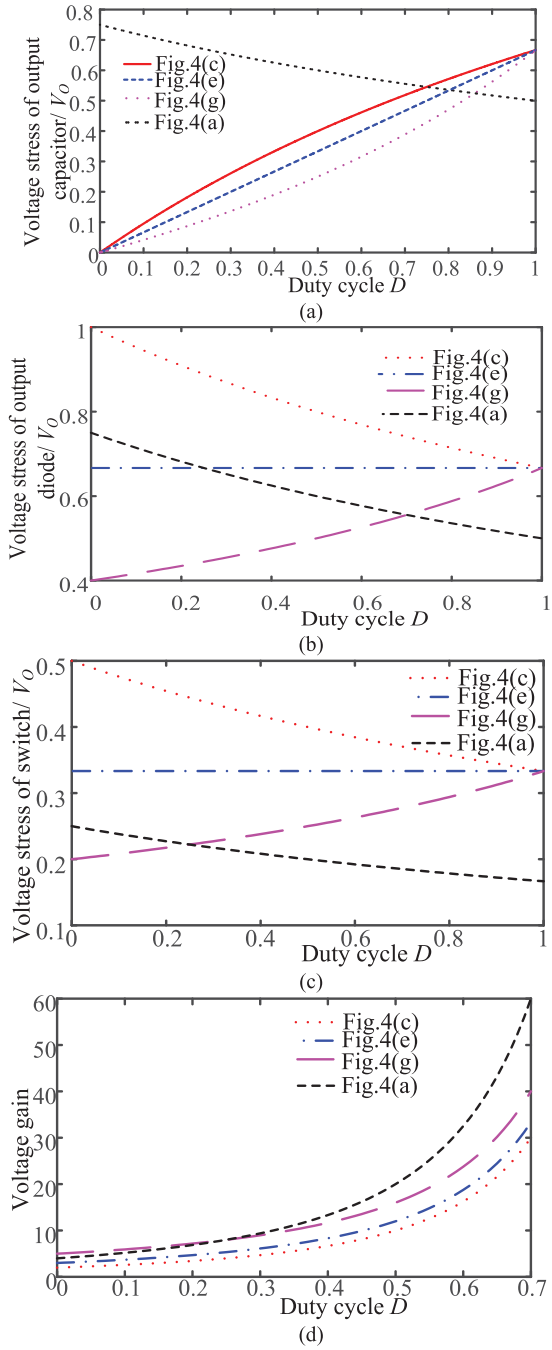


Fig. 5. Performance comparison among different converters under $N = 2$. (a) Voltage stress comparison of output capacitor. (b) Voltage stress comparison of output diode. (c) Voltage stress comparison of switch. (d) Voltage gain comparison.

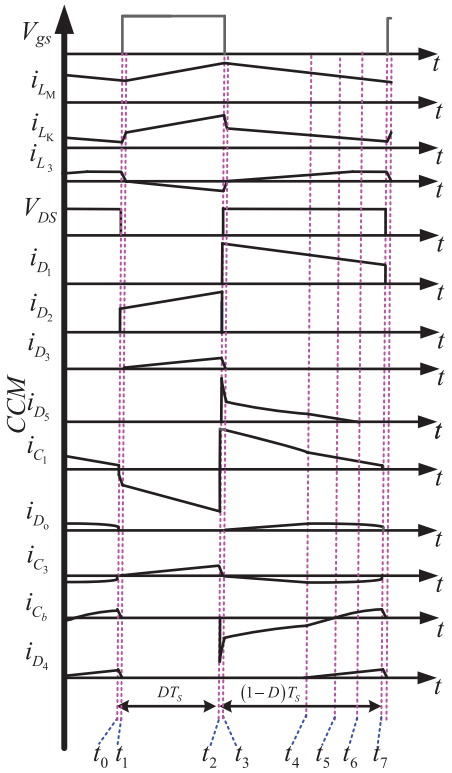


Fig. 6. Theoretical waveforms diagram of the presented converter at *CCM* operation.

Fig. 4(a) will be discussed below as a representative for it has the switch of the lowest voltage stress, the highest voltage gain, and the output diode of the lower voltage stress and the output capacitor voltage is nearly half of that of the output voltage.

C. Continuous Conduction Mode (CCM) Operation Principle of the Proposed Converter

The equivalent circuit of the proposed converter is shown in Fig. 4(b). The coupled inductor is modeled as a magnetizing inductor L_M, a primary leakage inductor L_K, and an ideal transformer. To simplify the circuit analysis of the proposed converter, the following conditions are assumed in order to facilitate analysis.

1) All capacitors are large enough, so their voltage is seen as a constant in one switching period.
2) The main switch and all diodes are seen as an ideal device.
3) Coupling coefficient K and turns ratio N of the coupled inductor are equal to $L_M/(L_M + L_{K_1})$ and N_1/N_2, respectively.

When the proposed converter is operated in *CCM*, the theoretical waveforms during one switching period are shown in Fig. 6. Current flow path of the operating modes is also shown in Fig. 7. The operating principle is described below in detail.

1) Mode I [t_0, t_1]: During this mode, the main switch S is turned ON. Meanwhile, diodes D_2 and D_4 are turned ON, and the other diodesD_1, D_3, D_5, and D_o are turned OFF. The current flow path is shown in Fig. 7(a). The inductor

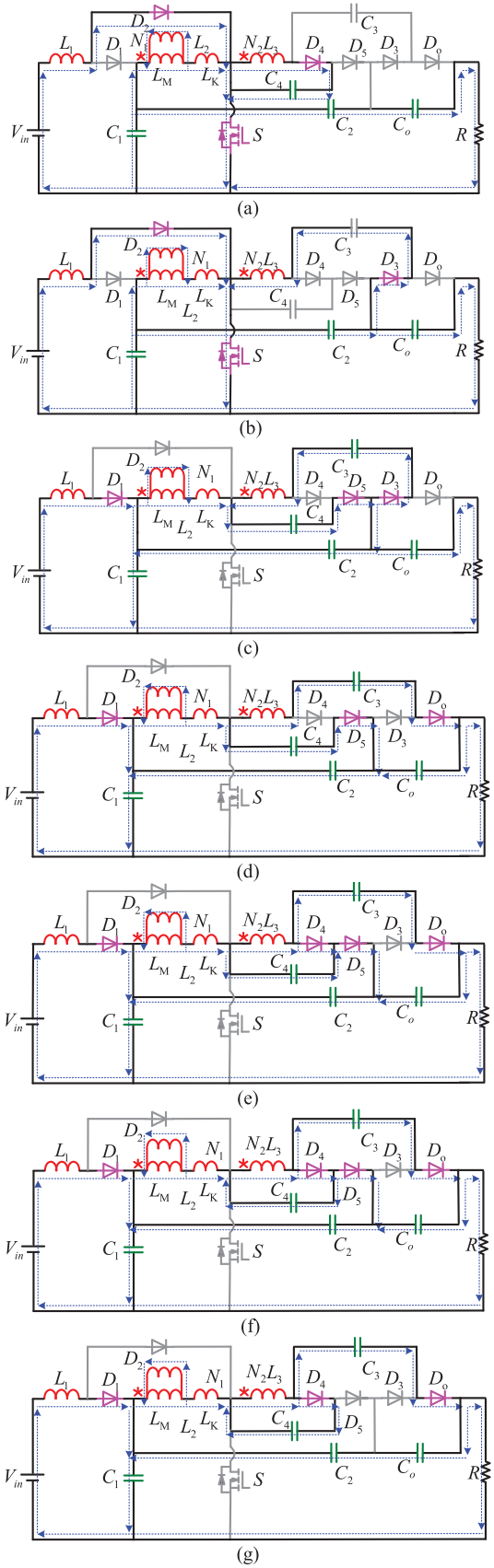


Fig. 7. Current flow path of operating modes during one switching period at *CCM* operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V. (f) Mode VI. (g) Mode VII.

L_1 is charged by an input source through diode D_2 and switch S. Output capacitor C_o is connected in series with capacitor C_2, capacitor C_1, and capacitor C_2 to release their energy into load R. The energy stored in C_1 is also released into the primary-side winding of the coupled inductor, so the leakage inductor current i_{L_K} increases linearly. The secondary-side current i_{L_3} decreases linearly, and capacitor C_4 of clamped capacitors is charged by the secondary-side winding through diode D_4. As a result, the secondary side is clamped by a clamped capacitor C_4 and its voltage is equal to $-V_{C_4}$. The voltage stresses of diodes D_3 and D_o are equal to $V_{C_3} + V_{C_4} - V_{C_2} - V_{C_1}$ and $V_o - V_{C_3} - V_{C_4}$, respectively. Until the current i_{L_3} is reduced to zero, this mode is ended.

2) Mode II [t_1, t_2]: During this time interval, the switch S remains ON, diodes D_1, D_5 and D_o are reverse biased, and diodes D_2 and D_3 are forward biased. The voltage stress of diode D_4 is equal to $V_{L_3} + V_{C_4}$. Fig. 7(b) shows the current-flow path in this interval. The inductor L_1 and the primary side are still charged by the input source and the capacitor C_1, respectively. Therefore, currents i_{L_1} and i_{L_K} keep increasing. Capacitor C_1 is connected in series with the secondary side of coupled inductor and capacitor C_2 to charge capacitor C_3 through diode D_3 and switch S. For the current of secondary side is overturned at $t = t_1$, the current of diode D_3 is increased from zero. The energy of load *R* is still provided by output capacitor C_o and capacitors C_1 and C_2. When S is turned off, this mode has ended.
3) Mode III [t_2, t_3]: During this interval, diodes D_1, D_3, and D_5 are turned on, and diode D_2 is turned off. The switch is turned off at $t = t_2$ and its voltage stress is clamped to $V_{C_1} + V_{C_2} - V_{C_4}$. The current flow path is shown in Fig. 7(c). Inductor L_1 is connected in series with the input source to provide their energy to capacitor C_1 through D_1. Moreover, the secondary side is connected with the clamped capacitor C_4 to release their energy to capacitor C_3 so that this inductor current i_{L_3} rapidly declines and its voltage is clamped by capacitors C_3 and C_4. Diode D_4 is clamped by capacitor C_3 and its voltage is equal to V_{C_3}. Moreover, the capacitor C_2 is charged by C_4, L_1, L_2 and input source through capacitor C_1 and diodes D_1 and D_5. Therefore, the clamped capacitor C_2 absorbs the energy stored in the leakage inductor and the other clamped capacitor C_4 builds a flowing path for C_2. Besides, the energy of load *R* is still provided by output capacitor C_o, and capacitors C_1 and C_2. When the current i_{D_3} of diode D_3 is reduced to zero, this mode ends.
4) Mode IV [t_3, t_4]: At $t = t_3$, the voltage and current across the secondary side start to reverse. Therefore, D_3 is reverse biased and output diode is forward biased. Therefore, i_{L_3} increases from zero. The current flow path is shown in Fig. 7(d). Diode D_3 is clamped by capacitors C_1, C_2, and C_o, and its voltage stress is equal to $V_{C_o} - V_{C_1} - V_{C_2}$. Two clamp capacitors C_4 and C_2 keep on the last state. C_3 is connected in series with the input source, inductor L_1, and the coupled inductor to provide their energy to output diode and load. When current through C_3 attains its maximum value, this mode is ended.
5) Mode V [t_4, t_5]: During this mode, diode D_4 is turned on. The secondary-side winding is connected in parallel with the clamped capacitor C_4 to release their energy to the other clamped capacitor C_2 through diode D_4. The current flow path is shown in Fig. 7(e). This mode ends when the current of flowing through clamped capacitor C_2 is reduced to zero.
6) Mode VI [t_5, t_6]: During this mode, the part energy of the secondary side of the coupled inductor is transferred to the clamped capacitor C_4 through diode D_4. The current flow path is shown in Fig. 7(f). The other clamped capacitor C_2 is charged by the input source, L_1, L_2, and L_3 through D_4, D_5, and C_1. When i_{D_5} is dropped to zero, this mode is ended.
7) Mode VII [t_6, t_7]: At $t = t_6$, clamped diode D_5 is turned off naturally. Fig. 7(f) shows the current flow path in this mode. Capacitors C_1 and C_o are charged as the previous mode. This mode ends when the switch S is turned on at the beginning of the next switching period.

D. Discontinuous Conduction Mode (DCM) Operation

To simplify the analysis procedure of the *DCM*, the identical assumption conditions need to be assumed in comparison with the conditions in *CCM*. Therefore, there is no duplicate description here to save space. The *DCM* operation of the proposed converter only refers to the coupled inductor, and inductor L_1 still works at *CCM*. When the proposed converter is operated in *DCM*, the theoretical waveforms during one switching period are shown in Fig. 8. In *DCM*, the proposed converter has seven modes and the only one mode is different from the modes of CCM. The first six modes are consistent with the latter six modes of CCM. Therefore, only the seventh operating principle is described below in detail.

Mode VII [t_6, t_7]: At $t = t_6$, all diodes are turned off except D_1. The current flow path of this mode is shown in Fig. 9. Capacitor C_1 is charged by the input source and inductor L_1, and load is charged by capacitors C_o, C_1, and C_2. When the switch S is turned on at the beginning of the next switching period, this mode ends.

III. Steady-State Analysis of the Proposed Converter

A. Voltage Gain Derivation

To simplify the analysis of the converter in *CCM* operation, Modes I and III do not take into account the steady state because their time is extremely short compared with that of other modes. The coupled-coefficient K is assumed to be as follows:

$$K = L_M/(L_K + L_M). \tag{1}$$

For the time duration of stage II, the following equations can be written according to Fig. 7(b)

$$V_{L_1}^{\mathrm{II}} = V_{\mathrm{in}} \tag{2}$$

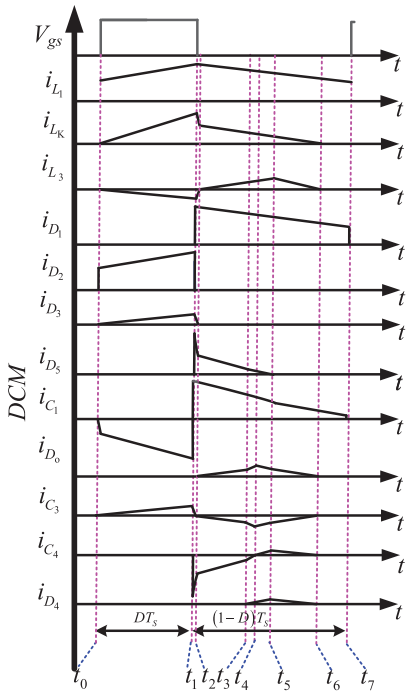


Fig. 8. Theoretical waveform diagram of the presented converter at *DCM* operation.

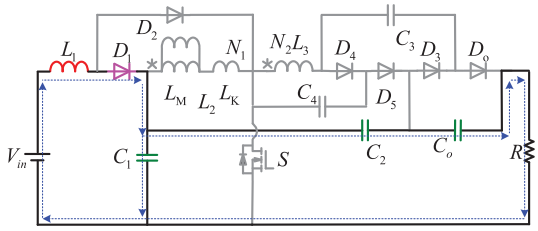


Fig. 9. Current flow paths of the seventh operating mode during one switching period at *DCM* operation.

$$V_{L_M}^{\mathrm{II}} = KV_{C_1} \tag{3}$$

$$V_{C_3} = (NK+1)V_{C_1} + V_{C_2}. \tag{4}$$

As illustrated in Fig. 7(d)–(g), the following equations can be formulated:

$$V_{L_1}^{\mathrm{IV}} = V_{L_1}^{\mathrm{V}} = V_{L_1}^{\mathrm{VI}} = V_{L_1}^{\mathrm{VII}} = V_{\mathrm{in}} - V_{C_1} \tag{5}$$

$$V_{L_M}^{\mathrm{IV}} + V_{L_K}^{\mathrm{IV}} = V_{C_4} - V_{C_2} \tag{6}$$

$$V_{L_M}^{\mathrm{IV}} = V_{L_M}^{\mathrm{V}} = V_{L_M}^{\mathrm{VI}} = V_{L_M}^{\mathrm{VII}} \tag{7}$$

$$V_{L_K}^{\mathrm{IV}} = V_{L_K}^{\mathrm{V}} = V_{L_K}^{\mathrm{VI}} = V_{L_K}^{\mathrm{VII}} \tag{8}$$

$$V_{C_b} = -NV_{L_M}^{\mathrm{IV}} \tag{9}$$

$$V_o = V_{C_1} - (N+1)V_{L_M}^{\mathrm{IV}} - V_{L_K}^{\mathrm{IV}} + V_{C_3}. \tag{10}$$

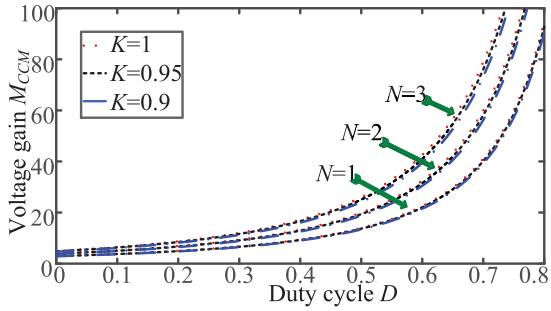


Fig. 10. Voltage gain versus duty cycle under various *N* and *K* CCM operation.

By applying the volt-second balance principle on L_1, the following equation is obtained as:

$$\int_{t_1}^{t_2} V_{L_1}^{\mathrm{II}} dt + \int_{t_3}^{t_7} V_{L_1}^{\mathrm{IV}} dt = 0. \tag{11}$$

Substituting (2) and (5) into (10), the voltage of capacitor C_1 is given

$$V_{C_1} = V_{\mathrm{in}}/(1-D). \tag{12}$$

By applying the volt-second balance principle on L_M and L_K, the following equations can expressed as:

$$\int_{t_1}^{t_2} V_{L_K}^{\mathrm{II}} dt + \int_{t_3}^{t_7} V_{L_K}^{\mathrm{IV}} dt = 0 \tag{13}$$

$$\int_{t_1}^{t_2} V_{L_M}^{\mathrm{II}} dt + \int_{t_3}^{t_7} V_{L_M}^{\mathrm{IV}} dt = 0. \tag{14}$$

Substituting (3)–(9) into (13) and (14), the output voltage can be written as

$$V_o = (2+NK+NDK)V_{C_1}/(1-D). \tag{15}$$

Substituting (12) into (15), the voltage gain is obtained as

$$M_{\mathrm{CCM}} = (2+NK+NDK)/(1-D)^2. \tag{16}$$

It can be seen that the relationship between voltage gain and turns ratio under different coupling coefficients is clearly visible in Fig. 10. As the *K* increases, the voltage gain increases. In addition, the voltage gain is quadratic. When *K* is equal to 1, the ideal voltage conversion can be written in the following equation and plotted as shown in Fig. 11:

$$M_{\mathrm{CCM}} = (2+N+ND)/(1-D)^2. \tag{17}$$

B. DCM Operation

In order to simplify the analysis of the operation principle under *DCM*, leakage inductor L_K of the coupled inductor and the Mode II are ignored. During Mode I, the following equations can be gained:

$$V_{L_1}^{I} = V_{\mathrm{in}} \tag{18}$$

$$V_{L_2}^{\mathrm{I}} = V_{C_1} \tag{19}$$

$$V_{L_3}^{\mathrm{I}} = NV_{C_1} \tag{20}$$

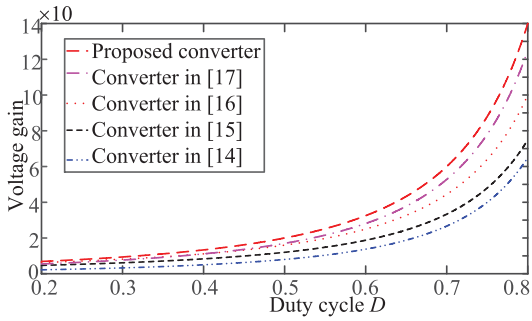


Fig. 11. Voltage gain against duty ratio of the proposed converter and converters in [14]–[17] under *CCM* operation, $N = 2$ and $K = 1$.

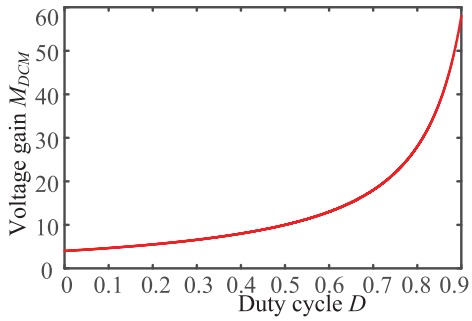


Fig. 12. Voltage gain against duty ratio of the proposed converter under *DCM* operation, $N = 2$, $R = 533\ \Omega$, $f_s = 50$ kHz, $L_2 = 336\ \mu$H, and $K = 1$.

$$V_{C_3} = V_{C_1} + V_{C_2} + NV_{C_1}. \tag{21}$$

The peak value of the magnetizing inductor current can be formulated as

$$I_{L_{2\mathrm{MP}}} = \frac{V_{\mathrm{in}}}{L_2} DT_S. \tag{22}$$

In the intervals of Modes III, IV, V, and VI, the following equations can be expressed based on Fig. 8(c)–(f):

$$V_{L_1}^{\mathrm{III}} = V_{L_1}^{\mathrm{IV}} = V_{L_1}^{\mathrm{V}} = V_{L_1}^{\mathrm{VI}} = V_{\mathrm{in}} - V_{C_1} \tag{23}$$

$$V_{C_4} = -V_{L_3}^{\mathrm{III}} = -V_{L_3}^{\mathrm{IV}} = -V_{L_3}^{\mathrm{V}} = -V_{L_3}^{\mathrm{VI}} \tag{24}$$

$$V_{L_2}^{\mathrm{III}} = V_{L_2}^{\mathrm{IV}} = V_{L_2}^{\mathrm{V}} = V_{L_2}^{\mathrm{VI}} \tag{25}$$

$$V_{C_2} = V_{C_4} - V_{L_2}^{\mathrm{III}} \tag{26}$$

$$V_o = V_{C_1} - (N+1)V_{L_2}^{\mathrm{III}} + V_{C_3}. \tag{27}$$

In the Mode VII, based on Fig. 8(g), the following equations are written as follows:

$$V_{L_1}^{\mathrm{VII}} = V_{\mathrm{in}} \tag{28}$$

$$V_{L_2}^{\mathrm{VII}} = 0 \tag{29}$$

$$V_{L_3}^{\mathrm{VII}} = 0. \tag{30}$$

Using the volt-second balancing principle on L_1, L_2, and L_3, the following equations can be written as

$$\int_0^{DT_S} V_{L_1}^{\mathrm{I}} dt + \int_{DT_S}^{T_S} V_{L_1}^{\mathrm{III}} dt = 0 \tag{31}$$

$$\int_0^{DT_S} V_{L_2}^{\mathrm{I}} dt + \int_{DT_S}^{(D+D_L)T_S} V_{L_2}^{\mathrm{IV}} dt = 0 \tag{32}$$

$$\int_0^{DT_S} V_{L_3}^{\mathrm{I}} dt + \int_{DT_S}^{(D+D_L)T_S} V_{L_3}^{\mathrm{III}} dt = 0. \tag{33}$$

Substituting (18)–(29) into (31), (32), and (33), the voltage conversion ratio can be expressed as

$$M_{\mathrm{DCM}} = (2 + N + ND)(D_L + D)/(1 - D)D_L. \tag{34}$$

Besides, on the basis of (34), the duty cycle D_L can be computed as

$$D_L = DV_{\mathrm{in}}(2 + N + ND)/[V_o(1 - D) - (2 + N + ND)V_{\mathrm{in}}]. \tag{35}$$

The average current of I_{C_o} is given as

$$I_{C_o} = \frac{D_L I_{L_{2MP}}}{4N + 2} - I_o = 0. \tag{36}$$

Then, the following equation is derived:

$$\frac{(2 + N + ND)D^2 V_{\mathrm{in}}^2 T_S}{(4N + 2)\left[V_o(1 - D) - (2 + N + ND)V_{\mathrm{in}}\right] L_2} = \frac{V_o}{R}. \tag{37}$$

Therefore, the normalized magnetizing-inductor time constant is defined as

$$\tau_{L_M} \equiv \frac{L_2 f_S}{R} \tag{38}$$

where f_S is the switching frequency.

Substituting (38) into (37), the voltage conversion ratio can be obtained as follows:

$$M_{\mathrm{DCM}} = \sqrt{\frac{(2 + N + ND)D^2}{(4N + 2)(1 - D)\tau_{L_M}} + \frac{(2 + N + ND)^2}{4(1 - D)^2}} + \frac{(2 + N + ND)}{2(1 - D)}. \tag{39}$$

The voltage conversion under *DCM* is shown in Fig. 12.

C. Boundary Operating Condition Between CCM and DCM

When the proposed converter is operated in the boundary-condition mode, the voltage conversion ratios in *CCM* and *DCM* are equal. According to (17) and (39), the boundary normalized magnetizing-inductor time constant $\tau_{L_{MB}}$ can be derived as

$$\tau_{L_{MB}} = \frac{4D(1 - D)^3}{(2 + N + ND)(4N + 2)}. \tag{40}$$

Therefore, the wave of $\tau_{L_{MB}}$ is shown in Fig. 13. Based on Fig. 13(a), it can be observed that the value of $\tau_{L_{MB}}$ downgrades as the turn ratio upgrades, and the maximum values under different turn ratios are provided. As turn ratio changes continuously, the three-dimensional figure in Fig. 13(b) can clearly show this process. It can be clearly seen that when τ_{L_M} is larger than $\tau_{L_{MB}}$, the proposed converter is operated in *CCM*.

D. Voltage Stress Analysis

To simplify the analysis, the influence of the leakage coefficient is ignored. Based on the above analysis, voltage stresses

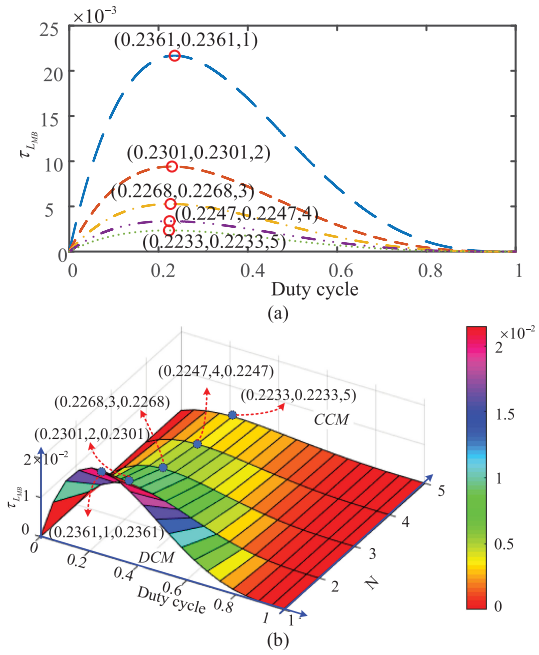


Fig. 13. Boundary values of *CCM* and *DCM* for various *N*. (a) Boundary values of *CCM* and *DCM* under $N = 1$, $N = 2$, $N = 3$, $N = 4$, and $N = 5$. (b) Boundary values of *CCM* and *DCM* for various *N*.

across the diodes D_1, D_2, D_3, D_5, and D_o are derived as

$$V_{D_1} = (1-D)V_o/(2+N+ND) \tag{41}$$

$$V_{D_2} = DV_o/(2+N+ND) \tag{42}$$

$$V_{D_3} = V_{D_5} = (N+1)V_o/(2+N+ND) \tag{43}$$

$$V_{D_o} = (N+1)V_o/(2+N+ND). \tag{44}$$

In Mode III, the secondary-side inductor is clamped by capacitors C_3 and C_4. Therefore, the voltage stress of the clamped diode can be obtained as follows:

$$V_{D_4} = NV_o/(2+N+ND). \tag{45}$$

Therefore, the voltage stress on the active switch can be expressed as

$$V_{\rm DS} = V_o/(2+N+ND). \tag{46}$$

E. Current Stress Analysis

In order to simplify the calculation, the extremely short time intervals $[t_0 - t_1]$ and $[t_2 - t_3]$ are ignored. When the magnetizing inductor L_M is large enough, the magnetizing current is considered as a constant. The simplified waveforms of the proposed converter are shown in Fig. 14. The average current flowing through the output diode D_o can be expressed as

$$I_{D_o} = I_o/(1-D). \tag{47}$$

During one switching period, the electric charge through the capacitors is zero. The time interval can be approximately obtained as

$$t_{2-6} = 2(1-D)T_s/(N+2) \tag{48}$$

$$t_{6-7} = (1-D)T_S - t_{2-6} = (1-D)NT_s/(N+2). \tag{49}$$

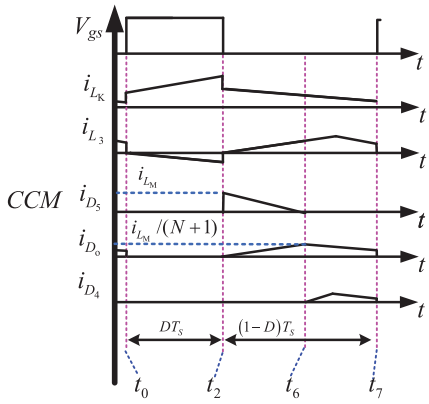


Fig. 14. Simplified waveforms.

During the time interval $[t_2, t_6]$, the average current flowing through the diode D_5 is calculated as

$$I_{D_5[t_2-t_6]} = I_o(N+2)/2(1-D). \tag{50}$$

During the time interval $[t_6, t_7]$, the average current flowing through the diode D_4 can be derived as

$$I_{D_4[t_6-t_7]} = I_o(N+2)/(N-ND). \tag{51}$$

Therefore, during the time interval $[t_0, t_2]$, the current through the secondary side of the coupled inductor can be obtained as

$$I_{L_3[t_0-t_2]} = I_o/D. \tag{52}$$

During the time interval $[t_2, t_7]$, by using Kirchhoff's current law, at the junction point of the secondary side L_3, diode D_4, and capacitor C_3, the current through the secondary side L_3 can be written as

$$I_{L_3[t_2-t_7]} = 2(N+1)I_o/(N-ND). \tag{53}$$

Then, the current through the primary side can be expressed as

$$I_{L_2[t_2-t_7]} = I_o/(1-D). \tag{54}$$

According to the magnetic flux conversation principle and Fig. 10, the following equation is given as

$$I_{L_2[t_0-t_2]} + NI_{L_3[t_0-t_2]} = I_{L_2[t_2-t_7]} + NI_{L_3[t_2-t_7]}. \tag{55}$$

Collecting the terms, during the time interval $[t_0, t_2]$, the average currents flowing through the primary side L_P can be obtained as

$$I_{L_2[t_0-t_2]} = (3ND+3D-N)I_o/D(1-D). \tag{56}$$

Therefore, during the time interval $[t_0, t_2]$, the current of capacitor C_1 is given as

$$I_{C_1[t_0-t_2]} = (3ND+2D+1-N)I_o/D(1-D) \tag{57}$$

$$I_{C_1[t_2-t_7]} = (3ND+2D+1-N)I_o/(1-D)^2. \tag{58}$$

Similarly, during the time interval $[t_2, t_7]$, while using Kirchhoff's circuit laws (KCL), at the junction point of the inductor L_1, diode D_1, and capacitor C_1, the current of the inductor L_1 can be written as

$$I_{L_1[t_2-t_7]} = (3ND+D+2-N)I_o/(1-D)^2. \tag{59}$$

TABLE II
PERFORMANCE COMPARISON AMONG DIFFERENT CONVERTERS

Regular	Converter in [17]	Converter in [16]	Proposed converter
Numbers of active switches	1	1	1
Numbers of diodes	5	6	6
Voltage gain	$(2+N)/(1-D)^2$	$[N(3D+2)+2-D]/(2-2D)^2$	$(2+N+ND)/(1-D)^2$
Voltage stress of active switch	$V_o/(N+2)$	$(2+ND-D)V_o/(3ND+2N+2-D)$	$V_o/(2+N+ND)$
Voltage stress of output diode	$(1+N)V_o/(N+2)$	$2NV_o/(3ND+2N+2-D)$	$(N+1)V_o/(2+N+DN)$
Voltage stress of output capacitor	V_o	V_o	$(N+1)V_o/(2+N+DN)$

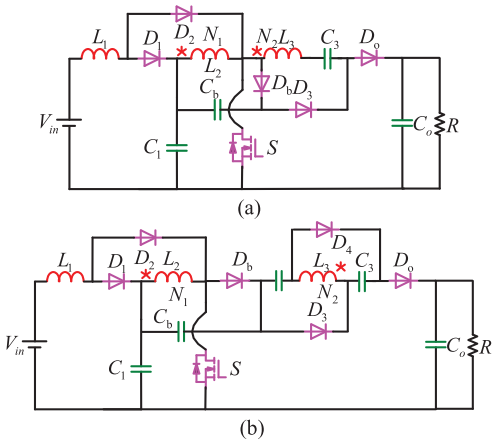


Fig. 15. Configuration diagram used for comparison purposes: (a) Converter with voltage lift cell in [17]. (b) Converter with voltage multiplier cell in [16].

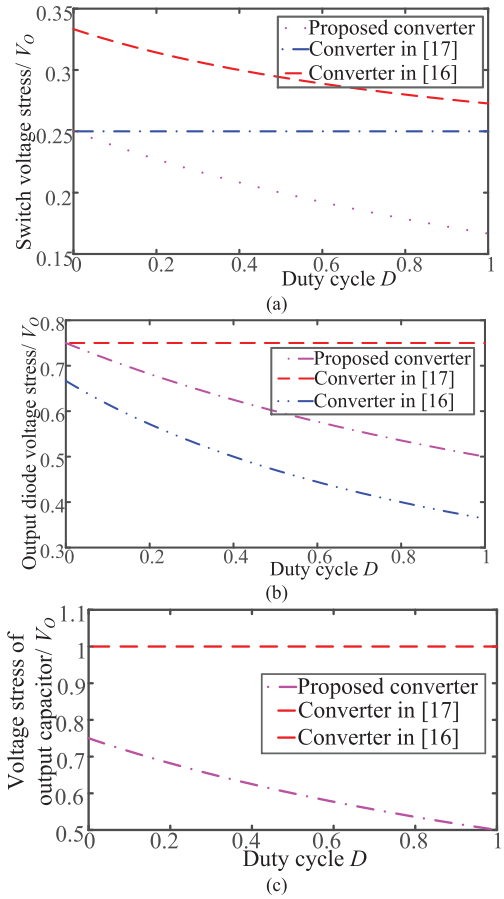


Fig. 16. Performance comparison among different converters under $N = 2$. (a) Switch voltage stress comparison. (b) Output diode voltage stress comparison. (c) Output capacitor voltage stress comparison.

Based on the ideal gain expression, during one switching period, the average current of the inductor L_1 can be calculated as

$$I_{L_1} = (2 + N + ND)I_o/(1 - D)^2. \tag{60}$$

According to the equivalence principle, during the time interval $[t_0, t_2]$, the average current of the inductor L_1 can be expressed as

$$I_{L_1[t_0-t_2]} = (2N - 2ND - D)I_o/D(1 - D)^2 \tag{61}$$

$$I_{L_1} = I_{L_1[t_2-t_7]}(1 - D) + I_{L_1[t_0-t_2]}D. \tag{62}$$

So, the root mean square (RMS) value of the switch S is

$$I_{S-\mathrm{RMS}} = \frac{\left(N + 2ND + 3D - 3ND^2 - 3D^2\right)\sqrt{D}P_o}{D(1 - D)^2V_o} \times \sqrt{\frac{K_L^2}{12} + 1} \tag{63}$$

where K_L is defined as $\Delta I_{L_K} = K_L I_{L_K[t_0,t_2]}$.

F. Comparative Analysis of Performance

For the sake of demonstrating the performance, the proposed converter is compared with those published in [16] and [17] as shown in Table II. On the basis of Table II and Fig. 15, the comparisons of voltage stresses of active switch, output capacitor, and output diode of three different circuits are, respectively, drawn under $N = 2$, as shown in Fig. 16(a), (b), and (c). Compared with the converter in [17], the number of diodes in the proposed converter is larger, but the number of the switch is same. Moreover, the voltage stresses of switch, output capacitor, and output diode of the proposed converter are lower. Therefore, the low-voltage rated switch and diode can be selected to improve efficiency and using low-voltage rated output capacitor increases power density. Although the numbers of the switch and diode is the same, the output diode voltage of the proposed converter is higher than that of the converter in [16]. Fortunately, the voltage stress of the switch of the proposed

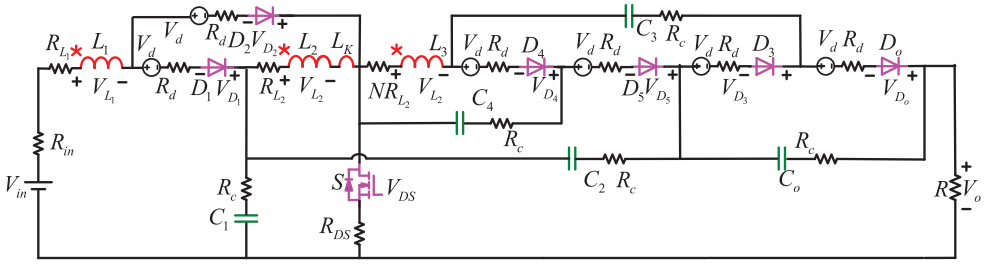


Fig. 17. Equivalent circuit based on parasitic parameters.

converter is less than that of the converter in [16]. Besides, the voltage stress of the output capacitor is far less than that of the converter so that it can be used to increase power density. Moreover, according to Fig. 11, the voltage gain of the proposed converter is higher than that of two other converters throughout the duty cycle range.

G. Analysis of Conduction Losses

The efficiency of the converter is affected by parasitic parameters. Thereby, all devices are assumed to be nonideal semiconductor device. In order to facilitate a functional analysis, many losses, such as the switching losses, the leakage inductor losses, magnetic core losses, and diode reverse recovery losses, are neglected. The equivalent circuit of the proposed converter is shown in Fig. 17, in which $R_{\rm in}$ denotes the resistances of the input source; R_{L_1} means the copper resistances of the inductor L_1; R_{L_2} represents the copper resistance of the primary side of the coupled inductor; $R_{\rm DS}$ and R_c are the conduction resistances of the active switch and capacitor, respectively; and V_d and R_d denote the forward voltage drop and the on-state resistance of the all diodes, respectively.

The small-ripple approximation method is used to approximate all the current through components by the dc components. Then, through voltage-second balance and capacitor-charge balance, the voltage gain including conduction losses can be derived as

$$M_{\rm CCM} = \frac{M_{\rm CCM} - \frac{(6N+ND-4D)V_d}{(1-D)V_{\rm in}}}{1+\frac{A_{L_2}R_{L_2}}{R}+\frac{A_dR_d}{R}+\frac{A_{\rm DS}R_{\rm DS}}{R}+\frac{A_{\rm in}(R_{\rm in}+R_{L_1})}{R}+\frac{A_cR_c}{R}} \tag{64}$$

where $A_{L_2}=\frac{2N^2D+3ND-N^2+3N^2D^2+6D^2N+6D+N}{D(1-D)^2}$ unnumbered eq. shown at the bottom of this page.

Based on the above analysis, the theoretical efficiency of the proposed converter is gained as

$$\eta=\frac{1-\frac{(6N+ND-4D)V_d}{(1-D)V_{\rm in}M_{\rm CCM}}}{1+\frac{A_{L_2}R_{L_2}}{R}+\frac{A_dR_d}{R}+\frac{A_{\rm DS}R_{\rm DS}}{R}+\frac{A_{\rm in}(R_{\rm in}+R_{L_1})}{R}+\frac{A_cR_c}{R}}. \tag{65}$$

Meanwhile, the theoretical efficiency of the converters in [16] and [17] is obtained according to the derivation process of the proposed converters.

IV. Parameters Design

A. Turns Ratio Design

The voltage stress of the switch and the operational duty cycle of the converter can be decided by the turns ratio of the coupled inductor, therefore, it is the major parameter in the circuit parameter design. Once the duty cycle is designed (in general, the optimal duty cycle is about $0.4\sim0.6$), an appropriate turns ratio can be acquired, which is written by

$$N=\left[V_o(1-D)^2-2V_{\rm in}\right]/\left[V_{\rm in}\left(1+D\right)\right]. \tag{66}$$

B. Magnetizing Inductor Design

Based on Fig. 7(d) and (48) and (50), the average magnetic current of the coupled inductor can be computed as

$$I_{L_M}=\left(N+2\right)I_{\rm o}/(1-D). \tag{67}$$

The magnetizing inductor can be designed by setting an acceptable current ripple on the magnetizing inductor, which

$$A_d=\frac{1}{D}+\frac{2N-2ND+(N+2)^2}{2N(1-D)}+\frac{(2ND+2+N-2D-3ND^2-D^2)}{(1-D)^3}$$

$$A_{\rm DS}=\frac{N+2+(8N+8N^2-2)-D^2(7N^2+3N+2)-11ND^3-3N^2D^4-10D^3}{D(1-D)^3}$$

$$A_{\rm in}=\frac{4ND-4D+4+4N-9ND^2-2D^2+3N^2D+N^2-4N^2D^2-ND^2}{(1-D)^4}$$

$$A_c=\frac{3N^2D+2ND+4N-ND^2+2D}{DN(1-D)}+\frac{(1+D)(N+1)(3ND+4D-N-D^2)}{D(1-D)^3}$$

is represented by

$$L_M \geq \frac{V_{\text{in}} D}{K_{L_M} I_{L_M} f_s}. \tag{68}$$

Combining (67) and (68) and collecting the terms, the magnetizing inductor can be gained as

$$L_M \geq \frac{V_{\text{in}}\ D(1-D)}{K_{L_M}\ (N+2)\, I_o f_s} \tag{69}$$

where K_{L_M} is the current ripple coefficient.

C. Output Capacitor Design

The purpose of the output capacitor C_o is to limit the output voltage ripple ΔV to a reasonable range. When the switch is turned on, the capacitor C_o releases energy to the load. Therefore, the electric charge can be written as follows:

$$\Delta Q = I_o D T_s \leq C_o \Delta V. \tag{70}$$

Besides, the output capacitor can be chosen as

$$C_o \geq V_o D/(\Delta V R f_s). \tag{71}$$

D. Small-Signal Mode of the Proposed Converter

In order to simplify the analysis for a small signal model of the presented converter in *CCM*, only modes II, IV, and VII are considered in the analytic process. According to the reference in [21], the state vector is defined as

$$x = [i_{L_1} i_{L_2} i_{L_3} \mu_{C_1} \mu_O]' \tag{72}$$

$$k\dot{x} = Ax + Bu. \tag{73}$$

And the input is defined as

$$u = [\mu_{\text{in}}]. \tag{74}$$

The average model of the proposed converter can be obtained by averaging the state equations of the ON period and OFF period (neglecting the short operating intervals). The converter is assumed to operate in *CCM*. Based on the model II, during switch-ON time $(0 - dT_S)$ the following state matrices are given as

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1/L_2 & 0 \\ 0 & 0 & 0 & N/L_3 & 0 \\ 0 & -1/C_1 & 1/C_1 & 0 & -1/RC_1 \\ 0 & N/C_1 & -N/C_1 & 0 & N/RC_1 - 1/RC_O \end{bmatrix} \quad \text{and}$$

$$B_1 = \begin{bmatrix} 1/L_1 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}. \tag{75}$$

Based on the model IV, during switch-OFF time $(dT_S - \alpha T_S)$, the following state matrix equations are written by:

$$A_2 = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{N+2}{2L_2(N+1)} & \frac{-1}{2L_2(N+1)} \\ 0 & 0 & 0 & \frac{N(N+2)}{2L_3(N+1)} & \frac{-N}{2L_3(N+1)} \\ \frac{1}{C_1} & 0 & 0 & 0 & \frac{-1}{RC_1} \\ \frac{N}{C_1} & 0 & \frac{2}{C_O} & 0 & \frac{N}{RC_1} - \frac{2}{RC_O} \end{bmatrix} \quad \text{and}$$

$$B_2 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}. \tag{76}$$

Based on the model VII, during mode V $(\alpha T_S - T_S)$, the following state matrix equations are obtained:

$$A_2 = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{N+2}{2L_2(N+1)} & \frac{-1}{2L_2(N+1)} \\ 0 & 0 & 0 & \frac{N(N+2)}{2L_3(N+1)} & \frac{-N}{2L_3(N+1)} \\ \frac{1}{C_1} & 0 & 0 & 0 & \frac{-1}{RC_1} \\ \frac{N}{C_1} & \frac{2}{C_O} & 0 & 0 & \frac{N}{RC_1} - \frac{2}{RC_O} \end{bmatrix} \quad \text{and}$$

$$B_2 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}. \tag{77}$$

According to the reference in [21], the following state space average matrix equations are obtained:

$$A = A_1 d + A_2(\alpha - d) + A_3(1 - \alpha) \tag{78}$$

$$B = B_1 d + B_2(\alpha - d) + B_3(1 - \alpha) \tag{79}$$

where α is equal to $d + d_c$, and d_c means the duty cycle of the electric charge.

Finally, (80) shown at the bottom of the next page can be gained

By introducing perturbation, the state variables and the duty cycle of the matrix are replaced by the sum of dc and ac (perturbation) terms as follows:

$$d = D + \hat{d}; i_{L_1} = [I_{L_1} + \hat{i_{L_1}}]; i_{L_2} = [I_{L_2} + \hat{i_{L_2}}];$$
$$i_{L_3} = [I_{L_3} + \hat{i_{L_3}}]; \mu_{C_1} = [V_{C_1} + \hat{\mu_{C_1}}]; \mu_{C_O} = [V_{C_O} + \hat{\mu_{C_O}}] \tag{81}$$

where I_{L_1}, I_{L_2}, I_{L_3}, V_{C_1}, and V_O are the steady-state values of the state variables, respectively.

Substituting (62) into (54), linearizing the final results and neglecting the higher order perturbation terms, and then removing the steady-state quantities, the small signal ac model of the converter is provided as follows:

$$k\frac{d(\hat{x})}{dt} = A\hat{x} + B\hat{u} + F\hat{d}. \tag{82}$$

When $A = 0$ and $B = 0$, the averaged dc matrix is used to derive the steady-state expressions of the state variables as follows:

$$\begin{cases} I_{L_1} = \dfrac{V_O}{R(1-D)}\left(1 + \dfrac{D(N-1)}{N - ND_c + 2D_c - 2D}\right) \\ I_{L_2} = NI_{L_3} \\ I_{L_3} = \dfrac{2V_O}{(N - ND_c + 2D_c - 2D)R} \\ V_{C_1} = \dfrac{(1-D)V_O}{(N+2+ND)} \\ V_O = V_O \end{cases}. \tag{83}$$

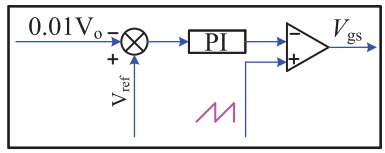


Fig. 18. Control block diagram of the proposed converter.

Besides, the equations are gained as follows:

$$F = \begin{bmatrix} \dfrac{(1-D)V_O}{(N+2+ND)L_1} = A_{13} \\ \dfrac{V_O\left(1 - \dfrac{1-D}{N+2+ND}\right)}{(N+2)L_2} = A_{33} \\ \dfrac{NV_O\left(1 - \dfrac{1-D}{N+2+ND}\right)}{(N+2)L_3} = A_{23} \\ \dfrac{2V_O(1-N)}{R(1-D)C_1Q} - \dfrac{2V_O(1+D)}{R(1-D)C_1} = A_{45} \\ \dfrac{6V_O}{RC_O} - \dfrac{NV_O}{RC_1} - \left(\dfrac{2}{C_O} + \dfrac{N}{C_1}\right)\dfrac{2V_O(1-N)}{RQ} \\ \quad + \dfrac{2NV_O}{R(1-D)C_1}\left(1 + \dfrac{D-ND}{RQ}\right) = A_{55} \end{bmatrix} \tag{84}$$

where Q is equal to $N - Nd_c + 2d_c - 2D$.

By adopting the Laplace transform of (84), the corresponding control-to-output transfer function can be obtained in (85) shown at the bottom of the next page.

The control block diagram of the presented converter is shown in Fig. 18. It can be seen that the controller is extremely simple and easy to implement. And it can be realized by using either digital or analog circuits.

$$A = \begin{bmatrix} 0 & 0 & 0 & A_{12} = \dfrac{-(1-d)}{L_1} & 0 \\ 0 & 0 & 0 & A_{21} = \dfrac{N+2+Nd}{2L_2(N+1)} & A_{22} = \dfrac{-(1-d)}{2L_2(N+1)} \\ 0 & 0 & 0 & A_{31} = N\dfrac{N+2+Nd}{2L_2(N+1)} & A_{32} = N\dfrac{-(1-d)}{2L_2(N+1)} \\ A_{41} = \dfrac{1-d}{C_1} & A_{42} = \dfrac{d}{C_1} & A_{43} = \dfrac{d}{C_1} & 0 & A_{44} = \dfrac{-1}{RC_1} \\ A_{51} = \dfrac{-N(1-d)}{C_1} & A_{52} = \dfrac{Nd}{C_1} + \dfrac{2-2d_c}{C_O} & A_{53} = \dfrac{-Nd}{C_1} + \dfrac{2d_c-2d}{C_O} & 0 & A_{54} = \dfrac{N}{RC_1} - \dfrac{2}{RC_O} \end{bmatrix}$$

and $B = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$ (80)

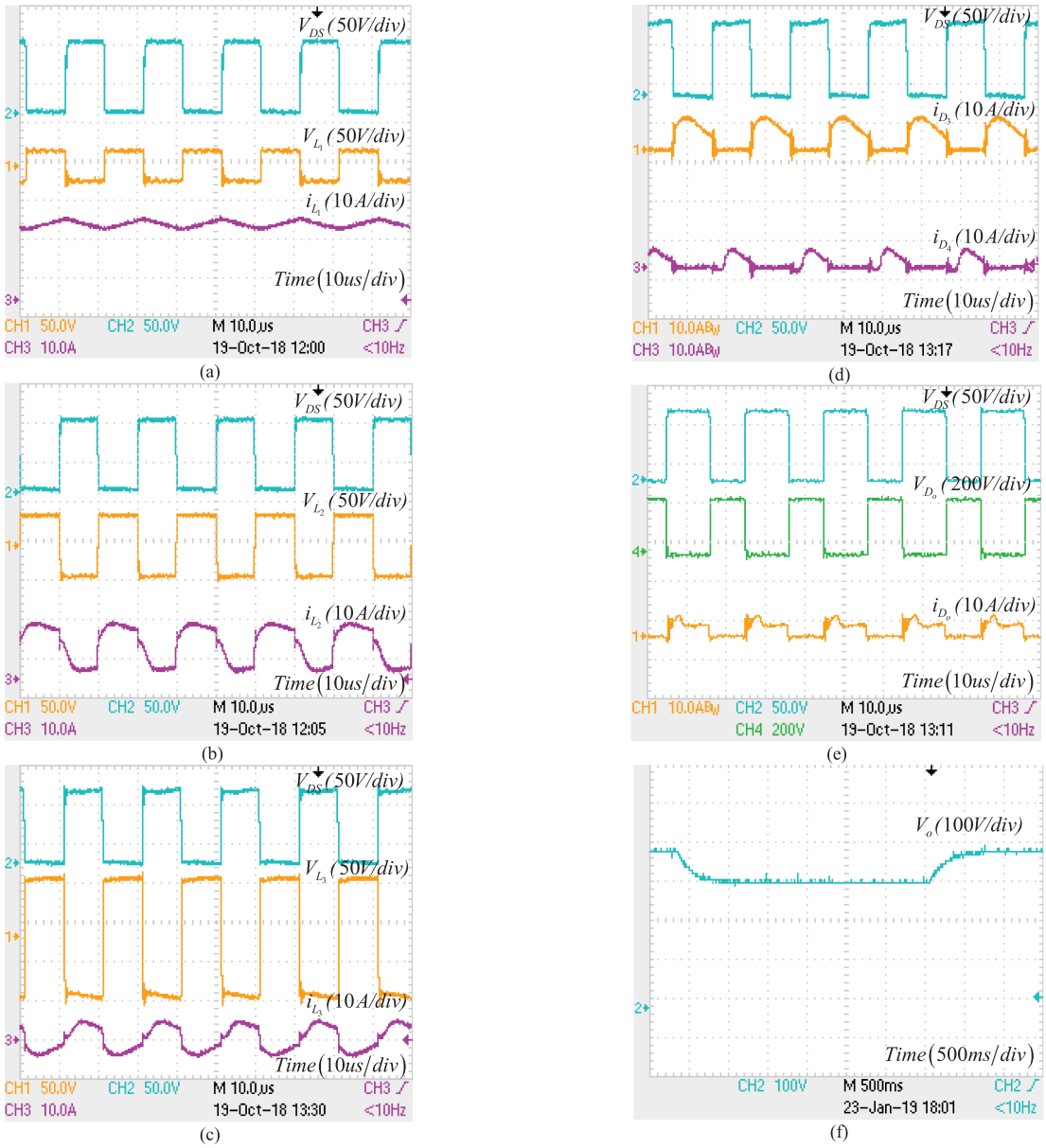


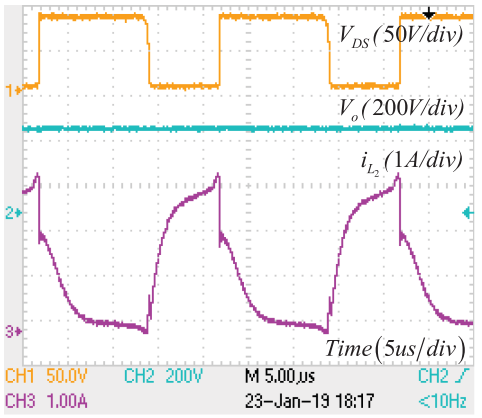
Fig. 19. Experimental waveforms of the presented converter under *CCM*. (a) $V_{\rm DS}$, V_{L_1}, and i_{L_1}. (b) $V_{\rm DS}$, V_{L_2}, and i_{L_2}. (c) $V_{\rm DS}$, V_{D_O}, and i_{L_3}. (d) $V_{\rm DS}$, i_{D_3}, and i_{D_4}. (e) $V_{\rm DS}$, V_{D_O}, and i_{D_O}. (f) V_O.

V. Experimental Verification

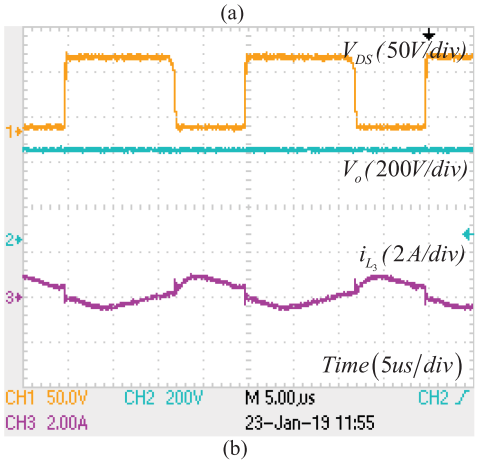
To verify the operating principle of the proposed converter, a prototype circuit is established in the laboratory and the specifications of its components are shown in Table III.

The presented converter is operated at *CCM* and its experimental waveforms are shown in Fig. 19(a)–(f) under the rated conditions. When the duty cycle is about 0.46, the voltage $V_{\rm DS}$ on the active switch is clamped about 87 V, as shown in Fig. 19(a), and the current and voltage across the inductor L_1 are also plotted in the picture. It can be seen that the current ripple of the input current (i_{L_1}) is small. Furthermore, the current and voltage from the primary side and secondary

$$G(S) = \frac{[A_{51}A_{13} + (A_{52} + \frac{L_2A_{53}}{L_3})A_{23} + SA_{55}][S^2 - A_{12}A_{41} - A_{21}(A_{42} + \frac{L_2A_{42}}{L_3} - SA_{44})] + M[A_{41}A_{13} + A_{22}(A_{42} + \frac{L_2A_{43}}{L_3})]}{[S^2 - (A_{52} + \frac{L_2A_{53}}{L_3})A_{22} - SA_{54}][S^2 - A_{12}A_{41} - A_{21}(A_{42} + \frac{L_2A_{42}}{L_3}) - SA_{44}] + MA_{22}(A_{42} + \frac{L_2A_{43}}{L_3})} \tag{85}$$



(a)



(b)

Fig. 20. Experimental waveforms of the presented converter under *DCM*. (a) $V_{\rm DS}$, i_{L_2}, and V_O. (b) $V_{\rm DS}$, i_{L_3}, and V_O.

TABLE III
SYSTEM PARAMETERS OF THE PROPOSED CONVERTER

System parameters	Specifications
Input voltage V_{in}	30 V
Output voltage V_o	400 V
Rated power P_o	300 W
Switching frequency: f	50 kHz
MOSFET Switch S	IRFP4568
Diodes D_1, D_2, D_4	VF30200C
Diodes D_3, D_5, D_o	FFA40UP35S
Capacitor C_1	100 μF
Capacitors C_2 , C_o	20 μF
Capacitors C_3 , C_4	10 μF
Inductor L_1	560 μH
Coupling inductors	$N = N_2 : N_1 = 2$, Core-ER49, $N = 33:17$, $L_M = 87.8$ μH, $L_K = 0.71$ μH

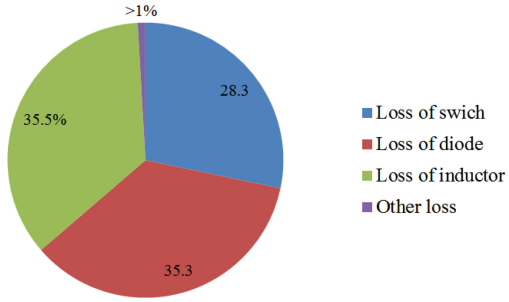
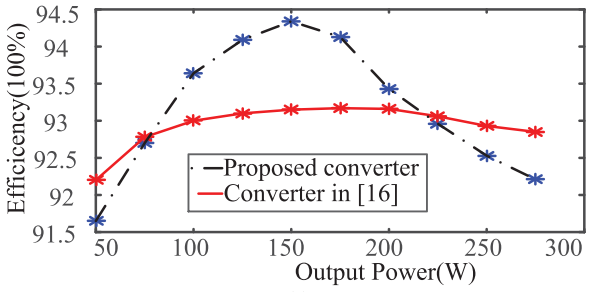
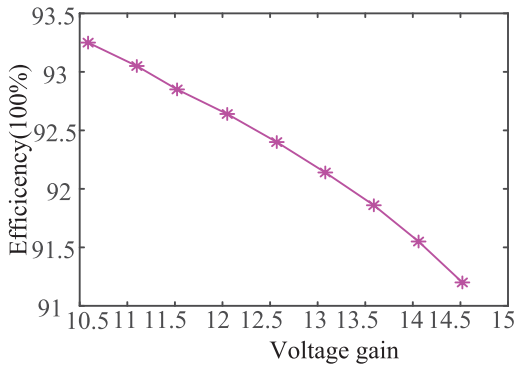


Fig. 22. Pie graph of loss breakdown at full load.



(a)



(b)

Fig. 21. Converter efficiency. (a) Efficiency of different converters. (b) Test efficiency versus voltage gain.

side of the coupled inductor are shown in Fig. 19(b) and (c), respectively. Fig. 19(d) shows the currents of the diodes D_3 and D_4, and the current of the clamped diode D_4 increases from zero. The current and voltage waveforms of the output diode are shown in Fig. 19(e), and the voltage is about 230 V. Then, the dynamic response performance of the proposed converter and the experimental result of the output voltage under the step load changing between 800 and 533 Ω are depicted in Fig. 19(f).

When the proposed converter in *DCM* operation works at $V_{\rm out} = 380$ V and $P_o = 80$ W, the currents of the primary side and secondary side of the coupled inductor are shown in Fig. 20(a) and (b), respectively. It can be seen that there is intermittent currents appearing in the coupled inductor and the output voltage is about 380 V as shown in the pictures. Therefore, it can be concluded that the theoretical analysis results are coincident with the experiments results here. Finally, the relationship between efficiency and output power variations is shown in Fig. 21(a). The maximum efficiency is about 94.4% at $P_o = 150$ W. Besides, the relationship between efficiency and voltage gain of the proposed converter at $R = 533$ Ω and $V_{\rm in} = 30$ V is shown in Fig. 21(b). The efficiency analysis is shown in Fig. 22 and it can be deduced that the loss of switch and diodes reaches 63.6%.

VI. Conclusion

In this article, novel passive lossless clamped circuits, which are composed of two capacitors and one diode, are proposed. One of the most important features is that one of two capacitors in the clamped circuits is used to construct a flowing path to release the energy stored in the leakage inductor and the other is used to absorb the leakage energy. Moreover, it is more flexible than the classical passive lossless clamped circuit and the number of the extra devices has not changed. Based on VLC, SVMC, and AVMC, a family of cascade dc–dc converters, which adopts the novel clamped circuit, is proposed. A converter topology deduced is taken as a representative, which is selected and analyzed in detail. As a result, the coupled inductor technology and the passive lossless clamped circuit are successfully integrated by the converter. Therefore, the efficiency is improved and the theoretically analyzed results are coincident with the experimental ones.

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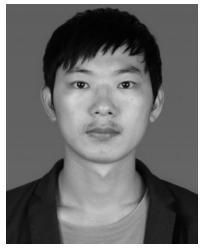

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