Thermal Stress Based Power Routing of Smart Transformer With CHB and DAB Converters

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***Abstract*—The smart transformer (ST) is a potential solution for an upgrade of the electric distribution grid, which enables to provide services to the grid and dc connectivity. However, the power electronics within the system are challenged by high reliability requirements. One possible solution to increase the reliability is to employ prognosis to predict the failures and avoid down times of the system. Traditional maintenance scheduling is based on the remaining useful lifetime (RUL) of the individual components or the forecasted failure probability. For a further increase of the time to the next maintenance, it is desired to have similar wear out of all components, which need to be maintained or exchanged. In this article, it is proposed to route the power internally in a modular power converter consisting of a cascaded H-bridge connected to dual active bridges in order to influence the RUL of its building blocks. Therefore, a thermal stress based wear-out control is designed for addressing the processed power dependent failures of the devices in the building blocks of the ST. Compared to the conventional power routing methods, the impact of the proposed system-level control considering electrical and thermal parameter variations is demonstrated using Monte Carlo analysis.**

***Index Terms*—Cascaded H-bridge, dual active bridge, power routing, reliability, smart transformer, thermal stress.**

I. Introduction

THE paradigm shift from fossil fuels to green technologies in the energy production has altered the conventional power system network with higher share of renewable energy sources and electric vehicle charging stations. This has posed challenges in the electrical distribution network with spatially distributed generations and bidirectional power flow. The smart transformer (ST) is a promising solution to address the power flow flexibility while catering the requirements of changing grid scenarios [1], [2]. However, expected lower reliability is one of the key challenges of the ST compared with the conventional low-frequency transformer.

One of the possible solutions to increase the system reliability is to carry out maintenance schedules based on prognosis. Prognosis is a technical process resulting in the determination of remaining useful lifetime (RUL). There are many scientific publications regarding the prognostic maintenance scheduling in high reliability industrial applications, aviation sector, etc., [3], [4]. However, fewer references investigate the maintenance scheduling focusing on the system level control algorithms to delay the maintenance. Since the ST is a modular system with multiple stages possibly located in remote areas, frequent maintenance schedules can result in very high costs. Therefore, a system level thermal-stress controller is proposed to optimize the maintenance schedules.

In order to develop a system level thermal stress control, the critical components and factors are to be identified. Power electronic devices and capacitors contribute to the major failures in converter systems [5], [6]. Power cycling of the devices resulting in thermal cycles is considered to be the crucial factor for the aging of devices. The existing literature mainly focuses on device level and converter level reliability by actively controlling the thermal cycles by different methods such as switching frequency control, active gate drivers, and modulation techniques [7]–[9]. For improving the reliability of a modular converter system comprising of many cells, the aging of the cells can be actively controlled by unequal sharing of the power depending on the remaining useful life of each module [10], [11]. Power routing using virtual resistance method is studied for low voltage inverter of the ST in [12]. For an ST composed of cascaded H-bridge (CHB) and dual active bridge (DAB) converters, power routing technique with virtual resistance is introduced in [13].

This article studies the impact of unequal power sharing on the reliability of the ST on a system level and the development of a power routing controller for the overall system. Power routing is achieved using virtual resistances for thermal stress control in the modular ST comprised of CHB converter cells and DAB cells as shown in Fig. 1. Virtual resistances provide the power references for each unit of the ST depending on the aging of that unit. The control of power flow through the cells based on their aging results in thermal stress based wear-out control of the overall system. Thus, the maintenance scheduling can be optimized in order to reduce the maintenance costs. Compared to the virtual resistance based methods in [12] and [13], a generalized validation of the impact of a system level power

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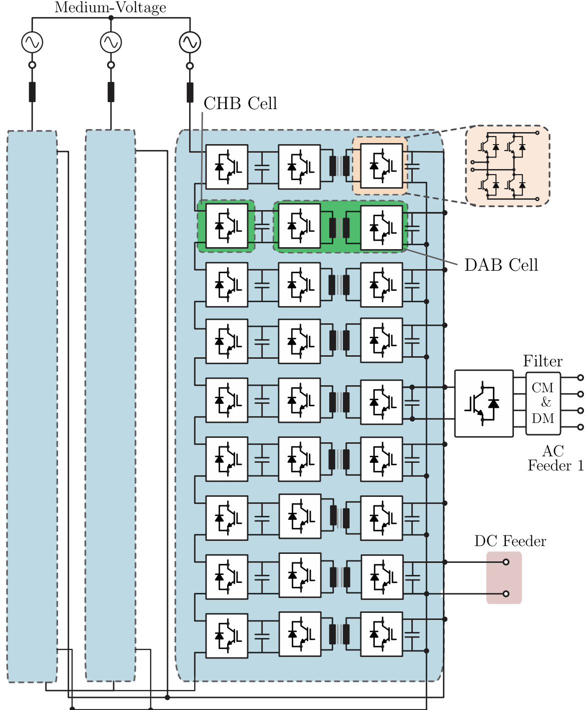


Fig. 1. ST architecture with CHB and DAB.

routing technique considering parameter variations using Monte Carlo analysis is provided in this article. Moreover, detailed analysis and experimental results along with a collector emitter voltage sensor for junction temperature estimation are presented as well.

The article is organized as follows. Section II introduces the investigated ST architecture and provides the motivation for the thermal stress based wear-out control. Design of the thermal stress based power routing controller based on virtual resistances is explained in Section III. Section IV discusses the implementation of the proposed power routing scheme in the laboratory setup and the effect on thermal stress due to power routing is illustrated. The impact of thermal stress based wear-out on the system RUL without and with the proposed control scheme is studied in Section V, and finally a conclusion is drawn in Section VI.

II. Power Routing in ST on System Level

This section introduces the reliability challenges in the ST and lays down the theoretical background of the proposed strategy for improving the reliability of the ST. The system description of the ST prototype is also presented.

A. Semiconductor Reliability Challenges

As discussed in the introduction, power electronic devices are one of the main sources of failures and thereby posing challenges to the reliable operation of the ST. To analyze the root cause of failures in power semiconductors, physics-of-failure approach has become the state of the art. Accordingly, the junction temperature fluctuations influence the aging and deterioration of the power modules as expressed in (1). Here, N_f denotes the number of thermal cycles to failure depending on the thermal swing ΔT, average junction temperature $T_{j,\mathrm{av}}$, and the device dependent parameters a_1, a_2, and a_3. The parameter $a_2 \approx 5$ makes N_f highly sensitive to junction temperature variations [14], [15]

TABLE I
ST Specification

Rated Power	MVAC	LVAC	Grid frequency	LVDC
1 MVA	10 kV	400 V	50 Hz	800 V

$$N_f = a_1(\Delta T)^{a_2} \cdot e^{\frac{a_3}{T_{j,\mathrm{av}}+273^\circ C}}. \quad (1)$$

Thermal cycles lead to fatigue and bond-wire liftoff. In this article, the bond-wire liftoff is considered as the main failure mechanism since the thermal fatigue of the solder joints become prominent only with very high thermal swings (greater than 100 K) [16], [17]. The power processed by the semiconductor module determines the amount of loss dissipation in the module and consequently the junction temperature. Power processed by the ST varies according to the grid conditions and results in the variation of device junction temperature. For fatigue analysis, Miner's rule can be applied to calculate the accumulated damage using [18]

$$D_{\mathrm{acc}} = \sum \frac{N_i}{N_{fi}} \quad (2)$$

where D_{acc} is the accumulated damage, N_i the number of cycles, and N_{fi} the durability of the ith stress range. When the accumulated damage becomes 1, the device fails.

B. Investigated ST Architecture

The investigated ST architecture is composed of a modular structure CHB and DAB converters. AC–DC stage is realized by the CHB converter and the dc–dc stage by the DAB converter. CHB converter connected to the MVac grid rectifies the ac voltage into dc. DAB dc–dc converters convert the rectified dc-link voltage of each CHB cell into low voltage dc while providing the isolation between MV and LV sides. Fig. 1 shows the system architecture. The system parameters are listed in Table I.

To implement a thermal stress control, junction temperature measurement of the devices is necessary. The collector emitter voltage (V_{ce}) is one of the most reliable temperature dependent electrical parameter to monitor the health of the device [19]. Hence, the modular cells of the ST are equipped with V_{ce} sensing system as shown in the Fig. 2. Moreover, the junction temperature estimation from the V_{ce} sensing makes the implementation of the thermal stress based control algorithms more practical.

C. Motivation for Thermal Stress Based Power Routing Control

The failures in the ST can be classified into two categories, the random failures and wear-out-based failures. To ensure the

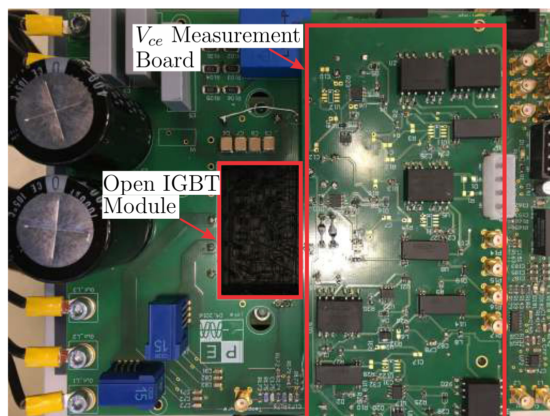


Fig. 2. Open IGBT module with V_{ce} measurement.

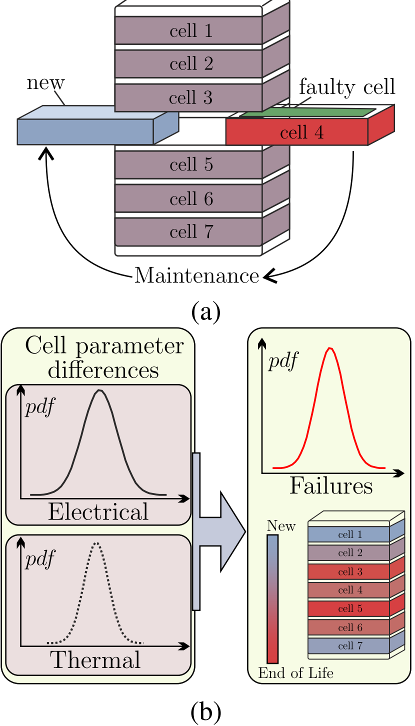


Fig. 3. (a) Failures and replacement cycle. (b) Wear-out-based failure distribution due to parameter differences.

reliable operation of the ST, the failure cases and replacement cycle are analyzed and are shown in Fig. 3.

Fig. 3(a) shows the replacement cycle in case of any failure including random failures. It is logical that when one cell fails, it is sent to maintenance and replaced irrespective of the failed component. Consequently, a modular ST system is comprised of cells with different aging [10].

Fig. 3(b) shows the failures due to the wear-out-based aging of ST. For a modular power converter system with N cells, the device dependent parameters such as average on-state voltage drop and on-state resistance vary between these cells due to the tolerances in the manufacturing process and because of the aging in operation. The heatsink temperatures also differ between the cells, even when they process the same power, depending on the

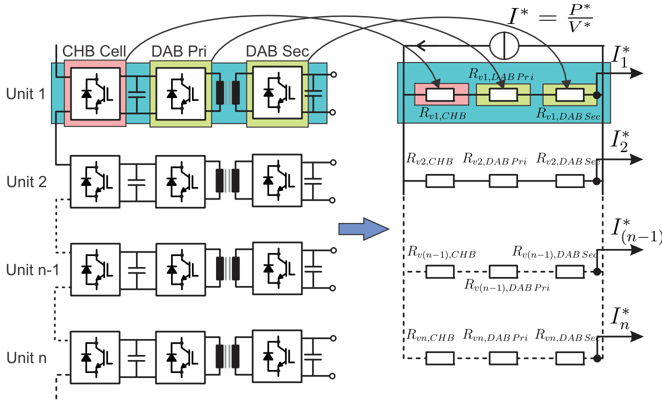


Fig. 4. Equivalent circuit design of virtual resistor based power routing in the ST with CHB and DAB.

spatial configuration of the heatsinks and the direction of flow of the coolant. These electrical and thermal parameter variations are modeled in this article with probability density function (pdf), which will result in different junction temperatures among the cells, and thereby different accumulated damages even if they process equal power. Thus, some of the cells fail earlier than the other ones, even when the power is equally distributed among them. This is illustrated as a pdf of failures in Fig. 3(a).

Therefore, it may be not optimal to distribute the same power through each cell since it results in different aging of the cells and subsequent failure at different time instants leading to higher number of maintenances. This gives motivation for the power routing concept: unequally distribute the power among converters in order to delay the failures and improve the system reliability [10], [12].

III. Design of Virtual Resistance Based Power Routing Controller

If the ST is composed of cells of different ages, equal thermal stress due to equal power sharing results in failures of cells at different instants, leading to frequent maintenances. Therefore, a power routing strategy based on virtual resistances is developed in this section to equalize the thermal stress among the differently aged cells.

1) Concept of Virtual Resistance: In the proposed strategy, each converter cell in the modular ST is represented by a resistor indicating the aging of that particular cell. This is shown graphically in Fig. 4 where the CHB and DAB cells in the ST architecture are represented by resistors. The more aged cell has a higher resistance than a new cell. Thus, the total current is divided among the units according to the combined resistance of each units as depicted in Fig. 4. Since the resistors are implemented in software to generate the current/power references, they are termed as virtual resistors.

2) Design of Virtual Resistance for Power Routing: The virtual resistance design is shown graphically in Fig. 5. The mission profile of the converter system for a time period generates the junction temperature profile for each converter. Since the converters are equipped with V_{ce} junction temperature sensing

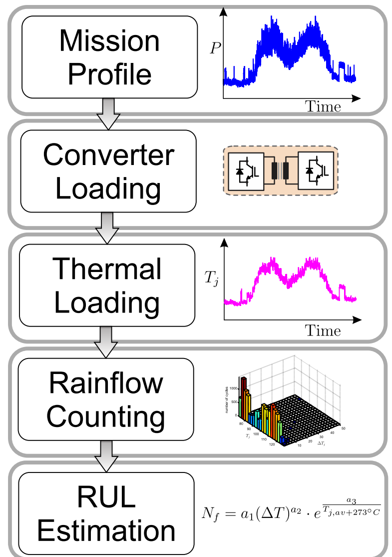


Fig. 5. Calculation of device wear-out from thermal cycling based on operating conditions.

system as shown in Fig. 2, the junction temperature profiles are obtained directly. This junction temperature profile of the past time period can be used to calculate the consumed lifetime ΔD_i of each cell using rainflow counting and the lifetime model as described in Section II [18]. Subsequently, the total accumulated damage can be calculated for each converter using the following:

$$D_i = \sum \Delta D_i \tag{3}$$

where (D_i) is the accumulated damage of the ith cell. Based on the accumulated damages of the semiconductor modules, the power distribution is changed to delay the power dependent failures.

As depicted in Fig. 4, $R_{vi,\text{CHB,IGBT}}$, $R_{vi,\text{CHB,DIODE}}$, $R_{vi,\text{DAB Pri}}$, and $R_{vi,\text{DAB Sec}}$ are calculated from their respective accumulated damages using the following relation

$$\text{Virtual reistor} \propto D_i. \tag{4}$$

$R_{vi,\text{CHB,IGBT}}$ and $R_{vi,\text{CHB,DIODE}}$ are the virtual resistance values for the insulated-gate bipolar transistors (IGBTs) and diode in the CHB, respectively, whereas $R_{vi,\text{DAB Pri}}$ and $R_{vi,\text{DAB Sec}}$ represent the virtual resistance values of primary and secondary side of DABs. For the next step, a weighted average of the virtual resistances of CHB and DAB modules in one power path is considered for the total virtual resistance calculation as expressed in the following:

$$R_{vi} = w_{i,\text{CHB ,IGBT}} \cdot R_{vi,\text{CHB,IGBT}} + w_{i,\text{CHB ,DIODE}} \cdot R_{vi,\text{CHB,DIODE}} + w_{i,\text{DAB}} \cdot \max(R_{vi,\text{DAB Pri}}, R_{vi,\text{DAB Sec}}), i\,\epsilon[1, N]. \tag{5}$$

The maximum virtual resistance value among the two bridges, [$\max(R_{vi,\text{DAB Pri}}, R_{vi,\text{DAB Sec}})$], is chosen for calculation (5) because both bridges process the same power and the bridge with higher virtual resistance is expected to fail first. For the CHB, however, power routing has relatively little impact on the total losses [11]. However, the loss distribution among IGBTs and diodes can be affected by routing the power. For the power flow from ac to dc stage, the diodes are more stressed than IGBTs. The damage accumulation of the most damaged IGBT and diode in a cell are considered for modeling CHB virtual resistance.

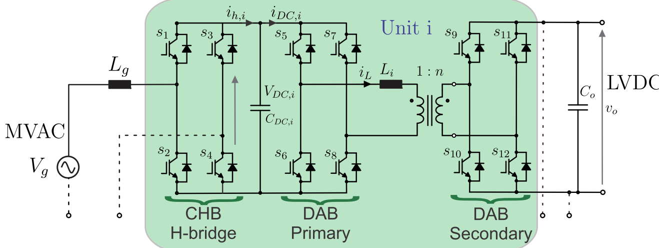


Fig. 6. Detailed schematic of CHB and DAB converter unit in the ST.

Finally, the power reference P_i^* is obtained by solving the virtual resistor network as illustrated in Fig. 4. For a system with $N = 3$ cells, the power references P_1^*, P_2^* P_3^* are given by

$$\begin{bmatrix} P_1^* \\ P_2^* \\ P_3^* \end{bmatrix} = \frac{P^*}{R_{v2}R_{v3} + R_{v1}R_{v2} + R_{v1}R_{v3}} \begin{bmatrix} R_{v2}R_{v3} \\ R_{v1}R_{v3} \\ R_{v1}R_{v2} \end{bmatrix}. \tag{6}$$

Therefore, the higher the value of virtual resistance, lower the processed power through each unit. The total power of the system is divided among the cells according to the value of the virtual resistance for the cell.

It is to be noted that for the implementation of power routing, the converters are not oversized and when the system is operated under full load, the converters process their rated power. The power routing strategy is active only during the partial load operation and the distribution transformer such as the ST operates at partial load for most of the time.

IV. Implementation of Power Routing

In order to realize the testing of the proposed power routing controller with virtual resistors, a control scheme for scaled down prototype of ST with five level CHB and two DABs has been developed in this section.

A. Control Scheme for CHB and DAB

Fig. 6 shows the detailed schematic of a unit composed of one CHB cell and one DAB cell. The unit is taken as the building block for MVac to LVdc conversion because if one of the cells in a unit fails, the power cannot flow through that unit since the cells are connected in series. For the studies, the device parameters described in Section III are utilized and the system parameters are given in Table II.

The overall control strategy for CHB and DAB converters in the ST is shown in Fig. 7(a) and (b), respectively. The CHB rectifier stage controls and shapes the input ac current and controls the total MVdc-link voltage. The current and voltage control is achieved through cascaded controller structure with proportional-resonant (PR) controller and proportional-integral (PI) controller, respectively [20]. The power references (P_i^*) generated by the virtual resistors are given to the power routing

TABLE II
SYSTEM PARAMETERS

Symbol	Description	Value
e (rms)	Grid voltage (rms)	$230\,V,\ 50\,Hz$
L_g	Filter inductance (MV side)	$3.8\ mH$
$V_{DC,1} = V_{DC,2}$	DC-link voltage reference	$250\ V$
V_0	DC-link voltage (LV side)	$250\ V$
n	MFT turn ratio	$1:1$
$f_{sw,CHB}$	Switching frequency of the CHB	$3\ kHz$
$f_{sw,DAB}$	Switching frequency of the DAB	$12\ kHz$

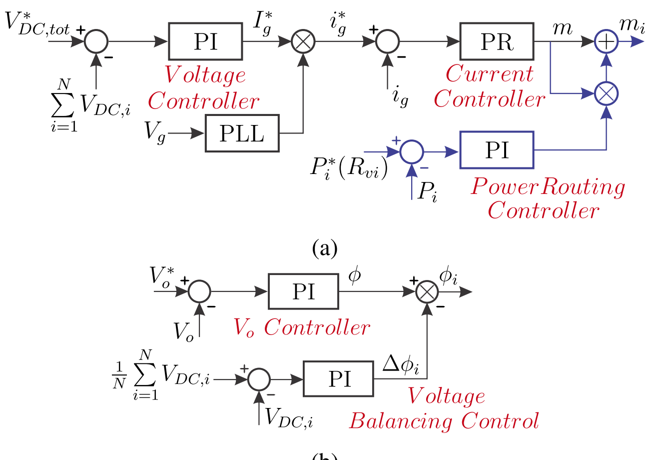


Fig. 7. (a) CHB control scheme with power routing controller. (b) DAB control scheme.

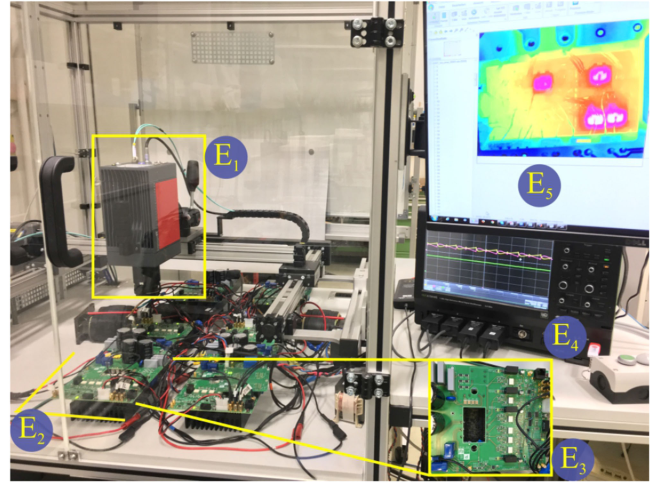


Fig. 8. Experimental setup (E_1: High speed thermal camera, E_2: CHB and DABs, E_3: Open module, E_4: Oscilloscope, E_5: Thermal image.

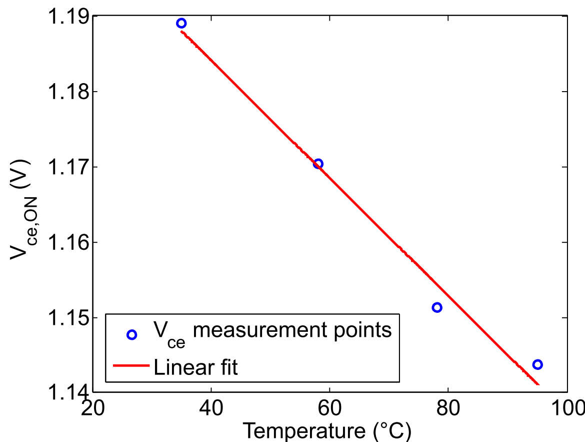


Fig. 9. V_{ce} variation with junction temperature.

controller as depicted in Fig. 7(a). The modulation index m produced by the PR controller is modified by the PI-based power routing controller to achieve different power flow through the dc links of CHB.

A control scheme with output and input voltage control is adopted for the DAB as shown in Fig. 7(b). The input MVdc-link voltages are balanced by the DAB, which is critical for the stability while processing unequal power through each H-bridge of the CHB. For the output LVdc-link voltage control, a PI voltage controller is designed using pole-zero cancelation technique [21].

B. Experimental Validation of Power Routing Controller

To validate the proposed power routing control strategy, a small scale prototype of a five level CHB connected to two DABs has been developed as illustrated in Fig. 8. The H-bridges of CHB and DAB are made with open-module DP25H1200T101616 from Danfoss to facilitate direct junction temperature measurements. A high speed infrared thermal camera is used to obtain the thermal response of the power semiconductors of the open module. The camera is controlled by an automatic positioning system for fast and accurate measurements. The setup is controlled by dSPACE SCALEXIO system. The V_{ce} measurement board integrated to each converter cell provides the junction temperature information and this is validated using the thermal camera. The variation of the V_{ce} versus temperature is shown in Fig. 9 and subsequently, the junction temperature is estimated using a fitting model for the selected device.

The controller of the ST should be able to maintain the reference LVdc voltage even when the power flowing through each unit is different. Moreover, the CHB dc-link voltages should be balanced and must be equal to their reference value. The proper functioning of power routing controller is tested by changing the power distribution among the ST units.

When the power routing is not activated, the DABs share the power equally as shown in Fig. 10. Here, a mission profile with a step change from $P_n = 1.2$ to $P_n = 2.4$ kW with each power cycle lasting for 10 s is applied as the input for the ST. Fig. 10(a) shows the output currents of DAB,1 ($i_{o,1}$) and DAB,2 ($i_{o,2}$) along with voltage across the load resistor (v_o) for the applied mission profile. Fig. 10(b) shows the zoomed image of the DAB currents when delivering balanced power. When the power references are changed, $i_{o,1}$ and $i_{o,2}$ change accordingly while v_o maintains the reference voltage of 250 V.

Fig. 11 shows the output currents of DABs and the output voltage when the power routing strategy is activated. The DAB,1 process $\approx 70\%$ more power than the DAB,2 in this case.

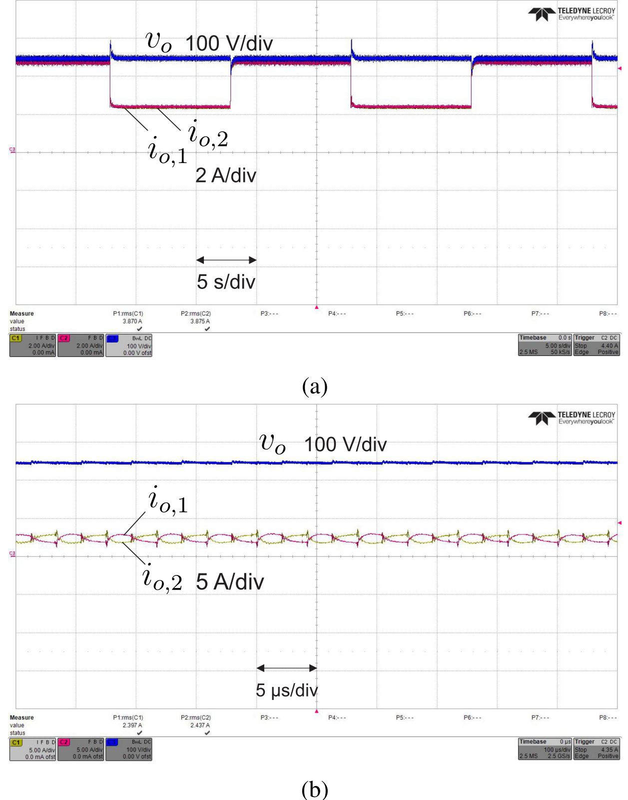


Fig. 10. (a) Output currents of both DABs ($i_{o,1-2}$) and the load voltage (v_o) for equal power sharing for the given mission profile. (b) Output currents of both DABs ($i_{o,1-2}$) and the load voltage (v_o) with time scale 5 μs/div.

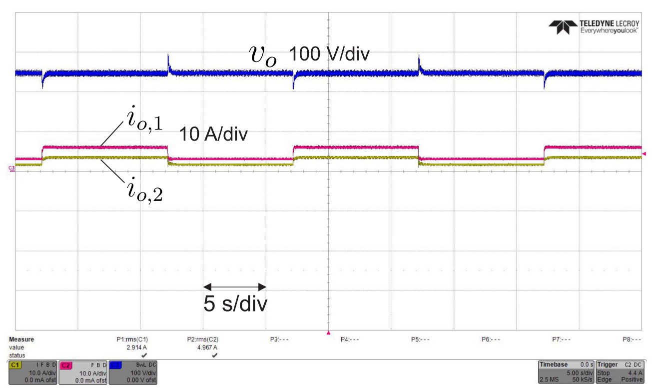


Fig. 11. Output currents of both DABs ($i_{o,1-2}$) and the load voltage (v_o) with activated power routing controller for the given mission profile.

The dc-link voltages of the CHBs are controlled and kept equal to the reference value, even with the unequal power sharing. This validates the proper functioning of the control scheme developed in Section III.

The temperature change in the primary side of the DAB in both modules are measured during the equal and unequal power sharing. The results of the high speed infrared camera measurement for DAB cell 1 showing the temperature of the IGBTs is shown in Fig. 12(a)–(c). The results show a difference of $\Delta T_b = 4\,^\circ$C in the junction temperature for the balanced power sharing mode with average junction temperature $T_{b,\text{avg}} = 83.5\,^\circ$C as in Fig. 12(a). When the power routing controller is activated, the average junction temperature of the DAB cell 2 reduces to $T_{l,\text{avg}} = 80.7\,^\circ$C and the temperature swing also reduces to $\Delta T_l = 2\,^\circ$C as illustrated in Fig. 12(b). Fig. 12(c) shows the temperature profile of the overloaded cell DAB,1, which has a higher average junction temperature of $T_{b,\text{avg}} = 87.7\,^\circ$C and a temperature swing of $\Delta T_l = 6\,^\circ$C.

This results in the different RULs of the cells and the Table III depicts the number of cycles to failure for the three cases using (1). The lifetime in Table III is normalized with respect to that of balanced power sharing. By lowering the thermal cycling in lightly loaded cell, the RUL has increased by 38 times. In this case, the lifetime of the overloaded cell has reduced by 10 times compared to that of balanced operation. The reduction of lifetime of overloaded cell is less than that of the increase in lifetime for the lightly loaded cell. The IGBT is rated for 25 A rms and is operated with a much lower current, and hence the lifetime reduction of overloaded cell is lower. This shows that at lower power levels, a net increase of the system lifetime is achieved through power routing.

The objective of the experiment is to validate the working of the designed power routing controller and its effect on the junction temperature and consequently the aging. It is clear that the power routing controller can influence the junction temperature of the modules and thereby the stress on the semiconductors in different cells of the ST.

V. Impact of Proposed Method on the Reliability of the ST

Scientific references perform the lifetime analysis based on analytical models [22], [23]. Therefore, in this article, an electro-thermal simulation model along with lifetime models are considered to analyze the reliability of the ST. In order to incorporate the deviations of the simulation parameters in a practical scenario, a sensitivity analysis using Monte Carlo simulation is performed and the results are analyzed in this section.

A. *Methodology of Reliability/Lifetime Study*

The methodology of lifetime estimation is presented in Fig. 5. In order to analyze the lifetime using the thermal stress analysis, a mission profile is used to generate the working condition of the power converter. Depending on the mission profile, the thermal loading of the converter is obtained using an electro-thermal model of the system. Once the junction temperature fluctuations are known, the lifetime can be calculated using the rainflow counting method and a lifetime model of the power device.

B. *Design of Electro-Thermal Model of ST for Validation of Virtual Resistance (VR)-Based Power Routing*

In order to conduct a lifetime analysis of the ST, an electro-thermal model of ten CHB cells connected to ten DAB cells are modeled in MATLAB. The model consists of electrical equations of CHB and DAB along with thermal models of the

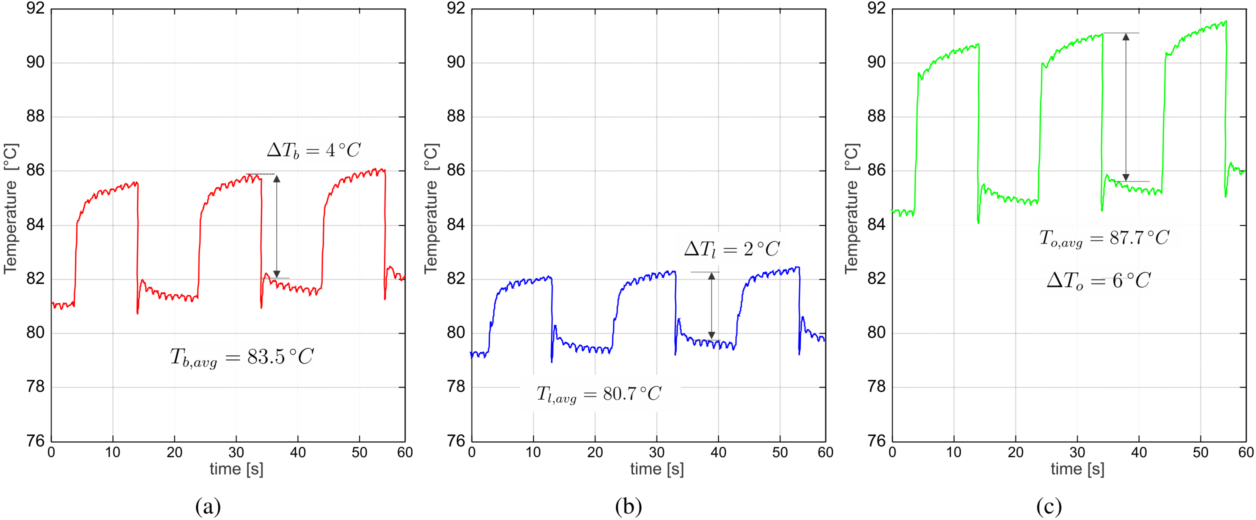


Fig. 12. Variation of primary side IGBT junction temperatures over time of the DAB cells for (a) balanced operation, (b) lightly-loaded cell, and (c) over-loaded cell.

TABLE III
NORMALIZED NUMBER OF CYCLES TO FAILURE (N_f) FOR EQUAL AND UNEQUAL POWER SHARING

Case	N_f (norm.)
Balanced	1
Over-loaded cell	$\frac{1}{10}$
Lightly-loaded cell	38

semiconductor switches and the heatsink for calculating the junction temperature of each device.

1) CHB Modeling: The unit comprising of CHB connected to DAB cell as shown in Fig. 6 is considered for describing the system model. The current and voltage in CHB is modeled using the electrical equations (7) and (8) from Fig. 6 [24]

$$L_g \frac{di_L}{dt} = \sum_{i=1}^{N} (m_i) v_{\mathrm{DC},i} - v_g \tag{7}$$

$$C_{\mathrm{DC},i} \frac{dv_{\mathrm{DC},i}}{dt} = i_{h,i} - i_{\mathrm{DC},i} \tag{8}$$

where m_i is the modulation index of each H-bridge.

When the powers processed by each H-bridge are equal, the modulation index applied to each of them are also equal. In case of power unbalance, the modulation index of the H-bridges varies [24]. Since the H-bridges are connected in series in the CHB, the total current flowing through each H-bridge remains the same. However, depending on the modulation index, the current sharing among the diodes and IGBTs changes.

2) DAB Modeling: Considering phase shift modulation for DAB cell i, the power is given by

$$P_i = \frac{m_{\mathrm{DAB},i} V_{\mathrm{DC},i}^2 D_i (1 - D_i) T_{\mathrm{sw,DAB}}}{2 L_i} \tag{9}$$

TABLE IV
ZVS OPERATING MODES OF DAB

Case	Primary Bridge	Secondary Bridge
$I_1 > 0$ and $I_2 > 0$	ZVS	ZVS
$I_1 > 0$ and $I_2 < 0$	non-ZVS	ZVS
$I_1 < 0$ and $I_2 > 0$	ZVS	non-ZVS

where P_i is the power processed by DAB cell i, $m_{\mathrm{DAB},i}$ is the modulation index of the cell DAB$_i$, $V_{\mathrm{DC},i}$ is the MVdc-link voltage, L_i is the leakage inductance, and $T_{\mathrm{sw,DAB}}$ is the switching time period.

In order to determine the zero voltage switching (ZVS) operation, the inductor currents at the switching instants $\frac{D_i T_{\mathrm{sw,DAB}}}{2}$ and $\frac{T_{\mathrm{sw,DAB}}}{2}$ are given by

$$I_1 = [(2D - 1) + M] \frac{V_{\mathrm{DC},i} T_{\mathrm{sw,DAB}}}{4 L_i} \tag{10}$$

$$I_2 = [1 + M(2D - 1)] \frac{V_{\mathrm{DC},i} T_{\mathrm{sw,DAB}}}{4 L_i}. \tag{11}$$

The ZVS condition of the primary and secondary bridge can be inferred from the inductor currents at switching instants I_1 and I_2, and are tabulated in Table IV.

Depending on the operating power, duty cycle D_i is calculated and subsequently the primary $i_{\mathrm{prim},i}$ and secondary currents $i_{\mathrm{sec},i}$ through the switches are also calculated [25].

3) Device Modeling and Loss Calculation: Once the current through the devices are obtained from the CHB and DAB models, the power losses are computed. The device used is the IGBT module DP25H1200T101616 from Danfoss and the device parameters are obtained experimentally in [26]. The switching losses ($P_{(\mathrm{sw,IGBT})}$) and the conduction losses ($P_{\mathrm{cond,IGBT}}$) of the IGBT are given by (12) and (13), respectively [27] as

$$P_{\mathrm{sw,IGBT}} = \frac{1}{T} \left(\begin{array}{l} \sum_{n=1}^{N_{\mathrm{sw(ON)}}} E_{\mathrm{ON}} \left(V_{\mathrm{ce}}, I_c, T_j \right) \\ + \sum_{n=1}^{N_{\mathrm{sw(OFF)}}} E_{\mathrm{OFF}} \left(V_{\mathrm{ce}}, I_c, T_j \right) \end{array} \right) \tag{12}$$

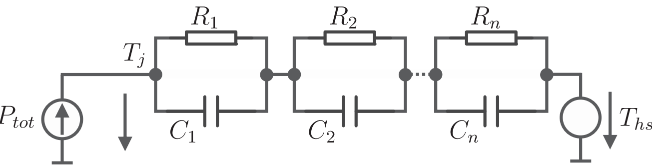


Fig. 13. Thermal model for IGBT and diode in the power module connected to the heatsink.

$$P_{\text{cond,IGBT}} = \frac{1}{T}\int_0^T V_{\text{ce}}\left(I_c(t), T_j\right) \cdot I_c(t)dt \tag{13}$$

where $N_{\text{sw(ON)}}$ and $N_{\text{sw(OFF)}}$ are the number of turn-ON and turn-OFF instants of the IGBT for the time interval T, V_{ce} is the collector–emitter voltage, I_c is the current flowing through the IGBT, and T_j is the IGBT junction temperature.

For computing diode losses such as the reverse recovery losses (P_{rec}) and conduction losses ($P_{\text{cond,diode}}$), (14) and (15) are used

$$P_{\text{rec}} = \frac{1}{T}\left(\sum_{n=1}^{N_{\text{sw}}} E_{\text{rec}}\left(V_{\text{f}}, I_f, T_d\right)\right) \tag{14}$$

$$P_{\text{cond,diode}} = \frac{1}{T}\int_0^T V_f\left(I_f(t), T_d\right) \cdot I_f(t)dt \tag{15}$$

where E_{rec} is the reverse recovery energy of the diode, V_f is the forward voltage drop, I_f is the current flowing through the diode, V_f is the voltage across the diode, and T_d is the diode die temperature.

4) Thermal Network Modeling: In order to calculate the junction temperature from the losses, a thermal network of the power device with the heatsink is modeled and the junction temperatures thus obtained is fed back for the loss computation. The thermal model consists of a Foster network with thermal resistances (R_i, $i \in [1, n]$) and capacitances (C_i, $i \in [1, n]$), where n is the order of the Foster network as shown in Fig. 13. The thermal model parameters for the open IGBT module are experimentally obtained in [26], and in this article, a third-order model is used.

The junction temperature T_j of the device (IGBT and diode) can be calculated from the following:

$$T_j(t) = Z_{\text{th},j-a} * P_{\text{tot}}(t) + T_{\text{hs}}(t) \tag{16}$$

where $Z_{\text{th},j-a}$ is the equivalent impedance of the Foster network, P_{tot} is the total losses in the device, T_{hs} is the heatsink temperature.

C. Validation of the Impact of Power Routing on the ST on System Level

To evaluate the impact of power routing on wear-out-based failures in the ST, a RUL estimation study without and with the power routing control has been carried out. The methodology shown in Fig. 5 is used for lifetime analysis. The ST with ten units comprised of ten CHB cells are fed with mission profile to evaluate the wear-out-based failure. It is assumed that all the cells have zero wear-out due to thermal cycling at the beginning of operation. The electrical parameters affecting the losses of the converters and the heatsink temperatures are different for each cell according to normal distribution. When the accumulated damage reaches unity according to (2), the cells are assumed to reach their end of life.

Without any thermal stress control, the individual CHB and DAB cells have different thermal cycling due to the differences

TABLE V
ESTIMATED RUL IN p.u. FOR ST WITH AND WITHOUT POWER ROUTING CONTROL (PRC)

Unit	CHB RUL (p.u.)		DAB RUL (p.u.)	
	Without PRC	With PRC	Without PRC	With PRC
1	1.00	1.19 (+0.19)	1.00	1.28 (+0.28)
2	1.06	1.22 (+0.16)	1.07	1.28 (+0.22)
3	1.14	1.23 (+0.10)	1.12	1.28 (+0.17)
4	1.21	1.28 (+0.07)	1.18	1.28 (+0.10)
5	1.28	1.30 (+0.01)	1.25	1.28 (+0.03)
6	1.36	1.35 (+0.01)	1.32	1.28 (-0.03)
7	1.44	1.38 (-0.06)	1.38	1.28 (-0.10)
8	1.54	1.44 (-0.10)	1.47	1.28 (-0.18)
9	1.64	1.51 (-0.14)	1.55	1.28 (-0.27)
10	1.74	1.57 (-0.17)	1.63	1.28 (-0.35)
	Mean ΔRUL (p.u.) = +0.005		*Mean* ΔRUL (p.u.) = -0.013	

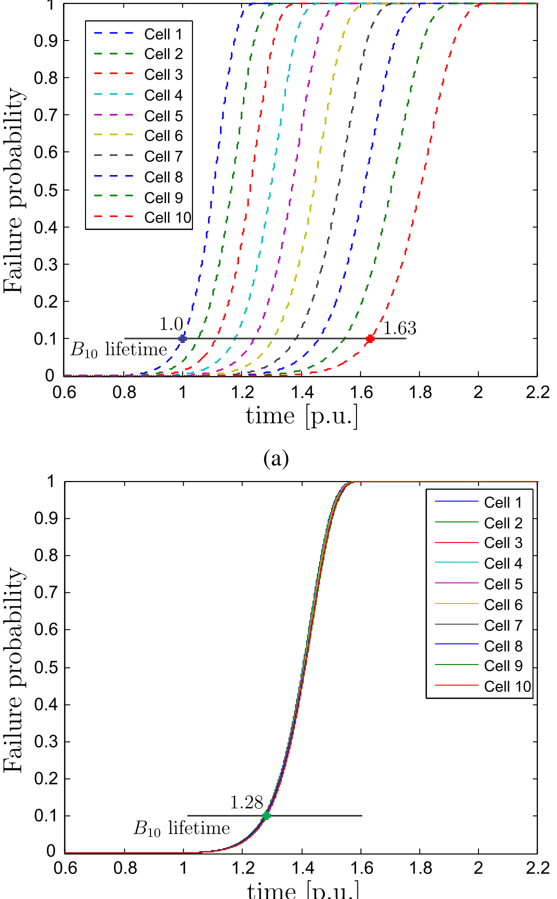


Fig. 14. Unreliability of the DAB cells (a) without power routing and (b) with power routing.

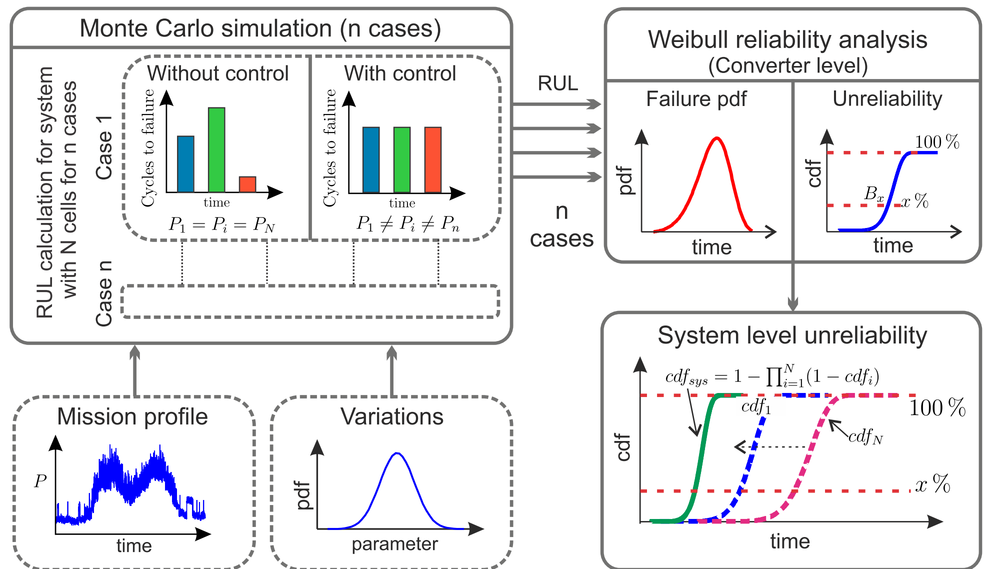


Fig. 15. Schematic representation of Monte Carlo analysis without and with power routing control.

in electrical and thermal parameters. Therefore, the wear-out of each cells are different and this leads to their failure at different times. The electro-thermal model of the ST generates the thermal cycling profile of the cells in accordance with the mission profile, and subsequently the wear-out-based RULs are calculated. Table V summarizes the results of the thermal stress based lifetime evaluation. The RUL values are normalized for CHB and DABs by the failure of first CHB and DAB cell respectively. The first CHB cell fails in 19th year and the first DAB cell in 18th year and these values are considered as the base value for per unit (p.u.) calculations.

The lifetime models such as (1) are obtained from the accelerated lifetime tests with a certain number of sample devices and the obtained experimental data are curve fitted to derive the relationship between lifetime and thermal stress [14], [28]. This implies that there is a degree of uncertainty in the derived parameters, and hence the calculated lifetime is not a single deterministic value. In this article, the device dependent parameters a_1, a_2, and a_3 are modeled by a normal distribution function assuming a variation of 5% [23]. Then, the estimated number of cycles to failure (1) follow the Weibull distribution and failure probability of the cells can be represented as unreliability curve or cumulative distribution function (cdf) given as follows:

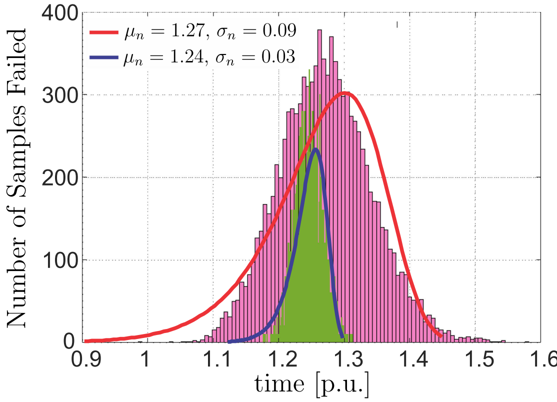
$$F(t) = 1 - \exp\left[-\left(\frac{t}{\alpha}\right)^{\beta}\right] \tag{17}$$

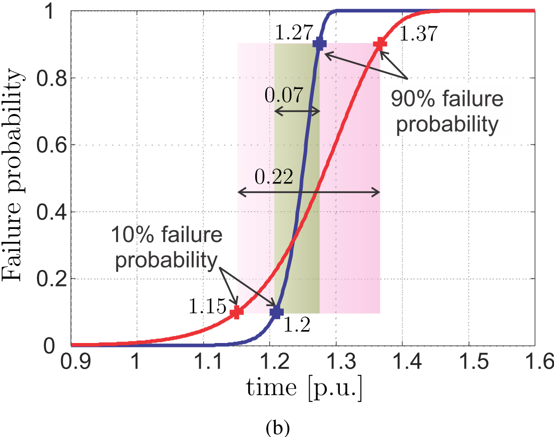
where α and β are the Weibull parameters and $F(t)$ denotes the cdf [22]. The unreliability curves for the DAB cells without and with thermal stress based power routing control is as shown in Fig. 14(a) and (b), respectively. Here, the cells are replaced when they reach 10% failure probability, also commonly known as the B_{10} lifetime [22]. Without power routing, it is clear from Fig. 14(a) that the DAB cells are replaced at different instants.

In order to control the thermal stress based aging, the power sharing between the units of the ST are dynamically changed according to the developed virtual resistor based power routing. The results of the case study are given in Table V. Compared to the conventional equal power sharing, the power routing method can effectively converge the RUL of the DAB cells, whereas it results in an improvement of the total estimated lifetime of the CHB cells. The power routing has lower impact in changing the loss distribution among the CHB cells due to the series connection of the cells. Whereas, for the DAB cells, the unequal power sharing can effectively vary the device losses, and hence the thermal cycling based wear-out is actively controlled. Failure of the first CHB cell is delayed by 19% with power routing strategy and that of the DAB cell is delayed by 28%.

When the thermal stress control is applied, the failure probability of the cells converge and the B_{10} lifetime becomes 1.28 p.u. as shown in Fig. 14(b). Thus, the number of maintenance can be reduced by manipulating the thermal stress among the cells. However, the mean RUL for DABs is decreased by 1.3% with the power routing method. On the other hand, for the CHB cells, a slight increase in the mean RUL of 0.5% is obtained by adopting the proposed control strategy.

1) Analysis of Thermal Parameter Sensitivity on Power Routing Control: For sensitivity analysis considering the thermal parameter variations, a Monte Carlo simulation for 1000 cases with and without power routing is carried out using the system model. The schematic representation of the analysis is shown in Fig 15. Here, the thermal parameters such as heatsink temperature and device parameters are considered as normal distribution with a standard deviation of 5% to emulate a real operating environment. The mission profile input along with the parameters given as the inputs to the electro-thermal model generates the number of cycles to failure or RUL of the system for two cases; without thermal stress control and with power routing for thermal stress control. As illustrated in Fig 15, the Monte Carlo simulation is performed for n cases and the RUL thus obtained follows a Weibull distribution. Subsequently, the pdf and cdf of the Weibull distribution of individual converter





(b)

Fig. 16. Monte Carlo analysis without and with power routing control. (a) Distribution of failures over time. (b) Unreliability or cumulative probability distribution over time.

cells are calculated. Finally, a system level unreliability/cdf is obtained using the formula given by

$$\mathrm{cdf}_{\mathrm{sys}} = 1 - \prod_{i=1}^{N}(1 - \mathrm{cdf}_i) \tag{18}$$

where $\mathrm{cdf}_{\mathrm{sys}}$ denotes the system level cdf and cdf_i indicates the cdf of a cell i.

Fig. 16(a) shows the failure distribution of the ST with ten DAB cells over the years with Monte Carlo analysis. During the normal operation without active thermal stress control, the earliest wear-out-based failures start around 19 years (considered as 1 p.u.) and reaching the maximum probability of failure around 1.27 p.u. years. The failure distribution approximated by a Weibull distribution has the mean and standard deviation as 1.27 and 0.09 p.u., respectively. From the Weibull distribution, the unreliability or the cumulative failure probability distribution can be obtained as shown in Fig 16(b). Unreliability plot illustrates clearly the spread of failure distribution without any thermal stress control. Here, 80% of failures are spread over 0.22 p.u. time, making the maintenance scheduling difficult.

To evaluate the impact of power routing, Monte Carlo analysis is repeated for the ST model with the virtual resistance based power routing control. The thermal parameters of the system remain the same as that of the normal operation. The thermal stress control is able to achieve a 3 times reduction in the standard deviation of failures compared to that of normal operation. However, the mean lifetime of the system is slightly decreased by 2.4% in comparison with normal operation. Fig. 16(b) depicting the unreliability curve vividly demonstrates the advantage of the proposed strategy. In this case, 80% of failures occur in a span of 0.07 p.u., resulting in a better maintenance scheduling. Moreover, the B_{10} lifetime of the system is improved by 4.4% or 11.4 months as shown in Fig. 16(b).

VI. Conclusion

For applications requiring very high reliability such as the ST, one of the possible solutions to increase the system reliability is to carry out maintenance schedules based on prognosis. Therefore, a power routing strategy for improving the reliability of power devices through thermal stress based wear-out control is adopted. Compared to the state of the art, a systematic development of a virtual resistance based system level control is presented, along with its validation in case of thermal and electrical parameter variations using Monte Carlo analysis. Monte Carlo analysis shows that the proposed strategy is able to reduce the standard deviation of the failure probability by 3 times compared to that of normal operation. Moreover, the proposed strategy improves the B_{10} lifetime of the system resulting from thermal stress based wear-out of the devices by 4.4% or 11.4 months. Experimental results demonstrate the potential of the ST control system to route the power internally to achieve thermal stress control.

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