Properties and Synthesis of Lossless Snubbers and Passive Soft-Switching PWM Converters

Xiang Yu, Jianhui Su, Shilin Guo, *Student Member, IEEE*, Shu Zhong, Yong Shi, and Jidong Lai

***Abstract*—This article investigates the synthesis of lossless snubbers and passive soft-switching converters, as well as their general properties, including topological properties and electrical properties. The aim is to find the possible simplest snubbers and soft-switching converters and to give suggestions on applications of the snubbers and the soft-switching converters. On one hand, the synthesis and the topological properties of the snubbers and the converters determine the complexity of the topologies and help find the least requirement that passive soft switching needs to fulfill. The topological properties are investigated by addressing the basic issues induced by the inductor/capacitor added for passive soft switching. Based on the topological properties, the snubbers and the converters are synthesized. On the other hand, the electrical properties determine the performance of the snubbers and converters, help understand the limitations and are investigated by two case studies accompanied with experimental verification. By investigation of the general properties, the possible simplest snubber is given, the tradeoff between the complexity and performance is discussed in detail, the suggestion of snubber applications is presented, and three kinds of reported passive soft-switching converters which are believed to have the most potential of wide application are discussed.**

***Index Terms*—Lossless snubber, pulsewidth modulation (PWM), soft switching, zero-current turn ON, zero-voltage turn OFF (ZVS).**

NOMENCLATURE

List of Acronyms

PWM	Pulsewidth modulation.
VSD	Voltage storage devices. Devices or subcircuits storing energy in the form of voltage.
ZCL	Zero-current inductor. The small inductor added to realize zero-current turning on.
ZVC	Zero-voltage capacitor. The small capacitor added to realize zero-voltage turning off.
ZCS	Zero-current turn-ON.
ZVS	Zero-voltage turn-OFF.
ZCZVS	Zero-current turn-ON zero-voltage turn-OFF.

List of Symbols

C_{gd}	The Miller capacitance (the drain–gate capacitance) of a switch.
C_r	Capacitance of a ZVC.
D	Duty cycle or diode.
D_b	Blocking diode for blocking inductor currents.
D_c	Clamp diode for clamping capacitor voltages.
i_g	Drive current of a switch.
L_r	Resonant inductor or its inductance. The resonant inductor works at a high frequency and resonant mode.
M	DC conversion ratio.
R_g	Gate resistance of a switch.
S	Active switch.
$t_{\rm on}$, $t_{\rm off}$	Duration for the variation of switch voltages in turn-ON and turn-OFF transitions.
$T_{r-\rm on}$, $T_{r-\rm off}$	Turn-ON and turn-OFF transition time of soft-switching converters.
T_s	Switching period.
VSD	Voltage storage device.
V, I	Voltage across an OFF-state switch and current through an ON-state switch.
V_g	Switch voltage stress without snubbers.
$V_{\rm plate}$	The drive voltage on the Miller platform in turn-OFF transitions.
V_r, I_r, Z_r, ω_r	Voltage amplitude, current amplitude, characteristic impedance and angular frequency of the resonance between L_r/ZCL and ZVC. $I_r = V_r/Z_r$, $Z_r = \sqrt{L_r/C_r}$, $\omega_r = 1/\sqrt{L_r C_r}$.
$W_{\rm coss}$	Energy in the output capacitor of an OFF-state switch.
$W_{\rm on\_loss}$	Dissipated energy in turn-ON transitions.
$W_{\rm off\_loss}$	Dissipated energy in turn-OFF transitions.
ZCL	Zero-current inductor.
ZVC	Zero-voltage capacitor.

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X. Yu, J. Su, S. Guo, Y. Shi, and J. Lai are with the School of Electrical Engineering and Automation, Hefei University of Technology, Hefei 230009, China (e-mail: yuxiang_hfut@163.com; su_chen@126.com; shilinguo@mail.hfut.edu.cn; shiyongmail@yeah.net; laijidong@126.com).

S. Zhong is with the Huawei Technologies Co. Ltd., Dongguan 523808, China (e-mail: zhongshusky@163.com).

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I. INTRODUCTION

FOR a higher power density and faster dynamic response, PWM converters need to work at a higher frequency, where switching losses and electromagnetic interference become severe problems. Soft-switching techniques in PWM converters have been proven to be effective in easing both problems, simultaneously preserving the merits of PWM, e.g., a fixed working

frequency [1]–[3]. Additional auxiliary circuits identified as snubbers are applied to conventional PWM converters to modify their switching trajectories for soft switching. According to the auxiliary switches used in snubbers, soft-switching techniques are classified as active or passive soft switching with active or passive snubbers, respectively [4]–[26]. Active soft switching uses auxiliary active switches to control switching transitions, resulting in additional drive circuits, extra switching losses and synchronization problems between the control signals of auxiliary and main active switches, complicating the operation, lowering the reliability, and increasing the cost [4]–[9]. For passive soft switching, only passive components are used. Hence, the circuits are easier to design, more reliable, and cost less, making passive soft switching attractive in various applications [10]–[26]. Conventional passive snubbers are dissipative [27], this article focuses on lossless snubbers, which are also called regenerative or nondissipative snubbers.

A large number of lossless snubbers and passive soft-switching converters have been proposed and evaluated [10]–[26]. The motivation for proposing new snubbers and passive soft-switching converters mainly comes from addressing the limitations and promoting the performance of previously proposed snubbers and converters. However, promoting the performance always complicates the snubbers and converters [28]–[33]. Applications of snubbers and soft-switching converters need to find a balance between the performance and complicity of the topologies. A way to address this issue is to investigate the synthesis of the snubbers and converters, as well as their general properties, including their topological and electrical properties. The synthesis of snubbers and converters and their topological properties determine the complexity and help identify the least requirement that passive soft switching needs to fulfill. The electrical properties determine the performance of the synthesized snubbers and converters, help understand their limitations, and help comprehend what needs to be sacrificed in terms of simplicity to address these limitations.

Few of the reported literatures investigate the synthesis and general properties of lossless snubbers and passive soft-switching converters. A representative work was performed in [34] and [35], which clarified the four problems to be addressed in the investigation of topological properties.

1) *Locations of ZCLs:* How to add ZCLs to the given PWM converters for zero-current turning on? The ZCL is a small inductor that is added to suppress the rise of the switch current in the turn-ON transition, so that zero-current turning on is achieved.
2) *Energy management for ZCLs:* How to handle the voltage spikes induced by the ZCLs during turn-OFF transitions?
3) *Locations of ZVCs:* How to add ZVCs to the given PWM converters for zero-voltage turning off? The ZVC is a small capacitor added to restrict the switch voltage increase during the turn-OFF transition, so that zero-voltage turning off is achieved.
4) *Energy management for ZVCs:* How to handle the current spikes induced by the ZVCs during turn-ON transitions?

Each problem is associated with a topological property. The work in [34], [35] gave properties 1 to 3 (developed in [34] and reviewed in [35]) to address the first three problems. With properties 1 and 3, the methods of locating ZCLs and ZVCs in conventional PWM converters were proposed. Thereafter, the proposed snubber cells were applied to comply with the locations of the ZCLs and ZVCs so that passive soft-switching converters were synthesized. The references also gave a property regarding how to achieve the minimum active switch voltage stress. It can be seen that the property regarding the energy management for ZVCs (called property 4 in this article) and synthesis of the snubbers were not investigated in [34] and [35]. Both dramatically influence the complexity of the snubbers and converters.

Fig. 1 shows the research routine of the topological properties and synthesis of passive soft-switching with the work performed in this article marked in blue. Based on properties 1 to 3 and the method of locating the ZCLs and ZVCs developed in [34] and [35], this article, as a further development, investigates property 4 and the synthesis of lossless snubbers and passive soft-switching converters, as shown in Fig. 1. The synthesis of the converters, i.e., applying snubbers to given PWM converters, is based on the concept of the largest connected subcircuit, which is used to locate the ZVCs in [34]. In addition, a complementarity property in snubbers (property 5) is also proposed to help the synthesis of the converters, as marked with the blue pentacle.

As illustrated in Fig. 1, the passive soft-switching PWM converters are classified into three groups: passive ZCS PWM converters with hard turning off, passive ZVS PWM converters with hard turning on, and passive ZCZVS PWM converters. The corresponding snubbers are turn-ON snubbers, turn-OFF snubbers and soft-switching snubbers, respectively. Although turn-ON snubbers and turn-OFF snubbers achieve partial soft switching, the resulting circuits are rather simple [11], [36]. Additionally, there is no need for complete ZCZVS switching for some circumstances, considering the distribution of the switching losses [22], [37]. This article focuses on turn-OFF snubbers, soft-switching snubbers, and their corresponding passive soft-switching converters since the synthesis of turn-ON snubbers and passive ZCS PWM converters is comparatively simple.

In addition to the synthesis and topological properties of snubbers and converters, the electrical properties are also investigated through two case studies accompanied with experimental verification. The electrical properties include limitations on realization of soft switching, variations of the dc conversion ratio and duty cycle, switching loss elimination, and increase of switch voltage stress and component current stress. Design considerations of the snubbers are given based on the electrical properties.

The aim of this article is to determine the simplest possible snubbers and soft-switching converters and give suggestions on their applications, which was not addressed in [34] and [35] and is rarely discussed in the other literature. The complexity of the topologies is taken as a very important consideration. By investigating the topological and electrical properties, it is determined that the realization of VSDs in property 4 greatly influences the

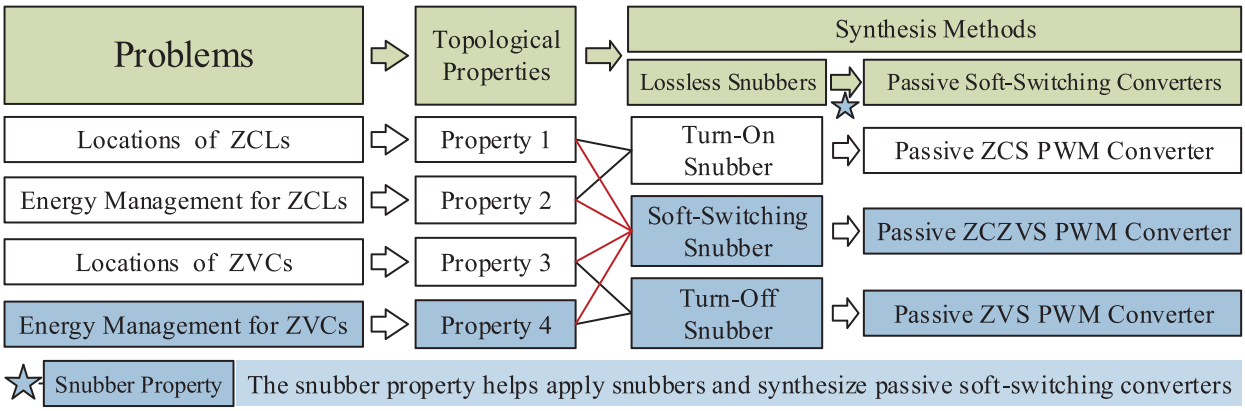

Fig. 1. Research routine of the topological properties and synthesis of passive soft-switching with the work performed in this article marked in blue.

complexity of the topologies and their performance, the simplest turn-OFF and soft-switching snubbers are L-C-D-D snubbers composed of a ZVC, a resonant inductor and two diodes, and there is a tradeoff between complexity and performance. This is described in detail in the applicability discussion section. The section also gives suggestions on snubber applications and discusses the three kinds of reported passive soft-switching PWM converters that are believed to have the most potential for wide application.

This article is organized as follows. The problem of energy management for ZVCs is investigated first in Section II, obtaining property 4. In the following is Section III, where turn-OFF snubbers and soft-switching snubbers are synthesized, and the complementarity between soft-switching snubbers (property 5) is analyzed. Section IV illustrates the synthesis of passive soft-switching converters. Section V gives the electrical properties of synthesized snubbers and converters by two case studies accompanied with experimental verification. At last, the applicability of the synthesized snubbers and converters is discussed in Section VI.

II. Topological Property—Energy Management for Zero-Voltage Capacitors

A. Assumptions and Underlying PWM Converters for Passive Soft Switching

Passive soft-switching PWM converters are synthesized by applying snubbers to given underlying PWM converters, whose characteristics need to first be clarified. The underlying PWM converters are defined the same as those in [34] and [35] and are characterized by having loops composed of a pair of switches and dc voltage sources, simultaneously possessing cutsets composed of the same pair of switches and current sources. Low-frequency filter capacitors and inductors in the underlying converters are taken as voltage sources and current sources, respectively. The loops and cutsets force a large overlap between the switch currents and voltages during switching transitions, inducing large switching losses. The ZCLs and ZVCs break the loops and cutsets, respectively, thus providing zero-current turning on and zero-voltage turning off.

Some assumptions are also made for investigating the topological properties following the existing Assumptions A1–A4 in [34], [35].

Assumption A5: In the ON state of an active switch, the energy trapped in the ZVC applied to that switch is transferred to the voltage sources or low-frequency filter capacitors of the main circuit directly or only through a voltage buffer stage.

Assumption A6: When analyzing lossless snubbers, low-frequency filter inductors are replaced by open circuits, and dc voltage sources or low-frequency filter capacitors are replaced by short circuits.

Assumption A7: During the ON state of active switches, the energy management circuits for the corresponding ZVCs work with the assumption that, in the energy management circuits, only two connections of the energy storage components exist with the ON-state switches shorted and the OFF-state switches opened. Additionally, the connection only changes once via diodes.

Assumption A8: When diodes are used to change the working state of inductors and capacitors there are only two methods: blocking the inductor currents using diodes in series with the inductors and clamping the capacitor voltages using diodes in parallel with the capacitors.

Assumption A1–A4 in [34] and [35] mainly define the underlying PWM converters and illustrate that the underlying converters will not be modified by the snubber components except by the insertion of a ZCL. The defined underlying PWM converters are conventional PWM converters with the active switches being current bidirectional.

Assumption A5 is the energy management requirement for ZVCs. To avoid current spikes induced by ZVCs during turn-ON transitions, the energy trapped in ZVCs in turn-OFF transitions has to be transferred to voltage sources or low-frequency filter capacitors of the main circuit in a controlled manner.

Assumption A6 follows closely with [38] and [39]. The components from snubbers and the underlying PWM converters work at high and low frequencies, respectively. The underlying converters only determine the low-frequency component of the inductor currents and capacitor voltages in the snubbers without influencing their high-frequency components. Assumption A6

allows for analyzing snubbers without considering the main circuits.

The basic principle for the energy transfer from an energy storage component to another energy storage component is that the connection of the energy storage components has to be changed via electronic switches [40], which is the basis of assumption A7. Only the diodes are electronic switches in lossless snubbers. To lower the circulating energy in energy management for ZVCs, the connection of the energy storage components only changes once via diodes during the ON state of the main active switches. The energy storage components have only two connection conditions with the ON-state switches shorted and the OFF-state switches opened.

Assumption A8 is based on the fact that after a switching action, the currents in the circuit are determined by the inductors and current sources, while the voltages are determined by the capacitors and voltage sources. Inductor currents and capacitor voltages can be used to control the transitions of the circuit working state with the help of diodes, which complies with the conditions in active soft switching [1].

Based on the definition of the underlying PWM converters and Assumptions A1–A8, the energy management circuits for ZVCs are derived, with the aim of finding the least requirement for the energy management for ZVCs.

B. Components in Energy Management for Zero-Voltage Capacitors

The voltage sources, low-frequency filter capacitors, and voltage buffer in assumption A5 are equivalent to the voltage storage devices (VSDs) defined in [34], [35], namely devices or subcircuits storing energy in the form of voltage. Thus, the task of energy management for ZVCs is that, during the on state of an active switch, the energy of the ZVC is transferred to a VSD. The realization of VSDs is described in Section IV, ensuring Assumption A5.

To transfer energy from a ZVC to a VSD without loss, an inductor is needed at the very least. The inductor is set to work at a high frequency, minimizing the volume and avoiding influence on the main circuit. This inductor is called a resonant inductor. Considering basic dc–dc converters, namely buck, boost, and buck–boost converters, an inductor is sufficient for an energy transfer between voltage sources. In other words, in the energy management for ZVCs, a resonant inductor is sufficient. Hence, energy storage components in energy management for a ZVC are a ZVC, a VSD, and a resonant inductor. Apart from the energy storage components, diodes are also needed to control their working states, i.e., their connections with one another.

C. Independent Loops in Energy Management for Zero-Voltage Capacitors

Energy storage devices, namely a ZVC, a VSD, and a resonant inductor, construct loops with diodes, realizing the energy management for a ZVC. According to Assumption A7, the energy storage devices have only two connections, and their connection only changes once via diodes. Loops of energy management for ZVCs are determined by the two points.

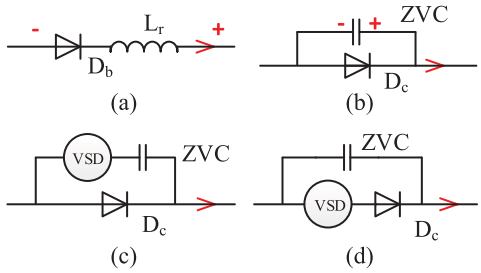

Fig. 2. Possible methods for changing the connections of a ZVC, a VSD, and a resonant inductor via a diode. (a) Method 1. (b) Method 2. (c) Method 3. (d) Method 4.

1) Only Two Connections of the Energy Storage Devices Exist: Among the zero-voltage capacitor *ZVC*, voltage storage device *VSD* and resonant inductor L_r, the connection has only four possibilities: {*ZVC*, *VSD*, L_r}, {*ZVC*, L_r}, {*VSD*, L_r}, and {*ZVC*, *VSD*}, i.e., subsets of {*ZVC*, *VSD*, L_r} excluding the empty subset and subsets with only one component. {*ZVC*, *VSD*} are abandoned for the reason that, in the connection, *ZVC* is clamped by *VSD*, which is helpless for energy transfer. Thus, the two connections of the energy storage devices have three possibilities.

1) *Combination 1:* {*ZVC*, *VSD*, L_r} and {*ZVC*, L_r};
2) *Combination 2:* {*ZVC*, *VSD*, L_r} and {*VSD*, L_r};
3) *Combination 3:* {*ZVC*, L_r} and {*VSD*, L_r}.

2) Connection of the Energy Storage Devices Only Changes Once via Diodes: For the sake of simplicity, the number of the diodes changing the connection is assumed to be one at first and is added when necessary. Resulting from Assumption A8, there are only four methods for changing the connection of *ZVC*, *VSD,* and L_r via a diode, as presented in Fig. 2, where the diode used for blocking the inductor current is called the blocking diode D_b, and the diode used for clamping the capacitor voltage is called the clamp diode D_c. The connection of the energy storage components before changing is named mode A, while the connection after changing is named mode B. The aforementioned four methods are expressed by the language of the set theory, shown as follows.

Method 1: Mode A $\rightarrow$ mode B. Mode A $=$ {Mode A $\mid$ $L_r \in$ Mode A}. Mode B $=$ {Mode B $\mid$ $L_r \notin$ Mode B}.
Method 2: Mode A $\rightarrow$ mode B. Mode A $=$ {Mode A $\mid$ *ZVC* $\in$ Mode A}. Mode B $=$ {Mode B $\mid$ *ZVC* $\notin$ Mode B}.
Method 3: Mode A $\rightarrow$ mode B. Mode A $=$ {Mode A $\mid$ *ZVC*, *VSD* $\in$ Mode A}. Mode B $=$ {*ZVC*, *VSD* $\notin$ Mode B}.
Method 4: Mode A $\rightarrow$ mode B. Mode A $=$ {Mode A $\mid$ *ZVC* $\in$ Mode A, *VSD* $\notin$ Mode A}. Mode B $=$ {Mode B $\mid$ *ZVC* $\notin$ Mode B, *VSD* $\in$ Mode B}.

Matching the four methods with the possibilities of the two connections in Section II-C1, there are only two options, with mode A switching to mode B.

1) Option A, with method 2 matching combination 2.
Mode A $=$ {Mode A $\mid$ *ZVC* $\in$ Mode A} $=$ {*ZVC*, *VSD*, L_r}.
Mode B $=$ {Mode B $\mid$ *ZVC* $\notin$ Mode B} $=$ {*VSD*, L_r}.
2) Option B, with method 4 matching combination 3.

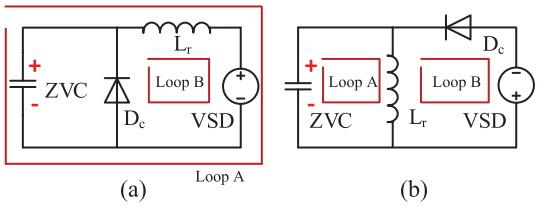

Fig. 3. Possible connections of the energy management circuit for *ZVC*, considering the energy storage components and the clamp diode. The polarity of the initial voltage of *ZVC* is marked. Loop A: energy transfer loop, loop B: inductor reset loop. (a) Option A: Loop A = {*ZVC*, *VSD*, L_r}. Loop B = {*VSD*, L_r, D_c}. (b) Option B: Loop A = {*ZVC*, L_r}. Loop B = {*VSD*, L_r, D_c}.

Mode A = {Mode A | *ZVC* ∈ Mode A, *VSD* ∉ Mode A} = {*ZVC*, L_r}.
Mode B = {Mode B | *ZVC* ∉ Mode B, *VSD* ∈ Mode B} = {*VSD*, L_r}.

A clamp diode is used for the transition from mode A to mode B and belongs to mode B as seen in method 2 and method 4 in Fig. 2. Considering the energy storage components, the energy management circuit for *ZVC* has two options. Mode A, namely {*ZVC*, *VSD*, L_r} or {*ZVC*, L_r}, is the mode where the energy management for *ZVC* starts, with a resonance between *ZVC* and L_r, resulting in an energy transfer from *ZVC* to L_r. Mode B, namely {*VSD*, L_r}, is the mode where the energy management for *ZVC* ends, with the interaction between *VSD* and L_r resulting in an energy reset of L_r. Thus, mode A and mode B are the *energy transfer mode* and *inductor reset mode*, respectively, which are controlled by a clamp diode and correspond to the two connections in assumption A7. The two modes exist in the form of loops, i.e., energy transfer loop A and inductor reset loop B, which are independent from one another. Hence, the energy management circuit for a ZVC is composed of an energy transfer loop and an inductor reset loop.

D. Component Polarity in Energy Management for Zero-Voltage Capacitors

If drawn, the two options of the energy management circuit for *ZVC*, i.e., option A and option B, are presented in Fig. 3, where loop A and loop B are marked. The initial voltage of *ZVC* is the voltage of *ZVC* before the energy management starts. The polarities of the components can be determined as follows:

Along the loop containing *ZVC* and *VSD*, the positive polarity of the initial voltage of *ZVC* is closed to and away from the positive polarity of *VSD* in option A and option B, respectively, which is similar to the situation in the buck and buck–boost converters. Otherwise, the volt-second balance of L_r will be violated.

Along the loop containing *ZVC* and D_c, the positive polarity of the initial voltage of *ZVC* is closed to the cathode of D_c, according to the requirement to clamp *ZVC*.

Assumption A7 indicates that the connection of the energy storage components only changes once, meaning that the energy management circuit for *ZVC* stops working after the inductor reset mode ends. Thus, the interaction between *ZVC* and L_r has to be restrained, i.e., loop A needs to be disabled. Similar to Assumption A8, there are only two alternatives. The method of clamping capacitor voltages with diodes has been used, leaving only the method of blocking inductor currents with diodes. Thus, a blocking diode D_b is inserted into loop A, as shown in Fig. 4.

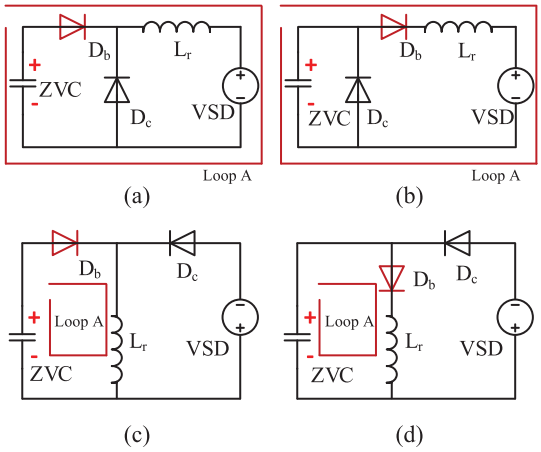

Fig. 4. Possible connections of the energy management circuit for *ZVC* with D_b added. Loop A: energy transfer loop. (a) Possibility A-I. (b) Possibility A-II. (c) Possibility B-I. (d) Possibility B-II.

Along the loop containing *ZVC* and D_b, the anode of D_b is closed to the positive polarity of the initial voltage of *ZVC*, restraining the interaction between *ZVC* and L_r after the inductor reset mode ends.

Assumption A7 also implies that after an active switch turns on, the energy management circuit for the ZVC applied to that active switch begins to work, and the energy transfer mode begins. Thus, the active switch *S* is part of the energy transfer loop, as shown in Fig. 5.

Along the loop containing *ZVC* and *S*, the drain or the collector of *S* is closed to the positive polarity of the initial voltage of *ZVC*, which is based on the fact that the resonance between *ZVC* and L_r begins with *S* turning on.

Fig. 5 gives the possible energy management circuits of a ZVC, which are summarized as follows.

Property 4—Energy management for ZVCs.

1) *Components:* A zero-voltage capacitor *ZVC*, a voltage storage device *VSD*, a resonant inductor L_r, an active switch *S*, and two diodes, one diode D_c for clamping, the other diode D_b for blocking.
2) *Independent loops:* An energy transfer loop for energy transfer from *ZVC* to L_r, and an inductor reset loop for resetting L_r.
   The energy transfer loop = {*ZVC*, L_r, *S*, D_b} + a subset of {*VSD*}. The inductor reset loop = {*VSD*, L_r, D_c} + a subset of {*S*, D_b}. Set {*VSD*} has two subsets, and set {*S*, D_b} has four subsets, resulting in eight possible energy management circuits for *ZVC*.
3) The polarities of the initial voltage of the ZVC, VSD, clamp diode, blocking diode are determined according to the polarity of the active switch, which is determined by the underlying converter.

The feasibility of the derived energy management circuits for ZVCs is verified via a PSIM simulation. The simulated waveforms and settings are shown in Fig. 6 and Table I, respectively. Note that Fig. 6(a) and (b) both have eight waveforms associated

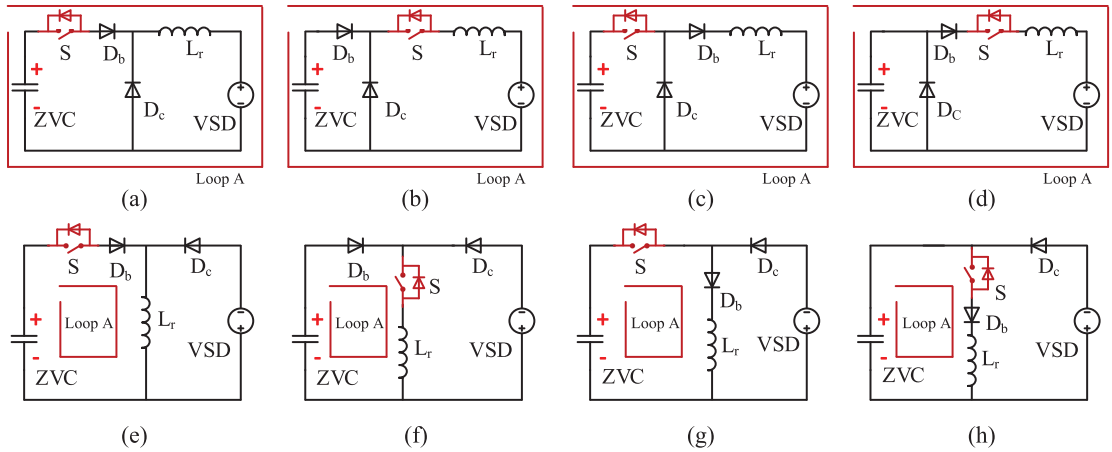

Fig. 5. Possible energy management circuits for *ZVC*. Loop A: energy transfer loop. (a) Possibility A-I-a. (b) Possibility A-I-b. (c) Possibility A-II-a. (d) Possibility A-II-b. (e) Possibility B-I-a. (f) Possibility B-I-b. (g) Possibility B-II-a. (h) Possibility B-II-b.

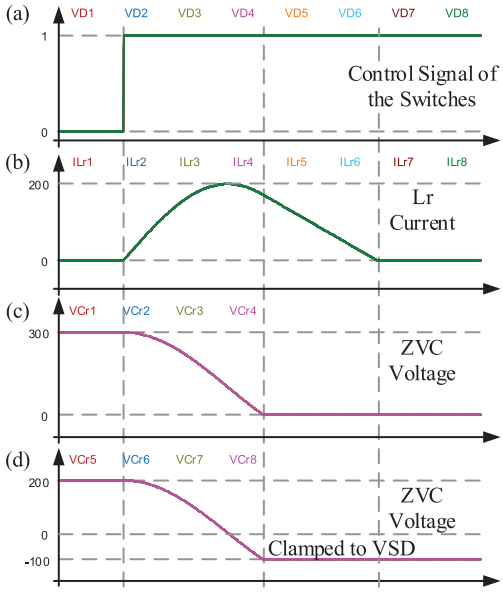

Fig. 6. Simulation waveforms of the energy management circuits for *ZVC*.

with circuits a to h in Fig. 5, respectively. Fig. 6(c) and (d) both have four waveforms, where the four waveforms in Fig. 6(c) are associated with circuits a to d in Fig. 5, respectively, and the four waveforms in Fig. 6(d) are associated with circuits e to h in Fig. 5, respectively. Because all the waveforms in the same subfigure are the same, they appear as a single curve.

All the energy management circuits work in the same manner.

1) The moment after *S* turns on, the resonance between *ZVC* and L_r begins, as well as the energy transfer mode. The voltage of *ZVC* then falls.
2) When the voltage of *ZVC* equals zero (circuits a to d) or that of *VSD* (circuits e to h), D_c turns on and the voltage of *ZVC* is clamped. The energy transfer mode ends and the inductor reset mode begins. The current of L_r begins to fall under the voltage of *VSD*.

TABLE I
SIMULATION SETTINGS OF THE ENERGY MANAGEMENT CIRCUITS FOR *ZVC*

Components	Circuit a-d in Fig. 5.	Circuit e-h in Fig. 5.
L_r	Current $i_{Lr1}-i_{Lr4}$	Current $i_{Lr5}-i_{Lr8}$
$=1\,\mu H$	Initial value: 0 A	Initial value: 0 A
ZVC (C_r)	Voltage $v_{cr1}-v_{cr4}$	Voltage $v_{cr5}-v_{cr8}$
$=1\,\mu F$	Initial Value: 300 V	Initial Value: 200 V
VSD	Voltage: 100 V	Voltage: 100 V
S	Ideal Switch	Ideal Switch
D_b , D_c	Ideal Diode	Ideal Diode
Simulator	PSIM. Time Step: 10 ns	

3) At the moment the current of L_r equals zero, the inductor reset mode ends.

III. SYNTHESIS AND PROPERTY OF LOSSLESS SNUBBERS

Property 4, as well as properties 1 to 3 in [34] and [35], define the least required rules that passive soft switching has to follow, with property 1 and property 2 for zero-current turning on, and properties 3 and 4 for zero-voltage turning off, as presented in Fig. 1. Thus, properties 3 and 4 are used to synthesize turn-OFF snubbers, while properties 1 to 4 are used to synthesize soft-switching snubbers. Based on the synthesized snubbers, passive soft-switching PWM converters are derived. A complementary property is found in soft-switching snubbers, helping synthesize passive ZCZVS PWM converters.

A. *Synthesis of Turn-OFF Snubbers*

Each active switch requires a ZVC for zero-voltage turning off. Property 3—locations of ZVCs means that the ZVC, auxiliary diodes and the voltage sources from the underlying converter make a closed loop with the active switch, and the diodes provide freewheeling paths for the switch current after the switch turns off. Property 4 is represented by the circuits in Fig. 5. D_b of circuits a and e in Fig. 5 fail to provide a freewheeling path for the current of *S*, which violates property 3. Circuits b,

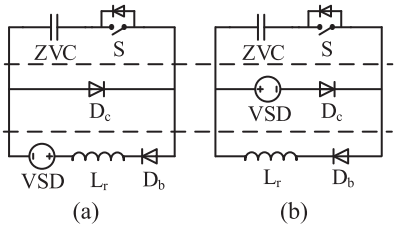

Fig. 7. Available turn-OFF snubbers for zero-voltage turning off. (a) Snubber A. (b) Snubber B.

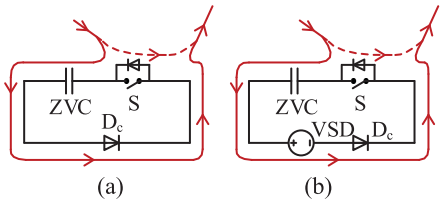

Fig. 8. Transfer of the switch current in a turn-OFF snubber when the switch turns off. (a) Snubber A. (b) Snubber B.

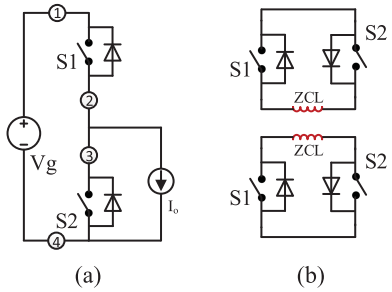

Fig. 9. (a) Possible locations of a ZCL according to property 1. (b) Possible locations of a ZCL with the voltage sources being shorted and current sources being opened.

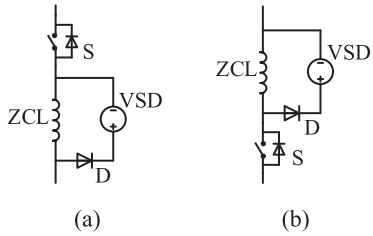

Fig. 10. Available turn-ON snubbers for zero-current turning on. (a) Snubber I with *ZCL* connected to the source (emitter) of *S*. (b) Snubber II with *ZCL* connected to the drain (collector) of *S*.

d, f, and h also do not comply with property 3 since *ZVC* and *S* make a loop containing L_r. Thus, only circuits c and g are used for zero-voltage turning off.

For the sake of convenience, circuits c and g are named turn-OFF snubber A and turn-OFF snubber B, respectively, and are redrawn in Fig. 7. The sequence of the components in the same branch is unlimited. *ZVC*, D_c, and *S* make the closed loop indicated in property 3. When *S* turns off, if the switch current flows from the source (emitter) to the drain (collector), the switch current freewheels through the anti-paralleled diode, naturally realizing zero-voltage turning off. If the switch current flows from the drain (collector) to the source (emitter), the branch composed of *ZVC* and D_c provides a freewheeling path for the switch current and suppresses the rise of the switch voltage, achieving zero-voltage turning off, as presented in Fig. 8. When *S* turns ON, *ZVC* interacts with L_r and is finally clamped by D_c. The energy of *ZVC* is managed as analyzed in Section II. It is determined that passive soft switching only needs to consider the situation where the current of the switch aimed at passive soft switching flows from the drain (collector) to the source (emitter). In the other situation where the current flows from the source (emitter) to the drain (collector), the switch turns off with the switch voltage being clamped by the anti-paralleled diode, achieving zero-voltage turning off by nature.

B. Synthesis of Soft-Switching Snubbers

The soft-switching snubbers are derived by the combination of properties 1 to 4.

Each pair of switches requires a ZCL for zero-current turning on, and the pair is characterized by making a closed loop with the voltage sources in the underlying PWM converters. Property 1—locations of ZCLs indicates that the ZCL is inserted in the loop. When the pair of switches are two active switches, the possible locations of the ZCL are presented in Fig. 9. With the voltage source replaced by a short circuit, property 1 means that the ZCL can only and must be connected to the drain (collector) or source (emitter) of either active switch from the pair. In regard to the condition that the pair of switches are an active switch and a diode, the conclusion remains. This observation is not included in [34] and [35].

Property 2—energy management for ZCLs requires the ZCL to make a new loop with a VSD and some auxiliary diodes. When the active switch that the ZCL serves turns off, the diodes can provide freewheeling paths for the current of the ZCL, and at the same time the VSD helps reset the ZCL.

Turn-ON snubbers are acquired by the combination of properties 1 and 2, as seen in Fig. 10. *ZCL* is connected to the drain (collector) or the source (emitter) of an active switch as indicated by property 1. Additionally, *ZCL* makes the loop described in property 2 with *D* and *VSD*. If the switch current flows from the drain (collector) to the source (emitter) and *S* turns off, the diode provides a freewheeling path for the current of *ZCL* and *VSD* helps reset *ZCL*. When *S* turns on, *ZCL* takes over the voltage that *S* undertakes in the off state and restricts the *di/dt* of *S*, achieving zero-current turning on. The polarity of *VSD* which is impressed on *ZCL* when S turns off must be opposite to that of the voltage of *ZCL* taken from *S* when *S* turns on, which means *VSD* helps reset *ZCL*.

Considering the turn-OFF snubbers in Fig. 7, i.e., the result of the combination of properties 3 and 4, the situation of L_r complies with property 2. L_r, D_c, D_b, and *VSD* make the loop described in property 2. Property 1 only forces the ZCL to be connected to the drain (collector) or the source (emitter) of an active switch. Thus, soft-switching snubbers complying

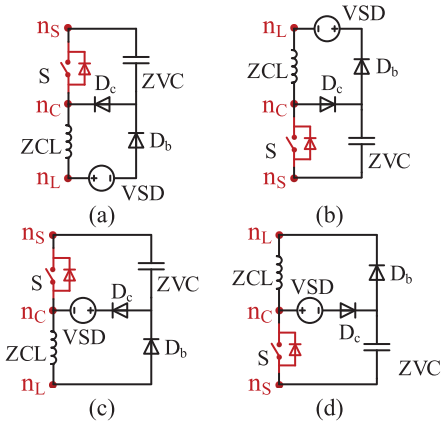

Fig. 11. Available soft-switching snubbers for zero-current turning on and zero-voltage turning off, with three points emphasized for locating a snubber in the underlying PWM converter. n_S: node on *S* side, n_C: node between *S* and *ZCL*. n_L: node on *ZCL* side. (a) Snubber A-I. (b) Snubber A-II. (c) Snubber B-I. (d) Snubber B-II.

with properties 1 to 4 are derived from turn-OFF snubbers with some modification, where the resonant inductor adjusts to be connected to the drain (collector) or the source (emitter) of the active switch. The resonant inductor functions as a ZCL, as presented in Fig. 11, where three points for locating the snubbers in the underlying PWM converters are marked.

C. Complementarity Between Soft-Switching Snubbers

A complementary property between soft-switching snubbers is found when applied to half-bridge topologies. Snubber A-I and snubber B-II are complementary to one another, as well as snubber A-II and snubber B-I. The complementarity between soft-switching snubbers helps simplify and unify the synthesis of passive ZCZVS PWM converters.

Property 5—Complementarity between soft-switching snubbers: If one switch from the pair of switches in the half-bridge topology makes a soft-switching snubber in Fig. 11 with the necessary added components, achieving ZCZVS switching, the other switch will make another soft-switching snubber from Fig. 11 with the same added components, automatically achieving ZCZVS switching. The two snubbers are complementary to one another, which may be snubber A-I and snubber B-II, or snubber A-II and snubber B-I.

As seen in Fig. 12, when *S1* makes soft-switching snubber A-I with the two diodes, *ZVC*, *ZCL,* and *VSD*, *S2* makes soft-switching snubber B-II with the same two diodes, *ZVC*, *ZCL,* and *VSD*, with V_g being shorted. With the focus transferring from *S1* to *S2*, the soft-switching snubber is transformed from snubber A-I to snubber B-II, and the clamp diode and blocking diode exchange locations with one another, which means, following properties 1–4, if *S1* achieves ZCZVS switching, the complementary switch *S2* acquires ZCZVS switching automatically.

The complementarity property, i.e., property 5, is proven as follows with snubber A-I and snubber B-II being the examples.

Fig. 13(a) shows snubber A-I with the switch emphasized in red and named *S1*. According to property 5, *S1* is from the

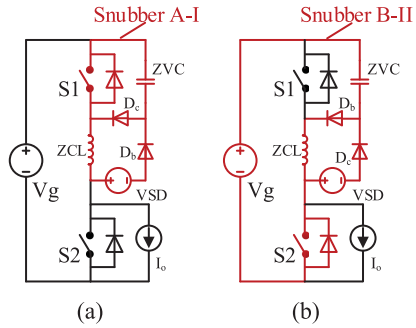

Fig. 12. Example of the complementarity between soft-switching snubbers when applied in a half bridge topology. (a) Snubber A-I. (b) Snubber B-II.

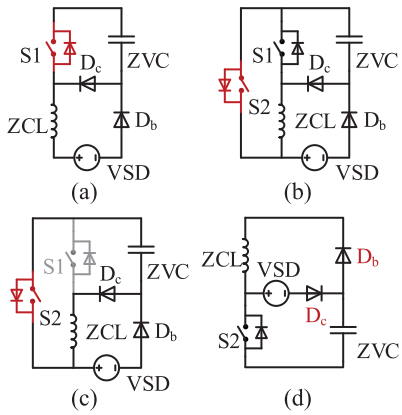

Fig. 13. Evolution process from snubber A-I centered on *S1* to snubber B-II centered on *S2*. (a) Snubber A-I centered on *S1*. (b) Add *S2* to form a loop with *S1* and *ZCL*. (c) Omit *S1*. (d) Snubber B-II centered on *S2*.

pair of switches in the half-topology where the other switch is named *S2*. According to property 1 and Fig. 9, *S1*, *S2,* and *ZCL* make a closed loop, which is shown in Fig. 13(b), where *ZCL* is assumed to be connected to the source (emitter) of *S1*. Omitting *S1*, the circuit made of *S2* and the added components is shown in Fig. 13(c) and (d). With the locations of D_c and D_b exchanged, Fig. 13(c) is the same as Fig. 13(d), which is snubber B-II. That is, property 5 is proven.

The turn-OFF snubbers and soft-switching snubbers derived in this section can be used for conveniently constructing passive soft-switching converters. Moreover, in the construction of passive ZCZVS converters, property 5 helps simplify the synthesis procedure of half-bridge ZCZVS converters and unify the realization of passive ZCZVS switching for dc–dc, dc–ac, and ac–dc converters.

IV. Synthesis of Passive Soft-Switching PWM Converters

A. Synthesis of Passive Zero-Voltage Turn-OFF PWM Converters

Properties 3 and 4, and the turn-OFF snubbers are used for the synthesis of passive ZVS PWM converters. Each active

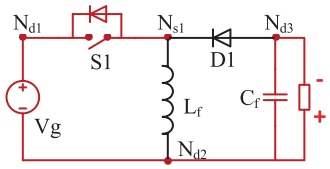

Fig. 14. Largest connected subcircuit composed of the active switch *S1* and voltage sources.

switch needs a turn-OFF snubber for zero-voltage turning off. The synthesis procedure is divided into the following three steps.

1) Determine the location of the turn-OFF snubbers. With the largest connected subcircuit composed of the active switch and voltage sources in the underlying PWM converter clarified, the two nodes on either side of the active switch in the subcircuit help locate the turn-OFF snubbers.
2) Apply turn-OFF snubbers A or B to the underlying PWM converter according to the two nodes in step 1. The polarities of the VSD and diodes in the snubber must comply with property 4.
3) Construct the VSD, which is detailed in Section IV-C.

The synthesis procedure is further explained by an example of a buck–boost converter. The largest connected subcircuit composed of *S1*, C_f, and V_g is shown in Fig. 14. N_{s1} is the only node on the source (emitter) side of *S1*. N_{d1}, N_{d2}, and N_{d3} are all nodes on the drain (collector) side of *S1*. The location of the turn-OFF snubber is determined by choosing one point from $\{N_{s1}\}$ and $\{N_{d1}, N_{d2}, N_{d3}\}$, respectively. The possible locations of the turn-OFF snubber are $\{N_{s1}, N_{d1}\}$, $\{N_{s1}, N_{d2}\}$, and $\{N_{s1}, N_{d3}\}$, as seen in Fig. 15. Two possible turn-OFF snubbers and three possible locations result in six converters.

B. Synthesis of Passive ZCZVS PWM Converters—A Unified Approach

There are two methods for synthesizing passive ZCZVS PWM converters: using soft-switching snubbers for simultaneous zero-current turning on and zero-voltage turning off, or using turn-ON snubbers and turn-OFF snubbers for zero-current turning on and zero-voltage turning off, respectively. The former method, which results in a simpler topology, is studied, while the latter was discussed in [14] and [41].

With the help of the three points $\{n_S, n_C, n_L\}$ marked in the soft-switching snubbers in Fig. 11 and with the help of properties 1 to 4, the passive ZCZVS PWM converters are synthesized by the following steps.

1) Identify the pair of switches requiring ZCZVS switching and locate the ZCL. As said before, each pair of switches, which makes a loop with the voltage sources, requires a ZCL for ZCZVS switching. The ZCLs are inserted in the loops.
2) Choose one switch from the pair, named *S1*. The ZCL must be connected to the source (emitter) or the drain (collector) of *S1*.
3) Identify the location of the soft-switching snubbers. In the largest connected subcircuit composed of *S1*, the voltage sources and ZCL in the underlying PWM converter, there are three types of nodes: the nodes on the *S1* side, the nodes between *S1* and ZCL and the nodes on the ZCL side. Three nodes are acquired by choosing one node from each type, named N_S, N_C, and N_L, which are used for locating the soft-switching snubbers.
4) Apply the soft-switching snubbers by matching $\{N_S, N_C, N_L\}$ with $\{n_S, n_C, n_L\}$. The available snubbers are influenced by the location of the ZCL. If the ZCL is connected to the source (emitter) of *S1*, snubber A-I or snubber B-I is used. If the ZCL is connected to the drain (collector), snubber A-II or snubber B-II is used.
5) Construct the VSD, which is covered in Section IV-C.

Each pair of switches that makes a closed loop with the voltage sources in the underlying converter requires a ZCL. Different pairs of switches making loops with the same voltage sources can use a common ZCL located in the common branch of the loops for zero-current turning on [35], [42].

The synthesis procedure can be applied to the underlying dc–dc, dc–ac, and ac–dc converters. It is the complementarity of soft-switching snubbers that makes the synthesis of passive ZCZVS dc–ac or ac–dc converters focus only on one active switch of the pair of switches in the underlying converter without considering the other switch, which is the same as the situation in dc–dc converters.

The passive ZCZVS half-bridge converters synthesized by this method are presented in Fig. 16 as an example. The two passive ZCZVS half-bridge converters are synthesized with the help of snubber B-I and the largest connected subcircuit composed of *S1*, *ZCL*, and V_g. It should be noted that the two converters can also be synthesized based on snubber A-II and the largest connected subcircuit composed of *S2*, *ZCL*, and V_g, due to the complementarity property. The location of *ZCL* in Fig. 16 has several possibilities, as presented in Fig. 9. The available snubbers are snubber A-I, snubber B-I, snubber A-II, and snubber B-II. Thus, many other passive soft-switching ZCZVS half-bridge converters can be synthesized.

Another example is found in the Undeland snubber, which is widely used in voltage-source inverters [42], [43], and can be synthesized by the method illustrated above. The Undeland snubber and the associated converter are shown in Fig. 17, where the largest connected subcircuit and the snubber are shown in Fig. 17(a) and (b), respectively. Due to the complementarity property, snubber B-I can also be used for the synthesis of the Undeland snubber and the associated converter.

C. Realization of VSDs

To complete the construction of a passive soft-switching converter, the VSD needs to be realized. The key for realizing the VSD is how to transfer the VSD's energy to the voltage source from the main circuit, as assumed in assumption A5. According to the reported literature, there are three main realizations for VSDs [10], [11], [13], [34].

Method 1: Using the dc voltage sources including the low-frequency filter capacitors in the main circuit for VSDs [11].

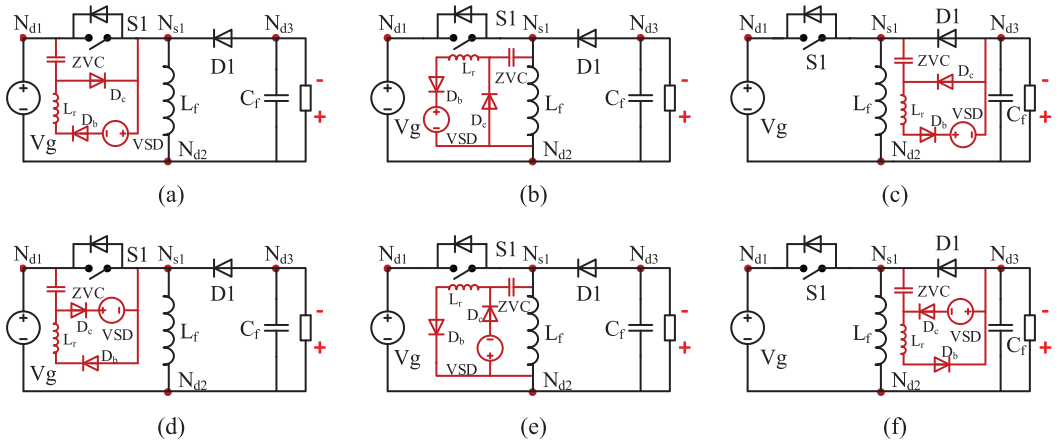

Fig. 15. Possible passive zero-voltage turn-OFF buck–boost converters. (a) Snubber A located at $\{N_{s1}, N_{d1}\}$. (b) Snubber A located at $\{N_{s1}, N_{d2}\}$. (c) Snubber A located at $\{N_{s1}, N_{d3}\}$. (d) Snubber B located at $\{N_{s1}, N_{d1}\}$. (e) Snubber B located at $\{N_{s1}, N_{d2}\}$. (f) Snubber B located at $\{N_{s1}, N_{d3}\}$.

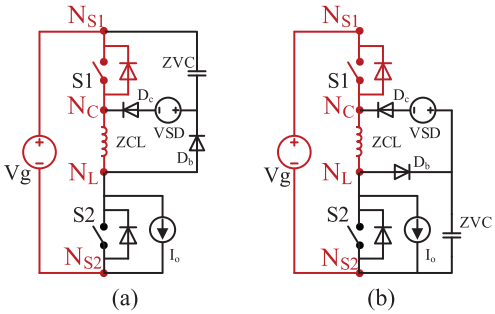

Fig. 16. Examples of passive ZCZVS half-bridge converters with the ZCL inserted in a certain place. The largest connected subcircuit composed of *S1*, *ZCL*, and the voltage sources is emphasized in red. (a) Snubber B-I located at $\{N_{S1}, N_C, N_L\}$. (b) Snubber B-I located at $\{N_{S2}, N_C, N_L\}$.

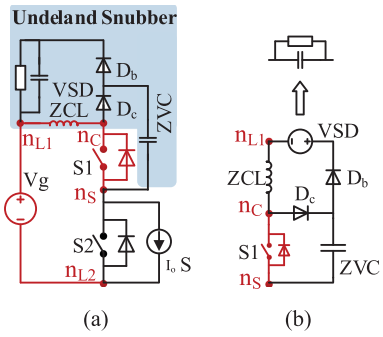

Fig. 17. Widely used Undeland snubber and the associated converter. (a) Largest connected subcircuit for the synthesis, emphasized in red. (b) Employed snubber for the synthesis, i.e., snubber A-II.

Method 2: Realizing a VSD by adding a low-frequency filter capacitor, whose energy is transferred to the dc voltage source in the main circuit by an auxiliary circuit [13].

Method 3: Realization of a VSD by a transformer or a coupled inductor [10].

Methods 1 and 3 transfer energy of a ZVC to the main circuit directly, as said in assumption A5, while method 2 transfers energy of a ZVC to the main circuit by a voltage buffer, which is the other manner for energy transfer in assumption A5. Method 2 and method 3 are investigated in detail in [34]. The VSDs in Fig. 16 can be realized by method 2, as are realized in cell V and cell VI in [34]. Method 1 is explained in detail in the following.

The VSDs in the passive soft-switching converters synthesized before are represented by dc voltage sources. If the VSD is connected to a voltage source (or a low-frequency filter capacitor) from the main circuit, and the polarities of the VSD and dc voltage source (or the low-frequency filter capacitor) are consistent with one another at their common connection point, the VSD can be replaced directly by the voltage source (or the low-frequency filter capacitor). It should be noted that the dc voltage sources from the main circuit are not only the visible voltage sources but also their composition. Additionally, the dc voltage sources used for VSDs need to satisfy the VSD limitations analyzed in Section V-B1.

The VSDs in Fig. 15 can be realized in this method, with the resulting converters presented in Fig. 18. The VSDs of circuits a and f in Fig. 15 cannot be realized in this way because there is no direct connection between the VSD and the dc voltage source (or the low-frequency filter capacitor) in circuit a and the polarity of the VSD in circuit f is not consistent with that of C_f at their common connection point. Three voltage sources exist in the underlying buck–boost converter, the input, output, and summation of the input and output, as indicated in Fig. 18. Circuit c in Fig. 18 fails to work properly because of the limitation on the VSD. Using an analysis similar to that in the VSD limitation section in Section V-B1, $V_{\rm vsd} < (V_{\rm in} + V_o)/2$ must be ensured for soft-switching, which is the reason why circuit c in Fig. 18 fails to work properly, where $V_{\rm vsd} = V_{\rm in} + V_o$. It is also observed that the passive ZVS buck–boost converter realized by applying turn-OFF snubber A can always be realized by applying turn-OFF snubber B, and vice visa, as implied in the Fig. 18 caption.

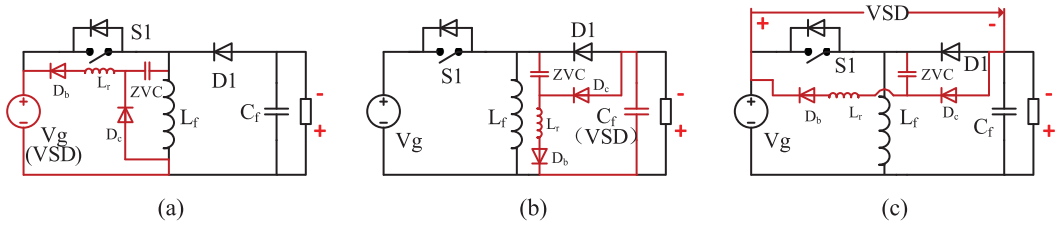

Fig. 18. Passive zero-voltage turn-OFF buck–boost converters using components from the main circuit as the VSD. (a) Derived from circuit b or d in Fig. 15 with V_g as the VSD. (b) Derived from circuit c or e in Fig. 15 with C_f as the VSD. (c) Derived from circuit c or d in Fig. 15 with $V_g + C_f$ as the VSD, which cannot work because of the VSD limitation, where $V_{\rm vsd} < (V_{\rm in} + V_o)/2$.

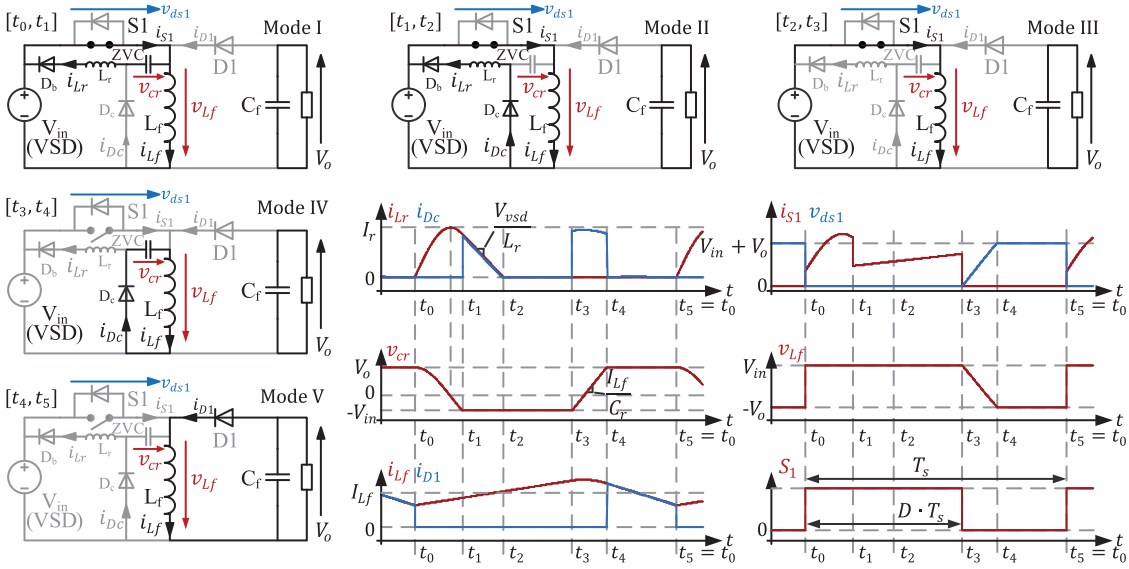

Fig. 19. Operation modes and the simulated key voltage and current waveforms of the passive ZVS buck–boost converter, including the L_r current i_{Lr}, the clamp diode current i_{Dc}, the ZVC voltage v_{cr}, the filter inductor current i_{Lf}, the main diode current i_{D1}, the switch current i_{s1}, the switch voltage v_{ds1}, the filter inductor voltage v_{Lf}, and the *S1* drive signal S_1. The designation of each mode and associated time duration are marked just above the associated circuit.

The realization of VSDs is further discussed in Section VI after clarifying the electrical properties of passive soft switching.

V. Case Studies and Electrical Properties of Passive Soft-Switching PWM Converters

The ZVS buck–boost converter in Fig. 18(a) and the ZCZVS half-bridge converter in Fig. 16(a) are analyzed and experimented on to illustrate the correctness of the synthesis method and to evaluate the performance of passive soft switching. The performance is evaluated by the electrical properties, which are investigated on the basis of the operation principles and are used to assist in designing the snubbers.

A. Operation Principles

The operation principles are first analyzed based on the following assumptions.

1) All switches and energy storage components are ideal without parasitic elements.
2) The current in the filter inductors and the voltage in the filter capacitors are taken as constant.

Thereafter, the influence of nonideal factors is discussed.

1) Passive Zero-Voltage Turn-OFF PWM Converters: Fig. 19 shows the operation modes and the simulated key voltage and current waveforms. The ZVS buck–boost converter works periodically from mode I to mode V, where mode III and mode V are the normal operation modes, mode I and mode II realize hard turning on of *S1* and mode IV completes zero-voltage turning off of *S1*. In the turn-ON transition, *D1* turns off immediately at the time *S1* turns on; the snubber works similarly to the energy management circuits for ZVCs, where mode I is the energy transfer mode and mode II is the inductor reset mode. While in the turn-OFF transition, i.e., mode IV, *ZVC* is charged linearly by the L_f current until *D1* turns on.

2) Passive ZCZVS PWM Converters: With ZCLs inserted in the loop composed of voltage sources and switches, operation with dead time, no dead time, or overlap between switches is allowed. For the sake of simplicity, the operation with no dead time is discussed in detail.

The operation modes and the simulated key voltage and current waveforms are shown in Fig. 20. The ZCZVS half- bridge converter works periodically from mode I to mode VII, where mode IV and mode VII are the normal operation modes, mode I

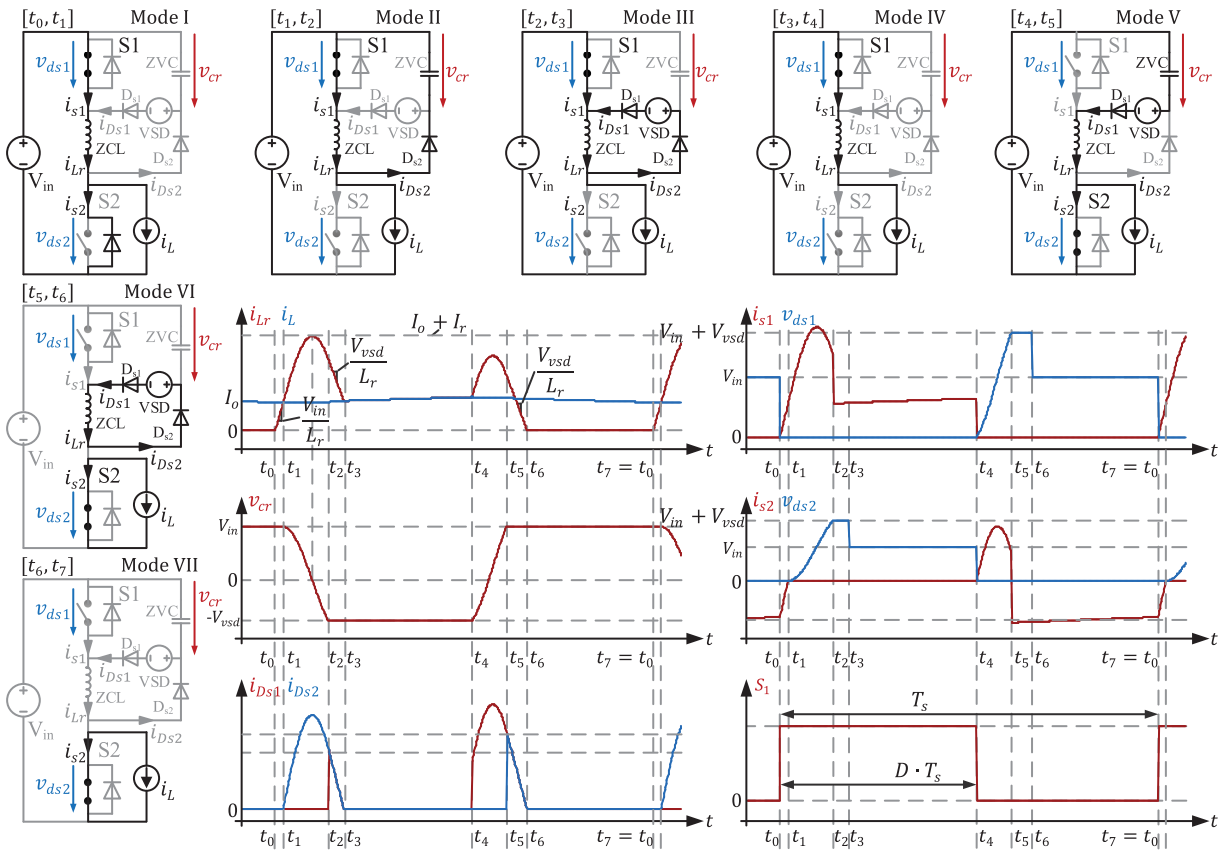

Fig. 20. Operation modes and the simulated key voltage and current waveforms of the passive ZCZVS half-bridge converter, including the ZCL current i_{Lr}, the filter inductor current i_L, the ZVC voltage v_{cr}, the snubber diode current i_{Ds1} and i_{Ds2}, the *S1* current i_{s1}, the *S1* voltage v_{ds1}, the *S2* current i_{s2}, the *S2* voltage v_{ds2}, and the *S1* drive signal S_1. The *S2* drive signal is complementary to the *S1* drive signal with no dead time. The designation of each mode and associated time duration are marked just above the associated circuit.

to mode III complete zero-current turning on of *S1* (zero-voltage turning off of *S2*), and mode V and mode VI realize zero-voltage turning off of *S1* (zero-current turning on of *S2*). In the turn-ON transition of *S1*, after mode I, where *ZCL* is charged linearly from zero to I_o, the snubber works similarly to the energy management circuits for ZVCs with *S1* being the served switch. Mode II is the energy transfer mode and mode III is the inductor reset mode. While in the turn-OFF transition of *S1*, due to the complementarity property, the snubber still works similarly to the energy management circuits for ZVCs, with *S2* being the served switch. Mode V is the energy transfer mode and mode VI is the inductor reset mode.

If dead time or overlap is employed, new operation modes corresponding to the dead time or overlap are inserted between the associated operation modes in Fig. 20. In general, the dead time lowers the energy in the resonant tank and is harmful for soft switching, while the overlap increases the energy in the resonant tank and is favored in passive soft switching. However, more complicated control logic is also induced due to employment of the overlap [44].

3) Influence of Nonideal Factors: The key nonideal factors in the snubber operation include the reverse recovery of diodes, parasitic inductors, and parasitic capacitors.

a) Reverse recovery of diodes: The reverse recovery of the snubber diodes occurs when the inductor reset modes ends. The reverse recovery current further discharges the ZVC and lowers its voltage. As for the reverse recovery of the diodes in the underlying converter, the reverse recovery of the diodes in the buck–boost converter has no effect on the snubber operation, while the reverse recovery of the diodes in the half-bridge converter works at the end of mode I (see Fig. 20). The reverse recovery of the body diode of *S2* induces more current in the ZCL, increases the energy in the resonant tank and is beneficial to soft switching.

b) Parasitic inductors: The problem of parasitic inductors is typical when applying the snubber in isolated converters [11], [12], [16], [37]. As analyzed in [37], parasitic inductors interact with the ZVC, pouring additional energy into the ZVC and increasing its voltage. In addition, the parasitic inductors in the loop composed of switches and ZVCs weaken the clamping effect of the ZVC on the switch voltage and need to be minimized.

c) Parasitic capacitors: Parasitic capacitors work when the voltage of the associated components varies. Thus, the parasitic capacitors of the components sharing the same changing moments of the impressed voltage with the ZVC are essentially in parallel with *ZVC* and function as part of the snubber. If the

TABLE II
LIMITATIONS IN THE REALIZATION OF PASSIVE SOFT SWITCHING IN THE ZVS BUCK–BOOST CONVERTER

Buck-Boost Converter	Turn-on Transition of *S1*		Turn-off Transition of *S1*	
Associated Mode Changing	Mode I and Mode II		Mode IV	
Required Variation	The *ZVC* voltage	The L_r current	The *ZVC* voltage	The L_r current
	From V_o to $-V_{in}$	From zero to zero	From $-V_{in}$ to V_o	Keep zero
Resulting Limitation	**VSD limitation**	**Duty Cycle Limitation**	**Load Limitation**	**No Limitation**
	$V_{vsd} < \frac{V_{in}+V_o}{2}$	$T_{r-on} < DT_s$	$T_{r-off} < (1-D)T_s$	—

TABLE III
LIMITATIONS IN THE REALIZATION OF PASSIVE SOFT SWITCHING IN THE ZCZVS HALF-BRIDGE CONVERTER

Half-bridge Converter	Turn-on Transition of *S1,* Turn-off Transition of *S2*		Turn-off Transition of *S1*, Turn-on Transition of *S2*	
Associated Mode Changing	Mode I, Mode II and Mode III		Mode V and Mode VI	
Required Variation	The *ZVC* voltage	The *ZCL* current	The *ZVC* voltage	The *ZCL* current
	From V_{in} to $-V_{vsd}$	From zero to I_o	From $-V_{vsd}$ to V_{in}	From I_o to zero
Resulting Limitation	**VSD limitation**	**Load Limitation**	**VSD Limitation**	**Load Limitation**
	$V_{vsd} < V_{in}$	$T_{r-on} < DT_s$	$V_{vsd} < V_{in}$	$T_{r-off} < (1-D)T_s$

capacitance of *ZVC* is relatively large compared with that of the parasitic capacitors, the influence of the parasitic capacitors can be ignored.

B. Electrical Properties

The electrical properties of the two example converters are investigated based on the operation principles to evaluate their performance, so that the snubbers are designed accordingly. It is noteworthy that most passive soft-switching PWM converters have similar electrical properties with those of the two examples.

1) Limitations on the Realization of Passive Soft Switching: Achieving passive soft-switching depends on the *ZVC* voltage and the L_r/ZCL current, which needs to reach a certain value, rendering limitations on the *VSD* voltage, duty cycle, and load current.

a) VSD limitation: The VSD limitation comes from the required resonant change of the *ZVC* voltage in turn-ON transitions of active switches. The possible maximum/minimum value of the *ZVC* voltage should be larger/smaller than the voltage that *ZVC* is to be clamped to. The limitations for the example buck–boost and half-bridge converter can be conveniently derived from Figs. 19 and 20 and are shown in Tables II and III, respectively. The VSD limitation in Table II is attained from considering that the example buck–boost converter is derived from Fig. 15(b) and is finally simplified to $V_{\rm in} < V_o$. The second VSD limitation in Table III is derived from the condition where $I_o = 0$, which is the worst case for soft-switching. The first VSD limitation for the example half-bridge converter shown in Table III is analyzed as an example. The required transition of the *ZVC* voltage in turning on of *S1* results in the limitation. The ZVC voltage needs to change from $V_{\rm in}$ to $-V_{\rm vsd}$, which occurs in mode II. According to Fig. 20, the possible minimum voltage of *ZVC* in mode II is $-V_{\rm in}$ and should be smaller than the voltage that *ZVC* is clamped to, i.e., $-V_{\rm vsd}$. Thus, the first VSD limitation is $V_{\rm vsd} < V_{\rm in}$.

The VSD limitation requires that the VSD voltage not be too high, which makes some realizations of the VSD with method 1 unworkable, as is the case in Fig. 18(c).

b) Duty cycle or load limitation: Duty cycle limitation is derived from the requirement of sufficient time for the complete transition of the *ZVC* voltage and L_r/ZCL current, i.e., the requirement of sufficient time for turn-ON and turn-OFF transitions. If the duration of the turn-ON/turn-OFF transition is associated with the load current, the limitation becomes load limitation. The results are shown in Tables II and III, where $T_{r-\rm on}$ and $T_{r-\rm off}$ are the turn-ON duration and turn-OFF duration, respectively, *D* is the duty cycle of *S1* and T_s is the switching period. $T_{r-\rm on}$ and $T_{r-\rm off}$ are detailed in Table IV, where V_r, I_r, and ω_r are the voltage amplitude, current amplitude, and angular frequency of the resonance between L_r/ZCL and *ZVC*, respectively, satisfying the following equations:

$$V_r = V_o\text{–}(V_{\rm vsd}\text{–}V_{\rm in}), V_{\rm vsd} = V_{\rm in}, \text{ for the buck–boost converter,}$$

$$V_r = V_{\rm in}, \text{ for the half-bridge converter,}$$

$$I_r = V_r/Z_r, Z_r = \sqrt{L_r/C_r}, \omega_r = 1/\sqrt{L_r\, C_r} \quad (1)$$

where L_r is the inductance of L_r/ZCL, C_r is the capacitance of *ZVC*, Z_r is the characteristic impedance.

Intuitively, the load limitation in Table II results in a minimum allowable load current. However, it is found that the load limitation in Table II for the buck–boost converter is always ensured, even for a large $T_{r-\rm off}$, which is associated with a small load current. $T_{r-\rm off}$ in the load limitation in Table II is determined by the L_f current and becomes larger if the load is small. Nevertheless, with the larger $T_{r-\rm off}$ is the lower effective duty cycle of *D1*, which still makes a considerable inductor current (see i_{Lf} and i_{D1} waveforms, Fig. 19) to provide the load current. In the ideal case, when the load current is small, the effective duty cycle of *D1* decreases to a level where the resulting inductor current is large enough to charge the ZVC in the OFF time of *S1*. In practice, as long as the converter works under CCM conditions, soft switching is attained. The load limitation in Table III contributes to the maximum allowable load current and $T_{r-\rm off}$ uses the high load approximation to estimate the maximum allowable load current.

2) DC Conversion Ratio and Duty Cycle: The dc conversion ratio determines the actual operation duty cycle, which has a

TABLE IV
SWITCHING TRANSITION TIME IN TABLES II AND III

Mode	Turn-on transition of $S1$, $T_{r\text{-}on}$	Turn off transition of $S1$, $T_{r\text{-}off}$
Transition Time of the Buck-boost Converter	$\cos^{-1}(-\frac{V_{vsd}}{V_r})/\omega_r + \frac{L_r}{V_{vsd}} I_r \sin(\cos^{-1}(-\frac{V_{vsd}}{V_r}))$	$\frac{C_r}{I_{L_f}}(V_o + V_{in})$
Transition Time of the Half-bridge Converter	$\frac{L_r}{V_{in}} I_o + \cos^{-1}(-\frac{V_{vsd}}{V_r})/\omega_r + \frac{L_r}{V_{vsd}} I_r \sin(\cos^{-1}(-\frac{V_{vsd}}{V_r}))$	No load solution: $\cos^{-1}(-\frac{V_{vsd}}{V_r})/\omega_r + \frac{L_r}{V_{vsd}} I_r \sin(\cos^{-1}(-\frac{V_{vsd}}{V_r}))$, High load approximation: $\frac{L_r}{V_{vsd}} I_o$.

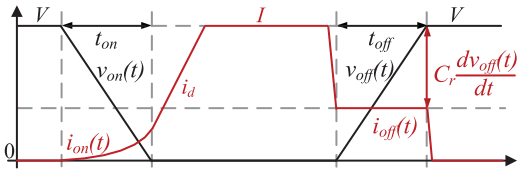

Fig. 21. Switch voltage and current waveforms with ZCL and ZVC equipped.

limitation in achieving passive soft- switching. The voltage at the switching point is used to identify the dc conversion ratio, which is v_{Lf} in Fig. 19 and v_{ds2} in Fig. 20. Employing a linear approximation on the rise and fall of the voltage and using the volt-second balance on the filter inductor, the dc conversion ratio M of the two example converters is attained.

For the ZVS buck–boost converter

$$M = \frac{V_o}{V_{\text{in}}} = \frac{DT_s + 0.5T_{r-\text{off}}}{(1-D)T_s - 0.5T_{r-\text{off}}} \tag{2}$$

where $T_{r-\text{off}}$ varies from nearly zero to nearly $(1 - D)\ T_s$ with the load current changing from maximum to nearly zero (see Fig. 19). Thus

$$D = D_{\min} \sim D_{\max} = \frac{M-1}{M+1} \sim \frac{M}{M+1}. \tag{3}$$

For the ZCZVS half-bridge converter

$$M = \frac{V_o}{V_{\text{in}}} \approx D - \frac{T_I}{T_s} + \frac{1}{2}\left(\frac{V_{\text{vsd}}}{V_{\text{in}}} - 1\right)\frac{T_{II}}{T_s} + \frac{V_{\text{vsd}}}{V_{\text{in}}}\frac{T_{III}}{T_s} \tag{4}$$

where T_I, T_{II}, and T_{III} are the durations of mode I, mode II, and mode III, respectively. The duty cycle is then calculated by the following:

$$D \approx M + \frac{T_I}{T_s} - \frac{1}{2}\left(\frac{V_{\text{vsd}}}{V_{\text{in}}} - 1\right)\frac{T_{II}}{T_s} - \frac{V_{\text{vsd}}}{V_{\text{in}}}\frac{T_{III}}{T_s}. \tag{5}$$

It can be seen that the duty cycle is influenced by the load current. Variations in the duty cycle should be considered when evaluating the duty cycle limitation and load limitation.

3) Switching Loss Elimination: The switching loss with the ZCL and ZVC employed is evaluated by the simplified models in [45] and [46] with some modification.

Considering MOSFET is the switch and assuming a linear change of switch voltages in the turn-ON and turn-OFF transitions, as illustrated in Fig. 21, turn-ON loss $W_{\text{on\_loss}}$ and turn-OFF loss $W_{\text{off\_loss}}$ are expressed by

$$W_{\text{on\_loss}} = \int_0^{t_{\text{on}}} v_{\text{on}}(t) i_{\text{on}}(t) dt + W_{\text{Coss}}, \tag{6}$$

$$W_{\text{off\_loss}} = \begin{cases} \text{if } W_{\text{off\_loss}} > 0, \\ \int_0^{t_{\text{off}}} v_{\text{off}}(t) i_{\text{off}}(t) dt - W_{\text{Coss}} \\ \text{else} \\ 0. \end{cases} \tag{7}$$

with

$$v_{\text{on}}(t) = V\left(1 - \frac{t}{t_{\text{on}}}\right),$$

$$i_{\text{on}}(t) = \frac{1}{L_r}\int_0^t (V - v_{\text{on}}(t))dt = \frac{V}{2L_r\ t_{\text{on}}} t^2$$

$$v_{\text{off}}(t) = \frac{V}{t_{\text{off}}} t, i_{\text{off}}(t) = I - C_r \frac{d\ v_{\text{off}}(t)}{dt} = I - C_r \frac{V}{t_{\text{off}}}$$

where W_{Coss} is the energy stored in the output parasitic capacitor of the switch in the turn-OFF transitions and dissipated in the switch channel in the turn-ON transitions [47]. In the turn-OFF transitions, the linear change of the switch voltage occurs when the drive signal is on the Miller platform. Thus,

$$\frac{d\ v_{\text{off}}(t)}{dt} = \frac{i_g}{C_{dg}}, i_g = \frac{V_{\text{plate}}}{R_g}, t_{\text{off}} = \frac{V}{i_g/C_{dg}}$$

where i_g is the drive current, C_{gd} is the Miller capacitance, R_g is the gate resistance, and V_{plate} is the drive voltage on the Miller platform in turn-OFF transitions. Then, the turn-ON loss $W_{\text{on\_loss}}$ and turn-OFF loss $W_{\text{off\_loss}}$ are as follows:

$$W_{\text{on\_loss}} = \frac{V^2 t_{\text{on}}^2}{24L_r} + W_{\text{Coss}}, \tag{8}$$

$$W_{\text{off\_loss}} = \begin{cases} \text{if } C_r < \dfrac{I\ R_g}{V_{\text{plate}}} C_{gd} - \dfrac{2W_{\text{Coss}}}{V^2}, \\ \left(\dfrac{I\ R_g}{V_{\text{plate}}} C_{gd} - C_r\right)\dfrac{V^2}{2} - W_{\text{Coss}} \\ \text{else} \\ 0. \end{cases} \tag{9}$$

which are the same as the models in [45] and [46], except that W_{Coss} is included in $W_{\text{on\_loss}}$. Summarizing $W_{\text{on\_loss}}$ and $W_{\text{off\_loss}}$ finds that passive soft switching eliminates the switching losses induced by the voltage–current overlapping and reverse recovery of diodes, but not the losses associated with the

output capacitor of the switch. Elimination of switching losses is associated with the size of L_r and C_r.

To minimize the switching losses

$$L_r \geq \frac{V \cdot t_{\rm on}}{I} \text{ and } C_r \geq \frac{I \cdot R_g}{V_{\rm plate}} C_{dg} \tag{10}$$

are recommended, contributing to the complete elimination of turn-OFF losses and more than a 90% reduction of the turn-ON losses if the hard turn-ON loss is estimated by $V\,I\,t_{\rm on}/2$ [27].

4) Switch Voltage Stress and Component Current Stress: Switch voltage stress directs the selection of switches, is positively related to ON-state resistance, and if possible, should not greatly increase when snubbers are employed. For the ZVS buck–boost converter, the switch voltage stress does not change (see Fig. 19), while for the ZCZVS half-bridge converter, the maximum switch voltage is increased by the *VSD* voltage (see Fig. 20). The increase is due to the reset requirement of *ZCL*, which is in series with the switches. In general terms, if *VSD* is realized by method 1 in Section IV-C, the switch voltage stress is increased to a relatively high level. If *VSD* is realized by method 2 or method 3, the VSD voltage is recommended to be limited between 0.2–0.5 V_g where V_g is the switch voltage stress without snubbers, so that the voltage stress does not increase too much and the ZCL is able to reset.

The component current stress directly influences the converter efficiency. A qualitative analysis is presented on the two example converters to investigate the influence of the snubber parameters, i.e., C_r and L_r, on the current stress of the underlying PWM converters and snubbers. According to the component characteristics, the rms active switch current, the average diode current, and the rms and peak inductor current are defined as the current stress. Additionally, the current stress of the snubber diodes is measured by the rms current of the resonant inductors. Thus, the current stress of the inductors and switches in the underlying converter and current stress of the resonant inductors in the snubber are analyzed.

For the ZVS buck–boost converter, the L_f current is first analyzed. With C_r increased, $T_{r-\rm off}$ is increased and the effective duty cycle of *D1* is decreased, thus, the inductor current is increased to provide the needed output current (refer to Fig. 19). To limit the increase in the L_f current, $T_{r-\rm off}$ should be limited below 1/10 of the period, which sets an upper limit of C_r. Second is the analysis of the current stress of *S1* and L_r. If C_r is determined, the current stress of both components are mainly influenced by L_r. A larger L_r contributes to a lower amplitude of the L_r and switch currents [see (1) and Fig. 19]. Thirdly, the current stress of *D1*, i.e., the average value, equals the output current and is not influenced by the snubber. Hence, considering the current stress, C_r should be limited and L_r is expected to be as large as possible.

As for the ZCZVS half-bridge converter, first the current stress of L_f is not influenced by snubbers. Second, the current stress of *S1* and *S2*, i.e., the rms current, is mainly influenced by mode I in the turn-ON transition of *S1* if the resonant periods of *ZVC* and *ZCL* are limited (see Fig. 20). A larger L_r contributes to a longer duration of mode I, thus increasing the current stress of *S1* but decreasing the current stress of *S2*. It is assumed that the total current stress of *S1* and *S2* is not changed by the variation in L_r. Thirdly, in regard to the current stress of the resonant inductor *ZCL*, on one hand, a larger L_r contributes to a longer transition time and a larger rms of the *ZCL* current (see Fig. 20). On the other hand, a smaller L_r as well as a larger C_r renders a larger peak value of the *ZCL* current [see (1) and Fig. 20]. Thus, considering the current stress, C_r should be small and L_r is recommended to be a value that limits the amplitude of the resonant current I_r to 0.5–1 times of the output current, so that both the rms and peak value of the *ZCL* current are kept reasonable.

C. Design Considerations and Experimental Evaluation

The design of snubbers is a multiobjective optimization problem [37], with the objectives defined by the electrical properties illustrated above and summarized in Table V. The electrical properties give a set of inequality constraints, according to which the values of *ZVC* and L_r/ZCL are determined. For both examples, it is desirable to have small *ZVC* values considering the component current stress. Thus, a minimum C_r associated with switching loss elimination is employed. In terms of the resonant inductor, the L_r value in the buck–boost converter is determined by the duty cycle limitation with $D_{\rm min}$ used. The value of *ZCL* in the half-bridge converter is determined by limiting the resonant current I_r to 0.5–1 times of I_o. By doing so, other inequality constraints are usually ensured. If not, a smaller C_r should be considered.

Except for the values of *ZVC* and L_r/ZCL, the VSD voltage also needs to be designed, which is constrained by the VSD limitation and switch voltage stress. For the ZVS buck–boost converter, the VSD voltage, i.e., $V_{\rm in}$, should be lower than $(V_{\rm in}+V_o)/2$. Thus, V_o should be larger than $V_{\rm in}$. In the half-bridge converter, $V_{\rm vsd}$ is recommended to be between 0.2 $V_{\rm in}$ and 0.5 $V_{\rm in}$.

Following the design recommendations, the two example converters are constructed and evaluated. The specifications of the underlying converters are shown in Table VI. The design specifications and design results of the snubbers are shown in Table VII, where the *ZVC* value in the buck–boost converter in the experiment is increased to 10 nF to alleviate its interaction with the parasitic inductors. A detailed step by step procedure for the design of the snubber in the ZCZVS half-bridge converter is given in the Appendix as an example. For the sake of simplicity, the VSD in the half-bridge converter is simulated with a 47 μF capacitor in parallel with a resistor.

Fig. 22(a) and (b) show the key voltage and current waveforms of the ZVS buck–boost converter, measured under a low load (0.1 A) and a rated load (1.5 A), respectively, including the drive signal S_1, switch voltage v_{ds1} and the L_r current i_{Lr}, with an enlarged view of the turn-OFF transition on the right side. The zero-voltage turning off is realized under both the low load and rated load and is judged by the drive signal and the associated switch voltage.

Fig. 23(a) to (d) illustrate the key voltage and current waveforms of the ZCZVS half-bridge converter, including the switch voltage v_{ds1}, v_{ds2}, *ZCL* current i_{Lr}, and drive signal S_1, S_2, with

TABLE V
ELECTRICAL PROPERTIES AND DESIGN CONSTRAINTS

Electrical Properties	ZVS Buck-Boost Converter	ZCZVS Half-Bridge Converter
VSD Limitation	$V_{vsd} < (V_{in}+V_o)/2$, i.e. $V_{in} < V_o$	$V_{vsd} < V_{in}$
Duty Cycle Limitation or Load Limitation	$T_{r\text{-}on}(L_r,C_r) < D{\cdot}T_s$	$T_{r\ on}(L_r, C_r, I_o) < D{\cdot}T_s$
	$T_{r\text{-}off} < (1\text{-}D){\cdot}T_s$ (always ensured)	$T_{r\text{-}off}\ (L_r, C_r, I_o) < (1\text{-}D){\cdot}T_s$
Dc Conversion Ratio and Duty Cycle	$D_{min} \sim D_{max}$	$D(L_r, C_r, I_o)$
Switching Loss Elimination	Minimum L_r and C_r	
Switch Voltage Stress	-	If possible, $V_{vsd} = 0.2\sim0.5V_{in}$
Component Current Stress	Limit the value of *ZVC*, enlarge the value of L_r as far as possible.	Limit the value of *ZVC*, limit resonant current I_r to 0.5~1 times of I_o.

TABLE VI
SPECIFICATIONS OF THE UNDERLYING CONVERTERS

	Buck-Boost	Half Bridge
Input Voltage	12 V	24 V
Output Voltage	24 V	12 V
Output Current	1.5 A	3 A
Switching Frequency	100 kHz	100 kHz
S1	FQP70N10	FQP70N10
D1/S2	FST20120	FQP70N10
Filter Inductor	100 uH	100 uH

TABLE VII
SPECIFICATIONS AND DESIGN OF THE SNUBBERS

	Buck-Boost	Half Bridge
Design of the ZVC		
C_{dg}	200 pF	200 pF
R_g	10 Ω	10 Ω
V_{plate} [(a)]	3.18 V	3.12 V
Switching Current *I*	4.5 A	3 A
ZVC	2.8 nF/10 nF[(c)]	1.9 nF/4.7 nF[(c)]
Design of the resonant inductor		
Design Considerations	$D_{min} = 0.33$	$I_o = 3$ A, $I_r = 0.8I_o$
L_r/ZCL [(b)]	75 uH/80 uH[(c)]	0.47 uH/0.47 uH[(c)]
Design of the VSD and snubber diodes		
VSD	12 V (V_{in})	0.2 V_{in} ≈ 5 V
Snubber Diodes	1N5819	1N5819

[(a)]Estimated from gate charge characteristics of the datasheet of FQP70N10 assuming the transconductance is constant.
[(b)]Calculated using the experimental value of *ZVC*.
[(c)]Calculated value/Experimental value.

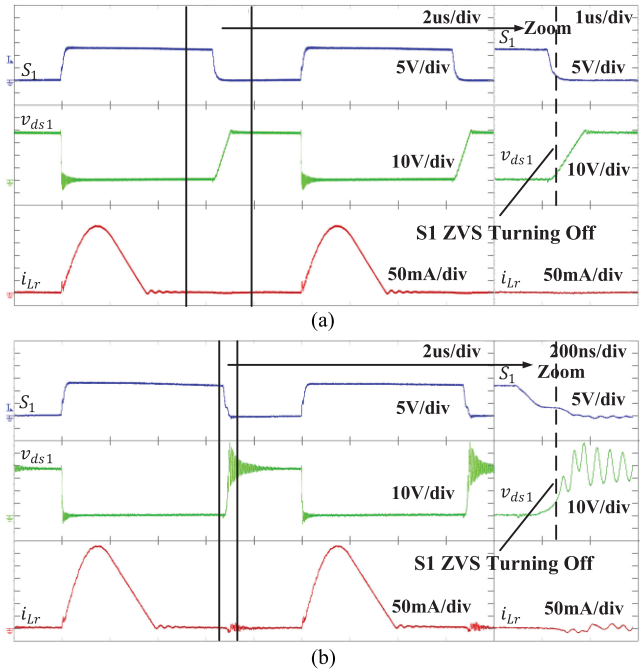

Fig. 22. Key voltage and current waveforms of the ZVS buck–boost converter, including the drive signal S_1, the switch voltage v_{ds1} and the L_r current i_{Lr}, with an enlarged view on the right side. (a) Measured under 0.1 A low load. (b) Measured under 1.5 A rated load.

enlarged views of the turn-ON transition and turn-OFF transition on the bottom side. Among the four figures, Fig. 23(a) and (b) are measured under low loads (0.25 A), while Fig. 23(c) and (d) are measured under the rated load (3 A). The zero current turning on and zero voltage turning off of *S1* and *S2* are realized in both load conditions, where zero current turning on is judged by the switch voltage and the ZCL current as shown in Fig. 23(a) and (c), and zero voltage turning off is judged by the switch voltage and drive signal, as shown in Fig. 23(b) and (d).

In both examples, the operation principles are verified by the L_r/ZCL current, from which the energy transfer process and inductor reset process are recognized as shown in Figs. 22(a) and (b), and 23(a) and (c). In addition, from the L_r/ZCL current and the switch voltage, the experimental transition time and duty cycle of the two example converters are attained and are shown in Fig. 24, where the calculated values [calculated from Table IV, (2) and (5)] are also presented. The experimental values are consistent with the calculated values, confirming the accuracy of the expressions. The duty cycle or load limitations listed in Tables II and III are then verified by the transition time and duty cycle. Moreover, the experimental values of $V_{\rm vsd}$, $V_{\rm in}$, and V_o accords with the designed values. That is, the VSD limitations are also satisfied.

Fig. 25(a) and (b) show the comparisons of the measured efficiency of the two soft switching converters with that of their hard switching counterparts and the estimated efficiency of the two converters. In the comparison with the estimated efficiency, the measured efficiency of both converters is lower under high loads. The cause may be that the snubber diode switching loss, the eddy current copper loss of L_r/ZCL and the loss due to parasitic oscillations are not included in the estimation. In regard to the comparison of the measured efficiency between soft-switching and hard-switching in the buck–boost converter, the snubber decreases the efficiency under low loads and high loads, and increases the efficiency under mid loads as shown in Fig. 25(a). Although a proper snubber design is conducted, the

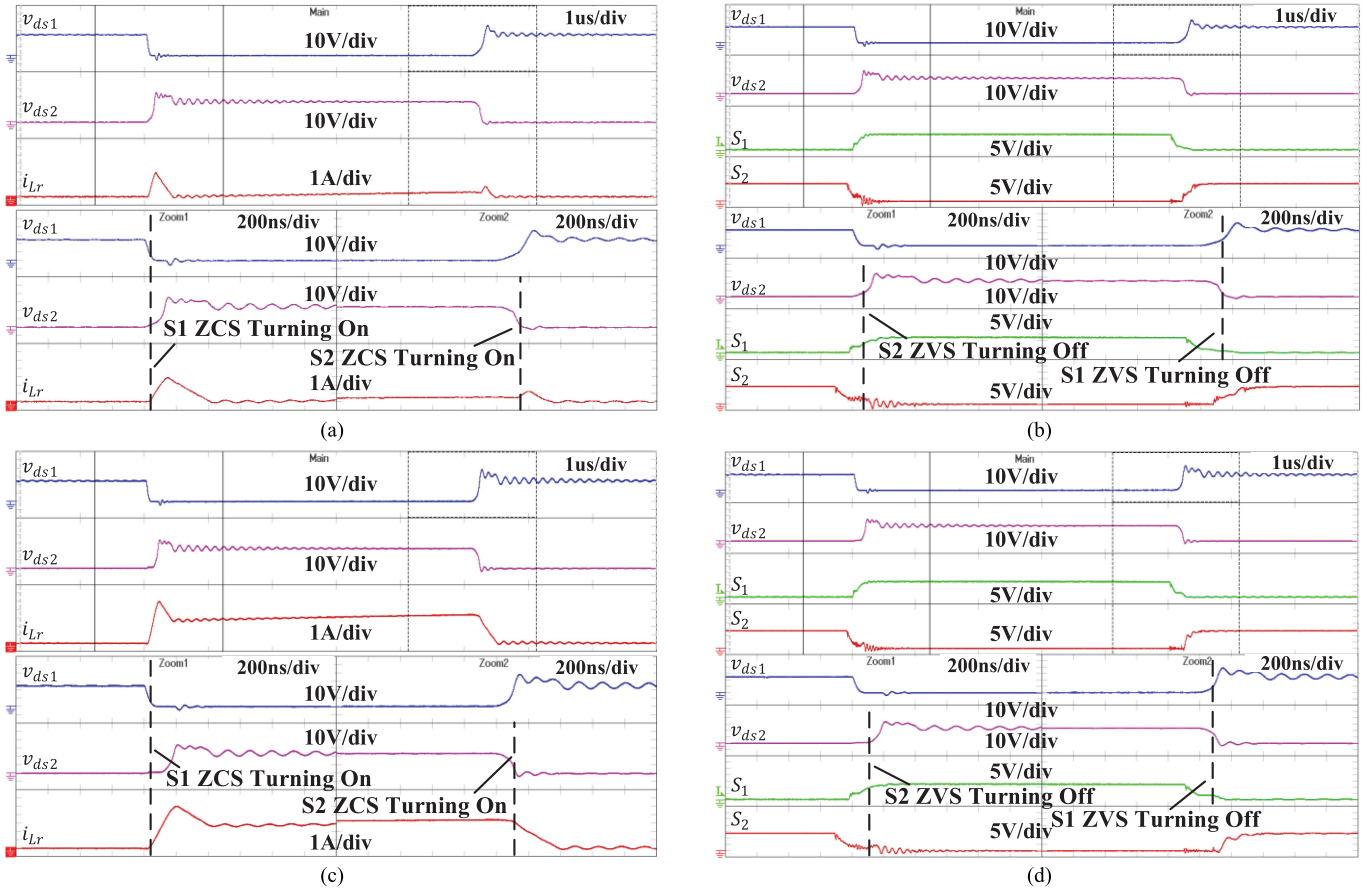

Fig. 23. Key voltage and current waveforms of the ZCZVS half-bridge converter, including the switch voltage v_{ds1}, v_{ds2}, the *ZCL* current i_{Lr}, and the drive signal S_1, S_2, with two enlarged views on the bottom side of each figure. (a) and (b) are measured at 0.25 A low load, (c) and (d) are measured at 3 A rated load.

component current stress is still increased and the reactive power is still induced as indicated in Fig. 19. On the other hand, the output parasitic capacitors of the MOSFET and the diode function as ZVCs in the hard switching buck–boost converter. The poor efficiency range of the ZVS converter may arise from the two points. The turn-OFF snubber may have good performance of efficiency for other converters, which needs further investigations. Moreover, in some cases, such as a fly-back or forward converter, a turn-OFF snubber is needed to suppress voltage spikes induced by leakage inductors [37], [48], [49]. As for the comparison of the measured efficiency between soft-switching and hard-switching half-bridge converters, although the energy poured into the VSD is dissipated, the efficiency is still increased by about 1%.

VI. Applicability Discussion

The applicability of snubbers and passive soft-switching PWM converters lies in making full use of the advantages while simultaneously alleviating the disadvantages. The advantages mainly come from eliminating the switching loss and are ensured by proper snubber design. The disadvantages revealed from the electrical properties include the VSD limitation, duty cycle limitation/load limitation, and the increase in the switch voltage and component current stresses. Another disadvantage is the increase in the complexity of the converters, which is associated with the topological properties. Among all disadvantages, the duty cycle limitation/load limitation and the increase in the component current stress can be mitigated by proper snubber design, as analyzed in Section V-B. Thus, it is believed that the applicability of snubbers and passive soft-switching converters is determined by the increase in the complexity of the converters, the VSD limitation, and the increase in the switch voltage stress. All three disadvantages are associated with VSD realizations.

A. VSD Realization Revisited

The VSD realizations performed in methods 1 and 2 are employed for the applicability discussion.

Method 1 offers the simplest snubbers and converters but has the strictest limitation on the VSD location and a limitation on the VSD voltage, i.e., the voltage of the dc voltage sources (or low frequency capacitors) in the main circuit. As a result, the output or the input is limited in most cases, which is the situation in the example ZVS buck–boost converter. In addition, when method 1 is used in ZCZVS switching, the increased switch voltage stress is uncontrollable and determined by the main

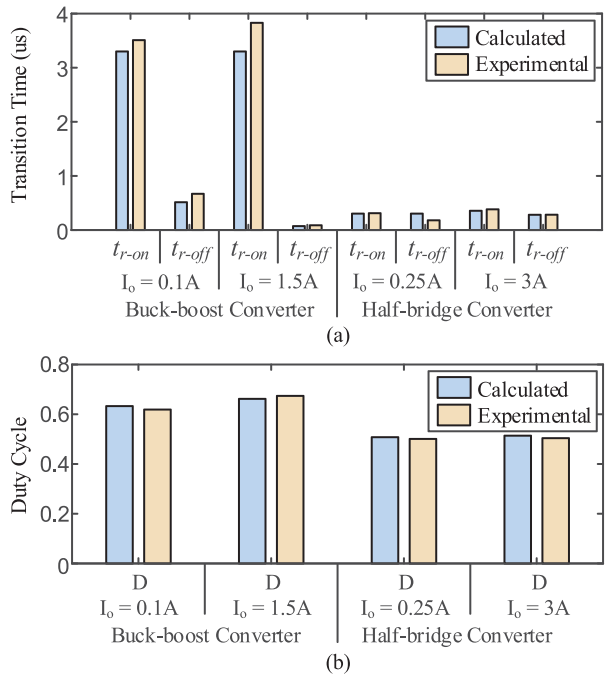

Fig. 24. (a) Transition time and (b) duty cycle of the ZVS buck–boost and ZCZVS half-bridge converter under a low load and the rated load.

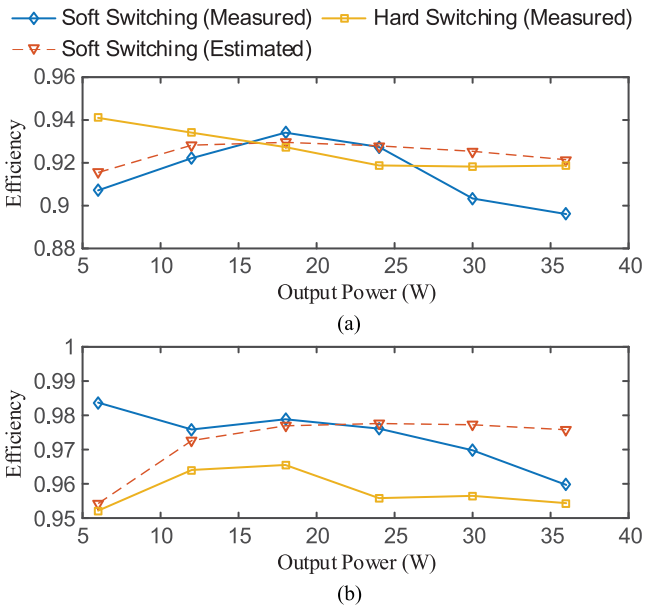

Fig. 25. Comparison of the measured efficiency of the two example soft-switching converters with that of their hard switching counterparts and with the estimated efficiency of the two converters. (a) ZVS buck–boost converter. (b) ZCZVS half-bridge converter.

circuit, which in some cases, makes the increase in the voltage stress relatively high.

As for method 2, three levels of complexity are further recognized according to the complexity of the auxiliary circuit for VSDs.

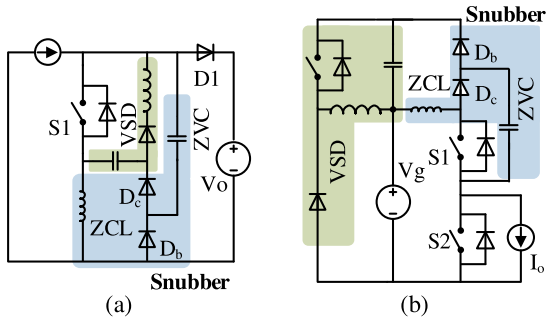

Fig. 26. (a) Example of VSD realization with method 2 of level 1, i.e., using only passive components for the VSD. (b) Example of VSD realization with method 2 of level 2, i.e., using a nonisolated converter for the VSD.

TABLE VIII
COMPARISON OF THE VSD REALIZATION METHODS

VSD realization	The Complexity of Snubbers and Converters	Limitation on the VSD location	Controllability of the VSD Voltage	VSD Efficiency
Method 1	Simplest	Strictest	Uncontrollable	Highest
Method 2 of Level 1	Simple	Strict	Variation with D and I_o	High
Method 2 of Level 2	Complex	Weak limitation	Totally Controllable	Low
Method 2 of Level 3	Most Complex	No limitation	Totally Controllable	Lowest

Level 1: Realize the auxiliary circuit with only passive components.
Level 2: Realize the auxiliary circuit with nonisolated converters.
Level 3: Realize the auxiliary circuit with isolated converters.

Examples of level 1 and level 2 realizations from [34] and [42] are shown in Fig. 26. As seen, level 1 realization has the simplest topology of the three levels. However, the VSD location is limited, and due to the employment of only passive components, the VSD voltage varies with the duty cycle D and load current I_o [45], [46]. The VSD voltage needs to be carefully designed to fulfill the VSD limitation and to limit the increase in the switch voltage stress, increasing the design complexity. As for level 2 and 3 realizations, both can set the VSD voltage at an expected value, which makes the VSD limitation easily fulfilled and conveniently controls the increase in the switch voltage stress. Level 2 realization is simpler but has a limitation on the VSD location. Although level 3 realization is more complicated, it is more flexible without limiting the VSD location.

It can be seen that the realization of VSDs greatly influences the complexity of the topologies and that there is a tradeoff between complexity and performance, as shown in Table VIII. This tradeoff needs to be considered in the application of snubbers and passive soft switching converters. It is also observed that the simplest turn-OFF snubber or soft-switching snubber is the snubber composed with a ZVC, a resonant inductor and two diodes (the L-C-D-D snubber), with method 1 realizing VSDs and some sacrifice in the performance.

B. Application of Snubbers to Given Underlying PWM Converters

For both turn-OFF snubbers and soft-switching snubbers, there are more than one topologies (see Figs. 7 and 11), more than one locations for assembling (see Fig. 14), and more than one realizations for VSDs. With variations of the topologies, the locations and the realizations of VSDs, the complexity and performance of the snubbers and converters change (see Table VIII). The complexity is taken as the primary consideration. Hence, the application of snubbers to given underlying PWM converters should systematically consider all the possibilities of snubbers, and pick the simplest one that fulfills the design specifications. If the resulting snubber is still too complicated, other technologies need to be considered.

C. Application of Passive Soft-Switching PWM Converters

After investigating the characteristics of the methods for VSD realizations, three kinds of passive soft-switching PWM converters are believed to have the most potential of wide applications. Each kind in some way mitigates the disadvantages in the application, including the increase in the complexity, the VSD limitation and the increase in switch voltage stress.

1) Isolated Zero-Voltage Turn-OFF DC–DC Converters With a Turn-OFF Snubber Where the VSD Is Realized by Method 1: Examples were given in [11], [12], [16]. Typical work has been done in [37], [48], and [49]. The snubber topology is simplest due to the realization of VSDs with method 1. The limitation on the input/output arising from the VSD limitation is mitigated by the transformers. Additionally, the voltage stress is not increased by the snubbers in zero-voltage conditions. The resonant inductor in the snubber can be conveniently integration into transformers as investigated in [16], [37], [48], and [49].

2) Three Level ZCZVS Converters With Two Snubbers Where the VSDs Are Realized by Method 1: Examples and typical work were investigated in [18], [20], and [44]. The snubber topology is simplest and the limitation on the input/output arising from the VSD limitation does not exist because the voltage source for the VSD is not involved in the operation of the switches that the snubber serves. The obstacle in the application may come from the increase in switch voltage stress which brings an increase in the ON-state resistance. More work needs to be performed to compare the three level ZCZVS converters with conventional three level converters.

3) Three-Phase ZCZVS Inverters With a Common ZCL for the Three Phase and With the VSDs Realized by Method 2 of Level 2: An example and typical work were given in [42]. Although the VSD realization method is rather complicated. Two factors help mitigate the complexity. One is that the three phase share the same VSD and the same ZCL. The other factor is that in medium and high power applications to which the three-phase inverter is always applied, the increased complexity becomes acceptable considering the power of the auxiliary circuit is not high. Because the VSD voltage is controllable, the VSD limitation can be easily fulfilled and the increase in switch voltage stress can be controlled to acceptable value.

VII. CONCLUSION

This article has proposed methods for the synthesis of passive ZVS and ZCZVS PWM converters, and has investigated the topological and electrical properties of the snubbers and converters. It is observed that the realization of VSDs greatly influences the complexity and performance of the converters, the simplest turn-OFF and soft-switching snubbers are the L-C-D-D snubbers, and there is a tradeoff between complexity and performance. The suggestion on snubber applications has been presented. And three kinds of reported passive soft-switching converters which are believed to have the most potential of wide application have been discussed.

APPENDIX
DETAILED DESIGN PROCEDURE FOR THE SNUBBER IN THE ZCZVS HALF-BRIDGE CONVERTER

This section gives a step by step procedure for the design of the snubber in the ZCZVS half-bridge converter, according to the specifications listed in Table VII.

Step 1: Determine the value of ZVC.

The value of *ZVC* is determined according to the condition for eliminating the switching loss, where (10) is employed

$$C_r \geq \frac{I\,R_g}{V_{\text{plate}}} C_{dg} = 1.9 \text{ nF}.$$

Thus, $C_r = 4.7$ nF is used.

Step 2: Determine the value of ZCL.

The value of *ZCL* is determined according to the condition for lowering the component current stress, where I_r needs to be limited to 0.5–1 times of I_o. $0.8I_o$ is employed for I_r. Using (1)

$$I_r = \frac{V_r}{Z_r} = V_{\text{in}} \sqrt{\frac{C_r}{L_r}}.$$

Then, $L_r = 0.47\ \mu$H.

Step 3: Choose snubber diodes and VSD voltage.

According to the condition for limiting the switch voltage stress, $V_{\text{vsd}} = 0.2$–$0.5\ V_{\text{in}}$ is recommended and $V_{\text{vsd}} = 0.2\ V_{\text{in}}$ is used. The diodes are chosen according to their voltage and current stress, which are identified with simulations. Diode 1N5819 is used.

Step 4: Verify the electrical properties.

Simulations under both the low load and rated load could be used to accelerate this step. All the conditions in Table V are satisfied.

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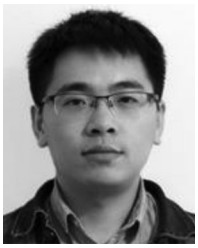
Xiang Yu received the B.Sc. degree in electrical engineering, in 2013, from the School of Electrical Engineering and Automation, Hefei University of Technology, Hefei, China, where he is currently working toward the Ph.D. degree in power electronics.

His current research interests include novel soft-switching topologies, magnetic component design, high power density converters, and wide-band-gap power semiconductor devices.

Jianhui Su received the B.Sc., M.Sc., and Ph.D. degrees from Hefei University of Technology, Hefei, China, in 1984, 1987, and 2003, respectively, all in electrical engineering.

He is currently a Full Professor with the School of Electrical Engineering and Automation, Hefei University of Technology, and an Associate Director of the Research Center for Photovoltaic System Engineering, Ministry of Education, Hefei. His research interests include renewable power generation, special power supply, distributed power generation systems, and high-voltage transducer control technologies.



Shilin Guo (S'16) received the B.Sc. and Ph.D. degrees in electrical engineering from Hefei University of Technology, Hefei, China, in 2013 and 2018, respectively.

From 2018 to 2019, he was a Postdoctoral Researcher at Lehigh University, Bethlehem, PA, USA. His current research interests include topology and design of high-frequency power converters, distributed power generation systems and micro grid control, magnetic design, and single stage audio power amplifier.

Shu Zhong received the B.Sc. and Ph.D. degrees in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2012 and 2018, respectively.

In 2018, he was with Huawei Technologies Co. Ltd., Dongguan, China, where has been engaged in product design, research, and development. His current research interests include high frequency power conversion, soft switching techniques, magnetic design, EMI, telecom power convention, and switching audio amplifiers.

Yong Shi received the B.Sc. degree in automation from Anhui University, Hefei, China, in 2008, and the Ph.D. degree in electrical engineering from Hefei University of Technology, Hefei, China, in 2015.

He is currently a Lecturer with the School of Electrical Engineering and Automation, Hefei University of Technology. His research interests include renewable energy generation technology, distributed power generation, and microgrid.

Jidong Lai received the B.Sc. degree in automatic engineering, and the M.Sc. and Ph.D. degrees in power electronics and power drives from Hefei University of Technology, Hefei, China, in 2004, 2007, and 2012, respectively.

He is currently an Associate Professor with the School of Electrical Engineering and Automation, Hefei University of Technology. His current research interests include special power supply, high-frequency power converters, distributed power generation, and microgrid control.