Phase-Locked Loop Combined With Chained Trigger Mode Used for Impedance Matching in Wireless High Power Transfer

Yongbin Jiang, *Student Member, IEEE*, Laili Wang, *Senior Member, IEEE*, Yue Wang, *Member, IEEE*, Min Wu, Zexian Zeng, Yonghui Liu, *Student Member, IEEE*, and Jing Sun

***Abstract*—In a wireless power transfer system (WPTS), the control technique of the active rectifier is vital for improving the transfer efficiency of the resonant network, expanding the operating range of the load, and increasing the power density. An indispensable component of such control technique is the accurate and reliable phase-locked method for the resonant current. However, the traditional phase-locked method based on the DSP controller tends to lose driver pulses, which might cause damage to the safe operation of the WPTS. This article illustrates the essential reason why the driver pulses lose and proposes a phase-locked loop combined with the chained trigger mode (PLL-CTM) that can lock the phase of the resonant current accurately and produce the driver pulses reliably. With the proposed PLL-CTM applied, the reliability of the WPTS can be enhanced tremendously. Furthermore, based on the PLL-CTM, this article also presents a double-side phase shift control (DPSC) strategy to achieve constant-current constant-voltage charging and minimize the power loss of the resonant network simultaneously. Finally, a 500-W WPT prototype is built to verify the feasibility of the DPSC with PLL-CTM. Benefiting from the DPSC with PLL-CTM, the WPTS not only obtains a high accuracy in steady state, but also achieves a good dynamic performance with the step change of R_{L} and R_{Eref}.**

***Index Terms*—Active rectifier (AR), chained trigger mode (CTM), double-side phase shift control (DPSC), phase-locked loop (PLL), wireless power transfer (WPT).**

I. Introduction

CONSIDERABLE advantages of the wireless power transfer (WPT) have given rise to a strong focus on both academic community and business domain throughout the world. With the merit of convenience and safety, it has been applied to various applications, such as biomedical plants [1], [2], underwater equipment [3], mobile phones [4], and electric vehicles (EVs) [5]. The power levels of the wireless power transfer system (WPTS) range from several milliwatts to tens of kilowatts.

Nowadays, one of the most promising applications for the WPT technique is in EVs. Generally speaking, there are two important aspects concerned by the EV manufacturer, especially for high power applications. On the one hand, the transmitter coil of the WPTS is commonly buried under the pavement, which makes it difficult to deal with the heat dissipation of the coil. Consequently, it is necessary to reduce the power loss of the resonant network as much as possible. On the other hand, the equivalent resistance of battery packs in EVs can change greatly according to their charging profile. The various equivalent load for the WPTS affects the transfer efficiency dramatically [6]–[8].

To improve the transfer efficiency in the whole charging process of battery packs, many researchers are dedicated to exploring and solving this challenge. An adaptive impedance matching method for the SS-type WPTS is proposed [7]–[9].

The typical fundamental harmonic equivalent circuit of the SS-type WPTS is shown in Fig. 1. According to [8] and [9], when the operating frequency ω_{s} is fixed as the resonant frequency ω_0 and the ac equivalent resistor R_{E} is fixed as a constant value R_{Eopt}, the transfer efficiency of the resonant network can achieve the maximum value. When the equivalent series resistances (ESRs) of the resonant network in two sides are represented as R_1 and R_2, respectively, the conditions for the maximum transfer efficiency are listed as

$$\begin{cases} \omega_{\mathrm{s}} = \omega_0 \\ R_{\mathrm{Eopt}} = R_2\sqrt{1+\frac{(\omega_{\mathrm{s}}M)^2}{R_1R_2}}. \end{cases} \tag{1}$$

Nevertheless, R_{E} gradually changes as the charging process goes with the uncontrolled rectifier in practical applications.

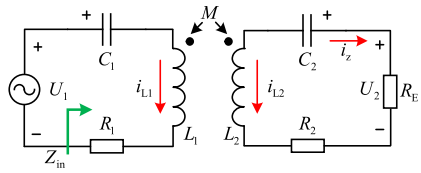


Fig. 1. Fundamental harmonic equivalent circuit of the SS-type WPTS.

Manuscript received January 26, 2019; revised April 18, 2019 and June 28, 2019; accepted August 8, 2019. Date of publication August 20, 2019; date of current version January 10, 2020. This work was supported in part by the Shaanxi Key Research & Development Plan under Grant 2018GY-043, in part by the Fundamental Research Funds for the Central Universities under Grant xjj2018186 and the Young Scientists Fund of the National Natural Science Foundation of China under Grant 51607141, and in part by the State Key Laboratory of Electrical Insulation and Power Equipment, Xi'an Jiaotong University. Recommended for publication by Associate Editor J. Acero. *(Corresponding authors: Yue Wang and Laili Wang.)*

The authors are with the State Key Laboratory of Electrical Insulation and Power Equipment, Xi'an Jiaotong University, Xi'an 710049, China (e-mail: jiangyongbin@stu.xjtu.edu.cn; llwang@mail.xjtu.edu.cn; yuewang@mail.xjtu.edu.cn; wm3117079009@stu.xjtu.edu.cn; zzx980318@stu.xjtu.edu.cn; liuyonghui@stu.xjtu.edu.cn; eliza999@stu.xjtu.edu.cn).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2019.2936708

Once R_{E} deviates from the optimal load, the transfer efficiency of the resonant network decreases tremendously. To deal with the problem, the active maximum efficiency point tracking (MEPT) method by using a dc–dc converter has been proposed to overcome the variation of the load resistance [8], [10], [11]. Although the dc–dc converter can solve the problem, an extra dc–dc converter must be added. Therefore, not only the system cost and power loss would increase, but the system power density would decrease. Recently, a novel phase-shift control method based on the active rectifier (AR) is proposed, which adjusts the phases of driver signals to change the ac equivalent impedance and achieve the maximum transfer efficiency [12]–[15]. Even though the zero-voltage switching (ZVS) operation of converters is not implemented, this control method is still meaningful and valuable in the WPTS for EV's charging, which can save a dc–dc converter and also achieve the maximum transfer efficiency simultaneously. However, a reliable phase-locked method is necessary to acquire the phase of the resonant current accurately, which is very difficult because of the high frequency and noises of the resonant current in high power applications.

Nowadays, many researchers devote themselves to the control of the AR. In [12], the resistive and reactive part of the equivalent load impedance of the AR can be controlled to optimize the transfer efficiency in the WPT. Similarly, a triple-phase-shift control strategy is proposed to achieve load matching while realizing ZVS [15]. However, the critical phase-locked method has not been presented for locking the resonant current in the secondary side. In [16], a direct phase control approach is proposed based on the second-order generalized integrator phase-locked loop (PLL). Unfortunately, due to the limit of the processor speed, this method is only applicable in several kilohertz, which is far below the common resonant frequency in the WPT. Commonly, to obtain the phase of the high-frequency resonant current, a traditional zero-crossing detection (ZCD) method is often applied to detect the zero-crossing point of the resonant current that can be used to synchronize and produce the driver signals [13], [17]–[19]. However, this traditional ZCD method is sensitive to noise disturbance and cannot be applied in high power applications directly. Recently, DSP controllers are relatively cheap and widely used in the wireless high power transfer with hundreds of kilohertz [14], [20]. Therefore, it is promising to develop an accurate and reliable method for locking the phase of the high-frequency resonant current based on the DSP controller in wireless high power transfer. In [14], based on the ZCD, a synchronization method between the driver signals and the secondary resonant current is proposed in the AR. In this method, the zero-crossing signal in the wireless high power transfer should be carefully processed to reduce its noises as much as possible. However, it is using the zero-crossing signal directly for synchronizing driver pulses that leads to lose driver pulses, which makes the system unstable. Take the topology of the main circuit in Fig. 3 as an example. When the inverter operates with the phase shift angle 180° and the AR operates in the synchronous rectification mode, the normal operating waveforms without pulse losing are shown in Fig. 2(a). Once the pulse losing happens, the maximum values of the resonant current and resonant voltage of coils and capacitors will

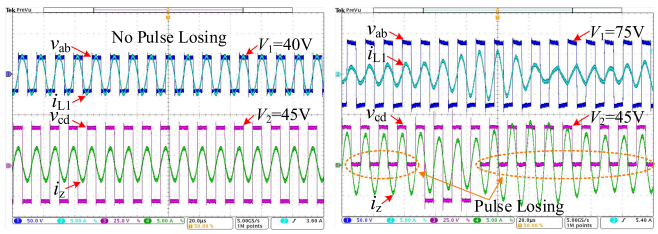


Fig. 2. Comparison of operating waveforms in different situations with constant output voltage $V_2 = 45$ V. (a) No pulse losing with $V_1 = 40$ V. (b) Pulse losing with $V_1 = 75$ V.

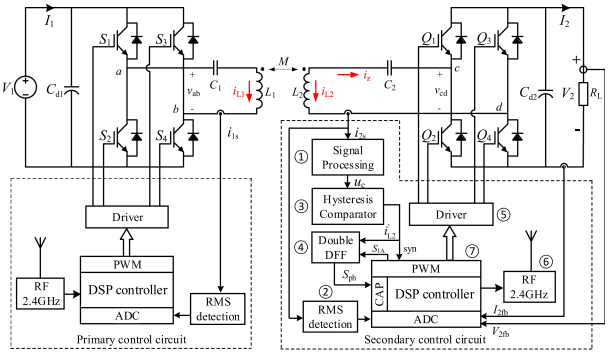


Fig. 3. Proposed system architecture for EV's battery charging.

increase tremendously to maintain the constant output voltage and constant output power, which might cause damage to the safe operation of the system. In a word, an accurate and reliable phase-locked method is vital for the impedance matching control of the AR and the safe operation of the WPTS.

To realize the impedance matching control of the AR more accurately and reliably by using the DSP controller, this article illustrates the essential reason why the driver pulses lose in the DSP controller and proposes the PLL combined with the chained trigger mode (PLL-CTM) that can lock the phase of the resonant current accurately and produce driver pulses reliably. With the proposed PLL-CTM applied, the reliability of the WPTS can be enhanced tremendously. This novel PLL-CTM is unique and prominent, which uses a variable reference signal produced by the pulse width modulation (PWM) module in the DSP controller and can be utilized to regulate the ac equivalent impedance of the AR. Based on the proposed PLL-CTM, this article also presents a double-side phase shift control (DPSC) strategy to achieve constant-current constant-voltage (CC/CV) charging for battery packs and minimize the power loss of the resonant network simultaneously. Finally, a 500-W WPT prototype is built to verify the feasibility of the DPSC with PLL-CTM. Benefiting from the DPSC with PLL-CTM, the WPTS not only obtains a high accuracy in steady state, but also achieves a good dynamic performance with the step change of R_{L} and R_{Eref}. The experiment results indicate that the maximum power loss rate of the resonant network can be limited to 2.47% with $k = 0.2$ and 3.39% with $k = 0.15$ in the whole charging process.

The rest of this article is organized as follows: Section II presents the proposed system architecture and operating principle of the series–series (SS) type WPTS. Section III gives

the relationship of control variables for realizing both CC/CV charging and impedance matching, and then, presents the DPSC strategy. Section IV reveals the basic reason why the driver pulses lose in the DSP controller. In Section V, based on the DSP controller, the PLL-CTM is proposed to lock the phase of the resonant current accurately and produce driver pulses reliably, which can avoid the driver pulse losing as much as possible. In Section VI, the experimental waveforms are shown to verify the feasibility of the DPSC with PLL-CTM. Finally, the conclusions are drawn in Section VII.

II. System Architecture

To achieve the CC/CV charging and impedance matching simultaneously in the whole charging process, a novel PLL with higher accuracy and reliability is proposed for the generation of driver signals in the AR. The whole system architecture is shown in Fig. 3 and illustrated in detail.

The topology of main circuits is composed of a high-frequency full-bridge inverter, an SS-type resonant network and a high-frequency full-bridge rectifier. The full-bridge inverter contains four switches ($S_1 \sim S_4$), which operates in complementary mode and converts a dc voltage V_1 into a high-frequency ac voltage $v_{\rm ab}$. The primary coil L_1 and its resonant capacitor C_1 are in series and stimulated by $v_{\rm ab}$, and the high-frequency alternating magnetic field is generated by L_1 consequently. According to the law of electromagnetic induction, a voltage is induced in the secondary side coil L_2, and powers the load $R_{\rm L}$ with the output dc voltage V_2 through a serial-resonant capacitor C_2 and the full-bridge rectifier.

The designed system control circuits can be divided into two parts, the primary control circuit and the secondary one. The secondary control circuit needs to produce required driver signals accurately and reliably according to the phase of $i_{\rm L2}$. Moreover, the secondary controller samples charging signals and sends them to the primary one by RF 2.4 GHz. The primary controller adjusts the charging current/voltage by changing the phase shift angle of the primary inverter. In this article, the secondary control circuits are the core of the whole system and contain seven blocks (①–⑦).

As shown in Fig. 3, $i_{\rm 2s}$ is the current transformer (CT) output signal of the secondary resonant current $i_{\rm L2}$. Then, $i_{\rm 2s}$ can be converted to a dc voltage by the accurate rms detection circuit (block ②). Meanwhile, a signal processing circuit (block ①) is adopted to acquire the phase of $i_{\rm L2}$ by converting a current signal to a voltage signal and adding a dc bias. Next, to restrain the resonant current zero-crossing noise produced by the high transfer power and hard switching mode of MOSFETs, a hysteresis comparator (block ③) is adopted to convert the voltage signal $u_{\rm c}$ to the square waveform $i'_{\rm L2}$. This square waveform $i'_{\rm L2}$ is input into the DSP controller as the synchronization signal of the PWM1 module. At this time, the DSP controller (block ⑦) produces a reference signal $S_{\rm 1A}$ by using the PWM1 module. According to the rising edges of $S_{\rm 1A}$ and $i'_{\rm L2}$, the phase signal $S_{\rm ph}$ is generated by the double D flip-flops (DFF) (block ④). Next, the DSP controller samples $S_{\rm ph}$ by using the CAP module and adjusts the phase of $S_{\rm 1A}$ continuously. Finally, based on the phase of $S_{\rm 1A}$, the driver signals of $Q_1 \sim Q_4$ are produced accordingly. The control loop is implemented with analogue circuits and digital processors at the same time. Consequently, the flexibility of the digital control and the rapidity of analogue circuits can be achieved simultaneously.

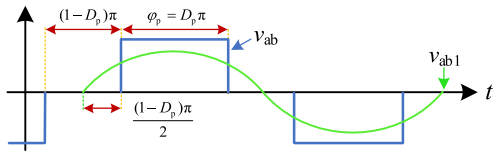


Fig. 4. Operating waveforms of the primary inverter.

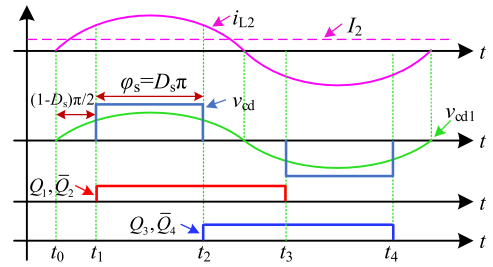


Fig. 5. Operating waveforms of the AR with zero reactive power.

III. Basic Theory Analysis

A. Equivalent Circuit Analysis

In the analysis of an SS-type WPTS in Fig. 3, the fundamental harmonic model is normally used [8], [10], [21], which is depicted in Fig. 1. U_1 and U_2 represent the fundamental components of $v_{\rm ab}$ and $v_{\rm cd}$, respectively. $I_{\rm L1}$ and $I_{\rm L2}$ represent the rms values of primary and secondary resonant currents, respectively. L_1 and L_2 are the self-inductances of primary and secondary sides, respectively. M is the mutual inductance and the coupling coefficient k of coupled inductors satisfies $k = M/\sqrt{L_1 L_2}$. $R_{\rm E}$ is the ac equivalent resistor of the high-frequency rectifier.

As shown in Fig. 3, the SS resonant tank is driven by a high-frequency full-bridge inverter that adopts the phase shift control with the fixed frequency. The operating waveforms of the inverter are shown in Fig. 4. When the phase shift angle is defined as $\varphi_{\rm p}$, which is proportional to the duty cycle $D_{\rm p}$ ($\varphi_{\rm p} = D_{\rm p}\pi$, $0 < D_{\rm p} < 1$), U_1 can be calculated by

$$U_1 = \frac{2\sqrt{2}}{\pi} V_1 \sin\left[\frac{D_{\rm p}\pi}{2}\right]. \tag{2}$$

B. Equivalent Impedance Analysis

When the phase shift control is applied in the AR with zero reactive power, the operating waveforms of the AR are shown in Fig. 5. $i_{\rm L2}$ is the secondary inductor current and U_2 is the fundamental component of $v_{\rm cd}$ with the phase shift angle $\varphi_{\rm s}$ ($\varphi_{\rm s} = D_{\rm s}\pi$, $0 < D_{\rm s} < 1$), which can be obtained by

$$U_2 = \frac{2\sqrt{2}}{\pi} V_2 \sin\left[\frac{D_{\rm s}\pi}{2}\right]. \tag{3}$$

TABLE I
SYSTEM PARAMETERS USED IN CALCULATION

Symbol	Quantity	Value
L_1 , L_2	Resonant inductances	116.86 μH
C_1 , C_2	Resonant capacitances	30 nF
k	Coupling coefficient	0.2
ω_0	Resonant angular frequency	5.34×10^5 rad/s
f_0	Resonant frequency	85 kHz
R_L	Load resistance	10 Ω

According to the operating waveforms of the AR in Fig. 5, i_{L2} charges the load only in the time duration t_1–t_2 and t_3–t_4 in one period. Then, the average current I_2 can be calculated by

$$I_2 = \frac{1}{T_s}\left(\int_{t_1}^{t_2} i_{L2}(t)dt + \int_{t_3}^{t_4} -i_{L2}(t)dt\right). \tag{4}$$

When i_{L2} and u_2 are in phase, I_2 can be obtained by

$$I_2 = \frac{2\sqrt{2}I_{L2}}{\pi}\sin\left[\frac{D_s\pi}{2}\right]. \tag{5}$$

Therefore, according to (3) and (5), the relationship between R_E and R_L can be obtained by

$$R_E = \frac{8}{\pi^2}\left(\sin\left[\frac{D_s\pi}{2}\right]\right)^2 R_L. \tag{6}$$

According to (6), R_E can be regulated by D_s.

C. System Characteristics

According to the relevant analysis in [8], in order to maximize the transfer efficiency of the resonant network, the SS-type WPTS should satisfy the preconditions, which are

$$\omega_s = \omega_0 = \frac{1}{\sqrt{L_1C_1}} = \frac{1}{\sqrt{L_2C_2}}. \tag{7}$$

Based on the aforementioned equation, the transconductance gain and the voltage gain of the WPTS are analyzed as follows.

1) Transconductance Gain of the System (TCGS): According to Fig. 1, under the frequency conditions (7), the transconductance gain of the resonant network can be obtained by

$$G_{iv} = \frac{I_{L2}}{U_1} = \frac{1}{\omega_0 k\sqrt{L_1L_2}}. \tag{8}$$

Substituting (2) and (5) into (8), the TCGS can be obtained by

$$G_{ivsys} = \frac{I_2}{V_1} = \frac{8\sin\left[\frac{D_p\pi}{2}\right]\sin\left[\frac{D_s\pi}{2}\right]}{\pi^2\omega_0 k\sqrt{L_1L_2}}. \tag{9}$$

According to (9), G_{ivsys} is independent of R_L. With the parameters listed in Table I, TCGS as a function of D_p and D_p under different k is plotted in Fig. 6(a). As k increases, the maximum value of G_{ivsys} gradually decreases. Nevertheless, if k is fixed, G_{ivsys} is the monotonic increasing function of both D_p and D_s.

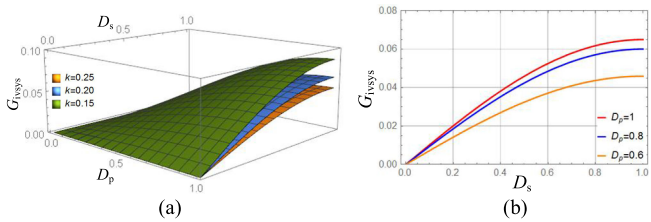


Fig. 6. Characteristics of the TCGS. (a) G_{ivsys} versus D_p and D_s with different k. (b) G_{ivsys} versus D_s with different D_p and k= 0.2.

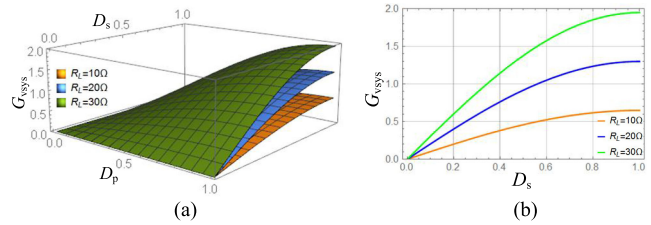


Fig. 7. Characteristics of the VGS. (a) G_{vsys} versus D_p and D_s with different R_L. (b) G_{vsys} versus D_s with different R_L and $D_p = 1$.

2) Voltage Gain of the System (VGS): According to (9), the VGS can be obtained by

$$G_{vsys} = \frac{V_2}{V_1} = \frac{8R_L\sin\left[\frac{D_p\pi}{2}\right]\sin\left[\frac{D_s\pi}{2}\right]}{\pi^2\omega_0 k\sqrt{L_1L_2}}. \tag{10}$$

With the parameters listed in Table I, the VGS as a function of D_p and D_s under different R_L is plotted in Fig. 7(a). Likewise, the VGS is also a monotonic increasing function of D_p and D_s. Generally speaking, when G_{ivsys} or G_{vsys} is fixed, there are lots of combinations between D_p and D_s that can achieve CC/CV charging. However, there are only parts of them that can also minimize the power loss of the resonant network in the whole charging process.

D. Efficiency Optimization of Resonant Network

In steady state, the efficiency of the resonant network η_{res} is determined by the ESRs of the resonant network. According to [8], η_{res} can be maximized if R_E matches its optimum value R_{Eopt} in (1). However, as the charging process goes, the equivalent load resistor R_L gradually increases [6], [22], which leads to the change of R_E correspondingly. To maximize the transfer efficiency of the resonant network in the whole charging process, R_E should be adjusted in real time to match the optimal value R_{Eopt}. Therefore, according to (1) and (6), we make

$$R_E = \frac{8}{\pi^2}\left(\sin\left[\frac{D_s\pi}{2}\right]\right)^2 R_L = R_{Eopt}. \tag{11}$$

Then, D_s can be calculated by

$$D_s = \frac{1}{\pi}\arccos\left[1 - \frac{\pi^2 R_{Eopt}}{4R_L}\right] \tag{12}$$

where R_L should satisfy

$$R_L > \pi^2 R_{Eopt}/8. \tag{13}$$

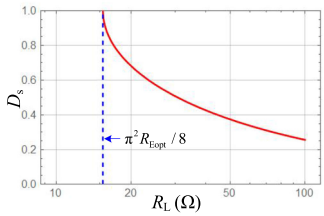


Fig. 8. Relationship between D_s and R_L when the impedance matching is achieved with zero reactive power.

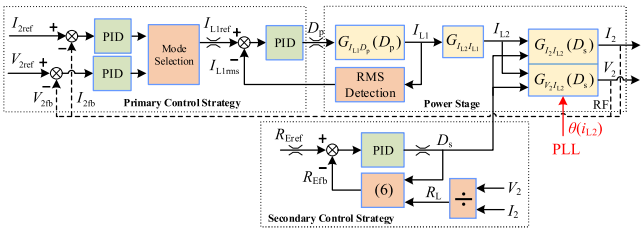


Fig. 9. Control diagram of the WPTS.

If R_L is smaller than $\pi^2 R_{Eopt}/8$, the AR needs to operate as a synchronous rectifier in order to reduce the power loss of the AR. Assuming R_1 and R_2 as 0.5 Ω, D_s versus R_L is plotted in Fig. 8. In summary, when R_L satisfies (13), D_s should satisfy (12) approximately to minimize the power loss of the resonant network.

E. Double-Side Phase Shift Control (DPSC)

In this article, there are two control aims: CC/CV charging for battery packs and the impedance matching to minimize the power loss of resonant network in the whole charging process. In order to achieve these two goals, a DPSC with PLL-CTM is proposed and depicted in Fig. 9.

In the secondary side, R_L changes continuously as the charging process goes. The secondary DSP controller samples the output voltage/current and calculates the ac equivalent resistance R_{Efb} based on (6). R_{Eref} is the instruction of the optimal equivalent resistor. Based on R_{Eref} and R_{Efb}, the secondary processor calculates D_s through the proportional-integral differential (PID) algorithm. However, according to Fig. 5, the successful generation of driver pulses depends on locking the phase of i_{L2} accurately and reliably, which will be presented in next section.

In the primary side, the control strategy contains two closed loops: the inner current loop of I_{L1} and the output current/voltage loop. The aim of the inner current loop of I_{L1} is to improve the systematic dynamic response of the WPTS and restrict the amplitude of i_{L1} to a safe region. Meanwhile, in the output current/voltage loop, the processor of secondary rectifier samples the charging current/voltage and sends them to the primary controller through radio frequency (RF) communication. Based on I_{2ref}, V_{2ref} and I_{2fb}, V_{2fb}, the processor of the primary inverter calculates the instructions of the inner current loop through the PID algorithm.

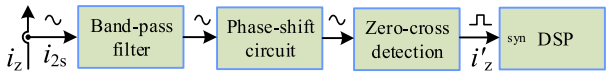


Fig. 10. Traditional method for synchronizing driver signals [14].

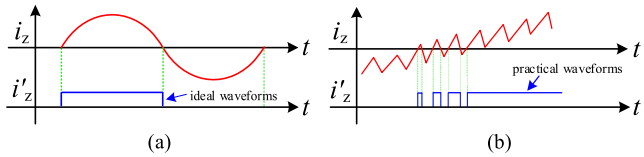


Fig. 11. Generation of the synchronization signal by using a ZCD circuit. (a) Ideal output waveform of comparator. (b) Amplified scope of the positive zero-crossing point of i_z in practical applications.

Similar to the traditional control method in the AR, the proposed DPSC also depends on the accurate and reliable phase locking of i_{L2}. However, the traditional phase-locked method based on the DSP controller tends to lose driver pulses due to the dither of the synchronization pulse. Next, we will illustrate the essential reason why the driver pulses lose and propose a novel PLL that can lock the phase of i_{L2} accurately and reliably.

IV. Analysis of the Traditional Synchronization Method

As shown in Fig. 3, the active impedance matching depends on the accurate and reliable phase-locked method of the resonant current. However, the traditional phase synchronization method is extremely sensitive to noise disturbance and tends to lose driver pulses, which may cause damage to the safe operation of the system. In this section, the reason why the driver pulses lose will be revealed in detail.

A. Shortcomings of the Traditional Synchronization Method

In the control of the AR, it is necessary to achieve the synchronization between the driver signals of MOSFETs and the resonant current in the secondary side. Typically, the traditional method for generating the synchronization signal is shown in Fig. 10 [14]. i_{2s} is the CT output signal of i_z and passes through a bandpass filter. Then, a phase-shift circuit is adopted to correct the phase error caused by detection circuits and band-pass filter. After that, a ZCD circuit generates the square wave i'_z, which is in phase with i_z. Finally, i'_z is input into the synchronization input port of the DSP controller. However, this method by using i'_z to directly synchronize driver signals has some shortcomings.

First, the square wave i'_z is produced based on a ZCD circuit, which is extremely sensitive to noise interference especially in high power applications and hard switching mode of MOSFETs. As shown in Fig. 11(a), there is only one rising edge of i'_z in the ideal case near the positive zero-crossing point of i_z. However, as shown in Fig. 11(b), in practical applications, the sinusoidal waveform contains noises inevitably that make i'_z produce a series of rising edges near the positive zero-crossing point of i_z. Therefore, the redundant pulses near the zero-crossing

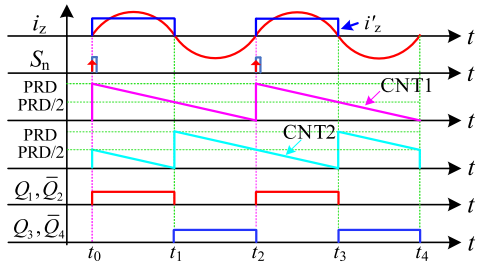


Fig. 12. Pulse generation mechanism based on the synchronization signal in the ideal case with no frequency dither.

point would fail to synchronize driver pulses, which is fatal for the system reliability.

Second, a bandpass filter and a phase-shift circuit are adopted to filter some noises and correct the phase error, respectively. However, the bandpass filter and the phase-shift circuit are sensitive to frequency variations, which tends to increase the detection error of the current phase. Consequently, it may lead to the failure of phase locking.

Third, the traditional method also tends to lose driver pulses, which is fatal for the safe operation of the system. The ideal case is shown in Fig. 12. i_z is the resonant current in the secondary side and i'_z is the corresponding zero-crossing square waveform. Take the synchronous rectification mode as an example, a typical generation mechanism of driver pulses is also depicted in Fig. 12. Here, PWM1 and PWM2 modules are used and their counters work in the down-count mode. When CNT1 counts to 0 naturally, Q_1 is forced to output 1 and Q_2 is forced to output 0. Meanwhile, when the counter counts to half of the period (PRD/2) naturally, Q_2 is forced to 1 and Q_1 is forced to output 0. The pulse generation mechanism of Q_3 and Q_4 is the same as Q_1 and Q_2, respectively. The only difference between them is the initial phase of the counter. When the rising edge of i'_z arrives, a synchronization pulse S_n is generated, which means the current values of CNT1 and CNT2 are updated immediately. In the synchronous rectification mode, CNT1 is updated as 0 and CNT2 is updated as PRD/2. If the initial values of the counters maintain constant and i_z has no frequency dither, CNT1 would count to 0 and CNT2 would count to PRD/2 naturally just before the rising edge of i'_z arrives. Therefore, the pulses would generate as we expect. However, that is so far from the truth in practice.

In practical applications, the initial values of the counters also change in real time due to the calculation in the DSP controller. Meanwhile, the position of the rising edge of i'_z also changes in real time. In that case, it is highly possible that the dither of i'_z will cause pulse losing. The phenomenon of "pulse losing" might happen in the leading leg (Q_1 and Q_2) or lagging leg (Q_3 and Q_4), respectively. Next, we will analyze the basic reason why these two legs lose pulses in detail.

1) Pulse Losing in the Leading Leg: As shown in Fig. 13(a), the square wave i'_z is in phase with the resonant current i_z and the rising edge of i'_z is represented as S_n. At t_0, the rising edge of i'_z arrives and S_n occurs. At this moment, CNT1 is initiated as 0. If the next rising edge of i'_z arrives at t_2 exactly, the pulses Q_1 and Q_2 are generated as Fig. 12. In practice, the next rising

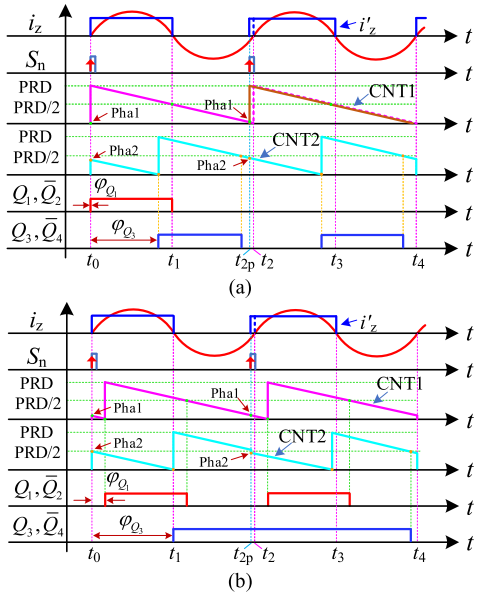


Fig. 13. "Pulse Losing" phenomenon by directly using the synchronization signal i'_z with frequency dither (a) in the leading leg (Q_1 and Q_2) when Pha1 is set near 0 or PRD ($\varphi_{Q1} \approx 0°$), and (b) in the lagging leg (Q_3 and Q_4) when Pha2 is set near PRD/2 ($\varphi_{Q3} \approx 180°$).

edge of i'_z may arrive at t_{2p} and S_n occurs at t_{2p} immediately. When CNT1 is initiated as a value close to but larger than 0 at t_{2p}, it is highly possible that the PWM1 module will lack a compare event, which results in a continuing low level of Q_1 and a continuing high level of Q_2. This phenomenon is called "Pulse Losing". Consequently, it will give rise to the oscillation of the WPTS and cause damage to the safe operation of the whole system. Generally speaking, if the initial value of CNT1 is near 0 or PRD at the moment when S_n occurs, which means that the phase of Q_1, φ_{Q1}, approaches $0°$, it is highly possible to lose driver pulses of Q_1 and Q_2.

2) Pulse Losing in the Lagging Leg: Similarly, as shown in Fig. 13(b), the square wave i'_z is also in phase with the resonant current i_z. At t_0, the rising edge of i'_z arrives and S_n occurs. At this moment, CNT2 is initiated as PRD/2. If the next rising edge of i'_z arrives at t_2 exactly, the pulses of Q_3 and Q_4 are generated as Fig. 12. In practice, the next rising edge of i'_z may arrive at t_{2p} and S_n occurs at t_{2p} immediately. When CNT2 is initiated as the value close to but smaller than PRD/2 at t_{2p}, it is highly possible that the PWM2 module will lack a compare event, which results in a continuing high level of Q_3 and a continuing low level of Q_4. Likewise, it will give rise to the oscillation of the WPTS and cause damage to the safe operation of the whole system. Generally speaking, if the initial value of CNT2 is near PRD/2 at the moment when S_n occurs, which means that the phase of Q_3, φ_{Q3}, approaches $180°$, it is highly possible to lose driver pulses Q_3 and Q_4.

B. Simulation Results

To verify "Pulse Losing" phenomenon and clearly illustrate the reason why the driver pulses ($Q_1 \sim Q_4$) lose in the control of the AR, a simulation model based on MATLAB is built. The

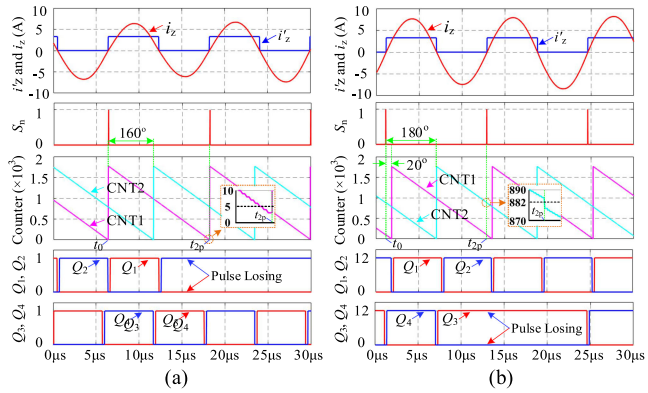


Fig. 14. Simulation results of the driver pulse generation based on the traditional phase synchronization method with frequency dither. (a) Pulse losing in the leading leg (Q_1 and Q_2). (b) Pulse losing in the lagging leg (Q_3 and Q_4).

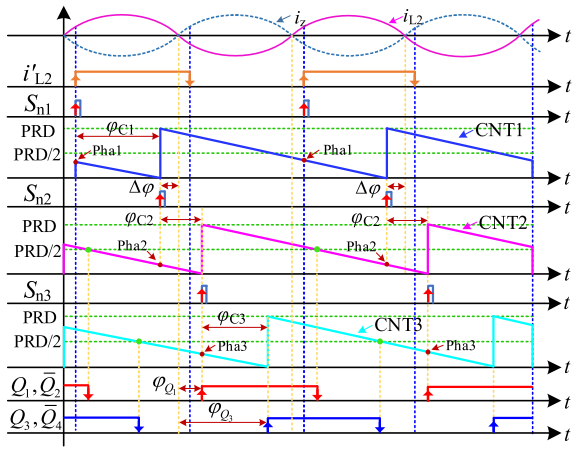


Fig. 15. Generation process of driver pulses based on the CTM.

parameters of the WPTS are set based on Table I and the input voltage V_1 is set to 80 V. The operating frequency is set to 85 kHz and PRD equals 1764. The operating waveforms with the driver pulse losing of Q_1 and Q_2 are shown in Fig. 14(a). At t_0, the initial value of CNT1 is near 0 (0°) and the initial value of CNT2 is near 784 (160°). At this moment, Q_1 is set to 1 and Q_2 is set to 0. However, the position of the next synchronization pulse S_n occurs in advance at $t_{2\mathrm{p}}$ and the current value of CNT1 that is close to but larger than 0, is updated as 1764 immediately. Therefore, the PWM1 module tends to miss a compare event and lose driver pulses Q_1 and Q_2, which is in accordance with the previous analysis.

Similarly, in Fig. 14(b), at t_0, the initial value of CNT1 is near 98(20°) and the initial value of CNT2 is near 882 (180°). At this moment, Q_3 is set to 0 and Q_4 is set to 1. However, the position of the next synchronization pulse S_n occurs in advance at $t_{2\mathrm{p}}$ and the current value of CNT2 that is close to but larger than 882 (PRD/2), is updated as 879 immediately. Therefore, the PWM2 module misses a compare event and loses driver pulses Q_3 and Q_4, which is also in accordance with the previous analysis.

V. Design of PLL-CTM

To overcome the mentioned disadvantages of the traditional phase synchronization method in Section IV, a novel PLL-CTM based on the DSP controller is proposed to produce driver pulses accurately and reliably in wireless high power transfer. The detailed operating principle is presented as follows.

A. Operating Principle of the Proposed PLL-CTM

1) Generation of Driver Pulses Based on the CTM: To illustrate the proposed PLL-CTM more clearly, the generation process of driver pulses based on the CTM will be presented first. Since the operating frequency may reach up to 100 kHz, the zero-crossing comparative method is commonly used [23]. As shown in Fig. 15, to suppress the noises and interference of the zero-crossing point of i_{L2}, a hysteresis comparator is adopted and the corresponding output signal is i'_{L2}. The counters of PWM1-3 modules take the down-count mode. The synchronization signal S_{n1} is used to represent the rising edge of i'_{L2} to initiate the phase of CNT1. Once CNT1 equals zero, a synchronization signal S_{n2} is produced, which is used to initiate the phase of CNT2. Similarly, once CNT2 equals zero, a synchronization signal S_{n3} is produced, which is used to initiate the phase of CNT3. The initial values of counters in PWM1-3 are represented as Pha1-3, respectively. Taking the moments of $S_{\mathrm{n1-3}}$ as datum points, the phases of counters in PWM1-3 can also be represented as $\varphi_{\mathrm{C1-3}}$, respectively. The driver signals Q_1 and Q_2 can be generated based on CNT2. Similarly, the driver signals Q_3 and Q_4 can be generated based on CNT3. The approach to generating driver pulses is called the CTM.

As shown in Figs. 5 and 15, if the synchronization signal S_{n2} can be accurately controlled at the left side of the positive zero-crossing point of i_z, the phases of CNT2 and CNT3 can be easily obtained by

$$\begin{cases} \varphi_{\mathrm{C2}} = (1 - D_\mathrm{s})\pi/2 + \Delta\varphi \\ \varphi_{\mathrm{C3}} = D_\mathrm{s}\pi \end{cases} \tag{14}$$

where the phase angle $\Delta\varphi$ is defined as the phase difference between S_{n2} and the positive zero-crossing point of i_z. According to (14), the initial values of CNT2 and CNT3 can be obtained, and thus, the impedance matching of the AR can be easily achieved with zero reactive power.

A significant advantage of driver-pulse generation based on the CTM is that the pulse losing can be avoided as much as possible by adjusting the phase of S_{n2} flexibly. The specific realization of the phase control of S_{n2} and the reasons why the pulse losing can be nearly avoided will be illustrated as follows.

2) Operating Principal of the PLL: As shown in Fig. 16, to observe and control the phase of S_{n2}, a reference signal S_{1A} is produced according to CNT1. When CNT1 equals 0, S_{1A} is forced to 1. When CNT1 equals PRD/2, S_{1A} is forced to 0. To detect the phase difference between S_{n1} and S_{n2}, the double DFF shown in Fig. 17 is adopted. The operating principle of the double DFF has been explained in [23]. Take i'_{L2} and S_{1A} as input signals, and then, the phase difference φ_{cap} can be obtained easily by using the CAP module in the DSP controller. As shown in Fig. 16, the phase difference $-\varphi_\mathrm{i}$ between the rising edge of

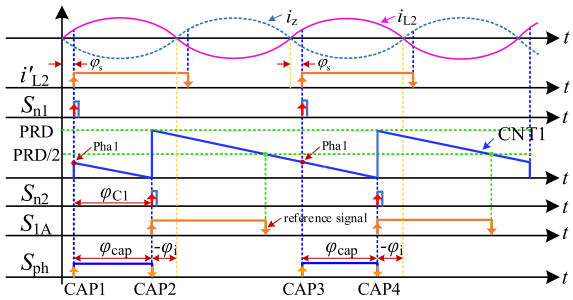


Fig. 16. Operating principal of the proposed PLL.

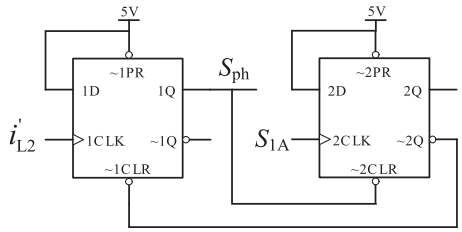


Fig. 17. Phase detection circuit with double DFF [23].

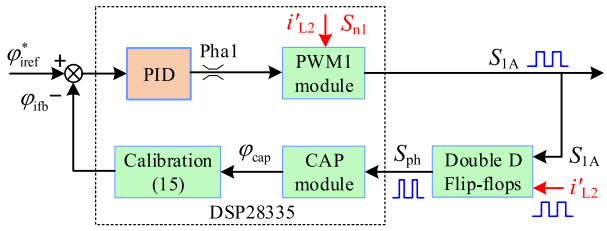


Fig. 18. Control diagram of the proposed PLL based on DSP28335.

S_{1A} and the positive zero-crossing point of i_z, can be calculated by

$$-\varphi_i = \pi - \varphi_s - \varphi_{cap} \tag{15}$$

where φ_s is the time-delay angle between the positive zero-crossing point of i_{L2} and the rising edge of i'_{L2}.

To control the phase of S_{n2}, which is at the moment of the rising edge of S_{1A}, a PLL based on DSP28335 is proposed and depicted in Fig. 18. First, the square wave i'_{L2} is used as the synchronization signal of PWM1 module in DSP28335. Second, DSP28335 produces a reference signal S_{1A} based on the PWM1 module. Then, the phase difference between i'_{L2} and S_{1A} can be detected by the double DFF. Third, DSP28335 captures the rising edge and falling edge of S_{ph} by using the CAP module and φ_{cap} can be obtained. Finally, through the calibration (15), the practical phase of S_{n2} can be acquired accurately. In Fig. 18, φ^*_{iref} is the reference signal of the phase of S_{n2} and φ_{ifb} is the corresponding feedback signal. Based on φ^*_{iref} and φ_{ifb}, the primary processor calculates the initial value of CNT1 through the PID algorithm. By adjusting the phase of CNT1, φ_{C1}, the synchronization signal S_{n2} can be controlled exactly.

3) Analysis of Avoiding "Pulse Losing": In order to explain the reason why the proposed PLL-CTM can nearly avoid the pulse losing in the impedance matching control of the AR, this section can be separated into the following three parts.

First, the reason why the reference signal S_{1A} in the PLL can be generated reliably is illustrated as follows. As shown in Fig. 15, the rising edge of i'_{L2} always lags behind the negative zero-crossing point of i_z due to the characteristics of the hysteresis comparator. In practical applications, S_{n2} should be set at the left side of the positive zero-crossing point of i_z with a constant phase angle $\Delta\varphi$ (commonly, $\Delta\varphi > 0°$) in steady state. Therefore, φ_{C1} is always smaller than 180° and Pha1 is always less than PRD/2. It is the lag time delay angle of S_{n1} and a constant phase angle $\Delta\varphi$ that can avoid pulse losing of the reference signal S_{1A} successfully.

Second, the reason why the driver signals Q_1 and Q_2 in the PLL can be generated reliably is illustrated as follows. In the traditional method, the pulse losing is unavoidable due to the dither of i'_{L2}. The basic reason for pulse losing has been revealed in Section IV. However, with the PLL applied, an additional synchronization pulse S_{n2} can be generated to substitute i'_{L2} and synchronize the phase of Q_1 and Q_2. Benefiting from the low-pass filtering characteristics of the PLL, the dither of S_{n2} can be reduced, which is helpful to avoid the pulse losing of Q_1 and Q_2. Moreover, in the impedance matching control of the AR, the rising edge of Q_1 commonly lags behind the positive zero-crossing point of i_z. Take the extreme case as an example. The rising edge of CNT2 is near the positive zero-crossing point of i_z. It is by inserting the angle $\Delta\varphi$ that the initial value of CNT2 can be prevented from being near 0 or PRD, which can decrease the possibility of the pulse losing of Q_1 and Q_2 as much as possible. In practical applications, the electromagnetic interference is unavoidable, which will cause the dither of the rising edge of i'_{L2} and S_{n2} more or less. Here, $\Delta\varphi$ commonly is set in the range from 10° to 45°, where the larger $\Delta\varphi$ is, the stronger the antiinterference capability of the WPTS will be. Benefiting from adding $\Delta\varphi$, the likelihood of the pulse losing can be extremely decreased.

Third, the reason why the driver signals Q_3 and Q_4 in the PLL-CTM can be generated stably is illustrated as follows. According to the previous analysis of the CTM, when CNT2 equals 0, S_{n3} can be generated to initiate the phase of CNT3 and synchronize the phase of Q_3 and Q_4. Take the extreme case as an example. The rising edge of Q_3 is near the negative zero-crossing point of i_z. The traditional synchronization method is shown in Fig. 13(b). φ_{Q3} is defined as the phase difference between the positive zero-crossing point of i_z and the rising edge of Q_3. Based on the previous analysis of the basic reason for pulse losing, when the initial value approaches PRD/2 ($\varphi_{Q3} \approx 180°$), it is highly possible to loss driver pulses Q_3 and Q_4. However, according to Fig. 15, with the CTM applied, if φ_{Q3} approaches 180°, the corresponding phase conditions of CNT2 and CNT3 should satisfy

$$\varphi_{Q3} = (\varphi_{C2} - \Delta\varphi) + \varphi_{C3} \approx 180°. \tag{16}$$

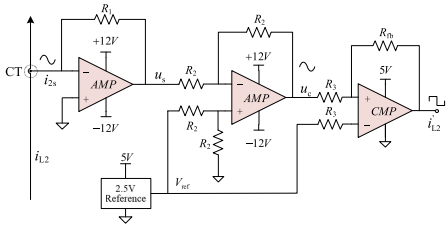


Fig. 19. Phase-detection circuit of i_{L2} [23].

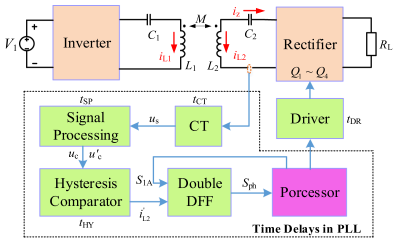


Fig. 20. Time-delay diagram in the whole system.

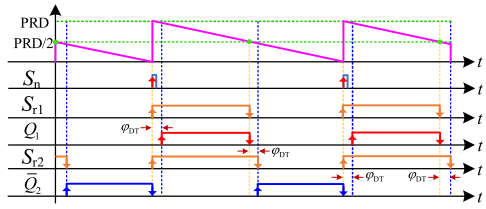


Fig. 21. Typical generation method of driver signals in consideration of the dead time.

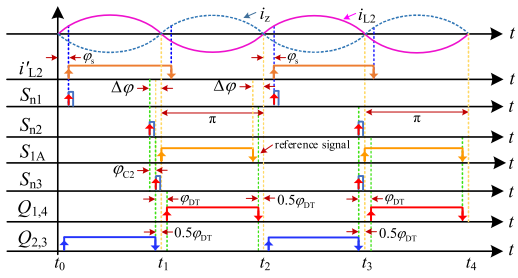


Fig. 22. Mechanism of the proposed synchronization method in practical applications.

In the impendence control of the AR, Q_1 always lags behind the positive zero-crossing point of i_z, so φ_{C2} is larger than $\Delta\varphi$, which makes it easier to prevent φ_{C3} from being close to 180° compared with the traditional method. Moreover, as shown in Fig. 15, Pha3 tends to be relatively smaller than PRD/2 compared with the traditional method. Consequently, the possibility of the pulse losing of Q_3 and Q_4 can be decreased as much as possible.

Above all, it is the reason why the proposed PLL-CTM that can significantly reduce the possibility of pulse losing in the impedance matching control of the AR.

B. Time-Delay Analysis in PLL

As shown in Figs. 3 and 18, the accurate phase control of S_{n2} depends on the calibration (15). Therefore, the time delays of the hardware design in the PLL should be analyzed in detail. The phase-detection circuit of i_{L2} is shown in Fig. 19. i_{2s} is the output current signal of the CT, which is converted to voltage signal u_s by R_1. u_s is regulated and u_c is proportional to u_s with a constant bias 2.5 V. Then, u_c is compared with reference voltage 2.5 V and the corresponding square wave i'_{L2} can be obtained by using a hysteresis comparator. As shown in Fig. 20, the time-delay angle φ_s from i_{L2} to i'_{L2} is similar to the previous analysis in [23]. Here, φ_s can be obtained by

$$\varphi_s = \varphi_{CT\_SP} + \varphi_{HY} \tag{17}$$

where φ_{CT_SP} is the time-delay angle of the current sampling and processing, which is defined as the phase difference between i_{L2} and u'_c (the ac component of u_c). φ_{HY} is the hysteresis time-delay angle that is defined as the phase difference between the positive zero-crossing point of u'_c and the rising edge of i'_{L2}. According to the analysis in [23], φ_{CT_SP} and φ_{HY} can be calculated by

$$\begin{cases} \varphi_{CT\_SP} = t_{CT\_SP} \times f_s \times 2\pi \\ \varphi_{HY} = \arcsin\left(\frac{N_I R_3 V_{ref}}{\sqrt{2} I_{L2} R_{fb}}\right) + t_{ac} \times f_s \times 2\pi \end{cases} \tag{18}$$

where N_I represents the rms ratio of i_{L2} and u'_c. According to (15), (17), and (18), φ_i can be evaluated accurately.

C. Control Loop Analysis in the PLL

In this article, a DPSC is adopted and its significant part is the accurate impedance matching control of the AR where the critical point is the accurate phase locking of i_{L2}. The previous analysis of the PLL-CTM ignores the practical dead-time angle of driver pulses φ_{DT} and the driver time-delay angle φ_{DR}. However, it is necessary to consider both the factors to improve the accuracy of phase locking in practical applications.

As shown in Fig. 21, in consideration of the dead time, the typical generation method of driver signals is different from the previous one in Fig. 12. The generation mechanism of S_{r1} is similar to Q_1 in Fig. 12. With the dead time considered, the rising edge of Q_1 lags behind S_{r1} with a dead-time delay angle φ_{DT}, while their falling edges are at the same moment. Meanwhile, the falling edge of S_{r2} lags behind S_{r1} with a dead-time delay angle φ_{DT}, while their rising edges are at the same moment. Then, Q_2 can be obtained since Q_2 and S_{r2} are complementary. It is noteworthy that the pulse generation mechanism of Q_3 and Q_4 is the same as Q_1 and Q_2, respectively.

Take the synchronous rectification mode as an example. When φ_{DR} is ignored firstly, the driver signals ($Q_1 \sim Q_4$) are depicted in Fig. 22. To realize the accurate impedance matching control of AR with zero reactive power, the zero-crossing point of i_z should stay at the midpoint of the dead time. Therefore, S_{n3} (the moment when CNT2 equals 0) should be ahead of the positive zero-crossing point of i_z with $\varphi_{DT}/2$. In order to observe and analyze the control performance of PLL easily, the reference signal S_{1A} should be produced in a specific way. Here, the mechanism to produce S_{1A} is the same as Q_1. According to Fig. 18, once φ^*_{iref} is set to 0°, the rising edge of S_{1A} will lock

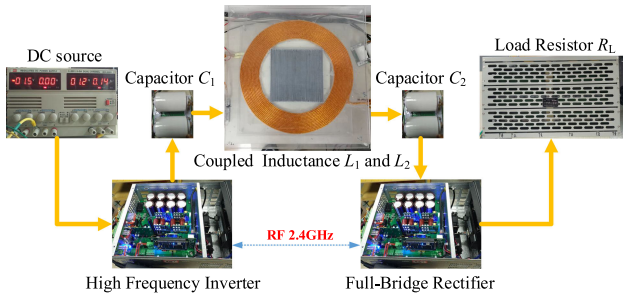


Fig. 23. Experimental prototype.

at the positive zero-crossing point of i_z. Therefore, as shown in Fig. 22, S_{n2} (the moment when CNT1 equals 0) must be ahead of the rising edge of $Q_{1,4}$ at least φ_{DT} to avoid pulse losing. Here, this phase is set to $1.5\varphi_{DT}$. Finally, in consideration of the dead time, the phases of CNT2 and CNT3, should be revised as

$$\begin{cases} \varphi_{C2} = (1 - D_s)\pi/2 + \Delta\varphi - \varphi_{DT}/2 \\ \varphi_{C3} = D_s\pi. \end{cases} \tag{19}$$

Since $0 < D_s < 1$, as long as $\Delta\varphi > \varphi_{DT}/2$, φ_{C2} must be larger than 0. According to the previous analysis, the pulse losing in the leading leg can be successfully avoided. The specific value of $\Delta\varphi$ needs to be adjusted based on different operating conditions in practical applications. In this article, in order to verify the proposed PLL-CTM and DPSC, $\Delta\varphi$ is set to φ_{DT}. When it comes to the lagging leg, the maximum value of D_s can be limited to prevent φ_{C3} from being close to PRD/2. Therefore, the pulse losing in the lagging leg can be successfully avoided.

Next, the driver time delay is considered. Commonly, for a given driver circuit, φ_{DR} is constant. Therefore, in order to achieve the impedance matching control of the AR with the zero reactive power accurately, the reference instruction φ^*_{iref} should be set to $-\varphi_{DR}$ to make S_{n2} moves left with φ_{DR}. Finally, v_{cd} can be controlled in phase with i_{L2} accurately.

VI. Experimental Verification

A. Experimental Prototype

To verify the feasibility of the DPSC with PLL-CTM, a 500-W experimental prototype is built up, which is shown in Fig. 23. The prototype includes a dc source, a high-frequency inverter, an SS-type resonant network, a full-bridge rectifier, and a sliding rheostat. Energy is transferred from a dc source to the sliding rheostat. The power devices used in the inverter and rectifier are MOSFETs (IXTQ96N20P). The detailed experimental parameters are listed in Table II.

B. Operating Waveforms of the Proposed PLL-CTM

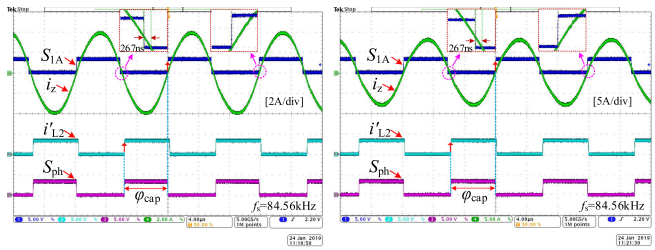
The dual positive edge triggered DFF with clear and preset, 74AC11074, is selected for the phase detection of two square wave pulses. i'_{L2} is used for setting to 1, and S_{1A} is used for resetting to 0. The output signal of the DFF is S_{ph}. Based on the analysis in Fig. 19, we set $R_3 = 1\,k\Omega$, $R_{fb} = 20\,k\Omega$, and $V_{ref} = 2.5$ V. With $V_{cc} = 5$ V and $V_{EE} = 0$ V, the half

TABLE II
Parameters of the WPTS

Symbol	Quantity	Value
L_1	Primary resonant inductor	118.43 μH
C_1	Primary resonant capacitor	29.92 nF
f_1	Primary resonant frequency	84.55 kHz
R_1	Primary ESR	0.12 Ω
L_2	Secondary resonant inductor	118.55 μH
C_2	Secondary resonant capacitor	29.88 nF
f_2	Secondary resonant frequency	84.56 kHz
R_2	Secondary ESR	0.11 Ω
N_1 , N_2	Number of turns	15
R_L	Load resistor	8–200 Ω
d	Face to face distance of coils	12.5 cm–15.8 cm
k	Coupling coefficient	0.15–0.2

TABLE III
Parameters of Time Delays

Symbol	Quantity	Value
t_{DR}	Driver delay	93 ns
t_{CT_SP}	Current sampling and signal processing Time delay	–10 ns
t_{DT}	Dead-time delay	266.7ns
t_{ac}	Action response time of comparator	35 ns
N_I	Current co-efficiency	4
V_{bW}	Hysteresis width	128.8 mV



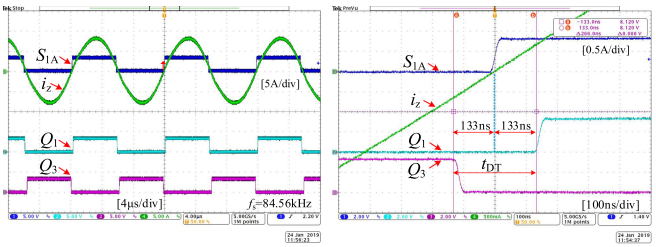
(a) (b)

Fig. 24. Operating waveforms of the proposed PLL-CTM with $R_L = 18\ \Omega$ and $k = 0.2$, when φ^*_{iref} is set to 0° and $\Delta\varphi$ is set to 8.1°. (a) $V_1 = 40$ V. (b) $V_1 = 80$ V.

hysteresis width can be calculated by $V_{up} = R_3V_{ref}/R_{fb} = 125$ mV theoretically. In terms of experimental measurement results, the relevant parameters are summarized in Table III.

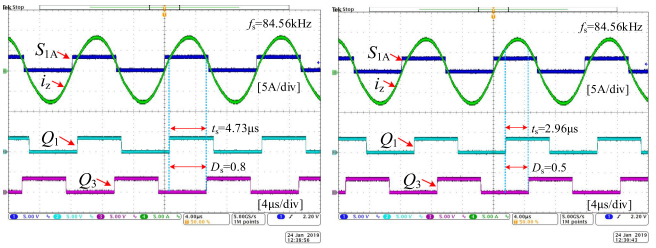
According to (17) and (18) and Table III, the hardware time-delay angle φ_s in the PLL can be evaluated in real time. Meanwhile, based on (15) and the CAP module in DSP28335, the feedback signal of the resonant current, φ_{ifb}, can be obtained. Consequently, the phase of the reference signal S_{1A} can be controlled accurately.

According to the previous analysis in Fig. 22, the rising edge of S_{1A} is located at the positive zero-crossing point of i_z and the falling edge of S_{1A} leads the negative zero-crossing point of i_z with t_{DT}. When V_1 is set to 40 and 80 V, respectively, the corresponding operating waveforms of the proposed PLL-CTM are shown in Fig. 24. When V_1 changes, the rms of i_{L2} will change and the time-delay angle φ_{HY} will also change. With the calibration (15), the rising edge of the reference signal S_{1A} will always track the positive zero-crossing point of i_z and the falling edge of S_{1A} leads the negative zero-crossing point of i_z with 267 ns (about t_{DT}).



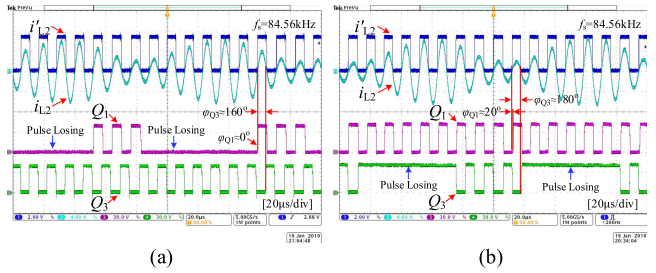
(a) (b)

Fig. 25. Operating waveforms of the driver signal, with $R_L = 18\,\Omega$, $k = 0.2$, and $V_1 = 80$ V, when φ^*_{iref} is set to 0° and $\Delta\varphi$ is set to 8.1° (a) in the long time scale and (b) in the short time scale.



(a) (b)

Fig. 26. Operating waveforms of the driver signal by using DPSC with PLL-CTM, with $R_L = 18\,\Omega$, $k = 0.2$, and $V_1 = 80$ V, when φ^*_{iref} is set to 0° and $\Delta\varphi$ is set to 8.1°. (a) $D_s = 0.8$. (b) $D_s = 0.5$.



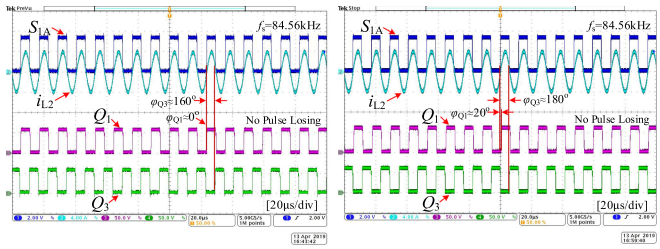
(a) (b)

Fig. 27. Pulse losing in the control of the AR with the traditional phase synchronization method, when $f_s = 84.56$ kHz (PRD = 1774), $R_L = 18\,\Omega$, $k = 0.2$, and $V_1 = 40$ V. (a) Pulse losing in the leading legs Q_1 and Q_2, with CNT1 near 0 ($\varphi_{Q1} \approx 0°$) and CNT2 set to 788 ($\varphi_{Q3} \approx 160°$). (b) Pulse losing in the lagging legs Q_3 and Q_4, with CNT1 set to 99 ($\varphi_{Q1} \approx 20°$) and CNT2 near 887 (PRD/2, $\varphi_{Q3} \approx 180°$).

Take the synchronous rectification as an example. Benefiting from the proposed PLL-CTM, the driver signals Q_1 and Q_3 can be generated in Fig. 25(a). The amplification map of Fig. 25(a) is shown in Fig. 25(b). In Fig. 25(b), the positive zero-crossing point of i_z is exactly at the middle point of the dead band, which is set to 266.7 ns. When the duty cycle D_s of the rectifier is changed, the corresponding operating waveforms are shown in Fig. 26. It can be seen that the driver signals can be controlled exactly with different D_s.

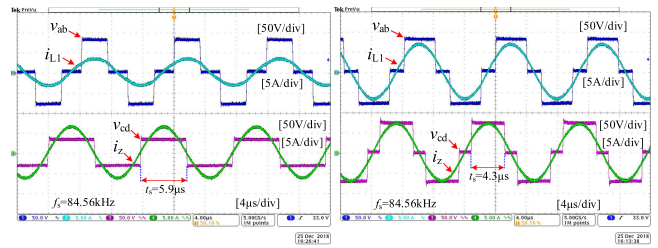
C. Verification and Solving of "Pulse Losing"

The measurement results with the traditional phase synchronization method are shown in Fig. 27. According to the traditional method in [14], the output signal of comparator i'_{L2} is used for the synchronization directly. According to the previous analysis, if the initial values of CNT1 and CNT2 are near 0 or PRD/2, it is highly possible to lose driver pulses. As shown in Fig. 27(a), the pulse losing of Q_1 and Q_2 does occur when the initial value of CNT1 is close to 0 ($\varphi_{Q1} \approx 0°$). In Fig. 27(b), the pulse losing of Q_3 and Q_4 does occur when the initial value of CNT2 is close to PRD/2 ($\varphi_{Q3} \approx 180°$). Therefore, the experimental results verify the previous analysis.



(a) (b)

Fig. 28. No pulse losing in the control of the AR with the proposed PLL-CTM, when $f_s = 84.56$ kHz (PRD = 1774), $R_L = 18\,\Omega$, $k = 0.2$, and $V_1 = 40$ V. (a) No pulse losing in the leading legs Q_1 and Q_2, when $\varphi_{Q1} \approx 0°$ and $\varphi_{Q3} \approx 160°$. (b) No pulse losing in the lagging legs Q_3 and Q_4, when $\varphi_{Q1} \approx 20°$ and $\varphi_{Q3} \approx 180°$.



(a) (b)

Fig. 29. Operating waveforms when both the ac impedance matching and CC charging are achieved at the same time by using the DPSC with PLL-CTM, with $k = 0.2$, $V_1 = 80$ V, $I_2 = 4$ A, and $\varphi^*_{iref} = -2.83°$ ($-\varphi_{DR}$). (a) $R_L = 8\,\Omega$. (b) $R_L = 18\,\Omega$.

In Fig. 28, with the proposed PLL-CTM applied in the AR, the phenomenon of "Pulse Losing" disappears, even when $\varphi_{Q1} \approx 0°$ and $\varphi_{Q3} \approx 180°$. Meanwhile, the resonant current operates reliably without any oscillation. Therefore, by using the proposed method, the "Pulse Losing" can be avoided, thus preventing the system from being damaged by oscillation.

D. Operating Waveforms of the DPSC With PLL-CTM

1) Steady-State Experimental Results: To verify the effectiveness of the proposed DPSC with PLL-CTM, the steady-state operation of the WPTS is investigated. In consideration of the driver time delay, φ^*_{iref} should be set to $-2.83°$ ($-\varphi_{DR}$). In the whole charging process, the instruction of R_E, R_{Eref}, is set to 12.05 Ω with $k = 0.2$ in the impedance matching control of the AR. In the CC mode, I_2 maintains 4 A and R_L is set to 8 and 18 Ω, respectively. When $R_L = 8\,\Omega$, the AR needs to operate as a synchronous rectifier because (13) cannot be satisfied. When $R_L = 18\,\Omega$, the AR operates in the impedance matching mode with $R_E = 12.05\,\Omega$, while the primary inverter maintains 4 A. The steady-state operating waveforms in the CC mode are shown in Fig. 29. Similarly, when the battery packs are in the CV mode, V_2 maintains 72 V and R_L is set to 20 and 40 Ω, respectively. The steady-state operating waveforms in the CV mode are shown in Fig. 30. Based on Figs. 29 and 30, the AR can be controlled with

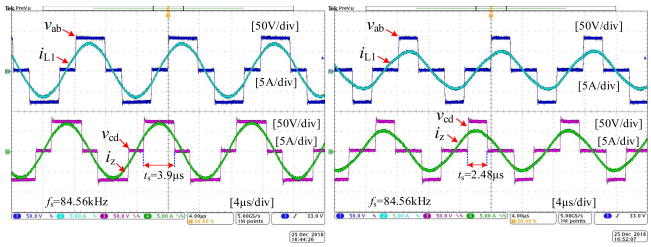


Fig. 30. Operating waveforms when both the ac impedance matching and CV charging are achieved at the same time by using the DPSC with PLL-CTM, with $k = 0.2$, $V_1 = 80$ V, $V_2 = 72$ V, and $\varphi^*_{\rm iref} = -2.83^\circ$ $(-\varphi_{\rm DR})$. (a) $R_{\rm L} = 20\ \Omega$. (b) $R_{\rm L} = 40\ \Omega$.

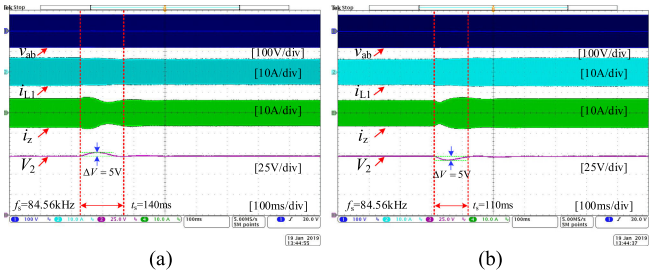


Fig. 31. Dynamic waveforms with the step change of $R_{\rm L}$, when both the ac impedance matching and CV charging are achieved at the same time with $k = 0.2$, $V_1 = 80$ V, $V_2 = 72$ V, $\varphi^*_{\rm iref} = -2.83^\circ$ $(-\varphi_{\rm DR})$, and $R_{\rm Eref} = 12.05\ \Omega$. (a) Changing $R_{\rm L}$ from 18 to 23 Ω suddenly. (b) Changing $R_{\rm L}$ from 23 to 18 Ω suddenly.

approximately zero reactive power and $R_{\rm E}$ can also be controlled as 12.05 Ω when (13) is satisfied, which proves that the WPTS can obtain a high accuracy in the impedance matching control of the AR by using the DPSC with PLL-CTM.

2) Dynamic Performance With the Step Change of $R_{\rm L}$ and $R_{\rm Eref}$: In order to verify the dynamic performance of the proposed DPSC with PLL-CTM, the operating waveforms with the step change of $R_{\rm L}$ and $R_{\rm Eref}$ are presented as follows. Fig. 31 shows the dynamic responses by changing $R_{\rm L}$ between 18 and 23 Ω suddenly, while $V_2 = 72$ V and $R_{\rm Eref} = 12.05\ \Omega$ are achieved. The dynamic setting times are 140 and 110 ms, respectively. Therefore, by using the proposed DPSC with PLL-CTM, Fig. 31 proves that the WPTS can achieve the impedance matching and constant output with the step change of $R_{\rm L}$ simultaneously, which is significant to the safe and reliable operation of the WPTS in the whole charging process of battery packs.

Fig. 32 shows the dynamic responses by changing $R_{\rm Eref}$ between 12 and 15 Ω suddenly, while $V_2 = 72$ V is maintained. The dynamic setting times are 120 and 130 ms, respectively. Therefore, by using the DPSC with PLL-CTM, Fig. 32 proves that the WPTS can achieve the impedance matching and constant output with the step change of $R_{\rm Eref}$ simultaneously, which is also significant to the safe and reliable operation of the WPTS.

In a word, by adopting the proposed DPSC with PLL-CTM, the WPTS can obtain perfect performances of the antiload disturbance and rapid dynamic response to adjust the ac equivalent resistance.

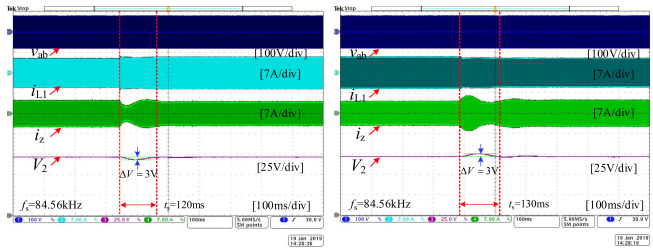


Fig. 32. Dynamic waveforms with the step change of $R_{\rm Eref}$, when the CV charging is achieved with $k = 0.2$, $V_1 = 80$ V, $V_2 = 72$ V, $R_{\rm L} = 40\ \Omega$, and $\varphi^*_{\rm iref} = -2.83^\circ$ $(-\varphi_{\rm DR})$. (a) Changing $R_{\rm Eref}$ from 12 to 15 Ω suddenly. (b) Changing $R_{\rm Eref}$ from 15 to 12 Ω suddenly.

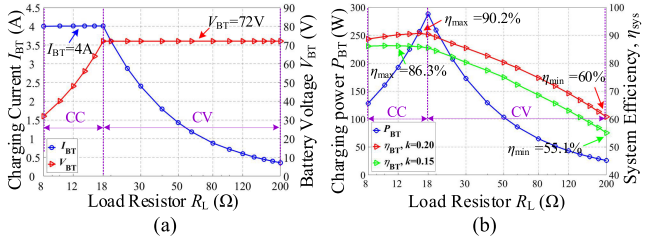


Fig. 33. Charging experiments simulated by a sliding rheostat with the proposed DPSC and PLL-CTM with $k = 0.2$ and 0.15. (a) Charging current and voltage versus $R_{\rm L}$. (b) Charging power and system efficiency versus $R_{\rm L}$.

E. Whole Charging Process

By adopting the proposed DPSC with PLL-CTM, the battery charging curves with different k are plotted in Fig. 33. By changing the resistance of the sliding rheostat to simulate the whole charging process, the designed WPTS will power to the varying load in the CC mode or CV mode with the constant $R_{\rm Eref}$. The charging current and voltage curves of the battery packs are shown in Fig. 33(a). In Fig. 33(b), the charging power gradually increases in the CC mode and gradually decreases in the CV mode. The system maximum efficiency can achieve 90.2% and 86.3% with $k = 0.2$ and $k = 0.15$ near the maximum output power point.

F. Power Loss in the Resonant Network

To evaluate the power loss of the resonant network $P_{\rm res}$, the power loss ratio of the resonant network can be defined as

$$R_{\rm res} = (P_{\rm res}/P_{\rm o}) \times 100\% \tag{20}$$

where $P_{\rm res}$ can be evaluated by

$$P_{\rm res} = I_{\rm L1}^2 \times R_1 + I_{\rm L2}^2 \times R_2. \tag{21}$$

With the same WPTS and the same operating conditions, the power loss ratio of the resonant network $R_{\rm res}$ can be measured with the proposed DPSC and the traditional variable frequency phase shift control (VFPSC) strategy [20]. $R_{\rm res}$ versus $R_{\rm L}$ with different k is plotted in Fig. 34. As can be seen in Fig. 34, by using the DPSC, the system can achieve a wider range of load resistor compared with the traditional VFPSC. Moreover, with the DPSC applied, $R_{\rm res}$ is much smaller than that of the traditional VFPSC, especially in the light load. Simultaneously,

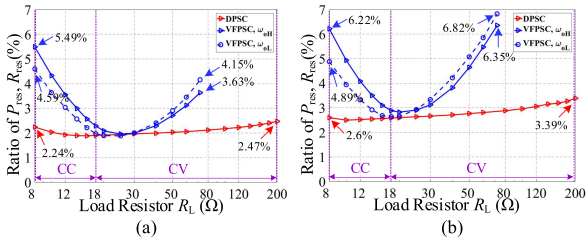


Fig. 34. Power loss ratio of the resonant network, $R_{\rm res}$, versus the load resistor $R_{\rm L}$ with different control strategies in the whole charging process. (a) $k = 0.2$. (b) $k = 0.15$.

the power loss ratio of $P_{\rm res}$ can also be maintained in a lower level, which is significant for the safe operation of coils.

VII. Conclusion

This article illustrates the essential reason why the driver pulses lose and proposes the PLL-CTM, which can lock the phase of the resonant current accurately and produce driver pulses reliably. With the proposed PLL-CTM applied in control of the AR, the WPTS can avoid pulse losing successfully and the reliability of the WPTS can be enhanced tremendously. Meanwhile, this article also presents the DPSC with PLL-CTM to achieve CC/CV charging for battery packs and minimize the power loss of the resonant network. The DPSC with PLL-CTM has perfect performances of antiload disturbance and rapid dynamic response to adjust the ac equivalent resistance. Finally, compared with the traditional VFPSC strategy, the DPSC with PLL-CTM not only expands the load range, but also minimizes the power loss of the resonant network. With the DPSC applied, the power loss of the resonant network can be limited to 2.47% with $k = 0.2$ and 3.39% with $k = 0.15$ in the whole charging process, which is significant for the safe operation of the WPTS.

References

[1] H. Liu, Q. Shao, and X. Fang, "Modeling and optimization of class-E amplifier at subnominal condition in a wireless power transfer system for biomedical implants," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 1, pp. 35–43, Feb. 2017.

[2] O. Knecht and J. W. Kolar, "Comparative evaluation of IPT resonant circuit topologies for wireless power supplies of implantable mechanical circulatory support systems," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 3271–3278.

[3] A. Askari, R. Stark, J. Curran, D. Rule, and K. Lin, "Underwater wireless power transfer," in *Proc. IEEE Wireless Power Transfer Conf.*, 2015, pp. 1–4.

[4] M. G. Eftekhar, Z. Ouyang, M. A. E. Andersen, P. B. Andersen, L. A. de S. Ribeiro, and E. Schaltz, "Efficiency study of vertical distance variations in wireless power transfer for e-mobility," *IEEE Trans. Magn.*, vol. 52, no. 7, pp. 1–4, Jul. 2017.

[5] Y. Jiang *et al.* "An optimal parameters design methodology of series-series resonant tank of wireless power transmission system for battery charging," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 1600–1605.

[6] G. Buja, M. Bertoluzzo, and K. N. Mude, "Design and experimentation of WPT charger for electric city car," *IEEE Trans. Ind. Electron.*, vol. 62, no. 12, pp. 7436–7447, Dec. 2015.

[7] D. Ahn, S. Kim, J. Moon, and I. Cho, "Wireless power transfer with automatic feedback control of load resistance transformation," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7876–7886, Nov. 2016.

[8] H. Li, J. Li, K. Wang, W. Chen, and X. Yang, "A maximum efficiency point tracking control scheme for wireless power transfer systems using magnetic resonant coupling," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3998–4008, Jul. 2015.

[9] J. Park, Y. Tak, Y. Kim, Y. Kim, and S. Nam, "Investigation of adaptive matching methods for near-field wireless power transfer," *IEEE Trans. Antennas Propag.*, vol. 59, no. 5, pp. 1769–1773, May 2011.

[10] T. Yeo, D. Kwon, S. Khang, and J. Yu, "Design of maximum efficiency tracking control scheme for closed-loop wireless power charging system employing series resonant tank," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 471–478, Jan. 2017.

[11] D. Ahn and S. Hong, "Wireless power transfer resonance coupling amplification by load-modulation switching controller," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 898–909, Feb. 2015.

[12] A. Berger, M. Agostinelli, S. Vesti, J. A. Oliver, J. A. Cobos, and M. Huemer, "A wireless charging system applying phase-shift and amplitude control to maximize efficiency and extractable power," *IEEE Trans. Power Electron.*, vol. 30, no. 11, pp. 6338–6348, Nov. 2015.

[13] E. Ozalevli *et al.*, "A cost-effective adaptive rectifier for low power loosely coupled wireless power transfer systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 7, pp. 2318–2329, Jul. 2018.

[14] R. Mai, Y. Liu, Y. Li, P. Yue, G. Cao, and Z. He, "An active-rectifier-based maximum efficiency tracking method using an additional measurement coil for wireless power transfer," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 716–728, Jan. 2018.

[15] X. Zhang *et al.*, "A control strategy for efficiency optimization and wide ZVS operation range in bidirectional inductive power transfer system," *IEEE Trans. Ind. Electron.*, vol. 66, no. 8, pp. 5958–5969, Aug. 2019.

[16] P. Tan, H. He, and X. Gao, "A frequency-tracking method based on a SOGI-PLL for wireless power transfer system to assure operation in the resonant state," *J. Power Electron.*, vol. 16, no. 3, pp. 1056–1066, 2016.

[17] Y. Lu, M. Huang, L. Cheng, W. Ki, S. U, and R. P. Martins, "A dual-output wireless power transfer system with active rectifier and three-level operation," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 927–930, Feb. 2017.

[18] B. Jang, S. Oh, Y. Park, and K. Y. Lee, "A high efficiency active rectifier with zero current sensing for loosely-coupled wireless power transfer systems," in *Proc. IEEE Int. Conf. Consum. Electron.—Asia*, 2016, pp. 1–2.

[19] Y.-J. Park *et al.*, "A design of inductive coupling wireless power receiver with high efficiency active rectifier and multi feedback LDO regulator," in *Proc. IEEE Wireless Power Transfer Conf.*, 2016, pp. 1–4.

[20] Y. Jiang, L. Wang, Y. Wang, J. Liu, M. Wu, and G. Ning, "Analysis, design, and implementation of WPT system for EV's battery charging based on optimal operation frequency range," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6890–6905, Jul. 2019.

[21] D. Ahn and S. Hong, "Wireless power transfer resonance coupling amplification by load-modulation switching controller," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 898–909, Feb. 2015.

[22] Y. Jiang, M. Wu, J. Liu, Y. Wang, L. Wang, and H. Zhang, "Analysis of optimal operation frequency range for battery charging in WPT system," in *Proc. Int. Power Electron. Conf.*, 2018, pp. 3863–3869.

[23] Y. Jiang, L. Wang, Y. Wang, J. Liu, X. Li, and G. Ning, "Analysis, design, and implementation of accurate ZVS angle control for EV battery charging in wireless high-power transfer," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 4075–4085, May 2019.

Yongbin Jiang (S'15) was born in Jiangsu, China, in 1990. He received the B.S. degree in electrical automatization from Jiangsu University, Jiangsu, China, in 2012, and the M.S. degree in instrument science and technology from Xi'an Jiaotong University, Xi'an, China, in 2015, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include wireless power transfer, high-frequency and high power density dc/dc converters, signal processing, and digital control technology.

Dr. Jiang was the recipient of the Best Paper Award of the IEEE 10th International Symposium on Power Electronics for Distributed Generation Systems in 2019.

Laili Wang (S'07−M'13−SM'15) was born in Shaanxi, China, in 1982. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2004, 2007, and 2011, respectively.

Since 2011, he has been a Postdoctoral Research Fellow with the Electrical Engineering Department, Queen's University, Kingston, ON, Canada. From 2014 to 2017, he was an Electrical Engineer with Sumida, Kingston. In 2017, he joined Xi'an Jiaotong University, as a Professor. His research interests include package and integration of passive devices in high-frequency high power density dc/dc converters, wireless power transfer, and energy harvesting.

Yue Wang (M'05) received the B.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 1994, the M.S. degree in electrical engineering from Beijing Jiaotong University, Beijing, China, in 2000, and the Ph.D. degree in electrical engineering from Xi'an Jiaotong University, in 2003.

He is currently a Full Professor with the School of Electrical Engineering, Xi'an Jiaotong University. His research interests include wireless power transfer, active power filters, multilevel converters, and high-voltage direct current.

Min Wu was born in Sichuan, China, in 1995. He received the B.S. degree in electrical automatization from Chongqing University, Chongqing, China, in 2017. He is currently working toward the M.S. degree in instrument science and technology with Xi'an Jiaotong University, Xi'an, China.

His research interests include wireless power transfer, high-frequency and high power density dc/dc converters, signal processing, and digital control technology.

Zexian Zeng was born in Fujian, China, in 1998. He is currently working toward the B.S. degree in electrical engineering and automation with Xi'an Jiaotong University, Xi'an, China.

His research interests include wireless power transfer and high-frequency and high power density dc/dc converters.

Yonghui Liu (S'19) was born in Hebei, China, in 1990. She received the B.S. degree in electrical engineering from the Harbin Institute of Technology, Heilongjiang, China, in 2013, and the M.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2016, where she is currently working toward the Ph.D. degree in electrical engineering.

Her research interests include modeling and control of converters, renewable energy integration, wireless power transfer, and voltage-source-converter-based high-voltage direct current.

Jing Sun was born in Anhui, China, in 1999. She is currently working toward the B.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China.

Her research interests include wireless power transfer and high-frequency and high power density dc/dc converters.