Modeling, Analysis, and Reduction of Harmonics in Paralleled and Interleaved Three-Level Neutral Point Clamped Inverters With Space Vector Modulation

Ruirui Chen, *Student Member, IEEE*, Jiahao Niu, *Student Member, IEEE*, Handong Gui, *Student Member, IEEE*, Zheyu Zhang, *Senior Member, IEEE*, Fei Wang, *Fellow, IEEE*, Leon M. Tolbert, *Fellow, IEEE*, Daniel J. Costinett, *Senior Member, IEEE*, Benjamin J. Blalock, *Senior Member, IEEE*, and Benjamin B. Choi

***Abstract*—Paralleling three phase three-level inverters is gaining popularity in industrial applications. However, analytical models for the harmonics calculation of a three-level neutral point clamped (NPC) inverter with popular space vector modulation (SVM) are not found in the literature. Moreover, how interleaving angle impacts the dc- and ac-side harmonics and electromagnetic interference (EMI) harmonics in parallel interleaved three-level inverters and how to optimize interleaving angle to reduce these harmonics have not been discussed in the literature. Furthering previous study, this article presents the modeling, analysis, and reduction of harmonics in paralleled and interleaved three-level NPC inverters with SVM. Analytical models for harmonic calculation are developed, and the dc-side harmonics characteristics of an NPC inverter are identified. The impact of interleaving angle on the ac-side voltage and dc-link current harmonics of parallel interleaved three-level NPC inverters is comprehensively studied. The impact of switching frequency and interleaving angle on EMI harmonics is also illustrated. Optimal interleaving angle ranges to reduce these harmonics are derived analytically. The developed models and harmonic reduction analysis are verified experimentally with two paralleled and interleaved three-level NPC inverters.**

***Index Terms*—Electromagnetic interference (EMI), harmonics, interleaving angle, paralleled converters, space vector modulation (SVM), three-level inverters.**

Manuscript received April 15, 2019; revised July 12, 2019; accepted August 23, 2019. Date of publication September 4, 2019; date of current version January 10, 2020. This work was supported in part by The Boeing Company and in part by NASA. This work also made use of the Engineering Research Center Shared Facilities supported by the Engineering Research Center Program of the National Science Foundation (NSF) and Department of Energy under NSF Award EEC-1041877 and the Center for Ultra-Wide-Area Resilient Electric Energy Transmission Networks Industry Partnership Program. Recommended for publication by Associate Editor D. O. Neacsu. *(Corresponding author: Ruirui Chen.)*

R. Chen, J. Niu, H. Gui, and B. J. Blalock are with the Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, TN 37996 USA (e-mail: rchen14@vols.utk.edu; jniu3@vols.utk.edu; hgui@vols.utk.edu; bblalock@tennessee.edu).

Z. Zhang is with Zucker Family Graduate Education Center, Clemson University, North Charleston, SC 29405 USA (e-mail: zheyu.zhang@ieee.org).

F. Wang, L. M. Tolbert, and D. J. Costinett are with the Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, TN 37996 USA, and are also with Oak Ridge National Laboratory, Oak Ridge, TN 37830 USA (e-mail: fred.wang@utk.edu; tolbert@utk.edu; daniel.costinett@utk.edu).

B. B. Choi is with NASA Glenn Research Center, Cleveland, OH 44135 USA (e-mail: benjamin.b.choi@nasa.gov).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2019.2939727

I. Introduction

THREE-PHASE voltage-source converters are very popular in medium- and high-power applications [2]. Compared with two-level converters, three-level converters have reduced voltage stress for devices, lower output current harmonics, and reduced electromagnetic interference (EMI) noise [3], [4]. Paralleling three phase converters is gaining popularity as it allows higher power rating or an increase in system reliability. In addition, by phase shifting the carriers of the paralleled converters, i.e., interleaving, the switching frequency harmonics can be reduced; as a result, the size and weight of passive components such as the dc-link capacitors and EMI filters can be reduced.

Pulsewidth modulation (PWM) method generates undesired harmonics. Identification of harmonics in a power converter is important for passive components design and reduction. Although time domain simulation can be used to investigate the harmonics, an analytical approach is more time efficient, and provides insightful views for understanding in most cases. An analytical approach is also necessary for case studies when several cases need to be investigated.

Harmonics generated by PWM can be determined using double Fourier integral analysis. Extensive study has been conducted on the harmonic analysis of two-level converters. The ac phase output voltage harmonics of a two-level converter with both carrier-based PWM and space vector-based PWM have been calculated in [5]. The dc-link current harmonics of a two-level inverter with sine-triangle modulation are calculated in [6] and [7]. For paralleled and interleaved two-level inverters, the impact of interleaving on harmonic voltages and currents on the ac side and dc side is analyzed in [8]–[15].

Compared to two-level inverters, the scenarios involved in three-level inverters are more complicated. The ac output voltage harmonic analysis of cascaded two two-level inverters with sinusoidal PWM (SPWM) is presented in [16]. The dead time introduced harmonics in the output voltage of a three-level neutral point clamped (NPC) inverter is analyzed in [17]. The ac-side harmonics of a three-level rectifier with SPWM is illustrated in [18]. All prior works on the harmonics analysis of three-level converters are for carrier-based SPWM.

Space vector-based PWM are more flexible and popular in three-level converters. Due to the existence of redundant space

vectors in three-level inverters, multiple control objectives such as balancing the neutral-point voltage, reducing EMI noise, and reducing switching loss can be achieved by selecting different redundant small vectors [19], [20]. Popular SVM schemes such as nearest three space vector (NTSV) [21], common-mode reduction (CMR) [22], and common-mode elimination (CME) [23] are developed. However, no literature is found on analytical models for harmonics calculation of SVM-based three-level inverters. Also, for the dc-side harmonics of a three-level NPC inverter, although in previous work the dc-link neutral point potential third-order fundamental frequency variation has been identified by time-domain analysis [24]–[26], the dc-side current harmonic frequency-domain characteristic has not been identified.

Moreover, how interleaving angle impacts the ac- and dc-side harmonics of parallel interleaved three-level NPC inverters and how to optimize interleaving angle to reduce these harmonics have not been investigated in previous work. Although some analysis on interleaved two-level inverters can be extended to three-level inverters, the study of this article shows that unique characteristics exist in interleaved three-level NPC inverters, and the optimal interleaving angles to reduce dc-side harmonics are quite different from the two-level inverter case.

In terms of EMI harmonics (which refers to harmonics in the frequency range 150 kHz–30 MHz), the nonlinear relationship between switching frequency and EMI filter corner frequency is discussed in [27] and [28]. Asymmetric interleaving has been applied to paralleled two-level inverters to reduce EMI noise [29]. However, there is still a lack of a comprehensive model on relationship between switching frequency, interleaving angle, and EMI filter corner frequency in paralleled inverters. Furthering past study, this article provides analytical models to clearly illustrate how switching frequency and interleaving angle impact the EMI filter corner frequency.

This article presents the modeling, analysis, and reduction of harmonics in paralleled and interleaved three-level NPC inverters with SVM. The organization of this article is as follows. Section II develops analytical models for harmonics calculation of three-level NPC inverter. Section III investigates the impact of interleaving angle on ac- and dc-side harmonics. Section VI studies the impact of switching frequency and interleaving angle on EMI harmonics. Section V conducts the experimental verifications, and Section VI concludes this article.

II. Analytical Model for Harmonic Calculation of Three-Level NPC Inverter

A. Three-Level SVM

The popular three-level SVM—NTSV scheme—is shown in Fig. 1. The vector dwell time calculation method is illustrated in [19]. The NTSV scheme uses all the redundant switching states of small vectors as shown in Fig. 1. Fig. 1 also shows the PWM sequences of NTSV in all subsectors of sector I. NTSV will be used as an example to develop analytical models and to conduct harmonic analysis in this article.

Different from two-level SVM, the sector is determined by both the reference angle and amplitude for three-level SVM. To better illustrate the harmonic calculation of three-level SVM,

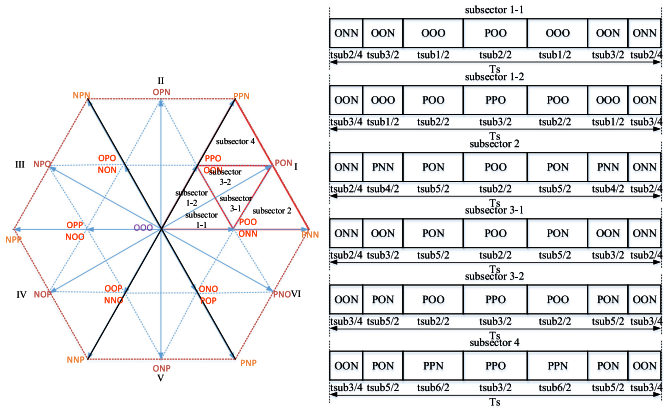


Fig. 1. Vectors of NTSV and the PWM sequences in sector I.

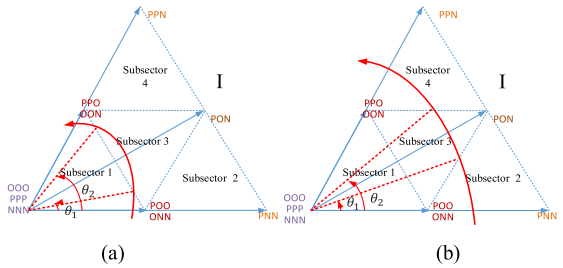


Fig. 2. Two subsector boundary angles in sector I: (a) region 2 and (b) region 3.

here three regions are defined as (1) based on the modulation index range

$$\text{region 1}: M \le \frac{1}{\sqrt{3}}; \text{region 2}: \frac{1}{\sqrt{3}} < M \le \frac{2}{3};$$
$$\text{region 3}: \frac{2}{3} < M \le \frac{2}{\sqrt{3}}. \tag{1}$$

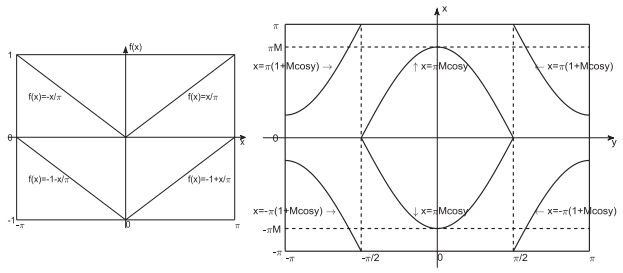
M is the modulation index which is defined as

$$M = V_{\text{phase}}/(V_{\text{dc}}/2)\,. \tag{2}$$

The voltage reference will go through a full circle for a fundamental period. When the reference is in region 1, it will only go through subsector 1 of sector I. When the reference is in region 2, it will go through sector I from subsector 1 to subsector 3 and then back to subsector 1. When the reference is in region 3, it will go through sector I from subsector 2 to subsector 3 and then to subsector 4. The cases in other sectors are the same. In both region 2 and region 3, the reference will go through different subsectors. For calculation purpose, two subsector boundary angles are defined as θ_1 and θ_2 as shown in Fig. 2. When in region 2, the boundary angles are calculated as (3). When in region 3, the boundary angles are calculated as (4)

$$\theta_1 = \arcsin\frac{1}{\sqrt{3}M} - \frac{\pi}{3}, \quad \theta_2 = \frac{2\pi}{3} - \arcsin\frac{1}{\sqrt{3}M} \tag{3}$$

$$\theta_1 = \frac{\pi}{3} - \arcsin\frac{1}{\sqrt{3}M}, \quad \theta_2 = \arcsin\frac{1}{\sqrt{3}M}. \tag{4}$$



(a) (b)

Fig. 3. (a) Three-level PD PWM carrier waveform. (b) Unit cell contour plot.

B. Analytical Model for AC Voltage Harmonics

The spectrum of pulsewidth modulated phase leg voltage can be expressed as (5) shown at the bottom of this page, [5]. Here, m and n are the fundamental and carrier baseband integer indices, respectively. The carrier and fundamental angular frequency are represented by ω_c and ω_0, respectively.

For carrier-based PWM, Fig. 3(a) shows the three-level phase disposition (PD) PWM carrier waveform, and the unit cell contour plot is shown in Fig. 3(b) when the sinusoidal reference is $f(y) = M\cos y$. Then, the harmonic coefficient C_{mn} can be determined as (6) shown at the bottom of this page.

SVM is functionally equivalent to carrier-based PWM. The basic idea to derive the analytical solution for three-level SVM is to redefine the integral limits in (6) by considering that the reference is no longer purely sinusoidal but is now made up of several segments across a full fundamental cycle.

For NTSV scheme shown in Fig. 1, in sector I subsector 2, the equivalent reference is the average of the applied vector volt–second, and is calculated as (7). Then, the inner integral limits can be determined as (8). The integral limits in other subsectors can be determined similarly.

For different regions, as the reference will go through different subsectors, the equivalent reference and double Fourier integral limits will be different. Table I summarizes the integral limits of sector I, sector II, and sector III in region 3. The integral limits for region 2 and region 1 are shown in the Appendix Tables VII and VIII.

TABLE I
DOUBLE FOURIER INTEGRAL LIMITS OF NTSV IN REGION 3 (SECTORS I, II, II)

y_s	y_e	x_r	x_f	$f(x,y)$
0	θ_1	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$\frac{V_{dc}}{2}$
θ_1	$\frac{\pi}{6}$	$-\pi(\frac{3}{2}Mcosy-\frac{1}{2})$	$\pi(\frac{3}{2}Mcosy-\frac{1}{2})$	$\frac{V_{dc}}{2}$
$\frac{\pi}{6}$	θ_2	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right)+\frac{1}{2})$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right)+\frac{1}{2})$	$\frac{V_{dc}}{2}$
θ_2	$\frac{\pi}{3}$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$\frac{V_{dc}}{2}$
$\frac{\pi}{3}$	$\frac{\pi}{3}+\theta_1$	$-\pi(\frac{3}{2}Mcosy)$	$\pi(\frac{3}{2}Mcosy)$	$\frac{V_{dc}}{2}$
$\frac{\pi}{3}+\theta_1$	$\frac{\pi}{2}$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right)+\frac{1}{2})$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right)+\frac{1}{2})$	$\frac{V_{dc}}{2}$
$\frac{\pi}{2}$	$\frac{\pi}{3}+\theta_2$	$-\pi$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right)+\frac{1}{2})$	$-\frac{V_{dc}}{2}$
		$\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right)+\frac{1}{2})$	π	
$\frac{\pi}{3}+\theta_2$	$\frac{2\pi}{3}$	$-\pi$	$-\pi(1+\frac{3}{2}Mcosy)$	$-\frac{V_{dc}}{2}$
		$\pi(1+\frac{3}{2}Mcosy)$	π	
$\frac{2\pi}{3}$	$\frac{2\pi}{3}+\theta_1$	$-\pi$	$-\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	$-\frac{V_{dc}}{2}$
		$\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	π	
$\frac{2\pi}{3}+\theta_1$	$\frac{5\pi}{6}$	$-\pi$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right)+\frac{1}{2})$	$-\frac{V_{dc}}{2}$
		$\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right)+\frac{1}{2})$	π	
$\frac{5\pi}{6}$	$\frac{2\pi}{3}+\theta_2$	$-\pi$	$-\pi(\frac{3}{2}Mcosy+\frac{3}{2})$	$-\frac{V_{dc}}{2}$
		$\pi(\frac{3}{2}Mcosy+\frac{3}{2})$	π	
$\frac{2\pi}{3}+\theta_2$	π	$-\pi$	$-\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	$-\frac{V_{dc}}{2}$
		$\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	π	

Dead time will impact the harmonics amplitude. As the dead time t_d is small in the studied system (2% of the switching period $T_{\rm sw}$), its impact on harmonics is very small and can be neglected. For applications where dead time is relatively large and needs to be considered, the inner integral limits shown in Table I should be modified by adding a term $2\pi t_d/T_{\rm sw}$ on the rising or falling edge according to the polarity of output current. For simplicity, dead-time effect is not shown in the models.

C. Analytical Model for DC-Link Current Harmonics of NPC

Fig. 4 depicts the switching pattern and the current paths of the two dc-link capacitors of a three-level active NPC (ANPC) inverter. The positive line current $i_p(t)$ of a three-level NPC

$$f(t)=\frac{A_{00}}{2}+\sum_{n=1}^{\infty}[A_{\rm on}\cos(ny)+B_{\rm on}\sin(ny)]+\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty\\(n\neq 0)}}^{\infty}[A_{mn}\cos(mx+ny)+B_{mn}\sin(mx+ny)],\ x=\omega_c t,\ y=\omega_0 t$$

$$C_{mn}=A_{mn}+jB_{mn},\ A_{mn}=\frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi}f(x,y)\cos(mx+ny)\,dxdy,\ B_{mn}=\frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi}f(x,y)\sin(mx+ny)\,dxdy \tag{5}$$

$$C_{mn}=\frac{1}{2\pi^2}\left[\int_{-\pi}^{-\frac{\pi}{2}}\int_{-\pi}^{-\pi(1+M\cos y)}\left(-\frac{V_{\rm dc}}{2}\right)e^{j(mx+ny)}dxdy+\int_{-\pi}^{-\frac{\pi}{2}}\int_{\pi(1+M\cos y)}^{\pi}\left(-\frac{V_{\rm dc}}{2}\right)e^{j(mx+ny)}dxdy+\int_{\frac{\pi}{2}}^{\pi}\int_{-\pi}^{-\pi(1+M\cos y)}\right.$$
$$\left.\times\left(-\frac{V_{\rm dc}}{2}\right)e^{j(mx+ny)}dxdy+\int_{\frac{\pi}{2}}^{\pi}\int_{\pi(1+M\cos y)}^{\pi}\left(-\frac{V_{\rm dc}}{2}\right)e^{j(mx+ny)}dxdy+\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}}\int_{-\pi M\cos y}^{\pi M\cos y}\left(\frac{V_{\rm dc}}{2}\right)e^{j(mx+ny)}dxdy\right] \tag{6}$$

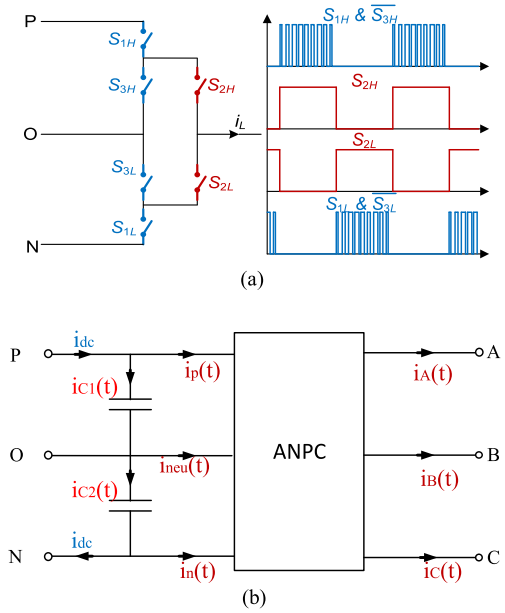


Fig. 4. (a) Switching pattern of a three-level ANPC. (b) Current path.

inverter is a combination of ac output currents and the uppermost switch S_{1H}. The ac output current can be considered as sinusoidal if its total harmonic distortion is small. Hence, the frequency-domain expression of switched current of phase A in the dc side can be derived as (9) shown at the bottom of this page. Here, s_{1H-a} represents the switching function of the uppermost switch S_{1H-a}. I_0 and $\varnothing$ are the amplitude of the phase output current and the phase angle, respectively.

The harmonic coefficient of switching function s_{1H-a} is expressed as C_{mn-1a}. According to the switching pattern, the double Fourier integral limits of C_{mn-1a} are similar to the derived phase output voltage model in Table I. The difference is that the function $f(x,y)$ is equal to 1 instead of $V_{\rm dc}/2$ for the positive half-cycle, and $f(x,y)$ is equal to zero instead of $-V_{\rm dc}/2$ for the negative half-cycle. Then, C_{mn-1a} can be determined, which is asymmetric in a fundamental cycle. This causes the input current frequency-domain characteristics to be quite different from two-level inverter case.

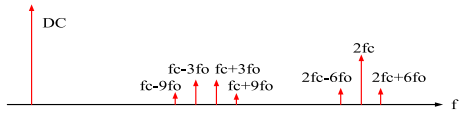


Fig. 5. DC-side current spectrum of a two-level inverter with SVM when PF = 1.

As C_{mn-1a} is determined, transforming (9) back to the time domain, the Fourier series of switched current of phase A in the dc side and harmonic coefficient C_{mn-a} are represented as (10) shown at the bottom of this page. The contribution of phase B and C switched currents to the dc-side current can be calculated similarly. Then, the harmonic coefficient C_{mn} of $i_p(t)$ is derived by summing all three phases as (11) shown at the bottom of this page. The harmonic spectrum of negative line current $i_n(t)$ is similar as $i_p(t)$ due to symmetry, and the neutral line current $i_{\rm neu}(t)$ harmonics can be calculated based on the relationship shown in (12) shown at the bottom of this page.

$$V_{\rm ref} = \frac{\sqrt{3}}{2} M \cos\left(y - \frac{\pi}{6}\right) \tag{7}$$

$$x_r = -\pi\left(\frac{\sqrt{3}}{2} M \cos\left(y - \frac{\pi}{6}\right)\right)$$

$$x_f = \pi\left(\frac{\sqrt{3}}{2} M \cos\left(y - \frac{\pi}{6}\right)\right). \tag{8}$$

To illustrate the difference of the dc-side current harmonics between a three-level NPC inverter and a two-level inverter, the dc-side current characteristics of the two-level inverter are briefly discussed. The dc-side current spectrum of a two-level inverter with SVM is calculated, and the main components are shown in Fig. 5. The dc input current spectrum has the dc component, odd order carrier harmonic components such as $f_c \pm 3f_0$, $f_c \pm 9f_0$, and even order carrier harmonic components such as $2f_c$, $2f_c \pm 6f_0$. Since the first carrier harmonic does not exist, the second carrier harmonic is the dominant component.

Then, based on the derived dc-side current harmonic model for a three-level NPC inverter, the current spectrum is calculated, and the main components are shown in Fig. 6. Fig. 6(a) shows

$$I_{{\rm dc}-a}(\omega) = s_{1H-a}(\omega) \otimes I_{0a}(\omega) = \frac{I_{0a}}{2}\left(e^{j\varnothing} s_{1H-a}(\omega - \omega_0) + e^{-j\varnothing} s_{1H-a}(\omega - \omega_0)\right) \tag{9}$$

$$I_{{\rm dc}-a}(t) = \frac{A_{00-a}}{2} + \sum_{n=1}^{\infty}\left[A_{0n-a}\cos(ny) + B_{0n-a}\sin(ny)\right] + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\left[A_{mn-a}\cos(mx+ny) + B_{mn-a}\sin(mx+ny)\right]$$

$$A_{00-a} = \frac{I_0}{2}\left(A_{01}\cos\varnothing + B_{01}\sin\varnothing\right),\ A_{mn-a} = \frac{I_0}{2}\left[\left(A_{m,n-1-1a} + A_{m,n+1-1a}\right)\cos\varnothing + \left(B_{m,n-1-1a} + B_{m,n+1-1a}\right)\sin\varnothing\right]$$

$$B_{mn-a} = \frac{I_0}{2}\left[\left(B_{m,n-1-1a} + B_{m,n+1-1a}\right)\cos\varnothing - \left(A_{m,n-1-1a} - A_{m,n+1-1a}\right)\sin\varnothing\right] \tag{10}$$

$$I_{\rm dc}(\omega) = s_{a1}(\omega) \otimes I_{0a}(\omega) + s_{b1}(\omega) \otimes I_{0b}(\omega) + s_{c1}(\omega) \otimes I_{0c}(\omega),\ C_{mn} = C_{mn-a}\left(1 + 2\cos\left(n\frac{2\pi}{3}\right)\right) \tag{11}$$

$$i_{\rm dc} - i_{c1}(t) = i_p(t),\ i_{c2}(t) - i_{\rm dc} = i_n(t),\ i_{neu}(t) = i_{C1}(t) - i_{C2}(t) = -i_p(t) - i_n(t) \tag{12}$$

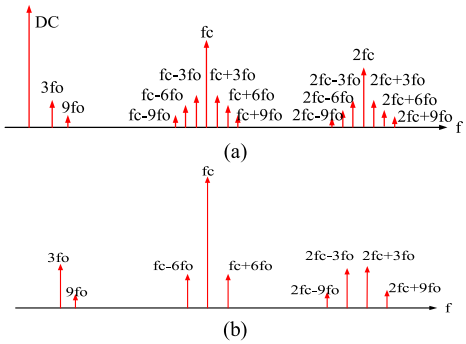


Fig. 6. DC-side current spectrum of a three level NPC inverter with NTSV when PF = 1. (a) Positive/negative line current. (b) Neutral line current.

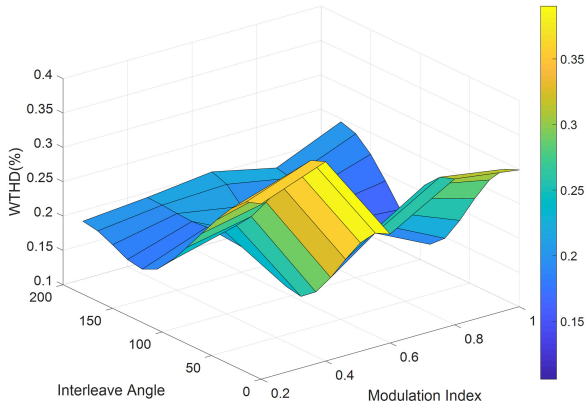


Fig. 7. AC-side line-to-line voltage WTHD versus interleaving angle ($f_0 =$ 400 Hz, $f_c = 20$ kHz).

the positive/negative line current spectrum, and Fig. 6(b) shows the neutral line current spectrum.

Unlike the spectrum of the two-level inverter, the positive/negative line current has the dc component, third-order harmonics, and $mf_c \pm 3nf_0$ carrier harmonics for both odd order and even order carrier harmonics. The neutral line current does not have a dc component, but it has the third harmonics, odd order carrier harmonic components such as f_c, $f_c \pm 6f_0$, and even order carrier harmonics components such as $2f_c \pm 3f_0$, $2f_c \pm 9f_0$. The third harmonic and all the carrier harmonics have doubled amplitude compared to the positive/negative line current harmonics. For both the positive/negative line current and neutral line current, the first carrier harmonic is the dominant component.

The difference of dc-side current harmonic characteristics between a two-level inverter and a three-level NPC inverter is caused by the NPC structure. The existence of the neutral line actually decouples the positive line and negative line current. Thus, more sideband harmonics exist in the NPC inverter.

III. Impact of Interleaving on AC- and DC-Side Harmonics

The impact of interleaving angle on ac-side voltage and dc-side current harmonics of parallel interleaved three-level NPC inverters is studied in this section. For two interleaved inverters, if the interleaving angle of inverter 2 is γ with respect to inverter 1, the harmonic amplitude of two interleaved inverters output can be determined as (13). From (13), it is obvious that interleaving can reduce the amplitude of the output harmonics

$$C_{mn,\text{avg}} = \frac{1}{2}\left|(C_{mn,1} + C_{mn,2}e^{im\gamma})\right| = C_{mn}\left|\cos\left(\frac{m\gamma}{2}\right)\right|. \quad (13)$$

A. Impact of Interleaving Angle on AC-Side Voltage Weighted Total Harmonic Distortion (WTHD)

The WTHD is a commonly used figure of merit to size the power filter requirements in the ac output side [5] and is used for interleaving angle optimization. With the developed models in Section II and (13), the ac-side line voltage harmonics WTHD is calculated as a function of modulation index and interleaving angle. The results are shown in Fig. 7. From Fig. 7, interleaving angle range around 90° is optimal to minimize WTHD for different modulation indexes. As the dominant high frequency components in the line voltage are the second carrier harmonic sidebands $2f_c \pm f_0, 90^\circ$ interleaving angle eliminates the second carrier harmonic and sideband and thus significantly reduces WTHD.

B. Impact of Interleaving Angle on DC-Link Capacitor RMS Current

Based on the spectrum analysis in Section II, the dc-side current of a three-level NPC inverter has both low frequency and high frequency components. The low frequency components can be controlled if there are front-end converters, or closed-loop control, and is not impacted by interleaving angle. The high frequency components are the result of PWM switching and must be handled by dc-link capacitors. DC-link capacitors are usually a weak point in the system and determine system reliability due to the thermal issues related to ripple current flowing through the capacitors. The capacitor high frequency ripple current rms value is used as the figure of merit for interleaving angle optimization. From Fig. 4(b) and the relationship shown in (12), the high frequency harmonics in the positive/negative line will flow through the dc-link capacitor.

With the developed models in Section II and (13), the normalized dc-link capacitor high frequency ripple current rms value is calculated as a function of modulation index, interleaving angle, and power factor. The results are shown in Fig. 8. The optimal interleaving angle range for dc-link capacitor ripple current rms value is highly dependent on power factor and modulation index. The results show different trends compared to the interleaved two-level inverters analyzed in [8].

When the modulation index is high and power factor is high, the minimum dc-link capacitor ripple current rms value can be achieved when the interleaving angle range is around 180°. This can be expected as the first carrier harmonic exists and is the dominant high frequency component in the dc-link capacitor current, and 180° interleaving angle will totally eliminate the first carrier harmonic and its sidebands.

When the modulation index is high and power factor is low, the minimum dc-link capacitor ripple current rms value can be achieved when the interleaving angle range is around 90°. This

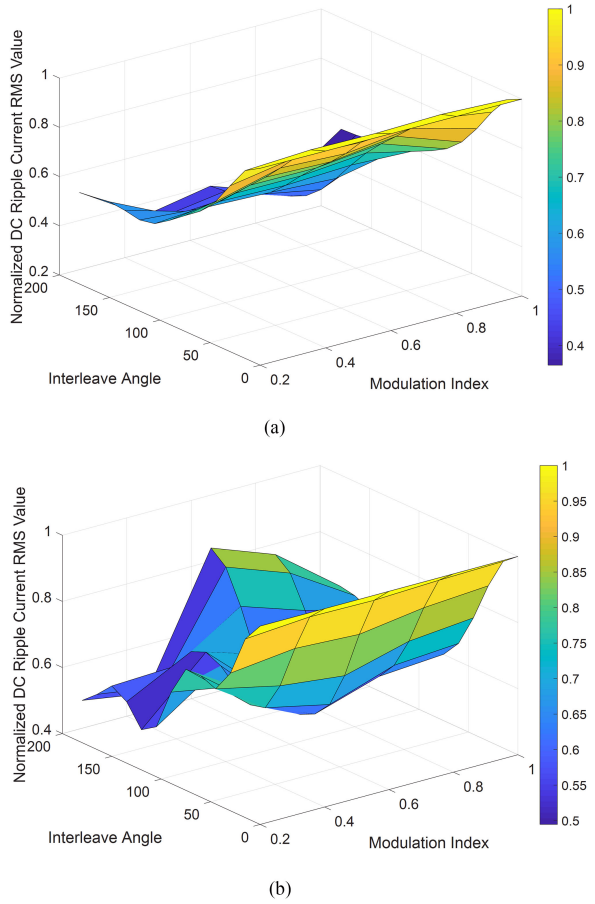


Fig. 8. DC-side dc-link capacitor ripple current rms value versus interleaving angle ($f_0 = 400$ Hz, $f_c = 20$ kHz). (a) PF $= 1$. (b) PF $= 0$.

is because the second carrier harmonic sidebands become the dominant high frequency component, and 90° interleaving angle will eliminate the second carrier harmonic and its sidebands.

When the modulation index is low (in region 1), the dc-link capacitor ripple current rms value shows a complicated variation trend when the interleaving angle varies. This is because both the first and second and high-order carrier harmonic sidebands are dominant in this case.

IV. Impact of Switching Frequency and Interleaving on EMI Harmonics

EMI filters are required in power converters to suppress the EMI harmonics and thus pass EMI standards. The size and weight of an EMI filter can be indicated by EMI filter corner frequency. A higher EMI filter corner frequency usually indicates a smaller filter. The impact of switching frequency and interleaving angle on EMI filter corner frequency is analytically derived in this section.

A. Relationship Between Switching Frequency and EMI Filter Corner Frequency

As the harmonics of ac-side voltage is calculated above, the EMI noise source for CM and differential-mode (DM) voltages

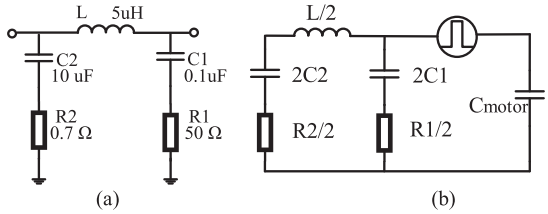


Fig. 9. (a) LISN used in DO-160 standards. (b) CM equivalent circuit.

can be determined as

$$V_{\mathrm{CM}} = \frac{V_A + V_B + V_C}{3} = \frac{1}{3}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} C_{mn}\cos\left(mx + ny\right)\left(1+2\cos\left(n\frac{2\pi}{3}\right)\right) \tag{14}$$

$$V_{\mathrm{DM}\text{–}A} = V_A - V_{\mathrm{CM}}. \tag{15}$$

EMI filter design methodology is illustrated in [30]. EMI filter corner frequency is determined by a certain EMI noise peak. The inverter-fed motor drive system in aircraft application is investigated. For CM noise, the motor CM impedance can be simply modeled as a capacitor [32]. EMI noise currents need to meet DO-160 standards. The LISN schematic defined in DO-160 standards [31] is shown in Fig. 9(a). The CM equivalent circuit for the CM noise propagation path is derived as shown in Fig. 9(b).

As the EMI noise source and noise propagation path impedance are determined, and EMI standards are given, the required CM noise attenuation can be determined as

$$I_{\mathrm{RA}(f_{\mathrm{index}})} = 20\log_{10}\left(\frac{V_{\mathrm{CM}(f_{\mathrm{index}})}\times 10^6}{Z_{\mathrm{CM}(f_{\mathrm{index}})}}\right) - I_{\mathrm{std}(f_{\mathrm{index}})} + \mathrm{Margin} \tag{16}$$

where $I_{\mathrm{RA}(f_{\mathrm{index}})}$, $I_{\mathrm{std}(f_{\mathrm{index}})}$, $V_{\mathrm{CM}(f_{\mathrm{index}})}$, and $Z_{\mathrm{CM}(f_{\mathrm{index}})}$ are the noise current required attenuation, EMI standards defined noise current limit level, CM noise voltage, and CM noise propagation path impedance at a certain frequency f_{index}, respectively.

After the required noise attenuation is calculated and the EMI filter type is selected, the noise peak frequency f_{pk} that determines the EMI filter corner frequency can be identified with the flowchart shown in Fig. 10. Then, CM filter corner frequency can be calculated as (18). Here, the filter type is indicated by k ($k = 2$ and $k = 4$ represent single and two stage LC filters, respectively).

Then, the CM filter corner frequency f_c as a function of switching frequency f_s can be calculated. Fig. 11 shows a case study calculation results ($C_{\mathrm{motor}} = 1\mathrm{nF}$) when one stage LC filter and two stage LC filter are assumed. The DM filter corner frequency calculation is similar and is not repeated here.

Resonance may exist in the CM noise propagation path impedance if there is not enough damping. If the resonance frequency is close to the switching frequency or its multiples, it may become the noise peak frequency and largely impact the CM filter corner frequency. However, as discussed in [33] and

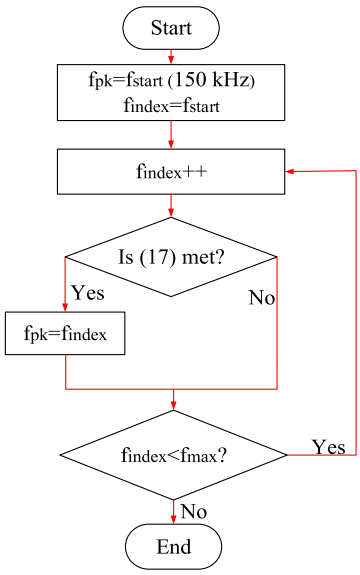


Fig. 10. Flowchart to determine the noise peak frequency.

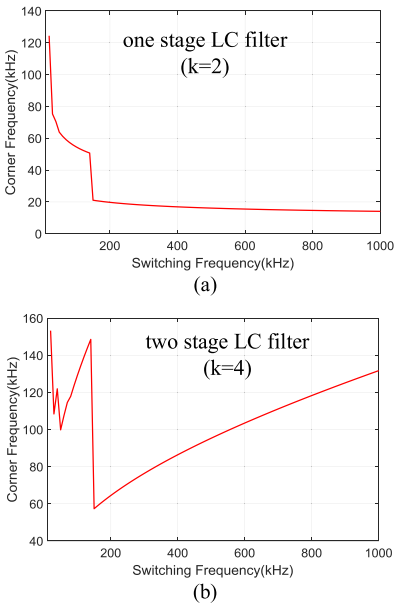


Fig. 11. Calculated corner frequency versus switching frequency. (a) Single-stage *LC* filter and (b) two-stage *LC* filter.

[34], for a high density EMI filter design, it is better to damp the impedance resonance first and then design the EMI filter.

$$I_{\mathrm{RA}(f_{\mathrm{index}})} \geq k\left(20\log_{10}\left(f_{\mathrm{index}}\right)-20\log_{10}\left(f_{\mathrm{pk}}\right)\right)+I_{\mathrm{RA}}\left(f_{\mathrm{pk}}\right) \tag{17}$$

$$\log_{10}\left(f_c\right)=\log_{10}\left(f_{\mathrm{pk}}\right)+\frac{I_{\mathrm{std}(f_{\mathrm{pk}})}-20\log_{10}\left(\dfrac{V_{\mathrm{CM}\left(f_{\mathrm{pk}}\right)}10^6}{Z_{\mathrm{CM}\left(f_{\mathrm{pk}}\right)}}\right)}{20k}. \tag{18}$$

From Fig. 11, several findings are observed. When 20 kHz $<$ f_s $<$ 150 kHz, f_c and f_s have a nonlinear relationship; some preferred f_s exists such as 140 kHz. When 150 kHz $<$ f_s $<$

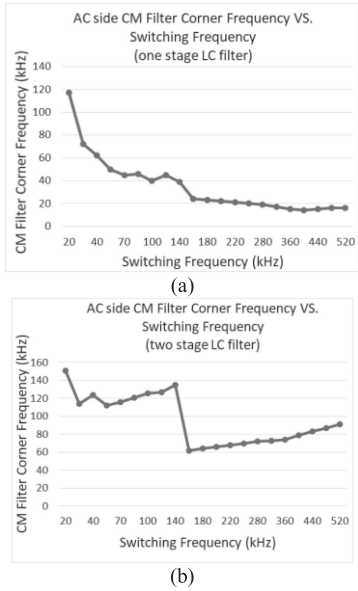


Fig. 12. Design results of ac-side CM filter corner frequency versus switching frequency. (a) Single-stage *LC* filter and (b) two-stage *LC* filter applied.

2 MHz, if a single-stage LC filter is applied, f_c has slight change as f_s increases. If two or multiple stage *LC* filters are applied, f_c increases fast as f_s increases. The findings provide a guideline for switching frequency and EMI filter type selection.

The nonlinear relationship between f_c and f_s in the 20–150 kHz range can be understood because the noise peak frequency and CM voltage amplitude are not linearly changed when switching frequency increases. The different trends of filter corner frequency between a single-stage LC filter and a multiple-stage filter when switching frequency is in the 150 kHz–2 MHz range can also be explained. As switching frequency increases, the *LC* filter impedance increases, and the DO-160 EMI standard limit decreases at a slow rate of around 30 dB/dec. For single-stage *LC* filter, the benefit gained from the increase of *LC* filter impedance is almost cancelled out by the decrease of the EMI standards limit. As a result, f_c has slight change as f_s increases. For multiple stage *LC* filters, *LC* filter impedance increases much faster as switching frequency increases and outweighs the decrease of EMI standard limit. Thus, f_c increases fast as f_s increases.

MATLAB/Simulink simulations were conducted to get CM filter corner frequencies for different switching frequencies as shown in Fig. 12. The trends of how the CM filter corner frequency varies with switching frequency match the model results and conclusions above.

B. Impact of Interleaving on EMI Filter Corner Frequency

According to (13), when symmetric interleaving ($\gamma = \pi$) is applied to two interleaved inverters

$$C_{mn,\mathrm{avg}}=C_{mn}\left|\cos\left(\frac{m\pi}{2}\right)\right|=\begin{cases}C_{mn}, & m \text{ is an even number}\\ 0, & m \text{ is an odd number.}\end{cases} \tag{19}$$

When asymmetric interleaving ($\gamma \neq \pi$) is applied to two interleaved inverters

$$C_{mn,avg} = C_{mn}\left|\cos\left(\frac{mr}{2}\right)\right| \leq C_{mn}. \tag{20}$$

Hence, symmetric interleaving will eliminate the odd number carrier harmonics while keeping the even number carrier harmonics amplitude unchanged. Asymmetric interleaving could reduce the amplitude of all the harmonic components. When the objective is EMI noise and EMI filter reduction which is determined by certain EMI harmonic peaks, asymmetric interleaving could be more effective.

The CM and DM voltage harmonics calculation, noise propagation path impedance calculation, and the noise peak frequency $f_{\rm pk}$ identification are illustrated in Section IV-A. Then, the relationship between interleaving angle and CM filter corner frequency is calculated as (21). The relationship between interleaving angle and ac-side DM filter corner frequency can be calculated similarly

$$\log_{10}(f_c) = \log_{10}(f_{\rm pk}) + \frac{I_{\rm std(f_{pk})} - 20\log_{10}\left(\dfrac{V_{\rm CM}(f_{\rm pk})\cos\left(\frac{m\gamma}{2}\right)10^6}{Z_{\rm CM}(f_{\rm pk})}\right)}{20\cdot k}. \tag{21}$$

From (21), EMI filter corner frequency is a function of switching frequency, modulation index, interleaving angle, EMI filter type, and EMI noise propagation path impedance. Interleaving angle can be optimized to increase EMI filter corner frequency.

Whether the switching frequency is located in the EMI frequency range or not will influence the trend how EMI filter corner frequency varies as interleaving angle changes. Hence, two case studies are conducted.

The first case is that switching frequency is $f_s = 70$ kHz($<$ 150 kHz). The CM and DM filter corner frequencies are calculated as a function of modulation index and interleaving angle. One stage filter is assumed ($k = 2$). The results are shown in Fig. 13.

From Fig. 13(a), the CM filter corner frequency peak is achieved when interleaving angle is around 180°, and the second optimal interleaving angle range is 30°–90°. From Fig. 13(b), the DM filter corner frequency peak is obtained when interleaving angle is around 30°–60°, and the second optimal interleaving angle range is around 120°–180°.

In this case, the first and second carrier harmonics are not in the EMI frequency range. Hence, the third to sixth carrier harmonics are the potential candidates which may determine EMI filter corner frequency. For CM voltage harmonics, the third and fifth harmonics are dominant, and 30°–60° and 150°–180° interleaving angle ranges are preferred for harmonics reduction according to Fig. 14. For DM voltage harmonics, the fourth and sixth harmonics are dominant, and 30°–60° and 90°–120° interleaving angle ranges are preferred for harmonics reduction.

The second case is that switching frequency is $f_s =$ 200 kHz($>$150 kHz). In this case, the first and second carrier harmonics are in the EMI frequency range. The analysis is similar. The CM and DM filter corner frequencies are also calculated,

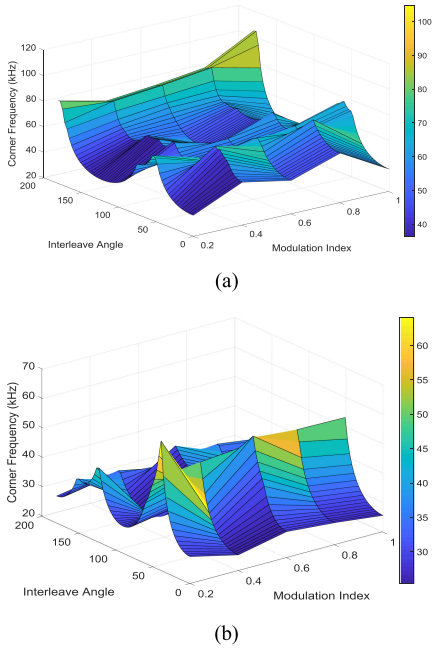


Fig. 13. EMI filter corner frequency versus interleaving angle ($f_s = 70$ kHz). (a) CM filter. (b) DM filter.

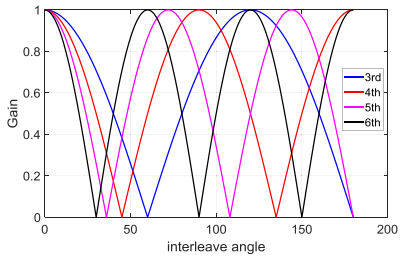


Fig. 14. Third, fourth, fifth, and sixth carrier harmonics gain versus interleaving angle.

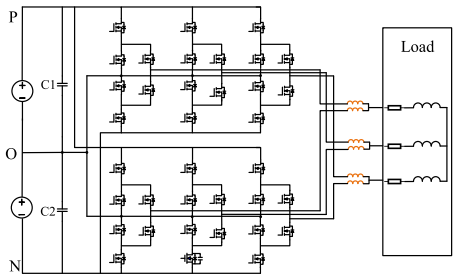


Fig. 15. Circuit schematic of two paralleled three-level ANPC inverters.

and the results show that the CM filter corner frequency peak is achieved when interleaving angle is around 180° while the DM filter corner frequency peak is achieved when interleaving angle is in the 90°–150° range.

V. Experimental Results

Two three-level NPC inverters are constructed to verify the developed models and harmonic reduction analysis. Fig. 15

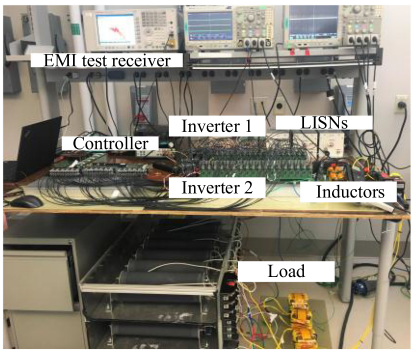


Fig. 16. Experimental platform of the paralleled three-level NPC inverters.

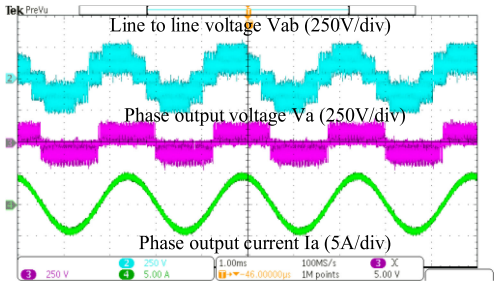


Fig. 17. AC-side output voltage and current.

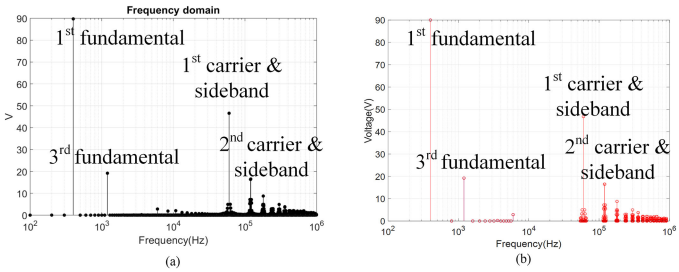


Fig. 18. Spectrum of ac-side phase output voltage. (a) Tested results. (b) Calculation results with developed models.

TABLE II
COMPARISON OF MAIN COMPONENTS OF AC PHASE OUTPUT VOLTAGE

Harmonics/V	f_0	$3f_0$	f_c	$2f_c \pm f_0$	$2f_c \pm 3f_0$
Tested	89	18.7	46	16	1.1
Calculated	90	19.2	46.8	16.6	1.3

shows the circuit schematic, and Fig. 16 shows the experimental platform. The dc voltage is 200 V, ac output fundamental frequency is 400 Hz, and carrier frequency is 60 kHz. *RL* load ($R = 20\ \Omega$, $L = 320\ \mu$H for each phase) is used.

A. Analytical Model Verification

Fig. 17 shows the ac-side output voltages and current with modulation index $M = 0.9$. Fig. 18(a) and (b) shows the tested phase output voltage spectrum and the calculated spectrum with the developed model, respectively. Table II summarizes the main components value comparison between tested results

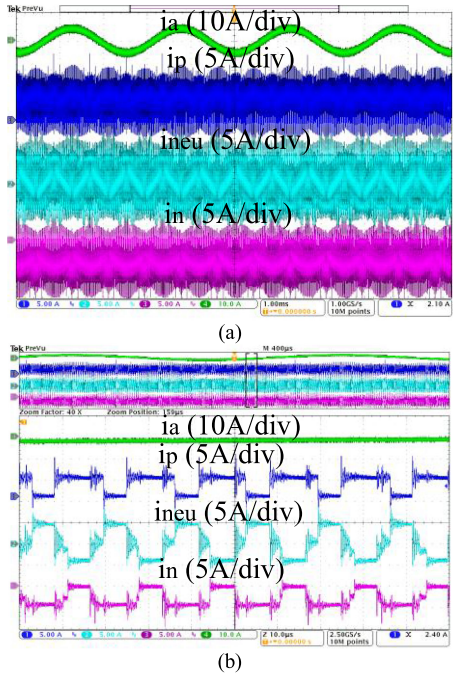


Fig. 19. DC-side input currents. (a) From top to bottom: output phase current i_a, input positive line current i_p, input neutral line current $i_{\rm neu}$, input negative line current i_n. (b) Zoom-in figure of (a) showing switching cycle waveforms.

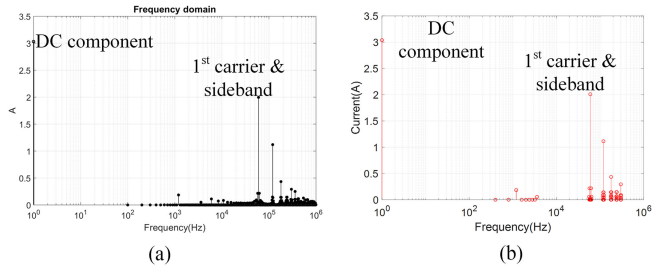


Fig. 20. Spectrum of dc-side positive line current. (a) Tested results. (b) Calculation results with developed models.

and calculated results. The calculated harmonics frequency and amplitude match well with tested results.

Fig. 19 shows the dc-side input currents waveforms including positive line current i_p, neutral line current $i_{\rm neu}$, and negative line current i_n. The definition of the currents is the same as shown in Fig. 4(b). Fig. 20(a) and (b) shows the tested positive line current spectrum and the calculated spectrum with the developed model, respectively. Fig. 21(a) and (b) shows the tested neutral line current spectrum and calculated spectrum with the developed model, respectively. The negative line current spectrum is the same as the positive line current.

Table III summarizes the main components comparison between tested results and calculated results. The calculated harmonics frequency and amplitude match well with tested results, and verifies the aforementioned dc-side current harmonic characteristics analysis.

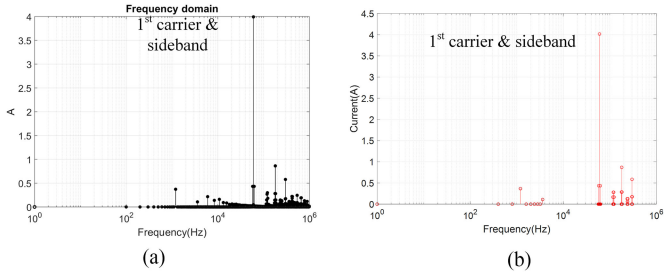


Fig. 21. Spectrum of dc-side neutral line current. (a) Tested results. (b) Calculation results with developed models.

TABLE III
COMPARISON OF MAIN COMPONENTS OF DC-SIDE LINE CURRENT

Harmonics/A	DC	$3f_0$	f_c	$f_c \pm 6f_0$	$2f_c$	$2f_c \pm 3f_0$
i_p tested	3.16	0.21	2.1	0.19	1.2	0.18
i_p calculated	3.02	0.18	2	0.22	1.1	0.15
i_{neu} tested	0	0.41	4.2	0.39	0	0.36
i_{neu} calculated	0	0.36	4.04	0.44	0	0.3

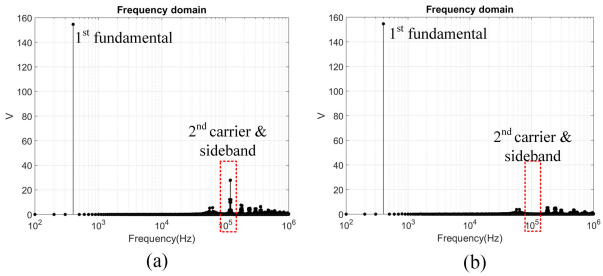


Fig. 22. Spectrum of the line voltage V_{ab} at $M = 0.9$. (a) 0° interleaving angle. (b) 90° interleaving angle.

TABLE IV
LINE VOLTAGE WTHD0 AT VARIOUS MODULATION INDEXES AND INTERLEAVING ANGLES

WTHD0 (%)	M=0.9	M=0.4
γ=0°	0.12	0.14
γ=90°	0.036	0.051
γ=180°	0.108	0.114

B. Impact of Interleaving on AC and DC Harmonics

The line voltage of paralleled inverters is measured with different modulation indexes and different interleaving angles. Fig. 22 shows the spectrum of measured line voltage harmonics with 0° and 90° interleaving angles, all at the condition $M = 0.9$. Table IV summarizes the WTHD0 of tested ac line voltage at different modulation indexes and interleaving angles. Minimum WTHD0 is achieved when interleaving angle is around 90°.

The dc-side currents are measured with different modulation indexes, different interleaving angles, and different power factors. Fig. 23 shows the dc-side input current waveforms with 0° and 180° interleaving angle, all at the condition $M = 0.9$. With the *RL* load ($R = 20\ \Omega$, $L = 320\ \mu$H for each phase), the power factor is nearly PF = 1. In Fig. 23, ringing can be observed in the switching cycle PWM waveforms. This is because the leads between the dc-link capacitor and switch phase leg are purposely increased for measuring input current. The ringing frequency is above megahertz and will not impact the switching frequency harmonic characteristics.

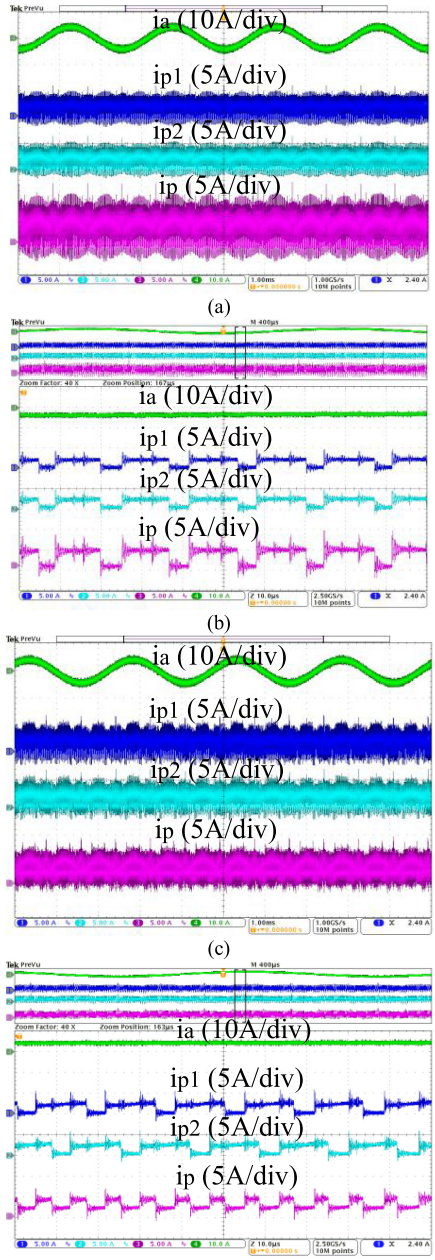


Fig. 23. DC-side current waveforms at $M = 0.9$ and PF = 1. From top to bottom: output phase current i_a, input positive line current of inverter $\#1 i_{p1}$, input positive line current of inverter $\#2 i_{p2}$, and total input positive line current i_p. (a) 0° interleaving angle. (b) Zoom-in figures of (a) showing switching cycle waveforms. (c) 180° interleaving angle. (d) Zoom-in figure of (c) showing switching cycle waveforms.

Fig. 24 shows the spectrum of positive line current harmonics. With 180° interleaving angle, the dominant components—the first carrier frequency and sideband harmonics—are eliminated. Because the high frequency components of i_p will go through dc-link capacitor C_1, around 180° interleaving angle eliminates dominant high frequency components and achieves minimum rms ripple current in capacitor C_1.

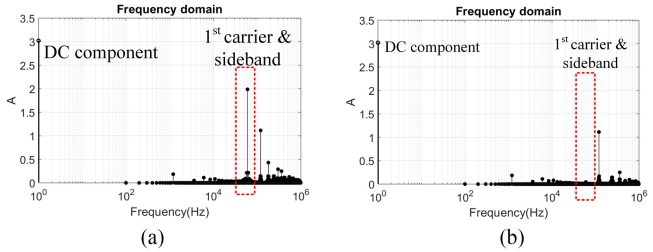


Fig. 24. Spectrum of the positive line current i_p at $M = 0.9$ and PF $= 1$. (a) 0° interleaving angle. (b) 180° interleaving angle.

TABLE V
DC-LINK CAPACITOR HIGH FREQUENCY CURRENT RMS VALUE WITH DIFFERENT MODULATION INDEXES AND INTERLEAVING ANGLES (PF $= 1$)

Capacitor high frequency current RMS (A)	M=0.9	M=0.4
γ=0°	1.76 (100%)	0.83(100%)
γ=90°	1.15 (65%)	0.51(61%)
γ=180°	0.79 (45%)	0.34 (41%)

Table V summarizes the dc-link capacitor high frequency current rms value at different modulation indexes and interleaving angles, all at power factor PF $= 1$. Different from the two-level inverter case, the minimum dc-link capacitor ripple current rms value can be achieved when the interleaving angle is around 180°.

To verify the analysis with a low power factor case, the *RL* load is changed to *L* load ($R = 0\ \Omega$, $L = 320\ \mu$H for each phase), and the fundamental frequency is increased to 3 kHz and dc voltage reduced to 100 V to limit the output current level. In this case, the power factor is PF $= 0$. Fig. 25 shows the dc-side input current waveforms with 0° and 90° interleaving angle, all at the condition $M = 0.9$.

Fig. 26 shows the spectrum of positive line current harmonics. With 90° interleaving angle, the dominant components—the second carrier frequency and sideband harmonics—are significantly reduced. It can be observed that the second carrier and sideband harmonics are not eliminated. This is because the ratio between the carrier frequency and fundamental frequency (60 kHz/3 kHz) is low in this case and the sidebands of the first carrier frequency harmonic overlap with the sidebands of the second carrier frequency harmonic.

Table VI summarizes the dc-link capacitor high frequency current rms value at different modulation indexes and interleaving angles, all at power factor PF $= 0$. In this case, the minimum dc-link capacitor ripple current rms value can be achieved when the interleaving angle is around 90°. This trend matches the conclusion in aforementioned analysis.

C. Impact of Interleaving on EMI Harmonics

EMI noise currents of the paralleled inverter system are measured with the EMI test receiver and RF probe following DO-160 standards. The operation condition is the same as previous. *RL* load is used. A 1-nF capacitor and a 100-Ω damping resistor are added between the three-phase *RL* load neutral point and ground to model the stray capacitance.

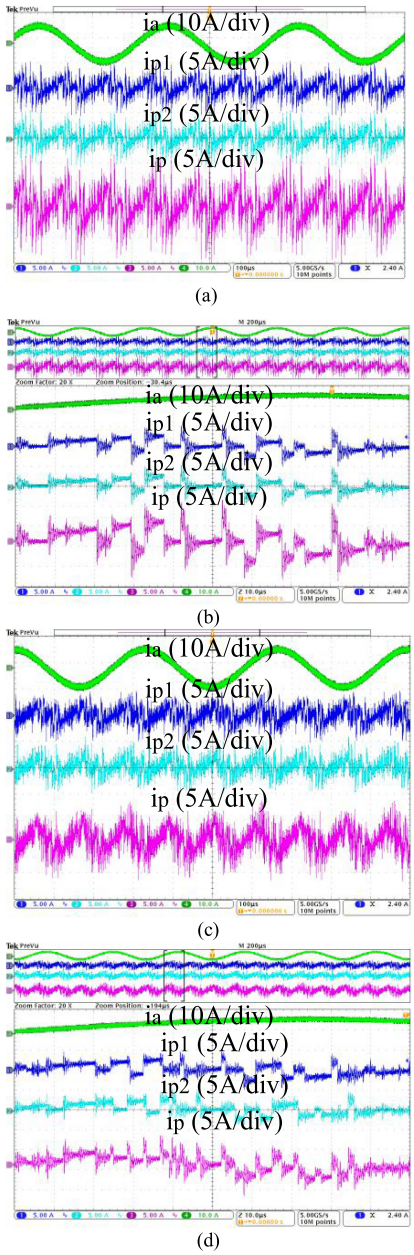


Fig. 25. DC-side current waveforms at $M = 0.9$ and PF $= 0$. From top to bottom: output phase current i_a, input positive line current of inverter $\#1$ i_{p1}, input positive line current of inverter $\#2$ i_{p2}, and total input positive line current i_p. (a) 0° interleaving angle. (b) Zoom-in figure of (a) showing switching cycle waveforms. (c) 90° interleaving angle. (d) Zoom-in figure of (c) showing switching cycle waveforms.

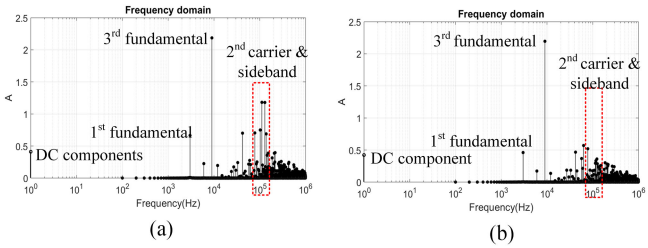


Fig. 26. Spectrum of the positive line current i_p at $M = 0.9$ and PF $= 0$. (a) 0° interleaving angle. (b) 90° interleaving angle.

TABLE VI
DC-LINK CAPACITOR HIGH FREQUENCY CURRENT RMS VALUE WITH DIFFERENT MODULATION INDEXES AND INTERLEAVING ANGLES (PF = 0)

Capacitor high frequency current RMS (A)	M=0.9	M=0.4
γ=0°	2.04 (100%)	0.72(100%)
γ=90°	0.93 (46%)	0.38(51%)
γ=180°	1.65 (81%)	0.49 (68%)

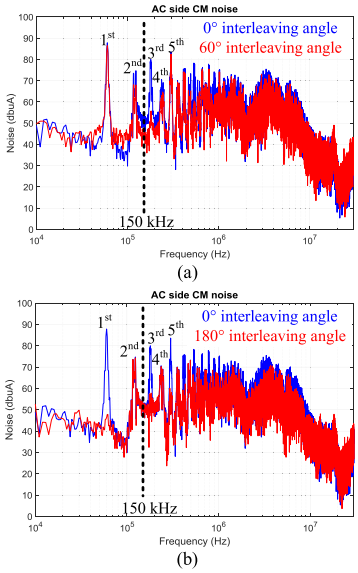


Fig. 27. Measured ac-side CM noise at different interleaving angles and their comparison with 0° interleaving angle. (a) 60° interleaving angle. (b) 180° interleaving angle.

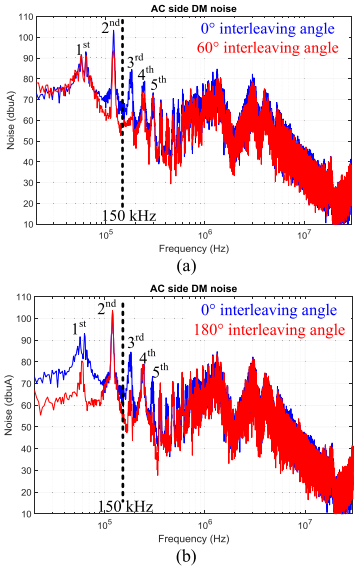


Fig. 28. Measured ac-side DM noise at different interleaving angles and their comparison with 0° interleaving angle. (a) 60° interleaving angle. (b) 180° interleaving angle.

EMI noise currents are measured at different interleaving angles. Figs. 27 and 28 show the measured ac-side CM noise and DM noise at several typical interleaving angles and their comparison with 0° interleaving angle, respectively. Different interleaving angles will reduce different carrier harmonics. For example, in Fig. 27(a), the 60° interleaving angle eliminates

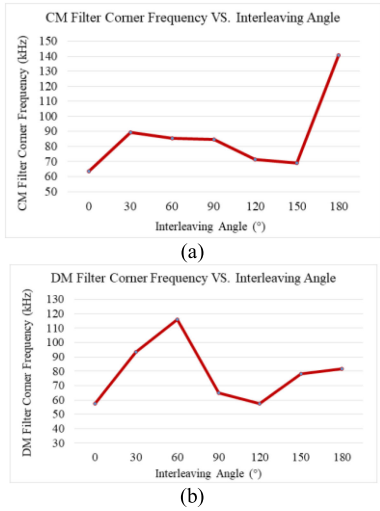


Fig. 29. EMI filter corner frequency versus interleaving angles. (a) CM filter. (b) DM filter.

the third carrier harmonics and reduces the second and the fourth carrier harmonics by half. With the measured EMI bare noises, EMI filter corner frequency can be determined. Fig. 29 summarizes the CM filter corner frequency and DM filter corner frequency at different interleaving angles when one stage filter is assumed. The trends match the conclusion in the aforementioned analysis. With 60-kHz switching frequency, CM filter corner frequency peak is achieved when the interleaving angle is around 180°, and the second optimal interleaving angle range is 30°–90°. The DM filter corner frequency peak is obtained when interleaving angle range is around 30°–60°, and the second optimal interleaving angle range is around 120°–180°.

VI. CONCLUSION

This article presents the modeling and reduction of harmonics in paralleled and interleaved three-level NPC inverters with SVM. First, the analytical models for the harmonics calculation of three-level NPC inverter with SVM are developed, and the unique dc-link current harmonics characteristic of the NPC inverter are identified. Accuracy of the models is experimentally verified.

Second, the impact of interleaving angle on ac- and dc-side harmonics is comprehensively studied. The optimal interleaving angle to reduce dc-link capacitor high frequency current ripple is derived and experimentally verified, which is highly dependent on power factor and modulation index and different from the two-level inverter case. For example, at high modulation index, optimal interleaving angle range is around 180° and around 90° for high power factor and low power factor, respectively. However, in the two-level inverter, the conclusion is opposite—the optimal interleaving angle range is around 90° and around 180° for high power factor and low power factor, respectively.

Third, the impact of switching frequency and interleaving angle on EMI harmonics is analytically studied. The optimal interleaving angle ranges for CM filter and DM filter corner frequency are also derived and experimentally verified, which

are highly dependent on switching frequency. For example, with 60-kHz switching frequency, around 180° and 30°–90° interleaving angle ranges are preferred for CM filter, and 30°–60° and 120°–180° interleaving angle ranges are preferred for DM filter.

APPENDIX

See Tables VII and VIII.

TABLE VII
DOUBLE FOURIER INTEGRAL LIMITS IN REGION 2 (SECTORS I, II, III)

y_s	y_e	x_r	x_f	$f(x,y)$
0	θ_1	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	$\frac{V_{dc}}{2}$
θ_1	$\frac{\pi}{6}$	$-\pi(\frac{3}{2}Mcosy-\frac{1}{2})$	$\pi(\frac{3}{2}Mcosy-\frac{1}{2})$	$\frac{V_{dc}}{2}$
$\frac{\pi}{6}$	θ_2	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right)+\frac{1}{2})$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right)+\frac{1}{2})$	$\frac{V_{dc}}{2}$
θ_2	$\frac{\pi}{3}$	$-\pi(\frac{3}{2}Mcosy)$	$\pi(\frac{3}{2}Mcosy)$	$\frac{V_{dc}}{2}$
$\frac{\pi}{3}$	$\frac{\pi}{3}+\theta_1$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$\frac{V_{dc}}{2}$
$\frac{\pi}{3}+\theta_1$	$\frac{\pi}{2}$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right)+\frac{1}{2})$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right)+\frac{1}{2})$	$\frac{V_{dc}}{2}$
$\frac{\pi}{2}$	$\frac{\pi}{3}+\theta_2$	$-\pi$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right)+\frac{1}{2})$	$-\frac{V_{dc}}{2}$
		$\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right)+\frac{1}{2})$	π	
$\frac{\pi}{3}+\theta_2$	$\frac{2\pi}{3}$	$-\pi$	$-\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	$-\frac{V_{dc}}{2}$
		$\pi(1+\frac{3}{2}Mcosy)$	π	
$\frac{2\pi}{3}$	$\frac{2\pi}{3}+\theta_1$	$-\pi$	$-\pi(1+\frac{3}{2}Mcosy)$	$-\frac{V_{dc}}{2}$
		$\pi(1+\frac{3}{2}Mcosy)$	π	
$\frac{2\pi}{3}+\theta_1$	$\frac{5\pi}{6}$	$-\pi$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right)+\frac{1}{2})$	$-\frac{V_{dc}}{2}$
		$\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right)+\frac{1}{2})$	π	
$\frac{5\pi}{6}$	$\frac{2\pi}{3}+\theta_2$	$-\pi$	$-\pi(\frac{3}{2}Mcosy+\frac{3}{2})$	$-\frac{V_{dc}}{2}$
		$\pi(\frac{3}{2}Mcosy+\frac{3}{2})$	π	
$\frac{2\pi}{3}+\theta_2$	π	$-\pi$	$-\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$-\frac{V_{dc}}{2}$
		$\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	π	

TABLE VIII
DOUBLE FOURIER INTEGRAL LIMITS IN REGION 1 (SECTORS I, II, III)

y_s	y_e	x_r	x_f	$f(x,y)$
0	$\frac{\pi}{6}$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	$\frac{V_{dc}}{2}$
$\frac{\pi}{6}$	$\frac{\pi}{3}$	$-\pi(\frac{3}{2}Mcosy)$	$\pi(\frac{3}{2}Mcosy)$	$\frac{V_{dc}}{2}$
$\frac{\pi}{3}$	$\frac{\pi}{2}$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$\frac{V_{dc}}{2}$
$\frac{\pi}{2}$	$\frac{2\pi}{3}$	$-\pi$	$-\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	$-\frac{V_{dc}}{2}$
		$\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	π	
$\frac{2\pi}{3}$	$\frac{5\pi}{6}$	$-\pi$	$-\pi(1+\frac{3}{2}Mcosy)$	$-\frac{V_{dc}}{2}$
		$\pi(1+\frac{3}{2}Mcosy)$	π	
$\frac{5\pi}{6}$	π	$-\pi$	$-\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$-\frac{V_{dc}}{2}$
		$\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	π	

REFERENCES

[1] R. Chen *et al.*, "Analytical analysis of AC and DC side harmonics of three-level active neutral point clamped inverter with space vector modulation," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2019, pp. 112–119.

[2] S. Bernet, "Recent developments of high power converters for industry and traction applications," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1102–1117, Nov. 2000.

[3] A. Nabea, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

[4] S. Kouro *et al.*, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[5] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Piscataway, NJ, USA: IEEE Press, 2003.

[6] M. Bierhoff and F. W. Fuchs, "DC link harmonics of three phase voltage source converters influenced by the pulse width modulation strategy—An analysis," in *Proc. 31st Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2005, pp. 491–496.

[7] B. P. McGrath and D. G. Holmes, "A general analytical method for calculation inverter dc-link current harmonics," *IEEE Trans. Ind. Appl.*, vol. 45, no. 5, pp. 1851–1859, Sep./Oct. 2009.

[8] D. Zhang, F. Wang, R. Burgos, R. Lai, T. Thacker, and D. Boroyevich, "Interleaving impact on harmonic current in dc and ac passive components for paralleled three-phase voltage-source converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2007, pp. 219–225.

[9] D. Zhang, F. Wang, R. Burgos, R. Lai, and D. Boroyevich, "Impact of interleaving on ac passive components of paralleled three-phase voltage-source converters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1042–1054, May/Jun. 2010.

[10] D. Zhang, F. Wang, R. Burgos, R. Lai, and D. Boroyevich, "DC-link ripple current reduction for paralleled three-phase voltage-source converters with interleaving," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1741–1753, Jun. 2011.

[11] L. Asiminoaei, E. Aeloiza, J. H. Kim, and P. Enjeti, "Parallel interleaved inverters for reactive power and harmonic compensation," in *Proc. IEEE Power Electron. Spec. Conf.*, 2006, pp. 1–7.

[12] L. Asiminoaei, E. Aeloiza, J. H. Kim, and P. Enjeti, "An interleaved active power filter with reduced size of passive components," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2007, pp. 219–225.

[13] S. K. T. Miller, T. Beechner, and J. Sun, "A comprehensive study of harmonic cancellation effects in interleaved three-phase VSCs," in *Proc. IEEE Power Electron. Spec. Conf.*, 2007, pp. 29–35.

[14] T. Beechner and J. Sun, "Harmonic cancellation under interleaved PWM with harmonic injection," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 1515–1520.

[15] Z. Quan and Y. Li, "Impact of carrier phase shift PWM on the dc link current of single and interleaved three-phase voltage source converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2017, pp. 3851–3855.

[16] N. Pratibha and S. Srinivas, "Spectral analysis of SPWM controlled cascaded three-level inverter drive," in *Proc. IEEE Region 10 Conf.*, Nov. 2016, pp. 697–702.

[17] I. Dolguntseva, R. Krishna, D. E. Soman, and M. Leijon, "Contour-based dead-time harmonic analysis in a three-level neutral-point-clamped inverter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 203–210, Jan. 2015.

[18] K. Song, M. Wu, V. G. Agelidis, and H. Wang, "Line current harmonics of three-level neutral-point-clamped electric multiple unit rectifiers: Analysis, simulation and testing," *IET Power Electron.*, vol. 7, no. 7, pp. 1850–1858, 2014.

[19] Y. Jiao, F. C. Lee, and S. Lu, "Space vector modulation for three-level NPC converter with neutral point voltage balance and switching loss reduction," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5579–5591, Oct. 2014.

[20] X. Zhang, D. Boroyevich, R. Burgos, P. Mattavelli, and F. Wang, "Evaluation of alternative modulation schemes for three-level neutral-point-clamped three-phase inverters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 2131–2138.

[21] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 637–641, Mar./Apr. 2001.

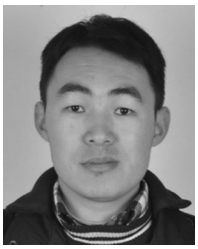
[22] H.-J. Kim, H.-D. Lee, and S.-K. Sul, "A new PWM strategy for common-mode voltage reduction in neutral-point-clamped inverter-fed ac motor drives," *IEEE Trans. Ind. Appl.*, vol. 37, no. 6, pp. 1840–1845, Nov./Dec. 2001.

[23] H. Zhang, A. Jouanne, S. Dai, A. K. Wallace, and F. Wang, "Multilevel inverter modulation schemes to eliminate common-mode voltages," *IEEE Trans. Ind. Appl.*, vol. 36, no. 6, pp. 1645–1653, Nov./Dec. 2000.

[24] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, Toronto, ON, Canada, vol. 2, 1993, pp. 965–970.

[25] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 242–249, Mar. 2000.

[26] J. Pou, R. Pindado, D. Boroyevich, and P. Rodriguez, "Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 6, pp. 1582–1588, Dec. 2005.
[27] R. Lai *et al.*, "A systematic topology evaluation methodology for high-density three-phase PWM AC-AC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2665–2680, Nov. 2008
[28] F. Luo, D. Boroyevich, P. Mattavelli, and X. Zhang, "On discussion of switching frequency impacts on dc-fed motor drive EMI filter design," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 623–627.
[29] L. Xing and J. Sun, "Motor drive system EMI reduction by asymmetric interleaving," in *Proc. IEEE 12th Workshop Control Model. Power Electron.*, 2010, pp. 1–77.
[30] F. Shih, D. Chen, Y. Wu, and Y. Chen, "A procedure for designing EMI filters for AC line applications," *IEEE Trans. Power Electron.*, vol. 11, no. 1, pp. 170–181, Jan. 1996.
[31] *Environment Conditions and Test Procedures for Airborne Equipment*, RTCA, Incorporated, RTCA/DO-160E, Dec. 9, 2004.
[32] F. Luo *et al.*, "Analysis of CM volt-second influence on CM inductor saturation and design for input EMI filters in three-phase dc-fed motor drive system," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1905–1914, Jul. 2010.
[33] R. Chen *et al.*, "Common-mode inductor saturation analysis and design optimization based on spectrum concept," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2018, pp. 2583–2588.
[34] F. Luo, D. Dong, D. Boroyevich, P. Mattavelli, and S. Wang, "Improving high-frequency performance of an input common mode EMI filter using an impedance-mismatching filter," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5111–5115, Jul. 2014.

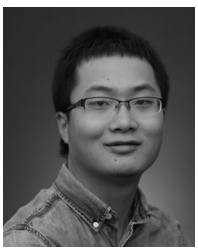


Ruirui Chen (S'15) received the B.S. degree from the Huazhong University of Science and Technology, Wuhan, China, in 2010, and the M.S. degree from Zhejiang University, Hangzhou, China, in 2013. He is currently working toward the Ph.D. degree with The University of Tennessee, Knoxville, TN, USA.

From 2013 to 2015, he was an Electrical Engineer with FSP-Powerland Technology Inc., China. His research interests include high power density converters for aircraft applications, multilevel converters, pulsewidth modulation techniques, converter paralleling control, and conducted electromagnetic interference.

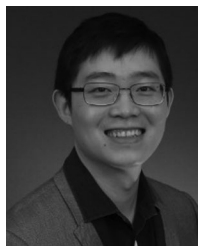
Jiahao Niu (S'16) received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2016, and is currently working toward the Ph.D. degree with The University of Tennessee, Knoxville, TN, USA.

His current research interests include design and control of high power ac drives, modular multilevel converters, and wide bandgap semiconductors and their applications.



Handong Gui (S'14) received the B.S. and M.S. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2013 and 2016, respectively, and is currently working toward the Ph.D. degree with The University of Tennessee, Knoxville, TN, USA.

His research interests include wide band-gap devices and applications, multilevel converters, and electrified transportation.



Zheyu Zhang (S'12–M'15–SM'19) received the B.S. and M.S. degrees from the Huazhong University of Science and Technology, Wuhan, China, in 2008 and 2011, respectively, and the Ph.D. degree from The University of Tennessee, Knoxville, TN, USA, in 2015, all in electrical engineering.

He is the Warren H. Owen–Duke Energy Assistant Professor of engineering with Clemson University, North Charleston, SC, USA. He was a Research Assistant Professor with the Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, from 2015 to 2018. Afterward, he joined General Electric Research as the Lead Power Electronics Engineer with Niskayuna, NY, USA, from 2018 to 2019. He has authored or coauthored more than 80 papers in the most prestigious journals and conference proceedings, filed more than ten patent applications with one licensed, authored one book and one book chapter, and presented four IEEE tutorial seminars. His research interests include wide band-gap-based power electronics, modularity and scalability technology, medium-voltage power electronics, advanced manufacturing and cooling technology (e.g., cryogenic cooling) applied in power electronics, and highly efficient, ultradense, cost-effective power conversion systems for electric propulsion, electrified transportation, renewables, energy storage, and grid applications.

Dr. Zhang is currently an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS. He was the recipient of two Prize Paper Awards from the IEEE Industry Applications Society and IEEE Power Electronics Society.

Fei (Fred) Wang (S'85–M'91–SM'99–F'10) received the B.S. degree from Xi'an Jiaotong University, Xi'an, China, in 1982, and the M.S. and Ph.D. degrees from the University of Southern California, Los Angeles, CA, USA, in 1985 and 1990, respectively, all in electrical engineering.

He was a Research Scientist with the Electric Power Lab, University of Southern California, from 1990 to 1992. He joined the GE Power Systems Engineering Department, Schenectady, NY, USA, as an Application Engineer in 1992. From 1994 to 2000, he was a Senior Product Development Engineer with GE Industrial Systems, Salem, VA, USA. During 2000 to 2001, he was the Manager of Electronic & Photonic Systems Technology Lab, GE Global Research Center, Schenectady and Shanghai, China. In 2001, he joined the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, VA, USA, as a Research Associate Professor and became an Associate Professor in 2004. From 2003 to 2009, he also served as the CPES Technical Director. Since 2009, he has been with The University of Tennessee and Oak Ridge National Lab, Knoxville, TN, USA, as a Professor and the Condra Chair of Excellence in Power Electronics. His research interests include power electronics and power systems.

Dr. Wang is a Founding Member and the Technical Director of the Multiuniversity National Science Foundation/Department of Energy Engineering Research Center for Ultra-Wide-Area Resilient Electric Energy Transmission Networks led by The University of Tennessee. He is a Fellow of the U.S. National Academy of Inventors.

Leon M. Tolbert (S'88–M'91–SM'98–F'13) received the bachelor's, M.S., and Ph.D. degrees in electrical engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 1989, 1991, and 1999, respectively.

He was with Oak Ridge National Laboratory, Oak Ridge, TN, USA, from 1991 until 1999. He was appointed as an Assistant Professor with the Department of Electrical and Computer Engineering, The University of Tennessee, Knoxville, TN, in 1999. He is currently the Min H. Kao Professor with the Min H. Kao Department of Electrical Engineering and Computer Science, The University of Tennessee. He is also a Part-Time Senior Research Engineer with the Power Electronics and Electric Machinery Research Center, Oak Ridge National Laboratory.

Dr. Tolbert is a Founding Member for the National Science Foundation/Department of Energy Research Center, Center for Ultra-Wide-Area Resilient Electric Energy Transmission Networks. He is a Registered Professional Engineer in the state of Tennessee. He was an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2007 to 2013. He was elected to serve as a Member-at-Large to the IEEE Power Electronics Society Advisory Committee for 2010–2012, Chair of the Power Electronics Society (PELS) Membership Committee from 2011 to 2012, and a member of the PELS Nominations Committee from 2012 to 2014. He was the Paper Review Chair for the Industry Power Converter Committee of the IEEE Industry Applications Society from 2014 to 2017. He was the recipient of the 2001 IEEE Industry Applications Society Outstanding Young Member Award and six Prize Paper Awards from the IEEE Industry Applications Society and IEEE Power Electronics Society.

Daniel J. Costinett (S'10–M'13–SM'18) received the Ph.D. degree in electrical engineering from the University of Colorado Boulder, Boulder, CO, USA, in 2013.

He is currently an Associate Professor with the Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville (UTK), TN, USA. Prior to joining UTK, he was an Instructor with Utah State University, Logan, UT, USA, in 2012. He is also a Joint Faculty with the Power Electronics and Electric Machinery Research Group, Oak Ridge National Laboratory, Oak Ridge, TN. His research interests include resonant and soft-switching power converter design, high efficiency wired and wireless power supplies, on-chip power conversion, medical devices, and electric vehicles.

Dr. Costinett is currently the Co-Director of Education and Diversity for the National Science Foundation/Department of Energy Research Center for Ultra-Wide-Area Resilient Electric Energy Transmission Networks. He currently serves as an Associate Editor for IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS and IEEE TRANSACTIONS ON POWER ELECTRONICS. He was a recipient of the National Science Foundation CAREER Award in 2017.

Benjamin J. Blalock (S'86–M'97–SM'06) received the B.S. degree from The University of Tennessee (UT), Knoxville, TN, USA, in 1991, and the M.S. and Ph.D. degrees from the Georgia Institute of Technology, Atlanta, GA, USA, in 1993 and 1996, respectively, all in electrical engineering.

He is the Blalock-Kennedy-Pierce Professor of analog electronics with the Department of Electrical Engineering and Computer Science, UT, where he directs the Integrated Circuits and Systems Laboratory. He has coauthored more than 200 refereed papers. He was an Analog IC Design Consultant for Cypress Semiconductor, Concorde Microsystems, Global Power Electronics, and Siart. His research interests at UT include analog/mixed-signal integrated circuit design for extreme environments (both wide temperature and radiation) across multiple semiconductor technologies, ultralow power analog signal processing, multichannel monolithic instrumentation systems, mixed-signal/mixed-voltage circuit design for systems on a chip, and gate drive integrated circuits for wide bandgap (SiC and GaN) power electronics.

Benjamin B. Choi received the B.S., M.S., and Ph.D. degrees from the University of Illinois, Champaign, IL, USA, in 1984, 1986, and 1990, respectively.

Since joining NASA Glenn Research Center, Cleveland, OH, USA, in 1990, he has been working on structural dynamics system modeling, analysis, and control, especially in vibration control using magnetic bearing system and artificial intelligence technology for nearly 12 years. Since then, he started looking at the development of a bearingless motor technology for the electric propulsion system for future aircraft and NASA missions. He had also extended his research view into suppressing blade resonance using piezoelectric materials or shape memory alloy. During the last ten years, he was involved in the propulsion electric grid simulator for future turboelectric distributed propulsion aircraft.