Composite DC Power Flow Controller

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***Abstract*—The utilization of a dc power flow controller in multiterminal HVDC (MTDC) can increase the control dimension of dc power flow, by which both the active power distribution capability and coordination control performance can be enhanced in MTDC. In this article, a novel concept of "composite dc power flow controller (CDCPFC)" has been proposed, and the general construction principles of technical frame have been given for function description. A specific CDCPFC topology has been implemented, which is featured with a straightforward dc–dc power conversion path via a transformerless structure. The operation principle, circuit characteristics, and control strategy of the proposed CDCPFC are analyzed in detail. Both simulation and experimental results proved that the proposed topology could realize power flow control function of two individual lines under various conditions with a good application prospect.**

***Index Terms*—Composite dc power flow controller (CDCPFC), dc power flow, dc power flow controller, multiterminal HVDC (MTDC).**

I. Introduction

With the rapid development of large-scale photovoltaic power plants/wind farms, the advanced high-voltage dc (HVDC) transmission technology has drawn great attention from both academia and industry. HVDC transmission with the advantages of long transportation distance and flexible operation has become a hotspot in the field of smart grid [1]–[4]. Compared with the two-terminal HVDC transmission system, the multiterminal HVDC system (MTDC) is more economical and flexible to solve the problems of large-scale renewable energy integration, large-capacity long-distance power transmission and transmission corridor shortage, and other issues. The converter station with the voltage source converter (VSC) technology can effectively control the input power into the MTDC system, whereas the power flow of each dc line is passively determined by its own line resistance [5]–[11].

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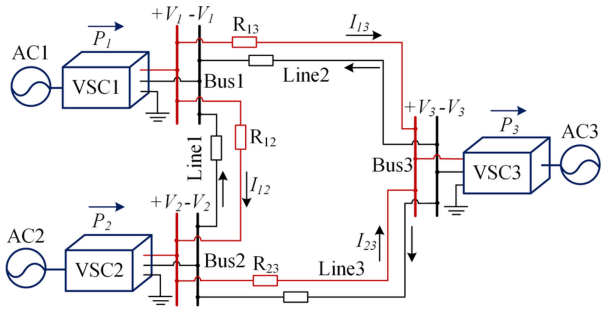

Fig. 1. Three-terminal ring-type dc grid.

The factors that determine the power flow in the dc grid are only the line resistance and the terminal dc voltage. Therefore, the power flow distribution of a given dc grid can only be changed by adjusting the line resistance and the terminal dc voltage. As shown in Fig. 1, the converter stations VSC1 and VSC2 inject power into a three-terminal ring-type dc grid, and they can be regarded as constant power sources. The converter station VSC3 plays the role as a constant voltage source, and it will output the power. Only by adjusting the output power of VSC1 and VSC2, the precise power flow control function can be realized for three individual lines. Consequently, a novel technology concept, a dc power flow controller (DCPFC), has been introduced to obtain the precise power flow control function in the dc grid.

DCPFC can be divided into resistance and voltage types [12]. Since a new equivalent line resistance is inserted by variable resistance as one type of the resistance-type DCPFC, it has the shortcomings of larger power losses and single-way adjustment capability [13].

From the view of topology, a voltage-type DCPFC can be divided into several different categories, including dc transformers, series adjustable voltage source (SAVS), and interline dc power flow controller (IDCPFC). The input and output sides of the dc transformer [14], [15] are connected to positive and negative transmission lines of different voltage levels, which is equivalent to an adjustable voltage source in series with the transmission line. A dc transformer has to withstand the system-level voltage with complex design and high cost. In [16] and [17], SAVS is proposed to adjust the power flow, and it can be embedded into the positive polarity line or negative polarity line. Although SAVS withstands a lower voltage level and power level, it needs an external power supply.

Without the support of any external power supply, IDCPFC [18]–[21] takes the capacitor as an energy transfer buffer to transfer partial power from one line to the other line, which can achieve power flow control capability by exchanging power

between two adjacent lines. Since IDCPFC can be equivalent to two voltage sources that are frequently put into operation and bypassed in two lines, the larger voltage and current ripples are the outstanding issues. By the inductor as the energy transfer buffer, a novel IDCPFC [22] is proposed to greatly reduce the voltage and current ripples. In [23], by the use of coupling inductors, line power flow reversal function is achieved in IDCPFC. Some developed IDCPFCs have been studied for the three-line scenario in [24] and [25], but all of them can only provide the active power flow control function for a single line.

From the view of the control performance, it can be seen that the main existing solutions in the MTDC system are based on the collaborative control of VSC stations and DCPFCs [26]–[28]. Multiple power flow control cannot be achieved by a single DCPFC. All above-mentioned IDCPFCs actively control the power flow of one line, whereas the other line's power flow changes passively. In other words, IDCPFCs cannot actively control the power flow of two lines simultaneously. The concept of a multiport DCPFC (MDCPFC) has been explored in [29] for the three-line scenario, which has a complex topology with a multiphase ac linkage transformer and a multiphase MMC.

Therefore, for all types of DCPFCs, there is a big improvement space for enhancing multiple dc power flow control capability in future complex MTDC scenarios.

In this article, a novel technical concept of "composite dc power flow controller (CDCPFC)" has been presented to achieve active multiple power flow control capability, which is based on several combination schemes of the existing SAVS and IDCPFC. Considering the characteristics of the energy flow path and the redundancy of the topology unit during combination, there are two composite layers in both function and topology; therefore, the proposed CDCPFC is totally different from all existing solutions. A detailed topology is, thus, given, and it is featured with a straightforward dc–dc power conversion path via a transformerless structure. With the new topology, the active control issue can, thus, be solved for two adjacent lines.

In Section II, the derivation and application of CDCPFC construction will be given, and the general functional framework of the CDCPFC is constructed. Based on the general functional framework, a novel CDCPFC topology is proposed in Section III with a detailed analysis of the corresponding decoupled control strategy for dual objectives. The simulation analysis and experimental verification results are given in Sections IV and V, respectively, and Section VI concludes this article.

II. Concept and Construction of CDCPFC

The technical concept of a CDCPFC stems from the request of two individual lines' active power flow control. For the active power flow adjustment of two lines, there should exist three operation modes.

1) Mode1: The power flow of both two lines need to be increased at the same time (*synchronous increasement mode*).
2) Mode2: The power flow of both two lines need to be decreased at the same time *(synchronous decreasement mode).*

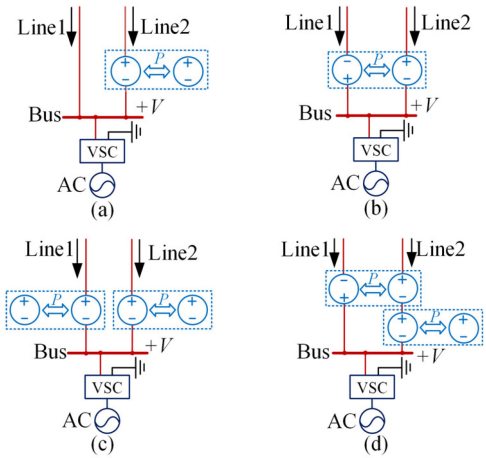

Fig. 2. Combined of DCPFC. (a) SAVS. (b) IDCPFC. (c) Combination Scheme I. (d) Combination Scheme II.

3) Mode3: The power flow of two lines will be increased and decreased, respectively (*divergent adjustment mode*).

For IDCPFC, the power flow of one line will be increased/decreased actively, whereas the power flow of the other line will be decreased/increased passively, which is regarded as a degraded divergent adjustment mode. That is, the power flow adjustment freedom of the IDCPFC cannot meet the request of two lines' free power flow control.

To cope with all kinds of possible power flow control conditions and to achieve the multiobjective dc power flow control capability, IDCPFC and SAVS can be configured by combination shown in Fig. 2. The redundant characteristics of its energy flow path and circuit topology functional unit are the basic starting point for the concept generation and topology construction of CDCPFC.

Mark: SAVS and IDCPFC need to be equipped in both positive and negative polarity lines with the same devices because dc-grid system presents the dual-polarity characteristics. For positive and negative polarity lines, the installation and the configuration method of the device are the same. For the convenience of theoretical analysis, a dc-grid system is simplified to unipolar in this article (i.e., positive polarity part). Negative polarity part can be obtained in the same way according to the positive polarity part.

A. Combination of DCPFC

The conceptual diagrams of SAVS and IDCPFC are first shown in Fig. 2(a) and (b), respectively. From Fig. 2(a), it is seen that SAVS can be equivalent to one voltage source inserted into one line, which exchanges power with an external voltage source. From Fig. 2(b), it is seen that the IDCPFC can be equivalent to two voltage sources inserted into two lines, respectively, which exchanges power with each other. Only one line's power flow can be actively controlled by the IDCPFC, whereas the other line's power flow can only be controlled passively (i.e., degraded divergent adjustment mode). Thus, SAVS and IDCPFC are regarded as a single-target DCPFC.

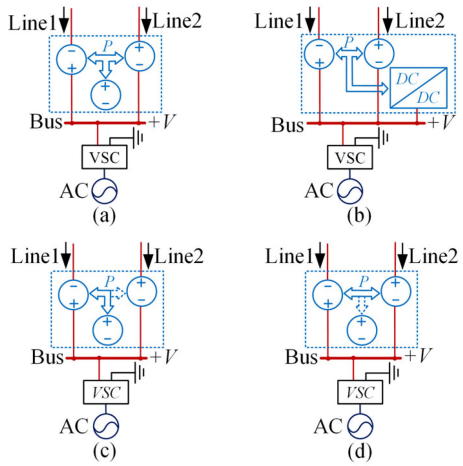

Fig. 3. General framework and function evolvement of a CDCPFC. (a) CDCPFC with an external voltage source. (b) CDCPFC with an external auxiliary circuit. (c) Degraded CDCPFC as SAVS. (d) Degraded CDCPFC as IDCPFC.

In this article, dual SAVSs will be used in combination, and it is termed Combination Scheme I, as shown in Fig. 2(c). Furthermore, single IDCPFC and single SAVS will be used in combination, and it is termed Combination Scheme II, as shown in Fig. 2(d). By combining two single-target DCPFCs in two schemes, a strong power flow control capability will be achieved for both dc lines, which means that all three above-mentioned operation modes of power flow control will be successfully realized by Combination Schemes I and II.

Compared with *Combination Scheme 1*, it is noted that *Combination Scheme II only* requires one external power source with a simpler structure and lower cost. However, in *Combination Scheme II*, more series voltage sources need to be inserted in lines. In *Combination Scheme II*, while one part is out of work, the other part can work alone.

For *Combination Scheme I* and *Combination Scheme II*, its combination mechanism means direct combination with the lack of overall combination optimization based on energy exchange path considerations. Thus, the combination scheme can be further developed, shown as follows for specific details.

B. Functional Composite Evolution Based on Combination Scheme

Considering the redundancy of equivalent voltage source in series into the line, *Combination Scheme II* can be further simplified and developed to obtain the general framework and functional evolution, as shown in Fig. 3, including the following.

1) The basic structure of the CDCPFC is termed "public external voltage source scheme of CDCPFC," as shown in Fig. 3(a). The scheme forms a T-shaped three-terminal energy exchange path between two lines. The power flow control dimension is enhanced, thereby achieving active control of the two lines' power flow.
2) If VSC plays the role of a constant voltage source in Fig. 3(a), an external auxiliary circuit can be introduced into the energy exchange path of the public external voltage source scheme. The external voltage source is replaced by an external auxiliary circuit connected with dc bus of VSC. It is termed "external auxiliary circuit scheme of CDCPFC," as shown in Fig. 3(b). Besides, the T-shaped three-terminal energy exchange path can enhance the control dimension, and the energy flow closed loop is formed with the dc bus, thereby achieving active control of the two lines' power flow.
3) If the external voltage source only exchanges energy with one line in Fig. 3(a), the three-terminal energy exchange path is simplified to the two-terminal path. That is, the SAVS function can be implemented, as shown in Fig. 3(c).
4) If two lines exchange energy with each other and do not exchange energy with the external voltage source, the three-terminal energy exchange path is simplified to the two-terminal path. Thus, the IDCPFC function can be implemented in Fig. 3(d).

As shown from the above-mentioned description in Fig. 3, the novel CDCPFC not only inherits the function of SAVS and IDCPFC, but also implements three modes of power flow control (i.e., achieve active control).

C. Performance Comparison

According to the abovementioned construction principles of CDCPFC, a brief comparison of main DCPFFCs has been given in Table I from the perspective of function and topology. From Table I, several conclusions are summarized as follows.

1) Both MDCPFC and the proposed CDCPFC have dual degrees of control freedom, and the other DCPFCs already published only have single degree of control freedom. It means only MDCPFC and CDCPFC can actively control power flow of two adjacent lines.
2) MDCPFC is realized by a hybrid ac–dc structure, and the proposed CDCPFC is realized by a straightforward dc–dc structure. The CDCPFC has the advantages of simple structure and low control complexity.
3) Due to the combination of both SAVS and IDCPFC, CDCPFC inherits the features of low cost, low power loss, and good control performance. Since there is no need to withstand the system-level voltage, CDCPFC can be introduced to MVDC and HVDC levels.

III. Specific Implementation of Topology

Based on the abovementioned general framework of CDPFC in Fig. 3, a series of novel topologies can be constructed, and all of them can provide the function of active power flow control for both lines. As shown in Fig. 4, a specific CDCPFC topology has been presented, whose topology analysis and control strategy are given in the following parts.

A. Topology Description

The equivalent circuit of the CDCPFC can be regarded as a three-port system, as shown in Fig. 4(a). The T-type energy exchange path is formed by three energy transfer ports. Port 1 and Port 2 are, respectively, indicated by $1\sim1'$ and $2\sim2'$, and they

TABLE I
PERFORMANCE COMPARISON OF DCPFCS

Type	Capability of DC power flow Control (Scenario: two adjacent lines)			Control freedom degree	Structure and control	Cost	Features
	Operation mode	I_1 (Line 1)	I_2 (Line 2)				
Variable Resistance	———	Decrease I_1 **actively**	———	1	Very Simple	Very Low	Low capacity; high loss
DC Transformer	———	Increase I_1 **actively** or decrease I_1 **actively**	———	1	Very Complex	Very High	Fault isolation; High capacity; withstand system-level voltage; high loss
Series Adjustable Voltage Source	———	Increase I_1 **actively** or decrease I_1 **actively**	———	1	Simple	Low	Need external power supply; low capacity; low loss
Interline DCPFC	Degraded Mode3	Increase I_1 **actively**	Decrease I_2 **passively**	1	Simple	Low	Low capacity; low loss;
	Degraded Mode3	Decrease I_1 **actively**	Increase I_2 **passively**	1			
Multiport DCPFC	Mode1	Increase I_1 **actively**	Increase I_2 **actively**	**2**	Very Complex	Low	Need multi-phase AC transformer and MMCs; low capacity; low loss
	Mode2	Decrease I_1 **actively**	Decrease I_2 **actively**	**2**			
	Mode3	Increase I_1 **actively**	Decrease I_2 **actively**	**2**			
Composite DCPFC	Mode1	Increase I_1 **actively**	Increase I_2 **actively**	**2**	Simple	Low	Need external power supply; low capacity; low loss
	Mode2	Decrease I_1 **actively**	Decrease I_2 **actively**	**2**			
	Mode3	Increase I_1 **actively**	Decrease I_2 **actively**	**2**			

are the interactive ports that control the lines' power flow. Both C_1 and C_2 are, respectively, embedded into line 1 and line 2. Port 3 ($3\sim3'$) is regarded as a power transfer port, usually connected with an external dc voltage source or auxiliary circuit.

As shown in Fig. 4(b), the proposed DCPFC topology consists of eight IGBTs (Q_1–Q_8), eight antiparallel diodes (D_1–D_8), five series diodes (D_{1b} to D_{5b}), one coupling inductor ($L_1 \| L_2$), two series output capacitors (C_1 and C_2) in two lines, and two bypass switches (S_1 and S_2), wherein the bidirectional switch consists of two IGBTs in parallel. The reference positive direction of each electrical quantity can be referred to Fig. 4.

When both S_1 and S_2 are closed, both C_1 and C_2 will be shorted, and the CDCPFC will be out of the normal operation (i.e., the bypass state). When both S_1 and S_2 are open, the CDCPFC will be put into operation, which has six equivalent circuits due to the switching actions of IGBTs. Considering the different directions of power flow in the lines, there are several power flow conditions. For the detailed analysis of operation principles, three typical conditions with different power flow directions and different control targets will be analyzed in the following parts.

B. Operation Principles

For the abovementioned three modes (Modes 1–3) of two lines' power flow control, the basic principles of their energy exchange paths are the same. If both Q_1/Q_2 are OFF, both V_{c1} and V_{c2} will continue to rise. Therefore, in order to keep the balance of V_{c1} and V_{c2}, it is necessary to construct an energy exchange path for transferring the capacitive energy to L_1 and L_2. Meanwhile, in order to keep the balance of I_{L1} and I_{L2}, it is necessary to construct the energy exchange path among coupling inductor, C_3, and external voltage source.

Condition 1: I_{c1} and I_{c2} are all in positive direction.

In this case, I_{c1} and I_{c2} are increased (Mode1), as an example, that is, equivalent positive dc voltage sources are in series into line 1 and line 2 (voltage directions of C_1 and C_2 shown in Fig. 5). The whole switching cycle can be divided into three

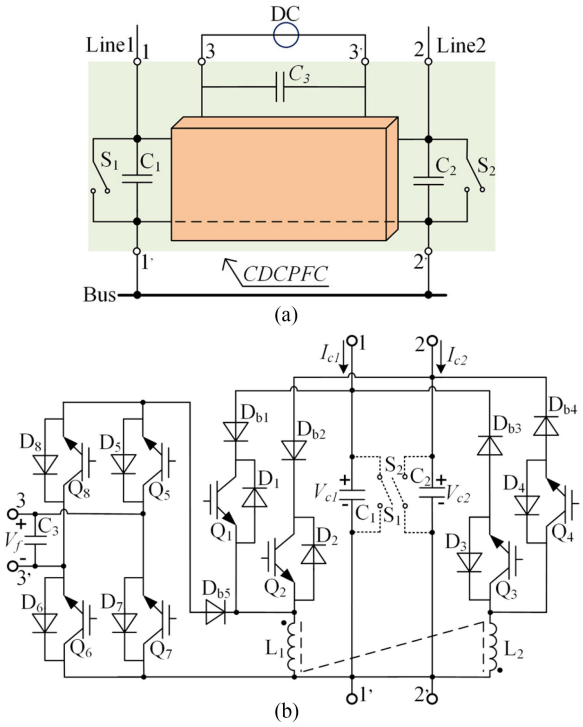

Fig. 4. Topology and configuration of CDCPFC. (a) External configuration diagram. (b) Topology.

substates during the steady-state operation, as shown in Fig. 5. A brief sketch is as follows.

1) Substate 1, first Q_1 is turned ON, C_1–L_1–Q_1–D_{b1} forms loop 1, as shown in Fig. 5(a). During the duration of this substate, L_1 transfers energy to C_1, and I_{L1} decreases linearly.
2) Substate 2, Q_1 is turned OFF/Q_2 is turned ON, then C_2–L_1–Q_2–D_{b2} forms loop 2, as shown in Fig. 5(b). During the duration of this substate, the energy is shifted from L_1 to C_2, and I_{L1} decreases linearly.
3) Substate 3, Q_2 is turned OFF/Q_5 and Q_6 are turned ON, then C_3–Q_5–D_{b5}–L_1–Q_6 forms loop 5, as shown in Fig. 5(c). During the duration of this substate, C_3 charges L_1, and I_{L1} increases linearly.

When Q_5/Q_6 are turned OFF and Q_1 is turned ON, another switching cycle begins. In this condition, only L_1 of $L_1\|L_2$ works, whereas L_2 of $L_1\|L_2$ is out of work. Q_1, Q_2, and Q_5/Q_6 are complementary to each other. Q_3, Q_4, Q_7, and Q_8 are always in the OFF state. Based on the abovementioned analysis, Q_1, Q_2, and Q_5/Q_6 need to be controlled.

Condition 2: I_{c1} and I_{c2} are all in negative directions.

Here, I_{c1} and I_{c2} are to be decreased (Mode2), as an example, that is, equivalent negative dc voltage sources are in series into line1 and line 2 (voltage directions of C_1 and C_2 are shown in Fig. 6). The whole switching cycle can be divided into three substates during the steady-state operation, as shown in Fig. 6. A brief sketch is as follows.

1) Substate 1, first open Q_3, C_1–L_2–Q_3–D_{b3} form loop 3, as shown in Fig. 6(a). During the duration of this substate, C_1 transfers energy to L_2, and I_{L2} increases linearly.

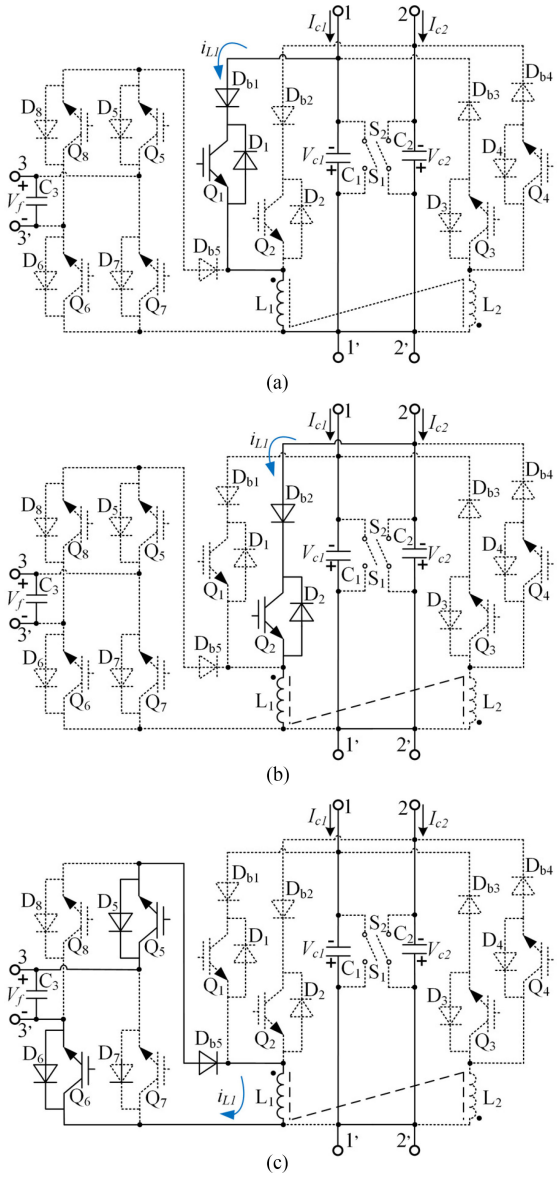

Fig. 5. Operation modes when I_{c1}/I_{c2} are in positive direction. (a) Loop 1 (only Q_1 is turned ON). (b) Loop 2 (only Q_2 is turned ON). (c) Loop 5 (only Q_5/Q_6 are turned ON).

2) Substate 2, Q_3 is turned OFF/Q_4 is turned ON, then C_2–L_2–Q_4–D_{b4} form loop 4, as shown in Fig. 6(b). During the duration of this substate, the energy is shifted from C_2 to L_2, and I_{L2} increases linearly.
3) Substate 3, Q_4 is turned OFF/Q_7 and Q_8 are turned ON, then C_3–Q_8–D_{b5}–L_1–Q_7 form loop 6, as shown in Fig. 6(c). L_2's energy is transferred to L_1 because of the coupling inductance. At this moment, the dot voltage polarity of L_1 and L_2 reverses. L_1 charges C_3, and I_{L1} decreases linearly. The energy of L_1 reaches the minimum during the switching cycle.

When substate 3 ends, substate 1 of another switching cycle begins. The energy is transferred from L_1 to L_2, and that cycle repeats. By coupling inductor, the power flow controller transfers some energy of C_1 and C_2 to C_3 to decrease I_{c1} and I_{c2}, whose specific switching mode is shown in Fig. 6. In this condition, Q_3,

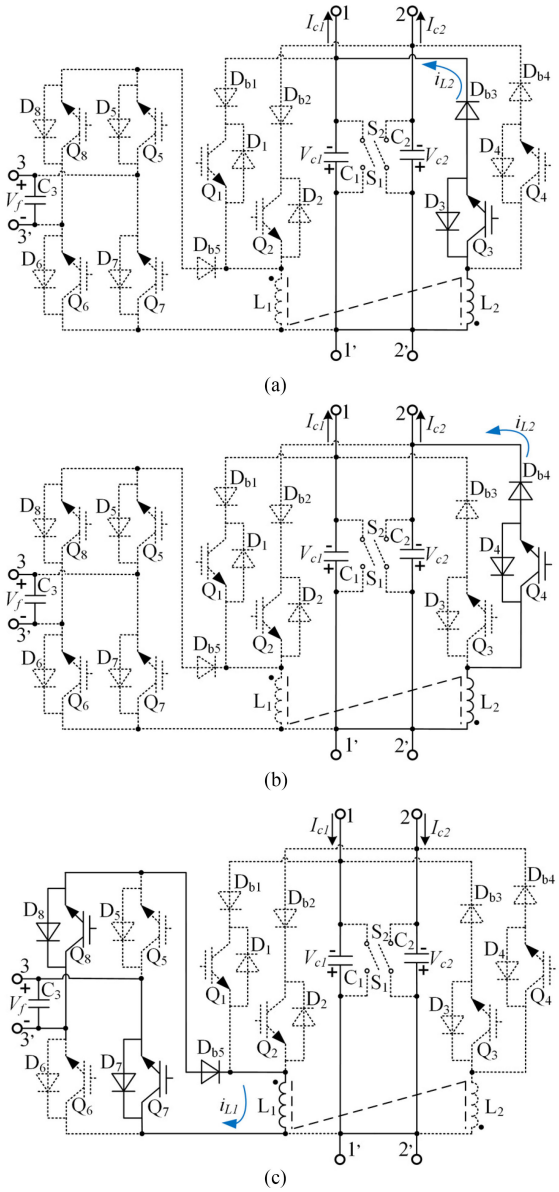

Fig. 6. Operation modes when I_{c1}/I_{c2} are in negative direction. (a) Loop 3 (only Q_3 is turned ON). (b) Loop 4 (only Q_4 is turned ON). (c) Loop 6 (only Q_7/Q_8 are turned ON).

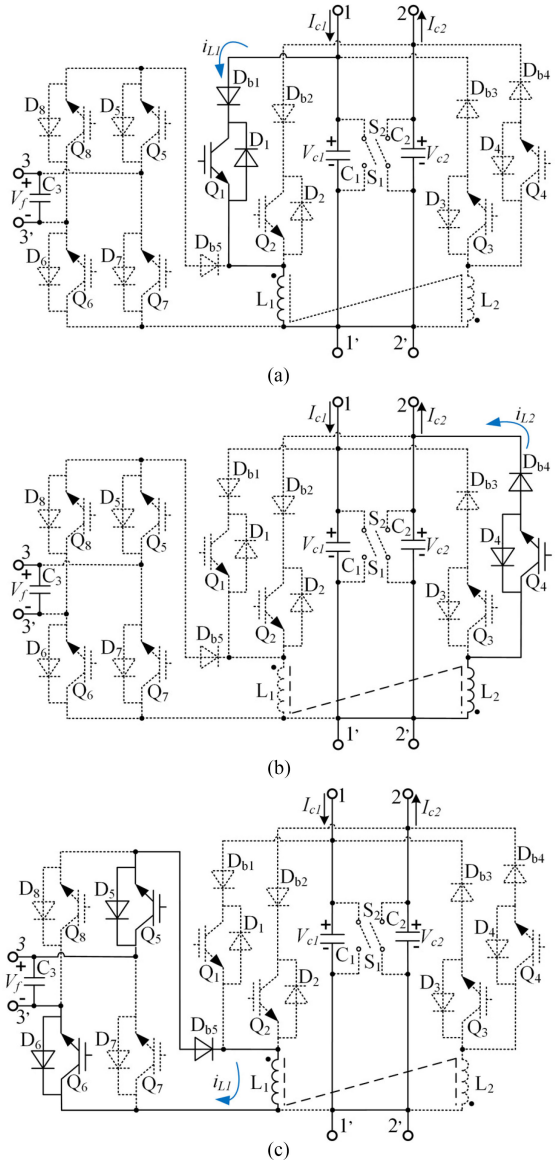

Fig. 7. Operation modes when I_{c1}/I_{c2} are in different direction. (a) Loop 1 (only Q_1 is turned ON). (b) Loop 4 (only Q_4 is turned ON). (c) Loop 5 (only Q_5/Q_6 are turned ON).

Q_4, and Q_7/Q_8 are complementary to each other. Q_1, Q_2 Q_5, and Q_6 are always in the OFF state. Based on the abovementioned analysis, Q_3, Q_4, and Q_7/Q_8 need to be controlled.

Condition 3: I_{c1} and I_{c2} are in different directions.

There are two conditions: I_{c1} is positive and I_{c2} is negative or I_{c1} is negative and I_{c2} is positive. According to the symmetry, I_{c1} is decreased and I_{c2} is increased (Mode3), as an example to illustrate the condition where I_{c1} is positive and I_{c2} is negative, that is, equivalent negative and positive dc voltage sources are in series into line1 and line 2 (voltage directions of C_1 and C_2 are shown in Fig. 7). The whole switching cycle can be divided into three substates during the steady-state operation, as shown in Fig. 7. A brief sketch is as follows.

1) Substate 1: First open Q_1, C_1–L_1–Q1–D_{b1} form loop 1, as shown in Fig. 7(a). During the duration of this substate, C_1 transfers energy to L_1, and I_{L1} increases linearly.
2) Substate 2: Q_1 is turned OFF/Q_4 is turned ON, then C_2–L_2–Q_4–D_{b4} form loop 4, as shown in Fig. 7(b). During the duration of this substate, the energy of L_1 is transferred to L_2 because of the coupling inductance. The energy is shifted from L_2 to C_2, and I_{L2} decreases linearly. If the increasing energy of L_1 in loop 1 is less than the decreasing energy of L_2 in loop 4, the decreasing energy of the inductance needs to be obtained from C_3.
3) Substate 3: Q_4 is turned OFF/Q_5 and Q_6 are turned ON, then C_3–L_1–Q_5–D_{b5}–Q_6 form loop 5 in Fig. 7(c). During the duration of this substate, L_2's energy is transferred to L_1 for the coupling inductance. C_3 charges L_1, and I_{L1} increases linearly. Otherwise, if the increasing energy of L_1 in loop 4 is more than the decreasing energy of L_2 in loop 4. L_1 charges C_3, and Q_7/Q_8 need to turn ON and I_{L1} decreases linearly in Fig. 6(c). When Q_5/Q_6 are

TABLE II
OPERATING STATUS OF CDCPFC

I_{c1}/I_{c2} direction	I_{c1}/I_{c2} control targets	V_x/V_y polarity	Controlled switching device	case
+/+	↑/↑	-/-	Q_1, Q_2, Q_5/Q_6	1
	↓/↓	+/+	Q_1, Q_2, Q_7/Q_8	2
	↑/↓	-/+	Q_1, Q_2, Q_5/Q_6 orQ_7/Q_8	3
	↓/↑	+/-	Q_1, Q_2, Q_5/Q_6 orQ_7/Q_8	4
-/-	↑/↑	+/+	Q_3, Q_4, Q_5/Q_6	5
	↓/↓	-/-	Q_3, Q_4, Q_7/Q_8	6
	↑/↓	+/-	Q_3, Q_4, Q_5/Q_6 orQ_7/Q_8	7
	↓/↑	-/+	Q_3, Q_4, Q_5/Q_6 orQ_7/Q_8	8
+/-	↑/↑	-/+	Q_1, Q_4, Q_5/Q_6	9
	↓/↓	+/-	Q_1, Q_4, Q_7, Q_8	10
	↑/↓	-/-	Q_1, Q_4, Q_5/Q_6 orQ_7/Q_8	11
	↓/↑	+/+	Q_1, Q_4, Q_5/Q_6 orQ_7/Q_8	12
-/+	↑/↑	+/-	Q_2, Q_3, Q_5/Q_6	13
	↓/↓	-/+	Q_2, Q_3, Q_7/Q_8	14
	↑/↓	+/+	Q_2, Q_3, Q_5/Q_6 orQ_7/Q_8	15
	↓/↑	-/-	Q_2, Q_3, Q_5/Q_6 orQ_7/Q_8	16
____	____	____	S_1, S_2	17

turned OFF and Q_1 is turned ON, another switching cycle begins.

The power flow controller balances the difference between C_1 and C_2 with C_3 to decrease I_{c1} and increase I_{c2}, whose specific switching mode is shown in Fig. 7. Q_1, Q_4, and Q_5/Q_6 are complementary to each other. Q_2, Q_3 Q_7, and Q_8 are always in the OFF state. Based on the abovementioned analysis, Q_1, Q_4, and Q_5/Q_6 need to be controlled.

According to the aforementioned analysis, combined with the current direction and the need for power flow control, the CDCPFC has a total of 17 kinds of conditions. Table II shows the opening and closing characteristics of the switch under each operating condition. The following switching action rules can be summarized for reference.

1) While I_{c1} is positive, Q_1 works, Q_3 shuts; while I_{c1} is negative, Q_3 works, Q_1 lockouts.
2) While I_{c2} is positive, Q_2 works, Q_4 shuts; while I_{c2} is negative, Q_4 works, Q_2 lockouts.
3) While control objectives I_{c1}/I_{c2} are increased, Q_5/Q_6 work, Q_7/Q_8 shut; while control objectives I_{c1}/I_{c2} are decreased, Q_7/Q_8 work, Q_5/Q_6 shut.

When I_{c1}/I_{c2} control objectives are different, the capacitance energy of one line is partially transferred to an inductor; the capacitor of the other line is required to obtain partial energy from the inductor. While the inductor requires energy from the capacitor, Q_5/Q_6 work, Q_7/Q_8 shut. While inductor needs to transfer energy to the capacitor C_3, Q_7/Q_8 works, Q_5/Q_6 shut.

C. Control Strategy

CDCPFC's control strategy is shown in Fig. 8(a). Case 12 (i.e., technology situation in Fig. 7) is taken as an example. The dispatch system sends control commands to the CDCPFC according to the system's power flow, that is, the current reference $I_{c1-\mathrm{ref}}$ and $I_{c2-\mathrm{ref}}$ of the controlled line. Meanwhile, according to the corresponding specific cases, CDCPFC will receive the case sequence instruction from the dispatch system. Some

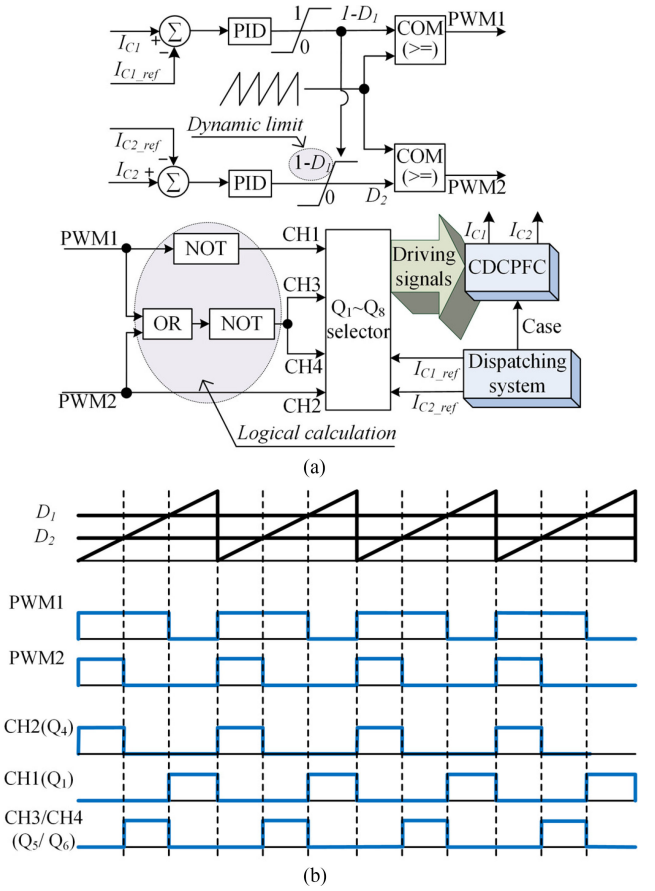

Fig. 8. Control scheme of CDCPFC. (a) Block diagram of the control strategy. (b) Switch signals in Case 12.

switches are selected to participate in the operation through the logic unit, the others that do not participate in the operation are locked. $I_{c1-\mathrm{ref}}$ and $I_{c2-\mathrm{ref}}$ are compared with the actual currents I_{c1} and I_{c2}. The difference obtained by the PID regulator is compared with the sawtooth carrier to generate PWM1 and PWM2 signals.

Finally, four driving signals are obtained, and they can be classified into three groups (i.e., CH1, CH2, and CH3/4) by a series of logical calculation, as shown in Fig. 8(a). The key function of the logical calculation part is to make the power flow control targets of the two lines completely decoupled, without any constraint on each other. For three groups of driving signals, their waveforms are complementary in each switching cycle.

In order to construct three sets of complementary driving signals, the concept of "dynamic limit value" is introduced in the control strategy, that is, the duty cycle of a group of input signals is limited with a set value to meet $D_1 + D_2 \leq 1$. In Fig. 8(a), for the PID unit, the upper limit of the output limiter unit is determined by $1 - D_1$. Thus, three sets of complementary driving signals can be obtained in the control strategy. For Case 12, the corresponding switching signal generation process is shown in Fig. 8(b) for reference.

D. Characteristics Analysis

Due to the symmetry of the proposed topology and 17 cases described previously, Case 12 is taken as an example to analyze

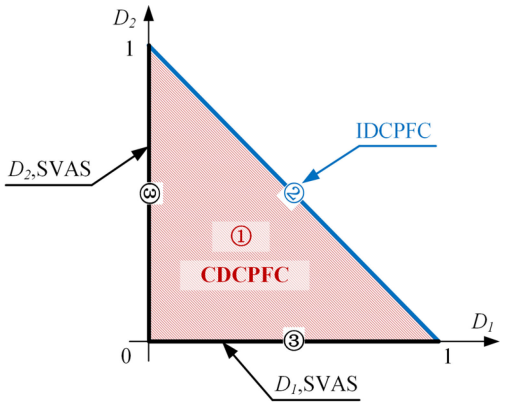

Fig. 9. Functional area of CDCPFC.

the control signal of CDCPFC in Fig. 8. Set the duty cycle of Q_1 as D_1, Q_4 as D_2 and Q_5/Q_6 as $1-D_1-D_2$. While the current of coupling inductance is continuous, the following equation can be obtained by the principle of voltage-second balance:

$$V_{c1}D_1T_s - V_{c2}D_2T_s - V_f(1-D_1-D_2)T_s = 0 \quad (1)$$

where T_s is the switching cycle.

While the voltages of C_1 and C_2 are continuous, according to the principle of amperes-second balance, we can obtain

$$I_{c1}(1-D_1)T_s + (I_{c1}-I_L)D_1T_s = 0 \quad (2)$$

$$(I_{c2}-I_L)D_2T_s + I_{c2}(1-D_2)T_s = 0. \quad (3)$$

The abovementioned equations are simplified, we can obtain

$$I_{c1} = D_1I_L \quad (4)$$

$$I_{c2} = D_2I_L \quad (5)$$

where I_L is the average inductor current.

Equations (4) and (5) have clarified the average model of the CDCPFC. The duty cycles D_1 and D_2 have a linear relationship with the line current, which indicates that D_1 and D_2 can control the current of two lines. According to (1), (4), and (5), we can obtain

$$V_{c1}I_1 - V_{c2}I_2 - V_fI_L(1-D_1-D_2) = 0 \quad (6)$$

$$I_L = I_{c1} + I_{c2} + (V_{c1}I_{c1} - V_{c2}I_{c2})/V_f. \quad (7)$$

Equation (6) is the power conservation equation, while CDCPFC efficiency is 100%. The ripple formulas of the capacitor voltage V_{c1} and V_{c2} can be derived as

$$\Delta V_{c1} = (I_L - I_{c1})I_{c1}T_s/I_LC_1 \quad (8)$$

$$\Delta V_{c2} = (I_L - I_{c2})I_{c2}T_s/I_LC_2. \quad (9)$$

In particular, when $D_1 + D_2 = 1$, the energy exchange exists only between C_1 and C_2, which means that the CDCPFC works as IDCPFC, as seen in the line ② of Fig. 9. When $D_1 = 0$ or $D_2 = 0$, the energy exchange exists only between C_1 and C_3 or C_2 and C_3, which means CDCPFC works as single SAVS, as seen in the lines ③ of Fig. 9. The triangle frame and its internal area ① are the workspace of CDCPFC. Compared with the control dimensions of the existing DCPFC (segments), it is easy to recognize the control dimension of CDCPFC (plane).

TABLE III
STRESS OF KEY COMPONENTS

Components	Stress Type	
	V_s	I_s
Q_1, Q_3, D_{b1}, D_{b3}	$\|V_{c1}\|+\|\max(V_{c1}, V_{c2}, V_f)\|$	I_L
Q_2, Q_4, D_{b2}, D_{b4}	$\|V_{c2}\|+\|\max(V_{c1}, V_{c2}, V_f)\|$	I_L
Q_5, Q_6, Q_7, Q_8	$0.5*\max(\|V_{c1}\|+\|V_f\|, \|V_{c2}\|+\|V_f\|)\|$	I_L
D_{b5}	$\max(\|V_{c1}\|+\|V_f\|, \|V_{c2}\|+\|V_f\|)$	I_L
C_1	$\|V_{c1}\|$	$2C_1\|\Delta V_{c1}\|/T$
C_2	$\|V_{c2}\|$	$2C_2\|\Delta V_{c2}\|/T$
C_3	$\|V_f\|$	---
$L_1 \| L_2$	$\|\max(V_{c1}, V_{c2}, V_f)\|$	I_L

Note: I_L, ΔV_{c1}, and ΔV_{c2} can be obtained by (7)–(9), respectively. And V_{c1} and V_{c2} can be obtained by the system power flow equations.

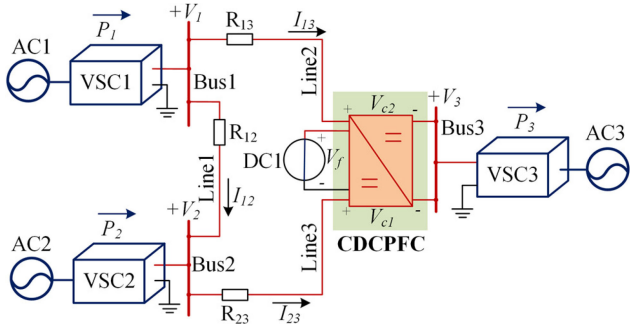

Fig. 10. Simulation model based on the three-terminal ring HVDC system.

The component stress is also a major concern in the practical design of the proposed CDCPFC, which will affect the sizing and cost of hardware. Therefore, the voltage and current stress, V_s and I_s for key components are, respectively, calculated and listed in Table III for reference.

IV. SIMULATION VERIFICATION

In order to verify the feasibility and validity of the proposed CDCPFC topology, an equivalent three-terminal ring-type dc transmission system model is built in MATLAB/Simulink environment, as shown in Fig. 10. The main information of the simulation case is summarized as follows.

1) For the convenience of analysis, only the positive polarity part is considered here.
2) VSC1 and VSC2 work in constant power mode, respectively, delivering 160 and 80 MW [22], respectively.
3) VSC3, as the system power output terminal, operates in constant voltage mode ($V_3 = 150$ kV).
4) CDCPFC is installed at VSC3 side. The capacitors C_1 and C_2 are in series with line 2 and 3, respectively. The external voltage source required by CDCPFC is represented by a 5 kV dc voltage source.
5) The simulation parameters are set to $C_1 = 7$ mF, $C_2 = 1.7$ mF, $L_1 = L_2 = L = 1$ mH, and the switching frequency is 1 kHz. The transmission line parameters are shown in Table IV [22].

According to Fig. 10, the power flow system equations are expressed by (10). From (10), it can be derived that the initial steady-state currents I_{13} and I_{23} of lines 2 and 3 are 0.61 and 0.97 kA, respectively.

TABLE IV
TRANSMISSION LINE PARAMETERS

Parameter	LINE1	LINE2	LINE3
Distance/km	200	300	100
Resistor/Ω	2	3	1

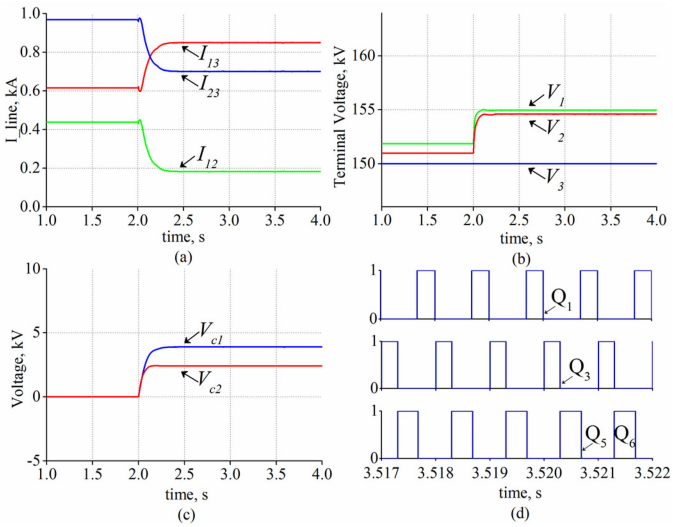

Fig. 11. Simulation results of startup. (a) I_{12}, I_{13}, I_{23}. (b) V_1, V_2, V_3. (c) V_{c1}, V_{c2}. (d) Q_1, Q_3, Q_5/Q_6.

$$\begin{cases} I_{12} = \dfrac{V_1 - V_2}{R_{12}} \\ I_{13} = \dfrac{V_1 - V_3 - V_{c2}}{R_{13}} \\ I_{23} = \dfrac{V_2 - V_3 - V_{c1}}{R_{23}} \\ P_1 = (I_{12} + I_{13})V_1 \\ P_2 = (I_{23} - I_{12})V_2. \end{cases} \tag{10}$$

A. Startup of CDCPFC

For this simulation, the CDCPFC is bypassed during the first stage (i.e., $t = 0 - 1$ s). At $t = 2$ s, CDCPFC gets instructions to control I_{13} and I_{23}, whose current reference values are 0.85 and 0.7 kA, then CDCPFC is put into operation.

The simulation results of the whole startup process are shown in Fig. 11. It is seen from Fig. 11(a) that the line current quickly responds when the CDCPFC is put into operation. Fig. 11(b) shows the terminal voltage curve of VSCs. The voltage curves of V_{C1} and V_{C2} are shown in Fig. 11(c). Fig. 11(d) shows the complementary switching signal waveforms. It can be seen from Fig. 11 that the simulation results during the whole startup phase are consistent with the theoretical analysis that verifies the correctness of the working principle.

B. Active Control of the One Line's Power Flow

For this simulation, the CDCPFC is first set to be operated in the steady state ($I_{13} = 0.9$ kA and $I_{23} = 0.6$ kA). At $t = 1$ s, the

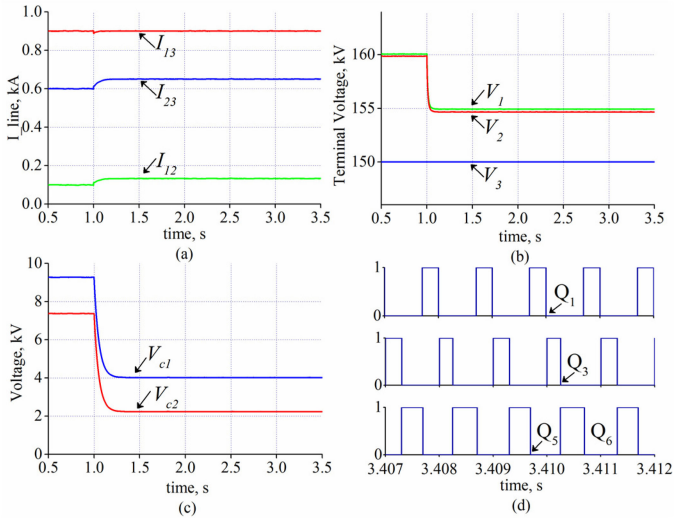

Fig. 12. Simulation results of one line's active control. (a) I_{12}, I_{13}, I_{23}. (b) V_1, V_2, V_3. (c) V_{c1}, V_{c2}. (d) Q_1, Q_3, Q_5/Q_6.

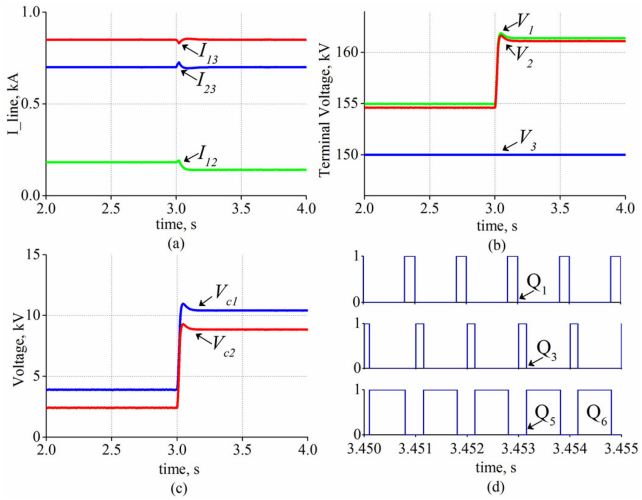

Fig. 13. Simulation results of VSC power output change. (a) I_{12}, I_{13}, I_{23}. (b) V_1, V_2, V_3. (c) V_{c1}, V_{c2}. (d) Q_1, Q_3, Q_5/Q_6.

CDCPFC is instructed to change the current reference value I_{23} from 0.6 to 0.65 kA, whereas I_{13} remains unchanged.

The whole simulation results are shown in Fig. 12. Three lines' current waveforms are shown in Fig. 12(a). The current I_{23} of line 3 changes from 0.6 to 0.65 kA, whereas the current I_{13} of line 2 keeps as 0.9 kA after a quick transient process. The capacitor voltage V_{c1} and V_{c2} are 4.01 and 2.25 kV, respectively, as shown in Fig. 12(b). The terminal voltage of VSC1 and VSC2 reaches 154.93 and 154.66 kV, as shown in Fig. 12(c). It can be seen from Fig. 12 that the simulation results are consistent with the theoretical analysis that verifies the active power flow control capability of the two lines.

C. Response to Disturbance

For this simulation, the CDCPFC is first set to be operated in the steady state ($I_{13} = 0.85$ kA and $I_{23} = 0.7$ kA). At $t = 3$ s, the output power of VSC2 is set to quickly rise from 80 to

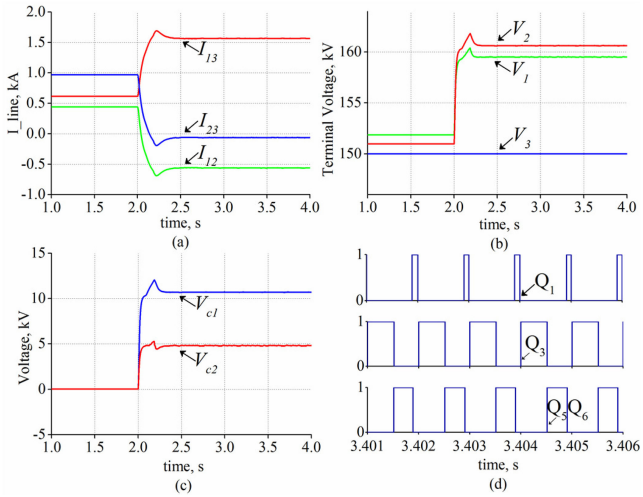

Fig. 14. Simulation results of power flow reversal. (a) I_{12}, I_{13}, I_{23}. (b) V_1, V_2, V_3. (c) V_{c1}, V_{c2}. (d) Q_1, Q_3, Q_5/Q_6.

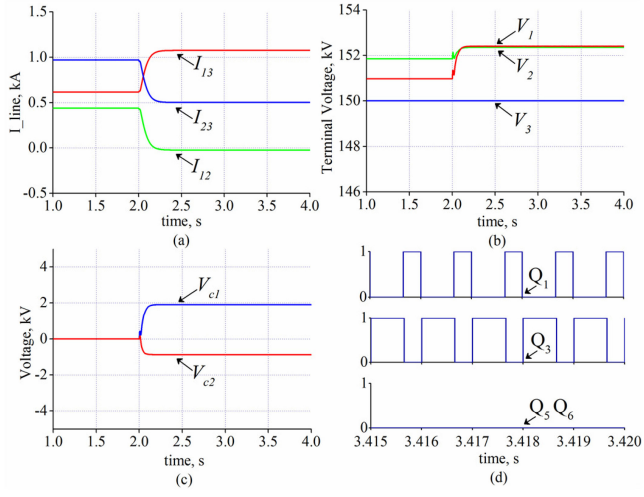

Fig. 15. Simulation results corresponding to IDCPFC. (a) I_{12}, I_{13}, I_{23}. (b) V_1, V_2, V_3. (c) V_{c1}, V_{c2}. (d) Q_1, Q_3, Q_5/Q_6.

90 MW (a step change), whereas VSC1 output power remains unchanged. For CDCPFC, the control reference value of both I_{13} and I_{23} remains unchanged. From Fig. 13(a), it is seen that after a short transient process of about 0.12 s, the power flow of a controlled line has rapidly returned to the desired current value. From Fig. 13(b) and (c), it is seen that VSC terminal voltages and V_{C1}/V_{C2} returned to their steady-state values after about 0.12 s. All the simulation results show that in the event of external disturbances (e.g., VSC output power change), the proposed CDCPFC control strategy exhibits good performance of fast responding and regulation.

D. Power Flow Reversal

This simulation is used to verify the power flow reversal process of line 3. Before the current reverses, the CDCPFC is bypassed and $I_{23} = 0.968$ kA. At $t = 2$ s, the CDCPFC is instructed to control I_{13} and I_{23} with current reference values of 1.56 A and -0.06 kA, respectively. The simulation results of the whole process are shown in Fig. 14. According to Fig. 1(a), the direction of I_{23} in line 3 is changed from the positive direction to the negative direction, and the direction of I_{13} in line 2 is not changed, thereby indicating that the CDCPFC can cope with power flow reversal scene. In Fig. 14(b) and (c), V_{C1} and V_{C2} are 4.81 and 10.69 kV, respectively, and the terminal voltages of VSC1 and VSC2 rise to 159.50 and 160.63 kV to meet the requirements of the power flow reversal.

E. Implementation of the IDCPFC Function

Set $D_1 + D_2 = 1$ (that is, blue line in Fig. 9), CDCPFC does not exchange power with external voltage source. CDCPFC achieves the power exchange between line 2 and line 3, equivalent to the function of IDCPFC.

At the initial time, the CDCPFC is bypassed. At $t = 2$ s, set CDCPFC to control the current I_{23} to reach 0.5 kA, and the simulation waveform is shown in Fig. 15. The capacitor voltage in series into line 2 and 3 is up to -0.87 and 1.90 kV, respectively, as shown in Fig. 15(c), which is consistent with

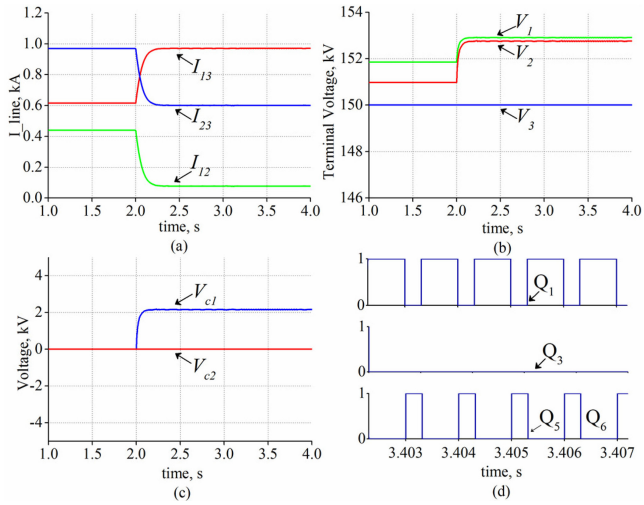

Fig. 16. Simulation results corresponding to SAVS. (a) I_{12}, I_{13}, I_{23}. (b) V_1, V_2, V_3. (c) V_{c1}, V_{c2}. (d) Q_1, Q_3, Q_5/Q_6.

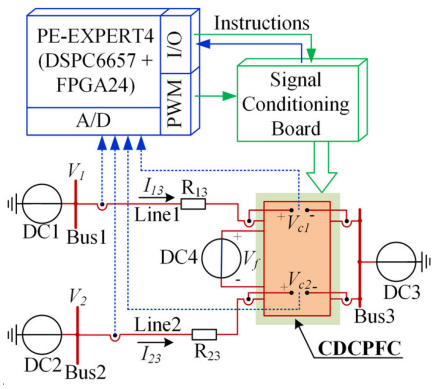

Fig. 17. Three-terminal dc grid experimental platform.

the theoretical values. The control signals of switch Q_1 and Q_3 are shown in Fig. 15(d). It is visible that only Q_1 and Q_3 work except Q_5/Q_6, which indicates that there is no power exchange

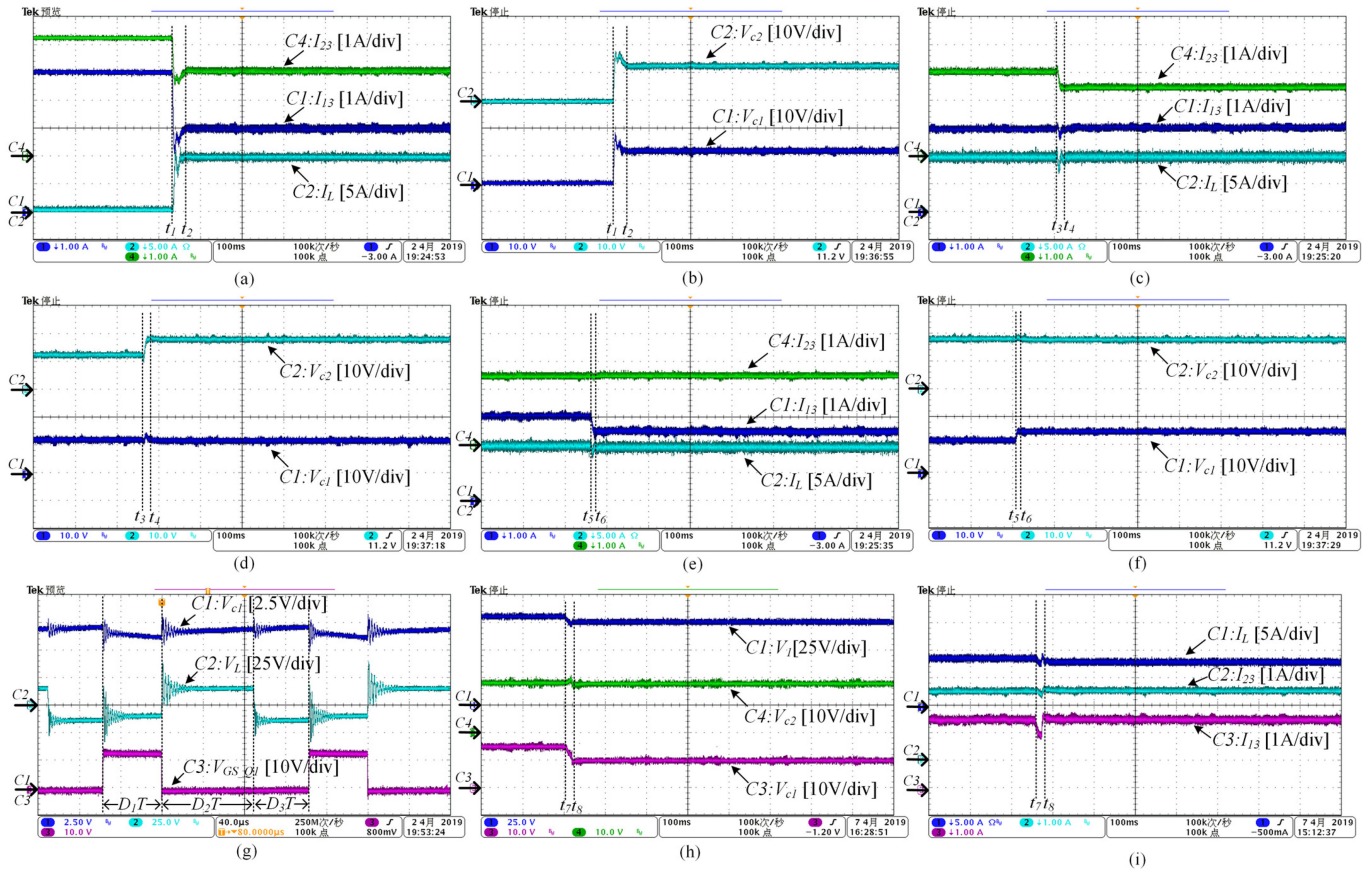

Fig. 18. Experimental waveforms. (a) Startup: currents I_{13}, I_{23}, and I_L. (b) Startup: voltages V_{c1} and V_{c2}. (c) Decreasing I_{23}: currents I_{13}, I_{23}, and I_L. (d) Decreasing I_{23}: voltages V_{c1} and V_{c2}. (e) Decreasing I_{13}: currents I_{13}, I_{23}, and I_L. (f) Decreasing I_{13}: voltages V_{c1} and V_{c2}. (g) Decreasing I_{13}: voltages V_{c1}, V_L, and driver signal V_{GS_Q1} after t_6. (h) Disturbance in V_1: the voltages V_1, V_{c1}, and V_{c2}. (i) Disturbance in V_1: currents I_{13}, I_{23}, and I_L.

between CDCPFC and the external source at this time. And the simulation results satisfy $V_{c1}I_{13} = V_{c2}I_{23}$, which is consistent with IDCPFC working characteristic [22].

F. Implementation of SAVS Function

Set $D_1 = 0$, that is, $V_{c2} = 0$ (that is, black line in Fig. 9), energy exchange path between CDCPFC and Line 2 is bypassed. Power exchange occurs between CDCPFC and Line 3, equivalent to the function of SAVS.

For this simulation, the CDCPFC is bypassed during the initial stage. At $t = 2$ s, set CDCPFC control target $I_{23} = 0.6$ kA, and the V_{C1} will be 2.16 kV, according to theoretical analysis. It is seen from Fig. 16(c) that the simulation results of V_{C1} are consistent with the theoretical values. The control signals of switch Q_1 and Q_5/Q_6 are shown in Fig. 16(d). It is visible that Q_5/Q_6 do not work except Q_3 according to the analysis of control strategy.

V. Experimental Verification

In order to verify the correctness and rationality of the CDCPFC topology proposed in this article, a downscale experimental system has been built in the laboratory. The three-terminal monopole architecture of the experimental system is shown in Fig. 17 for reference, which is consistent with the simulation case in Fig. 10. The main information of the experimental system is summarized as follows.

1) The proposed CDCPFC control strategy is implemented in the PE-Expert4 controller.
2) Three constant voltage sources V_1, V_2, and V_3 are 80, 90, and 50 V, respectively. External voltage source V_f = 10 V. All sources are implemented by Chroma dc power supply and pCUBE power supplies.
3) The line resistance R_{13} and R_{23} are 6 and 9.2 Ω, respectively.

Based on the experimental platform, typical experiments on power flow control function in Line 1 and 2 are carried out, and the corresponding waveforms are given in Fig. 18.

A. Experimental Study I (Startup of CDCPFC)

The experimental waveforms are shown in Fig. 18(a) and (b) when CDCPFC has been activated. At t_1, the control instructions are sent to control the currents I_{13} and I_{23} to 3 A simultaneously. It takes 30 ms for the currents to reach the steady-state value at t_2, and the capacitor voltages V_{C1} and V_{C2} rise from zero to 11.6 and 12.2 V.

B. Experimental Study II (Active Control of the One Line's Power Flow While Keeping the Other One Remained)

Fig. 18(c) and (d) shows the experimental waveforms of changing I_{23} while keeping I_{13} constant. At t_3, a control instruction is sent to control the current I_{23} to 2.5 A. Within 20 ms, the current I_{13} maintains at 3 A quickly after slight fluctuations and the current I_{23} reaches 2.5 A at t_4.

Fig. 18(e)–(g) shows the experimental waveforms of changing I_{13} while keeping I_{23} constant. At t_5, a control instruction is sent to control the current I_{13} to 2.5 A. Within 15 ms, both currents I_{13} and I_{23} maintain at 2.5 A after slight fluctuations. The steady-state waveforms of voltages V_{c1}, V_L, and driver signal V_{GS_Q1} after t_6 are shown in Fig. 18(g).

C. Experimental Study III (Response to Disturbance)

Fig. 18(h) and (i) shows the experimental waveforms of a step change in V_1. At t_7, V_1 is reset from 80 to 75 V, as a disturbance. Within about 24 ms, both currents I_{13} and I_{23} maintain at 2.5 A after slight fluctuations, which verifies good performance of fast responding and regulation.

According to the experimental waveforms of Fig. 18, the actual working characteristics are consistent with the above-mentioned theoretical analysis.

VI. Conclusion

This article presents the technological concept and general framework of a CDCPFC by comparing the different combination schemes of voltage-type dc power flow controllers. Based on the general framework, a specific topology circuit is proposed in this article. Its working principle, control strategy, and working characteristics are analyzed. A simulation model and experiment platform are built for verification. The conclusions are as follows.

1) CDCPFC can realize the flexible and active power flow control of two lines. The general framework has offered a guide for topology construction.
2) The proposed specific topology is suitable for a situation with all kinds of current directions. The ability of power flow control is so strong that the active control of the two lines' power flow can be achieved.
3) The proposed two-target control strategy can regulate the duty ratios within the three substates in one cycle, by which two control targets are completely decoupled.
4) CDCPFC might have extensive applications in future dc gird scenarios, such as complex MTDC system and dc distribution network.

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