Balanced Submodule Operation of Modular Multilevel Converter-Based Induction Motor Drive for Wide-Speed Range

Yerraguntla Shasi Kumar and Gautam Poddar

***Abstract*—Operation of the conventional modular multilevel converter (MMC) at low frequencies for the induction motor drive is difficult. The peak-to-peak voltage ripple of submodule (SM) capacitor increases abnormally at low frequencies of the drive. Recently, the problem of high voltage ripple has been solved by using back-to-back MMC without overloading the converter till very low frequency of the drive. In this back-to-back configuration, the grid-side MMC generates constant dc current source at its output instead of dc voltage source. Using this current source as input, the motor-side MMC drives a three-phase induction motor. It is shown that the voltage ripple of SM capacitor remains constant till very low frequency due to the dc current source. However, the average capacitor voltage controllers do not guarantee balanced operation of individual SM. In this article, the need for balancing controller of individual SM capacitors of back-to-back MMC is established experimentally. Therefore, this article proposes additional voltage-balancing controllers for the individual capacitor of grid-side MMC and motor-side MMC without disturbing the average controllers. The operating principle of this balancing controller has been presented analytically and verified experimentally. Finally, the operation of the drive with the proposed balancing controller is presented for wide speed range.**

***Index Terms*—Capacitor voltage ripple, modular multilevel converter (MMC), voltage-balancing control.**

I. Introduction

MODULAR multilevel converter (MMC) is very promising for medium- and high-voltage applications without any transformer. MMC is an ideal topology for medium-voltage variable-speed drives due to its features, such as modularity, scalability, quality waveforms, and low average switching frequency [1]–[3]. Submodule (SM) capacitors of conventional MMC suffer from large voltage ripple at low frequencies for the application of variable speed drive. The peak-to-peak voltage ripple of SM capacitors increases as the motor supply frequency ω_s decreases [4]. This problem limits the MMC for variable speed drive application. This problem was tackled in [5]–[14]. The additional common-mode voltage and circulating current-based techniques in [5]–[14] increase the peak of the arm currents to more than three times the nominal current [5].

This issue is solved by using a back-to-back MMC without overloading the converter [27]. According to [27], the grid-side MMC converts ac grid voltage to constant dc current $i_{\rm dc}$ as shown in Fig. 1. Motor-side MMC converts $i_{\rm dc}$ to variable voltage and variable frequency ac. Due to the current source at the input of motor-side MMC, the voltage ripple of the SM capacitor maintained constant till very low frequency of the drive [27].

In MMC, the SMs of each arm may not operate in balanced condition. The average capacitor voltage control strategies in [5]–[10] and [20]–[27] do not ensure the balanced operation of the SM capacitor voltages of each arm if they are not identical. This can happen due to unequal distribution of losses of semiconductor devices, variation of switching behavior of the semiconductor devices, difference in gate signals as all gate drivers do not have identical characteristics, ageing of components, etc. The average voltage controllers in [5]–[10] and [20]–[27] regulate the average capacitor voltage but not the capacitor voltage of individual SM. Therefore, an additional controller is required to balance the capacitor voltage of each SM without disturbing the average capacitor voltage. Unequal voltages of SM capacitors distort the output voltages and currents of the induction motor drive. Eventually, the operation of the MMC converter becomes unstable and the drive system trips. Hence, a suitable balancing strategy is needed for the stable operation of the MMC-based induction motor drive.

Few research works have been reported so far to balance the voltages of individual SM capacitors of MMC-based drives. Sorting algorithm has been proposed in [1] to maintain the individual SM capacitor's voltage. This method has been adopted again in [10]–[19]. These sorting algorithms can cause excessive unequal switching frequency among the SMs, resulting in higher losses in the converter [18]. The sorting algorithm is generally preferred for HVdc applications where large numbers of SMs are present [19]. Pulsewidth modulation (PWM)-based voltage balancing algorithm of SM capacitors is proposed in [2] and [20]. For MMC-based drive with a minimum number of SMs, PWM-based control method is preferred to sorting algorithm. Sorting algorithm does not perform well with less number of

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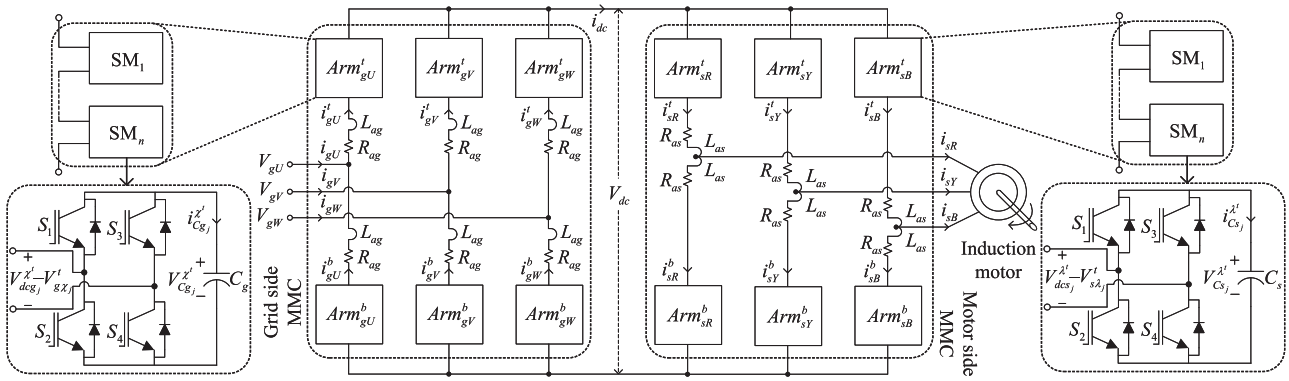

Fig. 1. Three-phase back-to-back MMC-based induction motor drive [27].

SMs. The effective high switching frequency can be achieved with PWM control [20].

In [2] and [20]–[24], the proposed balancing algorithm of motor-side MMC has common voltage reference for both average dc capacitor voltage controller and balancing controllers of individual SM. Coupling of these two controllers can affect the convergence of the SM capacitor voltage as presented in this article. The balancing algorithm within the PWM carrier cycle is implemented in [26]. However, [20]–[26] do not show the effectiveness of the proposed balancing algorithms from very low speed to rated speed operation of the drive. However, all these strategies are proposed for the configuration of standard MMC with constant input dc voltage.

This article aims at proposing a suitable balancing control strategy without compromising the input and the output performances of the MMC-based drive at all speeds. The proposed balancing strategy is specially targeted for back-to-back MMC configuration with intermediate constant dc current as shown in Fig. 1. The performance of the balancing algorithm needs to be validated from rated to very low speed of the drive. Therefore, the article is organized as follows.

First, the proposed balancing algorithm of grid-side MMC is presented. Next, the proposed balancing algorithm of motor-side MMC is given. Finally, experimental waveforms of the grid-side and motor-side MMCs with proposed balancing control methods are presented at different operating conditions.

II. Balanced Operation of Grid-Side MMC

In this section, a method is proposed to balance the individual SM capacitor voltages of the grid-side MMC. This balancing controller maintains individual SM capacitor voltages to their required value. Fig. 1 shows the configuration of the grid-side MMC which is directly connected to the grid. It keeps the grid current sinusoidal at unity power factor and generates regulated dc current source at the output. This current source acts as input to motor-side MMC drive.

A. Generation of Intermediate DC Current Source

For balanced operation, the legs of phases *U*, *V*, and *W* of grid-side MMC needs to generate equal dc currents $i^{U}_{\mathrm{dc}g}$, $i^{V}_{\mathrm{dc}g}$, $i^{W}_{\mathrm{dc}g}$, respectively. These three leg currents together generate the net dc current i_{dc}. Here, the dc current i_{dc} is kept constant for all operating conditions of the drive. The dynamical equation of net intermediate dc current i_{dc} produced by the grid-side MMC can be written as follows:

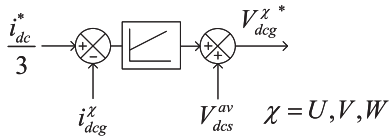

Fig. 2. Intermediate dc current control.

$$\left(\frac{2}{3}L_{ag}+\frac{4}{3}L_{as}\right)\frac{di_{\mathrm{dc}}}{dt}+\left(\frac{2}{3}R_{ag}+\frac{2}{3}R_{as}\right)i_{\mathrm{dc}}=V^{av}_{\mathrm{dcg}}-V^{av}_{dcs}$$

$$V^{av}_{\mathrm{dcs}}=\frac{1}{3}\sum_{\lambda=R,Y,B}\sum_{j=1}^{n}\left[V^{\lambda^t}_{\mathrm{dcs}_j}+V^{\lambda^b}_{\mathrm{dcs}_j}\right]$$

$$V^{\chi}_{\mathrm{dcg}}=\sum_{j=1}^{n}\left[V^{\chi^t}_{\mathrm{dcg}_j}+V^{\chi^b}_{\mathrm{dcg}_j}\right]V^{av}_{\mathrm{dcg}}=\frac{1}{3}\sum_{\chi=U,V,W}V^{\chi}_{\mathrm{dcg}}$$

$$i^{\chi}_{\mathrm{dcg}}=\frac{i^{t}_{g\chi}(t)+i^{b}_{g\chi}(t)}{2}\;i_{\mathrm{dc}}=\sum_{\chi=U,V,W}i^{\chi}_{\mathrm{dcg}}. \tag{1}$$

Here, $i^{t}_{g\chi}$ and $i^{b}_{g\chi}$ are the top and bottom arm currents of grid-side MMC. L_{ag} and L_{as} are the arm inductances of grid-side and motor-side MMCs. A coupled inductor L_{as} is used for motor-side MMC as shown in Fig. 1. R_{as} and R_{ag} are the arm resistances of grid-side and motor-side MMCs. $V^{\chi^t}_{dcg_j}$ and $V^{\chi^b}_{dcg_j}$ are the dc voltages generated by top and bottom jth SM of grid-side MMC. V^{χ}_{dcg} is the dc voltage generated per leg by the grid-side MMC. V^{av}_{dcg} is the net average dc bus voltage produced by the grid-side MMC. $V^{\lambda^t}_{\mathrm{dcs}_j}$ and $V^{\lambda^b}_{\mathrm{dcs}_j}$ are the dc voltages generated by top and bottom jth SM of motor-side MMC. V^{av}_{dcs} is the average dc voltage generated by the motor-side MMC.

Three independent closed-loop current controllers are introduced to control the intermediate dc current of each leg i^{χ}_{dcg} as shown in Fig. 2. These independent controllers ensure that each leg shares equal output dc current even if the legs are not identical.

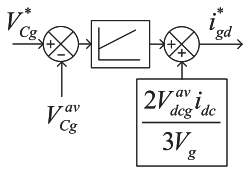

Fig. 3. Averaging control of SM capacitor voltage of grid-side MMC.

B. Regulation of SM Capacitor Voltage and Grid Current Control

To generate the dc current to drive the motor-side MMC, the grid-side MMC needs to draw active power from the grid voltage. This active power is used to balance the SM capacitor voltages. The difference of input and output active powers of grid-side MMC indicates the dynamics of the average capacitor voltage of SMs as given in (2).

In (2), i_{gd} is the d-axis grid current $i_{g\chi}$, while the d-axis coincides with the grid voltage vector V_g. C_g is the capacitance of grid-side SM. The average capacitor voltage V^{av}_{Cg} is estimated considering all $6n$ number of SMs of grid-side MMC as given in (2). $V^{\chi^t}_{Cg_j}$ and $V^{\chi^b}_{Cg_j}$ are the capacitor voltages of top and bottom SMs of grid-side MMC

$$\begin{aligned} &6nC_gV^{av}_{Cg}\frac{dV^{av}_{Cg}}{dt} = \frac{3}{2}V_g i_{gd} - V^{av}_{\mathrm{dc}g} i_{\mathrm{dc}} \\ &\Rightarrow \left(\frac{12nC_gV^{av}_{Cg}}{3V_g}\right)\frac{dV^{av}_{Cg}}{dt} = i_{gd} - \underline{\frac{2V^{av}_{\mathrm{dc}g} i_{\mathrm{dc}}}{3V_g}} \\ &V^{av}_{Cg} = \frac{1}{6n}\sum_{\chi=U,V,W}\sum_{j=1}^{n}\left[V^{\chi^t}_{Cg_j} + V^{\chi^b}_{Cg_j}\right] i_{g\chi} = i^t_{g\chi}(t) - i^b_{g\chi}(t). \end{aligned} \tag{2}$$

Using (2), a PI controller regulates V^{av}_{Cg} to its reference value V^*_{Cg} as shown in Fig. 3. At steady state, the constant d-axis current i_{gd} confirms balanced three-phase current drawn from the grid at unity power factor. Thus, the grid-side MMC draws balanced power from the grid and delivers it to the motor-side MMC when the grid voltage is balanced. However, this controller does not ensure that the capacitor voltage of individual SM converges to V^*_{Cg}. This individual capacitor voltage may even converge to abnormal value maintaining the average voltage V^{av}_{Cg} to V^*_{Cg}. Therefore, there is a need of an additional controller to regulate the capacitor voltage of each SM without affecting the average capacitor voltage V^{av}_{Cg}.

Since only averaging control is used to generate dc current source i_{dc} as shown in Fig. 2, all the SMs of each leg of grid-side MMC share equal output dc power. But they may have unequal losses. Therefore, input power to each SM should be different. The net input active power required by the grid-side MMC from the grid is equal to the output dc power P_{dc} and the net losses of all the SMs. The average capacitor voltage controller, shown in Fig. 3, generates the required d-axis current command i^*_{gd} to meet the net input active power. This net active power should be non-uniformly distributed among the arms and SMs to regulate the capacitor voltage of each SM as discussed earlier.

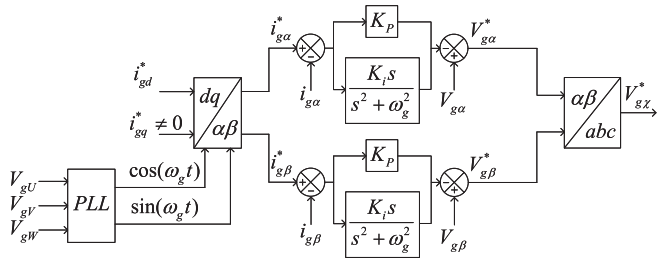

Fig. 4. Grid current control.

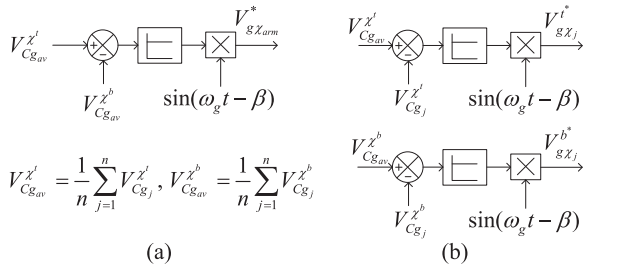

Fig. 5. Capacitor voltage-balancing controllers of grid-side MMC. (a) Arm balancing controller. (b) Individual SM balancing controller.

Traditional balancing methods in [2] and [20]–[26] are proposed for motor-side MMC having constant input dc voltage source. There is no grid-side MMC. In these papers, balancing of SM capacitor is achieved by applying varied dc voltage commands for different SMs. It is difficult to regulate the voltages of SM capacitors at low motor power using these methods for grid-side MMC, presented in Fig. 1. Here, at low motor power, the intermediate dc link voltage is approximately zero due to constant intermediate dc current. Hence, the grid-side MMC does not have sufficient dc voltage at the output to control the capacitor voltage of each SM. Thus, the balancing of SM capacitors of grid-side MMC is proposed to achieve harnessing constant ac grid voltage as explained below.

To balance the SM capacitor voltages of grid-side MMC, a small amount of reactive current i_{gq} is drawn by the grid-side MMC from the ac grid. The corresponding control block diagram is shown in Fig. 4. The magnitude of q-axis current i_{gq} is decided to correct the difference of power absorption among the SMs. However, the practical difference of absorption of active powers among the SMs is extremely small. Therefore, in this article, the magnitude of the reactive current command i^*_{gq} is chosen as 5% of the rated active current i^{rated}_{gd} as follows:

$$i^*_{gq} = 0.05 i^{\mathrm{rated}}_{gd}. \tag{3}$$

The rated input power factor of the drive is ensured as above 0.99. This additional q-axis current i_{gq} does not modify the drawn active power set by the averaging controller from the grid. Therefore, the averaging controller and the balancing controller of grid-side MMC are decoupled. Using this additional i_{gq}, the net active power drawn by each SM can be varied as explained in the following.

SM capacitor voltage controllers are proposed for arms and individual SMs as shown in Fig. 5. The bandwidth of this capacitor voltage controller is lesser than the inner grid current controller. The arm voltage balancing controller shown in Fig. 5(a) ensures that the average capacitor voltages of top $V_{Cg_{av}}^{\chi^t}$ and bottom $V_{Cg_{av}}^{\chi^b}$ arms of the grid-side MMC are equal. The voltage differences of SM capacitors within the arm are reduced by the individual SM balancing controller shown in Fig. 5(b). This arm and individual capacitor voltage controllers are implemented in stationary reference frame. A simple *P*-controller with small gain K_P^g is introduced for each arm and SM independently. The output of these controllers generates voltage commands $V_{g\chi_{arm}}^*$, $V_{g\chi_j}^{t^*}$, and $V_{g\chi_j}^{b^*}$, which lag the grid voltage of phase χ by 90^0 as shown in Fig. 5. Therefore, these voltage commands are in phase with the reactive currents of amplitude $3i_{gq}/2$ and draw active power to balance the arms and individual SM capacitor voltage. Thus, the net active power $3V_g i_{gd}/2$ drawn from the grid can be expanded as follows:

$$\frac{3}{2}V_g i_{gd} = \underline{\frac{3}{2}\left(V_{g\alpha}^* i_{g\alpha}^* + V_{g\beta}^* i_{g\beta}^*\right)} + \underline{\frac{3}{2}i_{gq}K_P^g \begin{pmatrix} \sum_{\chi=U,V,W}\left(V_{Cg_{av}}^{\chi^t} - V_{Cg_{av}}^{\chi^b}\right) \\ +\sum_{\chi=U,V,W}^{j=1}{}^{n}\left(V_{Cg_j}^{\chi^t} - V_{Cg_{av}}^{\chi^t}\right) \\ +\sum_{\chi=U,V,W}^{j=1}{}^{n}\left(V_{Cg_j}^{\chi^b} - V_{Cg_{av}}^{\chi^b}\right) \end{pmatrix}}$$

$$V_{Cg_{av}}^{\chi^t} = \frac{1}{n}\sum_{j=1}^{n} V_{Cg_j}^{\chi^t}, V_{Cg_{av}}^{\chi^b} = \frac{1}{n}\sum_{j=1}^{n} V_{Cg_j}^{\chi^b}. \quad (4)$$

Here, $i_{g\alpha}^*$ and $i_{g\beta}^*$ are the two-phase grid current commands. $V_{g\alpha}^*$ and $V_{g\beta}^*$ are the two-phase grid voltage commands. i_{gq} is the rms value of grid *q*-axis current. $V_{Cg_{av}}^{\chi^t}$ and $V_{Cg_{av}}^{\chi^b}$ are the average capacitor voltages of the top and bottom arm SMs.

In (4), the first underlined term is almost shared equally by the SMs. The second underlined term is the unequally shared power by the arms and SMs. This power is proportional to the deviation of capacitor voltage of arms and each SM from the average arm voltage $V_{Cg_{av}}^{\chi^t}$ or $V_{Cg_{av}}^{\chi^b}$. From (4), it can be observed that the average voltage controller of SM capacitor is decoupled from the arm and individual SM voltage controllers. The reason can be put as follows. Since, the arm balancing controller functions based on the difference between average capacitor voltage of top and bottom arms, it does not alter the total average capacitor voltage V_{Cg}^{av}. Hence, overall V_{Cg}^{av} controller is not affected by this arm voltage-balancing controller.

Similarly, the average arm voltage $V_{Cg_{av}}^{\chi^t}$ or $V_{Cg_{av}}^{\chi^b}$ is chosen as the reference for the individual SM capacitor voltage-balancing controller. Therefore, the arm voltage-balancing controller is not affected by the individual SM voltage-balancing controller. Moreover, the reactive current i_{gq} is used by the arm voltage and individual SM voltage-balancing controllers. On the other hand, the overall average capacitor voltage controller uses active grid current i_{gd}. Therefore, the overall average capacitor voltage controller, given in Fig. 3, is decoupled from the individual voltage-balancing controller of SM capacitor, given in Fig. 5, during transients.

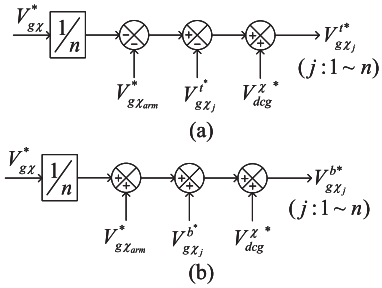

Fig. 6. Voltage command for each SM of grid-side MMC. (a) Top arm. (b) Bottom arm.

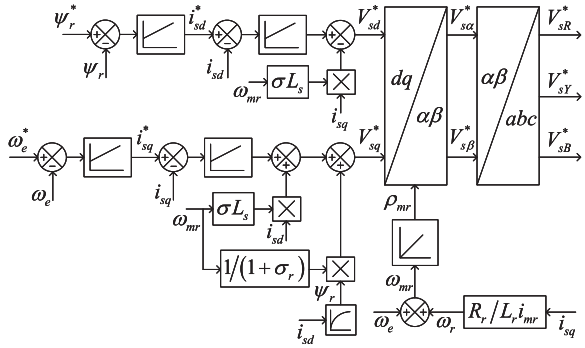

Fig. 7. Block diagram of rotor flux-oriented vector controller of induction motor drive.

Finally, all the outputs of the controllers given in Figs. 2, 4, and 5 are combined together to generate the net voltage commands $(V_{g\chi}^{t\ *}, V_{g\chi}^{b\ *})$ of top and bottom SMs of grid-side MMC as shown in Fig. 6.

III. Balanced Operation of Motor-Side MMC

In this article, input to the motor-side MMC is a controlled dc current source as shown in Fig. 1. Here, strategies are needed for tackling three major issues. The first issue is the uniform distribution of the dc source current among the three legs of the motor-side MMC. The second issue is the balancing of capacitor voltages of the SMs. The third issue is the balanced operation of the induction motor.

A. Balanced Motor Currents Using Vector Control of Induction Motor

Since the three-phase induction motor has balanced three-phase windings, the motor draws balanced three-phase currents when the applied motor voltages are balanced. Three-phase induction motor currents are controlled using the rotor flux-oriented vector controller as shown in Fig. 7. The output voltage commands of this controller V_{sR}^*, V_{sY}^*, and V_{sB}^* are uniformly distributed among the SMs. Therefore, the applied motor voltages are balanced when the capacitor voltages of the SMs are same.

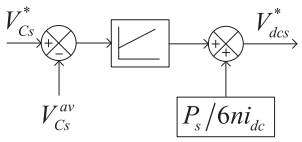

Fig. 8. Averaging control of SM capacitor voltage of motor-side MMC.

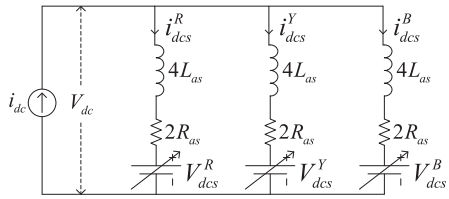

Fig. 9. DC equivalent circuit of motor-side MMC.

B. Average Capacitor Voltage Control and Distribution of DC Source Current

The motor-side MMC draws active power from the input dc current source $i_{\rm dc}$ and regulates the SM capacitor voltage. The dynamical equation of the average capacitor voltage V^{av}_{Cs} of each SM of motor-side MMC is given as

$$\begin{aligned} 6nC_sV^{av}_{Cs}\frac{dV^{av}_{Cs}}{dt} &= V^{av}_{\rm dcs}i_{\rm dc} - P_s \\ \Rightarrow \left(\frac{6nC_sV^{av}_{Cs}}{i_{dc}}\right)\frac{dV^{av}_{Cs}}{dt} &= V^{av}_{\rm dcs} - \frac{P_s}{i_{\rm dc}} \\ P_s &= \sum_{\lambda=R,Y,B} V_{s\lambda}i_{s\lambda} = 3V_si_s\cos\varphi_s, V^{av}_{Cs} \\ &= \frac{1}{6n}\sum_{\lambda=R,Y,B}\sum_{j=1}^{n}\left[V^{\lambda^t}_{Cs_j} + V^{\lambda^b}_{Cs_j}\right]. \end{aligned} \tag{5}$$

Here, V_s and i_s are the rms values of motor phase voltage and current. φ_s is the motor power factor angle and P_s is the motor input power. C_s is the capacitance of motor-side SM. $V^{\lambda^t}_{Cs_j}$ and $V^{\lambda^b}_{Cs_j}$ are the capacitor voltages of top and bottom SMs of grid-side MMC. Based on (5), a PI-controller is used to control V^{av}_{Cs} as shown Fig. 8.

This PI-controller generates the dc voltage command $V^*_{\rm dcs}$. $V^*_{\rm dcs}$ is distributed uniformly to all the SMs of motor-side MMC. The dc equivalent circuit of this operation is shown in Fig. 9. L_{as} and R_{as} are the self-inductance and its leakage resistance of each arm. If these parameters of three legs are identical and the net voltage $\sum_{j=1}^{n}[V^{\lambda^t}_{Cs_j} + V^{\lambda^b}_{Cs_j}]$ of SM capacitor of each leg is the same as others; then, the following relations are achieved:

$$\begin{aligned} V^R_{\rm dcs} &= \frac{V^*_{\rm dcs}}{V^{\max}_{\rm dcs}}\left(\sum_{j=1}^{n}\left[V^{R^t}_{Cs_j} + V^{R^b}_{Cs_j}\right]\right) \\ &= V^Y_{\rm dcs} = \frac{V^*_{\rm dcs}}{V^{\max}_{\rm dcs}}\left(\sum_{j=1}^{n}\left[V^{Y^t}_{Cs_j} + V^{Y^b}_{Cs_j}\right]\right) \\ &= V^B_{\rm dcs} = \frac{V^*_{\rm dcs}}{V^{\max}_{\rm dcs}}\left(\sum_{j=1}^{n}\left[V^{B^t}_{Cs_j} + V^{B^b}_{Cs_j}\right]\right) \end{aligned} \tag{6}$$

$$i^R_{\rm dcs} = i^Y_{\rm dcs} = i^B_{\rm dcs} = \frac{i_{\rm dc}}{3}. \tag{7}$$

Here, $V^{\max}_{\rm dcs}$ is the maximum dc voltage command. However, the parameters of MMC legs may not be exactly the same. The net voltage $\sum_{j=1}^{n}[V^{\lambda^t}_{Cs_j} + V^{\lambda^b}_{Cs_j}]$ of SM capacitor for each leg may not be the same to the others. But, in steady-state, the following voltage equation holds well from Fig. 9. The dc voltage drop across the inductors is zero. Fig. 9 suggests that $V^R_{\rm dcs} \approx V^Y_{\rm dcs} \approx V^B_{\rm dcs}$ as the leakage resistance drop $R_si^{\lambda}_{dcs}$ is negligibly small. Therefore, from (8), the net voltages of SM capacitors of all the three legs must be same as given in (9) in the following:

$$\begin{aligned} V_{\rm dc} &= R_si^R_{\rm dcs} + \frac{V^*_{dcs}}{V^{\max}_{\rm dcs}}\left(\sum_{j=1}^{n}\left[V^{R^t}_{Cs_j} + V^{R^b}_{Cs_j}\right]\right) \\ &= R_si^Y_{\rm dcs} + \frac{V^*_{\rm dcs}}{V^{\max}_{\rm dcs}}\left(\sum_{j=1}^{n}\left[V^{Y^t}_{Cs_j} + V^{Y^b}_{Cs_j}\right]\right) \\ &= R_si^B_{\rm dcs} + \frac{V^*_{\rm dcs}}{V^{\max}_{\rm dcs}}\left(\sum_{j=1}^{n}\left[V^{B^t}_{Cs_j} + V^{B^b}_{Cs_j}\right]\right) \end{aligned} \tag{8}$$

$$\begin{aligned} \sum_{j=1}^{n}\left[V^{R^t}_{Cs_j} + V^{R^b}_{Cs_j}\right] &= \sum_{j=1}^{n}\left[V^{Y^t}_{Cs_j} + V^{Y^b}_{Cs_j}\right] \\ &= \sum_{j=1}^{n}\left[V^{B^t}_{Cs_j} + V^{B^b}_{Cs_j}\right]. \end{aligned} \tag{9}$$

Since the motor draws the remaining three-phase active power from the source, each leg must draw equal active power from the current source $i_{\rm dc}$. Therefore, each leg approximately shares the dc current $i_{\rm dc}/3$.

C. Voltage Balancing of Arms and Individual SM Capacitors

Average capacitor voltage V^{av}_{Cs} controller ensures that each leg of motor-side MMC shares the input dc current equally and the net voltage of SM capacitor of each leg converges to the same value as shown in (9). However, this controller does not ensure the balancing of voltages among SM capacitors of each leg. This is due to the nonidentical power losses of SMs. The reasons are the nonidentical behavior of switching devices, gate drive circuitry, etc. This may cause unequal SM capacitor voltages that may lead to unstable operation of the drive.

Uniform capacitor voltages of SMs can be achieved by adjusting the power of each SM independently to meet the variable losses without disturbing the net power of each leg. This can be met by applying different voltage commands for different SMs. However, the net dc voltage command $2nV^*_{\rm dcs}$ applied to all the SMs of each leg must be the same for all three legs as given in (8). To achieve this, a method is proposed which is explained as follows.

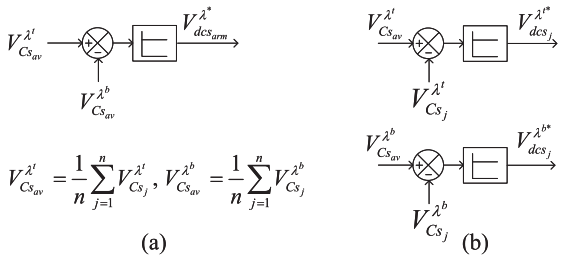

Fig. 10. Capacitor voltage-balancing controllers of motor-side MMC. (a) Arm balancing controller. (b) Individual SM balancing controller.

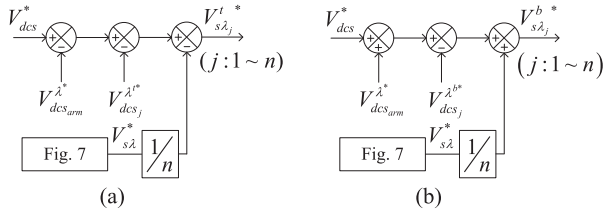

Fig. 11. Voltage command for each SM of motor-side MMC. (a) Top arm. (b) Bottom arm.

Similar to the grid-side MMC, voltage-balancing controller for the capacitor of motor-side MMC contains arm balancing controller and individual SM balancing controller as shown in Fig. 10. Average capacitor voltages of top arm $V^{\lambda^t}_{Cs_{av}}$ and bottom arm $V^{\lambda^b}_{Cs_{av}}$ of motor-side MMC are balanced using the proportional controller of gain K^s_P as shown in Fig. 10(a). This arm balancing controller generates additional voltage reference $V^{\lambda^*}_{\mathrm{dc}s_{arm}}$ for each SM as

$$V^{\lambda^*}_{\mathrm{dc}s_{arm}} = K^s_P\left(V^{\lambda^t}_{Cs_{av}} - V^{\lambda^b}_{Cs_{av}}\right). \tag{10}$$

These average arm capacitor voltage controllers do not alter the overall average capacitor voltage controller given in Fig. 8.

Capacitor voltage of individual SM of each arm is balanced using the error between the average capacitor voltage of each arm ($V^{\lambda^t}_{Cs_{av}}$ or $V^{\lambda^b}_{Cs_{av}}$) and its individual SM capacitor voltage ($V^{\lambda^t}_{Cs_j}$ or $V^{\lambda^b}_{Cs_j}$). This error is multiplied by K^s_P to generate additional dc voltage reference for each SM as

$$V^{\lambda^{t*}}_{\mathrm{dc}s_j} = K^s_P\left(V^{\lambda^t}_{Cs_{av}} - V^{\lambda^t}_{Cs_j}\right)$$
$$V^{\lambda^{b*}}_{\mathrm{dc}s_j} = K^s_P\left(V^{\lambda^b}_{Cs_{av}} - V^{\lambda^b}_{Cs_j}\right). \tag{11}$$

This individual capacitor voltage controller does not alter the average arm capacitor voltage controller.

Finally, the output of the motor current controller, SM capacitor voltage controllers are added to generate the voltage commands ($V^{t\ *}_{s\lambda_j}, V^{b\ *}_{s\lambda_j}$) for different SMs of motor-side MMC as shown in Fig. 11.

The existing algorithms given in [2], [20]–[24] for motor-side MMC use common voltage reference V^*_{Cs} for both averaging controller and SM balancing controller. Therefore, there is strong coupling between these two controllers. To minimize this interaction which may cause instability, the balancing controller is slowed down drastically compared to the averaging controller. The slowed down balancing controller does not perform well, as observed experimentally and shown in Section IV-D.

The proposed algorithm uses the average capacitor voltage of the top arm $V^{\lambda^t}_{Cs_{av}}$ as the reference voltage for balancing the top SMs. Similarly, the average capacitor voltage $V^{\lambda^b}_{Cs_{av}}$ of the bottom arm is used as the reference voltage to balance the bottom SMs as explained in earlier sections. The bandwidth of the overall averaging controller and the balancing controller can then be independently chosen. The experimental results show the improved balancing performance as given in Section IV-D.

The overall block diagram of the back-to-back MMC with proposed controllers is shown in Fig. 12. This block diagram shows the sensed signals from the converter, input and output of each controller.

IV. Experimental Results

An experimental setup is built in the laboratory to validate the performance of individual capacitor voltage-balancing controllers of grid-side MMC and motor-side MMCs. Fig. 13 shows the hardware setup with two SMs per arm. It is controlled by a digital signal processor (DSP) and a field-programmable gate array (FPGA)-based digital card. The MMCs are designed to match the available motor rating in the laboratory. The gate drivers of the IGBTs are chosen to be different. Thus, they cause substantial differences of operation of IGBTs. This leads to unbalanced operation of the SMs without a balancing algorithm. In the laboratory, grid-side MMC and motor-side MMC balancing controller effectiveness is tested at different operating conditions. Phase-shifted carrier-based sinusoidal PWM technique is used to validate the proposed control algorithms.

The detailed specifications of the experimental setup are summarized in Table I.

A. Grid-Side MMC Operation With Balancing Control

Here, different experimental waveforms of the SM capacitor voltages are shown with and without balancing control. Each SM capacitor voltage is maintained at 200 V.

Fig. 14(a) and (b) shows the effect of balancing controller on voltages of SM capacitors when no load is applied to the motor. In Fig. 14(a), without balancing control, the voltages of SM capacitors build up with large differences, and in steady state, they do not converge to the same value. Fig. 14(b) shows that with balancing control, the voltages of SM capacitors build up together and finally converges to the same value. Fig. 14(c) shows that without balancing control, the voltages of SM capacitors drift away from their steady values as soon as the load is applied to the motor. Fig. 14(d) shows the robust operation of SM capacitor voltages with balancing controller when sudden full load is applied to the motor. This confirms the necessity of the balancing controller. Fig. 14(e) and (f) shows the drifting of capacitor voltages when the balancing controller is suddenly disabled during normal operation of the drive. Fig. 14(e) shows the SM capacitor voltages of one leg of grid-side MMC and Fig. 14(f) shows the SM capacitor voltages of three legs of grid-side MMC. Fig. 14(g) and (h) shows the voltages of SM

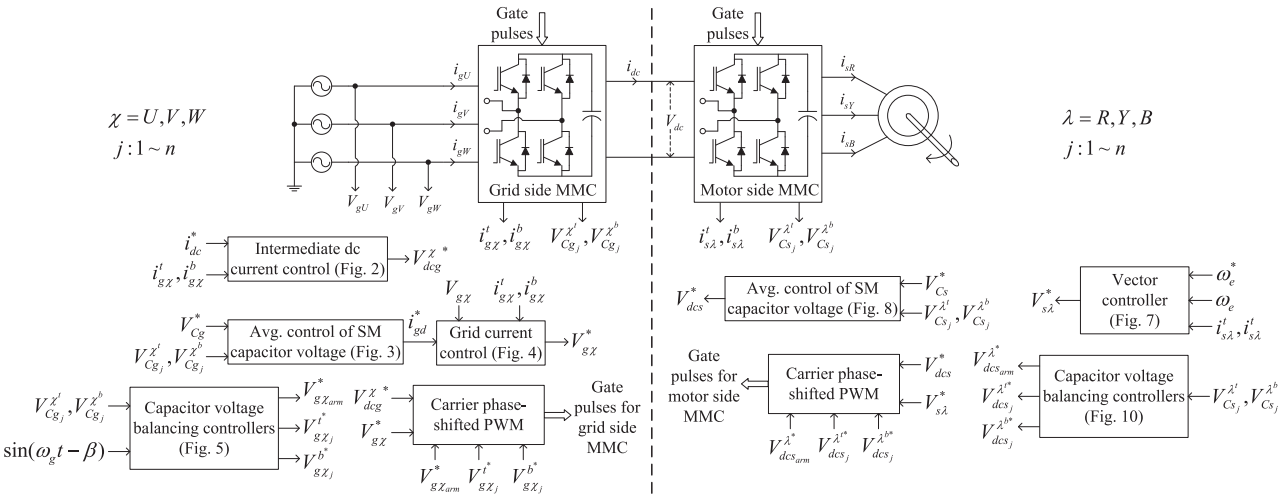

Fig. 12. Complete block diagram of the back-to-back MMC with proposed controllers.

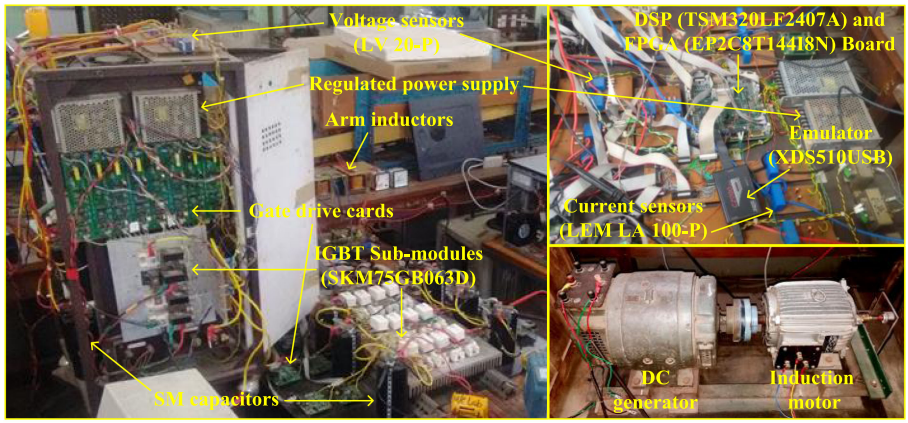

Fig. 13. View of complete experimental setup.

capacitors when balancing control was disabled and enabled after some time. Capacitor voltages are tried to drift away after disabling the balancing controller. However, they regain the desired voltage level when the balancing control is enabled again. Therefore, these waveforms confirm the effectiveness of the proposed balancing strategy for the grid-side MMC. Fig. 14(i) shows the grid voltage and sinusoidal grid current waveforms with the capacitor voltage-balancing controller. They confirm almost unity power factor operation of grid-side MMC. Fig. 14(j) shows the corresponding waveforms of voltages of SM capacitors and dc-link current $i_{\rm dc}$. Here, the dc-link current is maintained at 14 A.

B. Motor-Side MMC Operation With Balancing Control

The performance of balancing controller of motor-side MMC is shown in Fig. 15(a)–(f). Experimental waveforms of SM capacitor voltages of motor-side MMC are shown at different operating conditions. Each SM capacitor voltage is regulated at 200 V. Fig. 15(a) shows that without balancing controller the voltages of SM capacitors drift away when no load is applied to the motor. Fig. 15(b) shows that with the balancing controller, the voltages of SM capacitors are perfectly balanced and maintained at the same value at no load of the motor. Fig. 15(c) shows the drifting of capacitor voltages when the balancing controller is suddenly disabled during normal operation of the drive. Fig. 15(d) shows that the SM capacitor voltages regain the desired voltage level when the balancing control is enabled again. Fig. 15(e) shows the constant input dc-link current $i_{\rm dc}$ when motor load is applied suddenly. Therefore, the dc-link voltage command generated by motor-side MMC increases suddenly as shown in Fig. 15(e). The corresponding SM capacitor voltages of motor-side MMC are shown in Fig. 15(f). The SM capacitor voltages remain approximately constant even after the sudden change in motor load.

C. Operation of the MMC-Based Vector-Controlled Induction Motor Drive for Wide Speed Range

Operation of the vector controlled MMC-based induction motor drive with the proposed capacitor voltage-balancing controllers is shown in Fig. 16. Fig. 16(a)–(c) show the waveforms

TABLE I
SPECIFICATIONS OF EXPERIMENTAL SETUP

ELECTRICAL PARAMETERS FOR GRID SIDE MMC	
Line-to-line rms voltage	220 V
Rated frequency $\omega_g/2\pi$	50 Hz
Output dc-link current i_{dc}^*	14 A
Inductance L_{ag}	3.1 mH
Resistance R_{ag}	0.5 Ω
Capacitance C_s of each SM	4.7 mF
Number of SMs per arm n	2
Carrier frequency f_C	5 kHz
ELECTRICAL PARAMETERS FOR MOTOR SIDE MMC	
Line-to-line rms voltage	220 V
Rated frequency $\omega_s/2\pi$	50 Hz
Input dc-link current i_{dc}^*	14 A
Inductance L_{as}	3.1 mH
Resistance R_{as}	0.5 Ω
Capacitance C_s of each SM	4.7 mF
Number of SMs per arm n	2
Carrier frequency f_C	5 kHz
SPECIFICATIONS OF THE INDUCTION MOTOR	
Rated power P_s	2.5 HP
Rated line-to-line voltage	220 V
Rated line current i_s	7 A
Rated frequency $\omega_s/2\pi$	50 Hz
Number of poles P	4
Rated speed ω_e	1430 r/min
Power factor $\cos\varphi_s$	0.71
SPECIFICATIONS OF THE DC GENERATOR	
Rated power	2 kW
Type	Separately excited
Armature voltage	220 V
Field voltage	220 V
Armature current	9.5 A
Rated speed	1500 r/min

of the drive when the motor is driven at 1 p.u. frequency with rated torque. The intermediate dc current $i_{\rm dc}$ generated by grid-side MMC is shown in Fig. 16(a). Fig. 16(a) shows the actual intermediate dc-link voltage that has ripple due to the PWM operation of two MMCs at front-end and rear-end of the drive. Fig. 16(b) shows the SM capacitor voltages of motor-side MMC. The peak-to-peak voltage ripple of SM capacitor is 4 V. Arm currents and motor current of motor-side MMC are shown in Fig. 16(c). Fig. 16(d)–(f) show the relevant waveforms of the drive when it is operated at 0.5 p.u. frequency with rated load torque. Fig. 16(d) shows the constant intermediate dc-link current $i_{\rm dc}$. As explained earlier, the intermediate dc-link voltage $V_{\rm dc}$ decreases with motor supply frequency ω_s as shown in Fig. 16(d). SM capacitor voltages of motor-side MMC are shown in Fig. 16(e). At this frequency, the SM capacitor peak-to-peak voltage ripple remains at 4 V. The arm currents and the motor current of motor-side MMC are shown in Fig. 16(f). These waveforms confirm that no circulating current is needed to regulate the capacitor voltage ripple. The peak of arm current is the same as that at the base frequency. The drive is operated at 8 Hz and rated torque. The corresponding SM capacitor voltages are shown in Fig. 16(g). At this operating condition, the voltage ripple of the

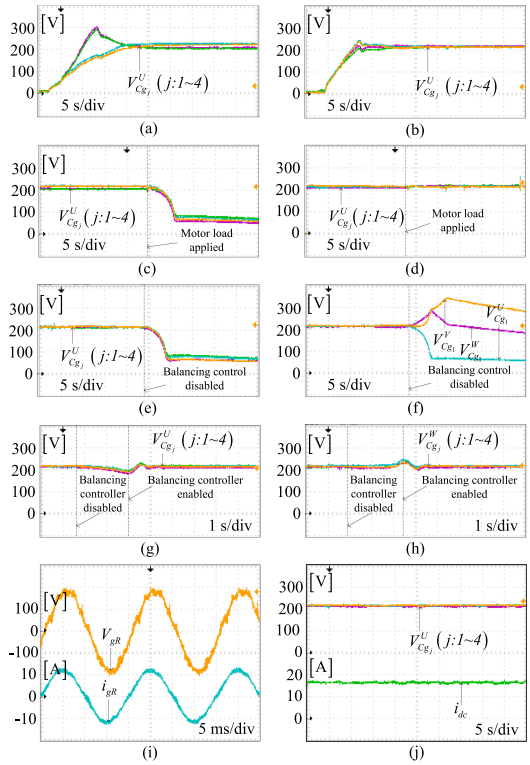

Fig. 14. Experimental waveforms of voltages of SM capacitors of grid-side MMC. Under no motor load condition: (a) without balancing control; (b) with balancing control. When sudden motor load is applied: (c) without balancing control; (d) with balancing control. When balancing control is disabled under motor load condition: (e) SM capacitor voltages of one leg; (f) SM capacitor voltages of three legs. When balancing control is disabled and enabled after some time: (g) SMs of *U*-leg; (h) SMs of *W*-leg. (i) Grid voltage and grid current. (j) SM capacitor voltages and dc-link current.

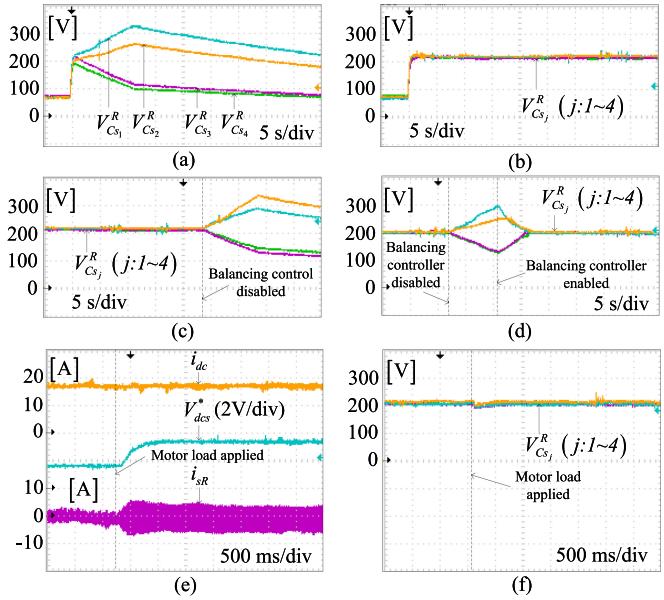

Fig. 15. Experimental waveforms of SM capacitor voltages of motor-side MMC. (a) Without balancing control under no motor load condition. (b) With balancing control under no motor load condition. (c) When balancing control disabled. (d) When balancing control is disabled and enabled after some time. (e) DC-link current, dc-link voltage command, and motor current when sudden motor load is applied. (f) SM capacitor voltages of motor-side MMC when sudden motor load is applied.

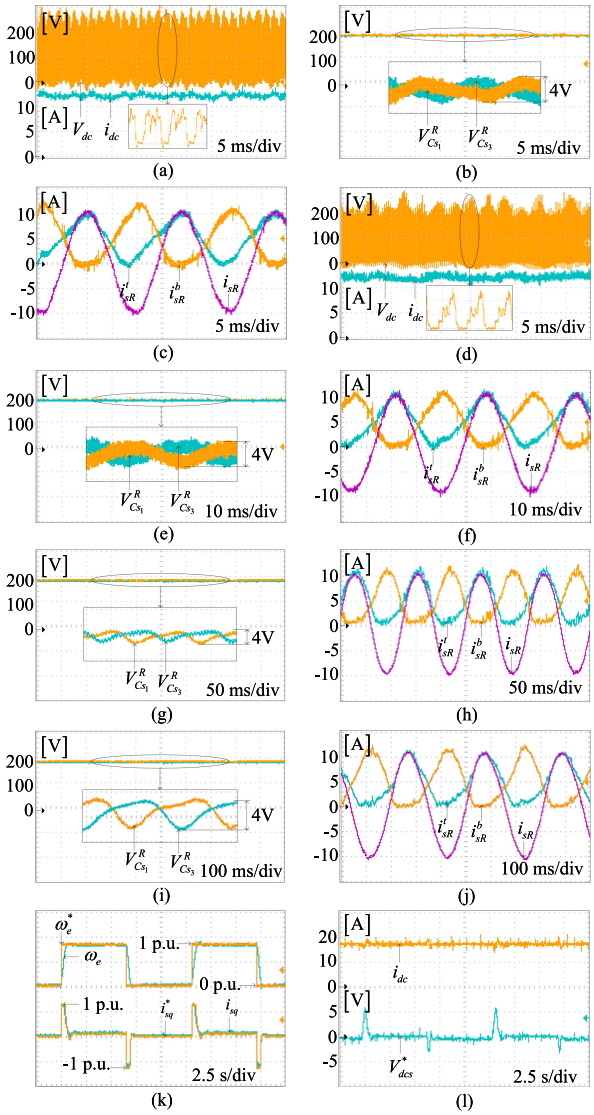

Fig. 16. Experimental waveforms when $\omega_s/2\pi = 51$ Hz and rated torque. (a) Intermediate dc current and dc voltage. (b) SM capacitor voltages of motor-side MMC. (c) Arm currents and motor current of motor-side MMC. Experimental waveforms when $\omega_s/2\pi = 27$ Hz and rated torque. (d) Intermediate dc current and dc voltage. (e) SM capacitor voltages of motor-side MMC. (f) Arm currents and motor current of motor-side MMC. Experimental waveforms when $\omega_s/2\pi = 8$ Hz and rated torque. (g) SM capacitor voltages of motor-side MMC. (h) Arm currents and motor current of motor-side MMC. Experimental waveforms when $\omega_s/2\pi = 3.33$ Hz and rated torque. (i) SM capacitor voltages of motor-side MMC. (j) Arm currents and motor current of motor-side MMC. Experimental waveforms under sudden speed change. (k) Rotor speed and torque current for sudden speed change from 0 to 1 p.u. (l) Intermediate dc current and dc voltage reference.

SM capacitor remains constant at 4 V. The arm currents and the motor current of motor-side MMC are shown in Fig. 16(h). The arm currents show the same peak as base frequency operation of the drive. Finally, this drive is operated at standstill operation with rated torque. At this condition, the motor supply frequency ω_s is 3.33 Hz. The corresponding SM capacitor voltages and arm currents of motor-side MMC are shown in Fig. 16(i) and (j), respectively. The SM capacitor voltages are balanced, and their peak-to-peak voltage ripple remains constant at 4 V, which is the same as that obtained at the base frequency.

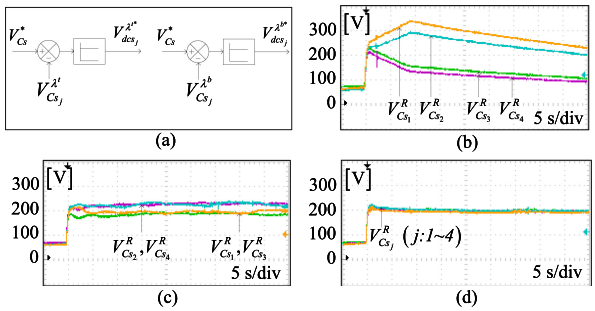

Fig. 17. Experimental SM capacitor voltages of motor-side MMC. (a) Existing individual balancing controller [2]. (b) With existing balancing algorithm when the bandwidth of balancing controller is one order less than averaging controller. (c) With existing balancing controller when the bandwidth of balancing controller is two order less than averaging controller. (d) With proposed balancing algorithm.

The transient operation of this MMC-based drive is shown in Fig. 16(k) and (l). Fig. 16(k) shows the actual rotor speed and the motor torque current when the motor speed command is changed from 0 to 1 p.u. and vice versa. During this large transient, actual motor toque current i_{sq} follows its reference i^*_{sq} very closely as shown in Fig. 16(k).

Fig. 16(l) shows the corresponding intermediate dc current $i_{\rm dc}$ and intermediate dc voltage command $V^*_{\rm dcs}$ of motor-side MMC. Fig. 16(k) and (l) confirm the capability of this MMC-based drive to meet high performance during motor mode and regenerative mode of operations.

D. Comparison of Existing and Proposed Algorithms of Motor-Side MMC

The control block diagram of the existing algorithm in [2] and [20]–[24] is shown in Fig. 17(a). The existing balancing controller uses common voltage reference V^*_{Cs} for both average capacitor voltage controller and individual balancing controller. This algorithm is experimentally applied to the motor-side MMC where its input is constant dc current as shown in Fig. 1. Fig. 17(b) shows that the balancing controller is not able to balance the SM capacitor voltages when its bandwidth is one order lesser than the averaging controller. The SM capacitor voltages diverge and reach the overvoltage limit. This is conformed to the explanation given in the previous sections.

When the bandwidth balancing controller is made two order lesser than the averaging controller, the SM capacitor voltages slowly converge with large differences as shown in Fig. 17(c). However, the capacitor voltages remain balanced during transient and in steady state with the proposed balancing controller as shown in Fig. 7(d). This confirms the need of the proposed balancing controller for back-to-back MMC configuration with intermediate constant current for drive applications.

V. Conclusion

This article has presented voltage balancing controllers for SM capacitors of grid-side and motor-side MMCs. Balancing of individual SM capacitor of grid-side MMC is achieved by drawing a small amount of nonzero reactive current from the

grid. This reactive current does not alter the average voltage V_{Cg}^{av} of SM capacitors of grid-side MMC. With the help of this reactive current, SMs of grid-side MMC draw nonuniform active power from the grid to meet the nonuniform losses of SMs. Thus, uniform capacitor voltages of all the SMs of grid-side MMC are ensured.

Voltage balancing of SM capacitors of motor-side MMC is achieved by applying nonuniform dc voltage commands to the SMs to meet the nonuniform losses of SMs. The proposed strategy does not alter the net voltage command of each leg. It also does not affect the average voltage V_{Cs}^{av} controller for the SM capacitors of motor-side MMC. However, this strategy directs the capacitor voltages of all SMs to the same value. These balancing strategies of grid-side MMC and motor-side MMCs have been verified experimentally at different operating conditions. The overall performance of the drive is validated at different speeds with the proposed balancing controllers. Finally, the experimental comparison of the existing algorithm and the proposed algorithm has been presented. Experimental results confirm that the proposed balancing controllers are necessary for stable operation of the back-to-back MMC-based variable speed drive.

REFERENCES

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bologna Power Tech Conf.*, Jun. 2003, vol. 3, p. 6.

[2] M. Hagiwara and H. Akagi, "Control and experiment of pulse width modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.

[3] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.

[4] A. Korn, M. Winkelnkemper, and P. Steimer, "Low output frequency operation of the modular multi-level converter," in *Proc. IEEE* Energy Convers. Congr. Expo., 2010, pp. 3993–3997.

[5] A. Antonopoulos, L. Ängquist, S. Norrga, K. Ilves, L. Harnefors, and H. -P. Nee, "Modular multilevel converter ac motor drives with constant torque from zero to nominal speed," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1982–1993, May/Jun. 2014.

[6] W. Kawamura, Y. Chiba, M. Hagiwara, and H. Akagi, "Experimental verification of an electrical drive fed by a modular multilevel TSBC converter when the motor frequency gets closer or equal to the supply frequency," *IEEE Trans. Ind. Appl.*, vol. 53, no. 3. pp. 2297– 2306, May/Jun. 2017.

[7] B. Li *et al.*, "An improved circulating current injection method for modular multilevel converters in variable-speed drives," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7215–7225, Nov. 2016.

[8] B. Li, S. Zhou, D. Xu, S. Finney, and B. Williams, "A hybrid modular multilevel converter for medium-voltage variable-speed motor drives," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4619–4630, Jun. 2017.

[9] S. Du, B. Wu, and N. Zargari, "Delta-channel modular multilevel converter for a variable-speed motor drive application," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6131–6139, Aug. 2018.

[10] S. Zhou, B. Li, M. Guan, X. Zhang, Z. Xu, and D. G. Xu, "Capacitance reduction of the hybrid modular multilevel converter by decreasing average capacitor voltage in variable-speed drives," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1580–1594, Feb. 2019.

[11] K. Wang, Y. Li, Z. Zheng, and L. Xu, "Voltage balancing and fluctuation suppression method of floating capacitors in a new modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 60, no. 5, pp. 1943–1954, May 2013.

[12] J. Kolb, F. Kammerer, M. Gommeringer, and M. Braun, "Cascaded control system of the modular multilevel converter for feeding variable-speed drives," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 349–357, Feb. 2015.

[13] S. Debnath, J. Qin, and M. Saeedifard, "Control and stability analysis of modular multilevel converter under low-frequency operation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5329–5339, Sep. 2015.

[14] J.-J. Jung, H.-J. Lee, and S.-K. Sul, "Control strategy for improved dynamic performance of variable-speed drives with the modular multilevel converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 2, pp. 371–380, Jun. 2015.

[15] A. Dekka, B. Wu, R. L. Fuentes, M. Perez, and N. R. Zargari, "Voltage-balancing approach with improved harmonic performance for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 5878–5884, Aug. 2017.

[16] L. Luo, Y. Zhang, L. Jia, and N. Yang, "A novel method based on self-power supply control for balancing capacitor static voltage in MMC," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1038–1049, Feb. 2018.

[17] Y. Li, E. A. Jones, and F. Wang, "The impact of voltage-balancing control on switching frequency of the modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2829–2839, Apr. 2016.

[18] R. Darus, J. Pou, G. Konstantinou, S. Ceballos, R. Picas, and V. G. Agelidis, "A modified voltage balancing algorithm for the modular multilevel converter: Evaluation for staircase and phase-disposition PWM," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4119–4127, Aug. 2015.

[19] D. Siemaszko, "Fast sorting method for balancing capacitor voltages in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 463–470, Jan. 2015.

[20] M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel PWM inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1786–1799, Jul. 2010.

[21] M. Hagiwara, I. Hasegawa, and H. Akagi, "Start-up and low-speed operation of an electric motor driven by a modular multilevel cascade inverter," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1556–1565, Jul./Aug. 2013.

[22] Y. Okazaki, M. Hagiwara, and H. Akagi, "A speed-sensorless start-up method of an induction motor driven by a modular multilevel cascade inverter (MMCI-DSCC)," *IEEE Trans. Ind. Appl.*, vol. 50, no. 4, pp. 2671–2680, Jul./Aug. 2014.

[23] S. Du, B. Wu, K. Tian, N. R. Zargari, and Z. Cheng, "An active cross-connected modular multilevel converter (AC-MMC) for a medium-voltage motor drive," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 4707–4717, Aug. 2016.

[24] M. Abdelsalam, M. Marei, S. Tennakoon, and A. Griffiths, "Capacitor voltage balancing strategy based on sub-module capacitor voltage estimation for modular multilevel converters," *CSEE J. Power Energy Syst.*, vol. 2, no. 1, pp. 65–73, Mar. 2016.

[25] A. Dekka, B. Wu, N. R. Zargari, and R. L. Fuentes, "A space-vector PWM-based voltage-balancing approach with reduced current sensors for modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2734–2745, May 2016.

[26] F. Deng and Z. Chen, "Voltage-balancing method for modular multilevel converters under phase-shifted carrier-based pulsewidth modulation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4158–4169, Jul. 2015.

[27] Y. S. Kumar and G. Poddar, "Control of medium voltage ac motor drive for wide speed range using modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2742–2749, Apr. 2017.

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