Active Saturation Mitigation in High-Density Dual-Active-Bridge DC–DC Converter for On-Board EV Charger Applications

Seyed Amir Assadi, *Student Member, IEEE*, Hirokazu Matsumoto, *Member, IEEE*, Mazhar Moshirvaziri, *Member, IEEE*, Miad Nasr, Mohammad Shawkat Zaman, *Student Member, IEEE*, and Olivier Trescases, *Senior Member, IEEE*

***Abstract*—This article presents a transformer saturation prevention algorithm (SPA) targeting dual-active-bridge (DAB) dc–dc converters utilized in bidirectional, two-stage electric vehicle (EV) on-board battery chargers. Saturation prevention is achieved by detecting the variation in transformer current slope near the boundary of saturation and applying duty-cycle offsets to the DAB converter full bridges. Compared to alternative methods of saturation mitigation, the proposed algorithm offers the following benefits: Lower transformer design safety margins which enable volume reduction with minimal harm to efficiency, and low-cost implementation using a single low-cost current sensor even at high converter switching speeds. Experiments on a custom 6.6-kW on-board EV charger confirm the controller functionality and initial converter analysis. A peak converter efficiency of 96.8% with a transformer volume of 80 cm^3 is achieved, which is a 50% volume reduction in comparison to other academic works.**

***Index Terms*—Battery chargers, converters, dc–dc power conversion, digital control, ferrites, field programmable gate arrays, power electronics, transformers, vehicles.**

I. Introduction

ADVANCEMENTS in control techniques and semiconductor technologies have enabled the cost-effective use of bidirectional power electronics in automotive applications. Bidirectional power capability expands the functionality of conventional on-board chargers (OBCs) to include vehicle-to-grid (V2G) [2] and vehicle-to-vehicle (V2V) [3] operation. Bidirectional OBCs often use a two-stage architecture, consisting of a dc–ac and dc–dc converter, as shown in Fig. 1. The dc–ac converter is responsible for power-factor correction, while the dc–dc converter implements a battery charging algorithm, and provides galvanic isolation using a high-frequency transformer.

Manuscript received March 6, 2019; revised May 27, 2019; accepted August 19, 2019. Date of publication September 2, 2019; date of current version January 10, 2020. This work was supported in part by the Natural Sciences and Engineering Research Council of Canada and Havelaar Canada. Recommended for publication by Associate Editor R. Zane. *(Corresponding author: Seyed Amir Assadi.)*

The authors are with the University of Toronto, Toronto, ON M5S 3G4, Canada (e-mail: amir.assadi@mail.utoronto.ca; hmatsumoto@aoyagakuin.jp; m.moshirvaziri@gmail.com; miad.nasr@utoronto.ca; Shawkat.Zaman@utoronto.ca; ot@ece.utoronto.ca).

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Digital Object Identifier 10.1109/TPEL.2019.2939301

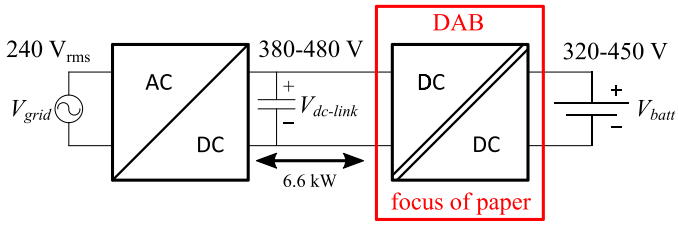

Fig. 1. Conventional two-stage OBC. The focus of this article is the saturation mitigation of the transformer in the isolated DAB converter.

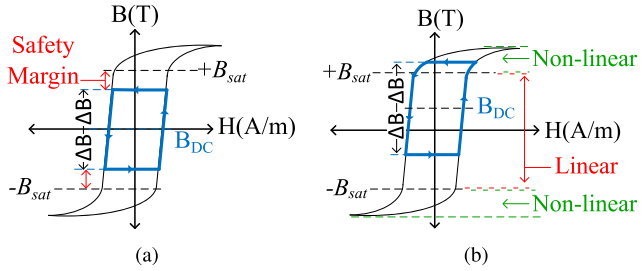

Fig. 2. Typical ferrite BH curve with (a) $B_{\text{dc}} = 0$ and (b) nonzero B_{dc}. The bold blue path outlines the traversed B in a DAB converter.

This article focuses on the saturation mitigation of a transformer in a dual-active-bridge (DAB) converter with a target efficiency of 97%, used as the dc–dc stage of a bidirectional, 6.6-kW electric vehicle (EV) OBC. The OBC charges an EV battery with a voltage V_{batt} between 320 and 450 V, from a dc link with a voltage $V_{\text{dc-link}}$ between 380 and 480 V. Emerging wide-bandgap, high-voltage silicon carbide (SiC) devices offer the opportunity to shrink converters by scaling up the switching frequency $f_s = \frac{1}{T_s}$, and reducing the size of passive components. An increase in f_s reduces the magnetic flux density swing ΔB, and the transformer core volume, while maintaining a high safety margin to avoid saturation. The transformer safety margin is defined as the difference between ΔB and saturation flux density B_{sat}, as shown in Fig. 2. A sufficiently large magnetic flux density offset B_{dc} can push the transformer operation into saturation, in the nonlinear region of the core BH curve, as shown. As the magnetic flux density B increases to near B_{sat} in ferrimagnetic cores, the permeability μ_r gradually changes nonlinearly

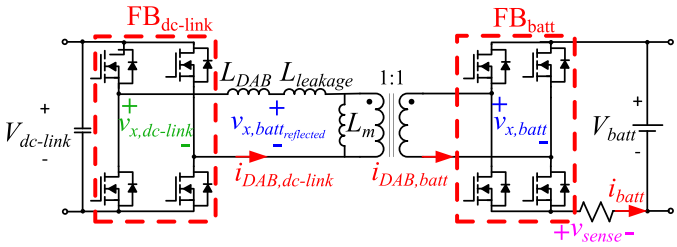

Fig. 3. DAB converter topology. i_{DAB} referred to FB$_{\text{dc-link}}$ is labeled $i_{\text{DAB,dc-link}}$ (similar for $i_{\text{DAB,batt}}$).

resulting in a slow change in current slope. Under saturation, this change in slope results in large current spikes, increased losses, and potentially irreversible damage in the dc–dc converter. The application of nonzero net volt-seconds by the DAB converter full bridges (FBs), results in a nonzero transformer B_{dc}, which is exacerbated by the utilization of superior Figure of Merit devices due to a lower on-resistance. Mismatch in device parameters and tolerances contribute to the nonideal volt-seconds, while conduction path resistance dampens their impact on B_{dc}.

The DAB converter volume and efficiency relies on the choice of f_s, ΔB, and core volume. A passive or active saturation mitigation technique is required to protect the DAB transformer from saturation in situations with low safety margin and high B_{dc}. Existing state-of-the-art techniques require costly additional circuitry, do not provide a safe range of ΔB up to B_{sat}, and in some cases, are not readily compatible with mass production, as described in Sections I-A and I-B.

This article proposes a saturation prevention algorithm (SPA) that requires no additional sensors, while providing a safe ΔB range close to B_{sat}. The SPA calculates the instantaneous slope of $i_{\text{DAB,batt}}$, through the measurement of i_{batt} at twice the switching frequency. Through the self-reference of current slope measurements, the onset of saturation is detected regardless of converter power level, and corrective action is taken by the SPA.

The DAB operating principles are briefly described in Section II, including an analysis of transformer saturation safety margin. The minimum transformer size for a target efficiency of 97% is presented in Section III through volume and efficiency analysis. The SPA methodology and implementation are described in Section IV. Experimental validation and benchmark comparisons are presented in Section VI.

A. State-of-the-Art Passive Mitigation Techniques

In passive saturation mitigation techniques, additional passive components or an overdesign of the transformer accommodate the nonzero net volt-seconds. In [4], the dc currents flowing through the transformer windings, $< i_{\text{DAB,batt}} >_{T_s}$, and $< i_{\text{DAB,dc-link}} >_{T_s}$, are blocked by capacitors. In comparison with the $i_{\text{DAB,batt}}$ and $i_{\text{DAB,dc-link}}$ waveforms from the DAB converter of Fig. 3, the incorporation of a small series capacitance increases the peak inductor current and semiconductor switching device rating. For the DAB converter defined in Fig. 1, 15 μF of series capacitance on each transformer winding protects the transformer without increasing the switching device rating. The large capacitance ensures a low steady-state capacitor operating voltage, though sufficient voltage safety margin is necessary for load transients and start-up (making ceramic capacitors a costly option). To meet thermal ratings, capacitors must be placed in parallel [5]–[7]. The high current and switching frequency required from dc-blocking capacitors in an EV OBC result in additional volume and increased cost. For example, using four FFB14D0336K capacitors significantly exceeds the minimum capacitance and the operation voltage required, but only just meets the thermal requirements. The volume of these four capacitors at 36 cm^3 is approximately equal to the transformer core box volume. In [8], a safety-margin of 20% with respect to B_{sat} is incorporated by using a large core and air gaps.

B. State-of-the-Art Active Mitigation Techniques

Active saturation mitigation is achieved through the application of corrective net volt-seconds. In [9], a custom core redirects flux to a sense winding off of the main flux path when the core is saturated. In [10], B_{dc} is measured through the connection and perturbation of an external ferrite loop. The coupling between the external ferrite and the main core is complex and expensive for mass production. In [11], Hall Effect sensors placed in the transformer air gaps measure B_{dc}, while harming efficiency by reducing the transformer magnetizing inductance. In [12] and [13], $< i_{\text{DAB,batt}} >_{T_s}$, $< i_{\text{DAB,dc-link}} >_{T_s}$, and subsequent B_{dc} are regulated to near zero, through duty cycle and current-mode control, respectively. Despite the additional control overhead, [12] is not able to guarantee complete B_{dc} elimination for all operating points. Furthermore, [12] requires two additional sensors, sampling circuitry, and subsequent signal isolation, which increases the cost. Shunt resistor based sensors that are capable of detecting the current in the transformer winding are expensive compared to the overall converter cost and have a low bandwidth due to the high common-mode voltage tolerance requirement. High-bandwidth hall-effect sensors are similarly expensive. In [14], it is shown that the transformer B_{dc} can be reduced with zero-voltage switching implemented through precise dead time, which requires additional sensing circuitry.

II. Dual-Active Bridge

A. Operation Principles

The galvanically isolated DAB converter consists of two FBs connected by an inductor and transformer. Each FB generates voltages $v_{x,\text{dc-link}}$ and $v_{x,\text{batt}}$, as shown in Fig. 3. The magnitude and direction of power flow P_{DAB} is determined by the magnitude and polarity of phase-shift φ between each FB, as given by

$$P_{\text{DAB}} = \frac{V_{\text{batt}} V_{\text{dc-link}}}{n_{1,2} 2\pi f_s (L_{\text{DAB}} + L_{\text{leakage}})} \varphi \left(1 - \left|\frac{\varphi}{\pi}\right|\right) \quad (1)$$

where $n_{1,2}$ is the transformer turns ratio, L_{leakage} is the transformer leakage inductance, and L_{DAB} is the inductor placed in series with the transformer [15]. In this application, $V_{\text{dc-link}}$ is

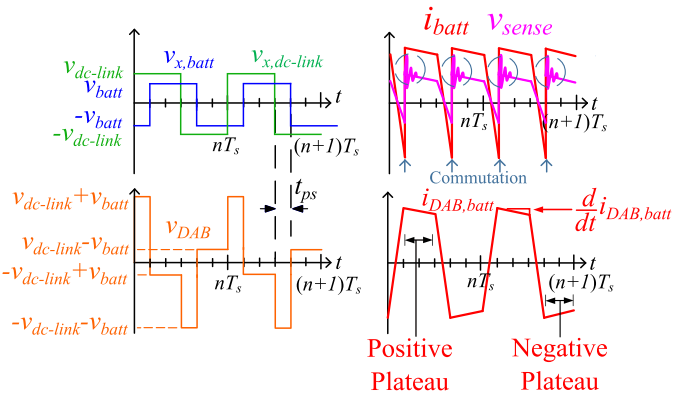

Fig. 4. Waveforms of $v_{x,\text{dc-link}}$, v_{sense}, $v_{x,\text{batt}}$, v_{DAB}, i_{batt}, and $i_{\text{DAB,batt}}$. During t_{ps}, $|v_{\text{DAB}}| \approx |V_{\text{dc-link}}| + |V_{\text{batt}}|$. In the plateau, $|v_{\text{DAB}}| \approx |V_{\text{dc-link}}| - |V_{\text{batt}}|$.

controlled by the dc–ac converter, while V_{batt} is dependent on the battery state of charge (SOC).

The rate of change of the current flowing through the inductor (assuming a 1:1 transformer), is approximated by

$$\frac{d}{dt}i_{\text{DAB,dc-link}} \approx \frac{d}{dt}i_{\text{DAB,batt}} \approx \frac{v_{\text{DAB}}}{L_{\text{DAB}} + L_{\text{leakage}}} \tag{2}$$

where

$$v_{\text{DAB}} = v_{x,\text{dc-link}} - v_{x,\text{batt}} \tag{3}$$

as shown in Fig. 4. With T_s as the switching period, the time delay between the leading and lagging FB t_{ps} is given by

$$t_{ps} = T_s \frac{\varphi}{2\pi}. \tag{4}$$

B. Transformer B_{dc}

The ΔB of the DAB transformer in Fig. 3 is given by

$$\Delta B = \frac{1}{nA_e} \int_{t+\frac{T_s}{4}}^{t} V_{\text{batt}} dt \tag{5}$$

where A_e is the core cross-section area, and n is the number of turns in the transformer. In general, ΔB is directly proportional to V_{batt} and $V_{\text{dc-link}}$, and inversely proportional to transformer size and f_s. Galvanically isolated converters that lack dc-blocking capacitors, such as the DAB, do not inherently prevent dc current in the transformer windings. The dc current in the FB_{batt} connected winding is approximated by

$$< i_{\text{DAB,batt}} >_{T_s} = \frac{\Delta D \cdot 2 \cdot V_{\text{batt}}}{R_{\text{dc}}} \tag{6}$$

where the net volt-seconds applied to the transformer is a function of V_{batt}, and ΔD is the equivalent mismatched duty cycle applied to FB_{batt}, while R_{dc} is the total resistance of the FB_{batt} conduction path. The equation for $< i_{\text{DAB,dc-link}} >_{T_s}$ is defined similarly to (6). The subsequent B_{dc} is given by

$$B_{\text{dc}} = \frac{n(< i_{\text{DAB,batt}} >_{T_s} + < i_{\text{DAB,dc-link}} >_{T_s})}{\mathscr{R}_c A_e} \tag{7}$$

where $\mathscr{R}_c$ is the core reluctance.

III. DAB Volume and Efficiency Analysis

In high-density applications, the power loss of a specific component is as important as the overall converter loss. The DAB is designed to achieve the following:

1) small transformer volume and loss, through the choice of ΔB and f_s;
2) sufficiently low switching loss to reduce overhead for switching-device liquid cooling.

To reduce the switching loss, the high-frequency converter requires a low power loop inductance. The choice of surface-mount devices reduces the loop inductance of the converter, while making cooling much more difficult. Leveraging the availability of liquid cooling in EVs, the large surface area of the transformer provides a relatively easy means of cooling through potting. Therefore, a design that results in a higher transformer loss and lower switching loss can benefit from a reduced overall cooling overhead. The tradeoff between MOSFET and transformer losses is balanced through the choice of transformer wire gauge, core material, core temperature, f_s, ΔB, and core volume. A peak coolant temperature of 50 °C is assumed in this design.

A. Wire Loss Versus Wire Gauge

Litz wire is used in this application due to the high-frequency operation. The choice of 40 AWG strand wire (79 μm diameter) greatly reduces the skin effect within the potential converter frequency range of 100–300 kHz, which corresponds to a skin depth of 200–120 μm. The 10 AWG lumped wire gauge ensures that the temperature of the wire does not exceed the insulation rating, while considering the incorporation of the ferrite core loss, and the chill plate temperature. The optimization of lumped wire gauge based on temperature and loss is a further potential dimension of design.

B. Core Loss Versus Core Material

The transformer material is chosen based on the performance factor [16] $\mathcal{P}$ as given by

$$\mathcal{P} = f_s \cdot \Delta B. \tag{8}$$

When comparing multiple ferrite materials against f_s, for the same loss density, the ferrite with the highest $\mathcal{P}$ can sustain the highest ΔB without saturating. A transformer using this material requires the fewest number of turns to sustain a high voltage, thereby making it an ideal choice for the DAB converter. The $\mathcal{P}$ of various ferrites from the manufacturer TDK is shown in Fig. 5. For frequencies below 300 kHz, N97 material yields the highest $\mathcal{P}$ at 90 °C over the majority range of core loss densities characterized by TDK.

C. Core Loss Versus Core Temperature

The core temperature is chosen to minimize core loss, while respecting wire temperature insulation ratings, as described in the following.

1) *Core Loss*
   In ferrites, the temperature at which the second maximum of permeability occurs T_{SMP} corresponds to a minimum

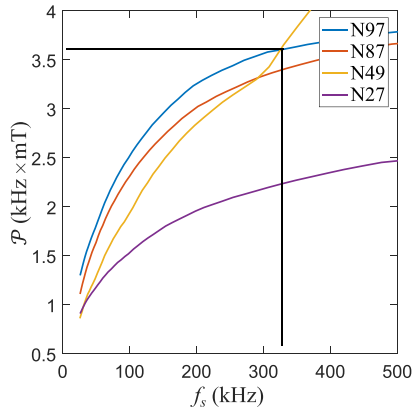

Fig. 5. Performance factor $\mathcal{P}$ for N97, N87, N49, N27 ferrites from TDK, at 90 °C with a loss density of 550 kW/m^3.

core loss, which is unique for each material [17], [18]. The DAB transformer is designed with N97 material whose $T_{SMP} \approx 80°\text{C}-90°\text{C}$, which is below the wire insulation rating.

2) *Saturation Magnetic Flux Density*
Core saturation magnetization, and hence B_{sat}, reduces as the temperature rises to the Curie temperature. For N97 material, B_{sat} decreases from 510 to 410 mT, as temperature rises from 25°C to 100°C [19].

D. Core Loss Versus f_s, ΔB, and Volume

The core loss of a transformer is linearly proportional to volume, while the Steinmetz approximation is often used to define the relationship with f_s and ΔB. The choice of f_s and ΔB is a tradeoff between the core loss density, the eddy current loss of the ferrite, and the area of the BH loop that is traversed. The core volume presents a tradeoff between ΔB and the total transformer loss. In Section III-B, N97 material is chosen based on the desired range of frequencies. The material datasheet [19], however, does not provide core loss data for the operating conditions, $f_s > 50$ kHz and $\Delta B > 200$ mT. The resonant core loss measurement scheme that is described in [20] was used in conjunction with a thermal chamber test environment to measure the N97 core loss properties. Measurements are conducted using a high bandwidth current sensor and amplifier.

E. Complete Converter Loss Analysis

For a target converter loss, the smallest N97 transformer that operates with the lowest f_s and ΔB can achieve the conditions that are described at the start of Section III. The total loss for the DAB converter, including switching, conduction, core and eddy current loss, is modeled for the analysis. The switching loss model is linearly proportional to f_s and independent of ΔB, according to [21]. The cumulative eddy current and core loss density that are measured in Section III-D are extrapolated for cores of different volumes. The ETD family of cores are considered for this analysis. The calculated total converter loss at rated power over the design space is shown in Fig. 6(a).

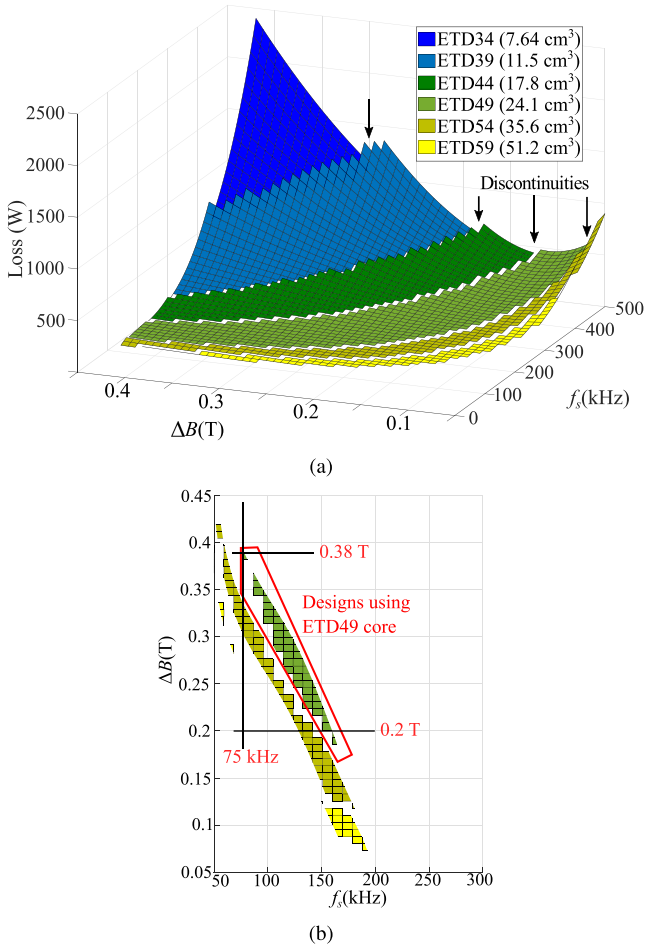

Fig. 6. (a) Calculated total converter loss versus ΔB and f_s. (b) Converter designs that result in a total converter loss of 198 W.

TABLE I
DAB TRANSFORMER SPECIFICATIONS

Parameter	Value	Unit
Operation frequency	125	kHz
Power	6.6	kW
Turns ratio	1:1.08 ≈ 11.5:12.5	
ΔB	0.37	T
Volume:		
core (ETD49, N97)	40.3	cm^3
+ windings =	80	cm^3
+ cooling pot =	117.9	cm^3

The granularity of standard core sizes within a family results in discontinuities over the design space.

The design space that satisfies a target converter loss of 198 W (97% efficiency) is shown in Fig. 6(b). The smallest core, ETD49, is possible with a converter $f_s > 75$ kHz and core 0.2 T$< \Delta B <$ 0.38 T. Portions of the ETD49 core design space operate transformers with a low safety margin. The transformer and converter specifications summarized in Tables I and II were chosen to test the proposed SPA under conditions where

TABLE II
DAB CONVERTER AND SPA SPECIFICATIONS

Parameter	Value	Unit
$V_{dc-link}$	380-480	V
V_{batt}	320-450	V
Peak power	6.6	kW
Transformer	See Table I	
Switching frequency	125	kHz
DAB inductance	10	μH
MOSFET	C3M0065090J	
Controller	Xilinx Spartan 6	
ADC:		
sample rate	1	Msps
resolution	12	bit
Diff amp bandwidth	200	MHz
SPA:		
$\lvert\Delta m\rvert$ threshold	0.813	A/μs
K	24.2	-
$\lvert\Delta m_d\rvert$ threshold	20	12-bit base

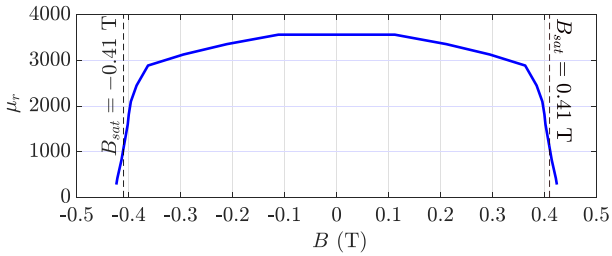

Fig. 7. Calculated μ_r from measured B and H for N97 ferrite. $|B_{\text{sat}}| = 0.41$ T [19].

algorithms that rely on the measurement of the dc component of current or B cannot operate effectively, namely at the edge of saturation and at a high switching frequency.

IV. TRANSFORMER SATURATION AND $i_{\text{DAB,BATT}}$

Voltage difference between $V_{\text{dc-link}}$ and V_{batt} appear across the inductor placed between $\text{FB}_{\text{dc-link}}$ and the transformer. The B waveform resulting from (5) is triangular with the positive peak corresponding to the end of the positive $i_{\text{DAB,batt}}$ plateau and the negative peak corresponding to the end of the negative plateau. For a transformer designed with $|\Delta B| < |B_{\text{sat}}|$, positive saturation occurs when $(B + B_{\text{dc}}) > +B_{\text{sat}}$, while negative saturation occurs when $(B - B_{\text{dc}}) < -B_{\text{sat}}$. Core saturation results in a sharp drop in μ_r as shown in Fig. 7.

With l as the magnetic path length, and $\mathcal{F}$ as the magnetomotive force, $|v_{x,\text{batt}_{\text{reflected}}}|$ is expressed by

$$|v_{x,\text{batt}_{\text{reflected}}}| = \left| \frac{nA_e\mu_r\mu_o}{l}\frac{d}{dt}\mathcal{F} + n\mathcal{F}\frac{d}{dt}\frac{\mu_o\mu_r A_e}{l} \right| \quad (9)$$

which decreases under saturation. With $L_{\text{DAB}} \gg L_{\text{leakage}}$, the slope of $i_{\text{DAB,batt}}$ and $i_{\text{DAB,dc-link}}$ is approximated by

$$\frac{d}{dt} i_{\text{DAB,batt}} \approx \frac{d}{dt} i_{\text{DAB,dc-link}} \approx \frac{v_{x,\text{dc-link}} - v_{x,\text{batt}_{\text{reflected}}}}{L_{\text{DAB}}}. \quad (10)$$

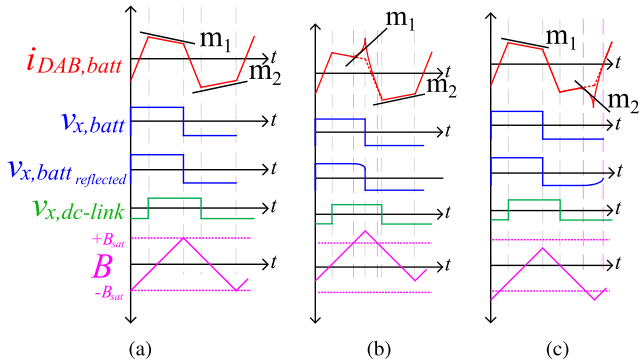

Fig. 8. Waveforms of $v_{x,\text{dc-link}}$, $v_{x,\text{batt}}$, $v_{x,\text{batt}_{\text{reflected}}}$, $i_{\text{DAB,batt}}$, and B when the core is (a) not saturating, saturating (b) positively, and (c) negatively.

As a result, saturation initially appears as a sharp change at the end of the negative and positive plateau of $i_{\text{DAB,batt}}$, as shown in Fig. 8. The subscript 1 refers to terms that correspond to the end of the positive plateau while subscript 2 refers to those corresponding to the end of the negative plateau. The SPA defines the slope $m_1 = \frac{d}{dt} i_{\text{DAB,batt}}$ at the end of the positive plateau and $m_2 = -\frac{d}{dt} i_{\text{DAB,batt}}$ at the end of the negative plateau. Slope m_1 changes under positive saturation and m_2 changes under negative saturation, as shown in Figs. 8(b) and 8(c), respectively. These changes in current slope are not prominent in $i_{\text{DAB,dc-link}}$ as the DAB inductor resists the sharp changes in current that occur during saturation. The SPA deduces the polarity of saturation from Δm, which is defined as

$$\Delta m = m_1 - m_2. \quad (11)$$

Three assumptions simplify the derivation of Δm.

1) For simplicity, $i_{\text{DAB,batt}}$ and $i_{\text{DAB,dc-link}}$ have a similar magnitude and slope. For transformers with a nonunity turns ratio, the variable n can be replaced with the respective turns of the primary and secondary.
2) Negative feedback of the current through L_{DAB} prevents the effect of saturation from appearing in $i_{\text{DAB,dc-link}}$.
3) At the boundary of saturation, $\mathcal{R}_{c,1} \approx \mathcal{R}_{c,2}$. This is an approximation, since saturation is a gradual occurrence.

To solve for Δm, the voltage applied by FB_{batt} is first expressed in terms of the net transformer B

$$\begin{aligned} v_{x,\text{batt}} &= nA_e\frac{d}{dt}B \\ &= n\frac{d}{dt}\frac{(ni_{\text{DAB,batt}} - ni_{\text{DAB,dc-link}})}{\mathcal{R}_c} \\ &= \frac{n^2}{\mathcal{R}_c}\frac{d}{dt}(i_{\text{DAB,batt}} - i_{\text{DAB,dc-link}}) \\ &\quad + n^2(i_{\text{DAB,batt}} - i_{\text{DAB,dc-link}})\frac{d}{dt}\frac{1}{\mathcal{R}_c} \\ &= \frac{n^2}{\mathcal{R}_c}\frac{d}{dt}(i_{\text{DAB,batt}}) - \frac{n^2}{\mathcal{R}_c}\frac{d}{dt}(i_{\text{DAB,dc-link}}) \\ &\quad - \frac{n^2}{\mathcal{R}_c^2} i_{\text{M}}\frac{d}{dt}\mathcal{R}_c \end{aligned} \quad (12)$$

where i_{M} is the transformer magnetizing current, and $\mathscr{R}_c$, $i_{\mathrm{DAB,batt}}$ and $i_{\mathrm{DAB,dc-link}}$ vary with time. In (12), both $i_{\mathrm{DAB,batt}}$ and $i_{\mathrm{DAB,dc-link}}$ are decomposed into a *sat* component that is influenced by transformer saturation (0 when the core is not saturating), and a *plateau* component that represents the power-flow current

$$\begin{aligned} v_{x,\mathrm{batt}} = &\frac{n^2}{\mathscr{R}_c}\frac{d}{dt}(i_{\mathrm{DAB,batt,sat}} + i_{\mathrm{DAB,batt,plateau}}) \\ &- \frac{n^2}{\mathscr{R}_c}\frac{d}{dt}(i_{\mathrm{DAB},dc-\mathrm{link,sat}} + i_{\mathrm{DAB,dc-link,plateau}}) \\ &- \frac{n^2}{\mathscr{R}_c^2} i_{\mathrm{M}} \frac{d}{dt}\mathscr{R}_c. \end{aligned} \tag{13}$$

Applying assumptions 1 and 2 to (13) results in

$$v_{x,\mathrm{batt}} = \frac{n^2}{\mathscr{R}_c}\frac{d}{dt}(i_{\mathrm{DAB,batt,sat}}) - \frac{n^2}{\mathscr{R}_c^2} i_{\mathrm{M}} \frac{d}{dt}\mathscr{R}_c. \tag{14}$$

Rearranging (14) in terms of $i_{\mathrm{DAB,batt,sat}}$

$$\frac{d}{dt} i_{\mathrm{DAB,batt,sat}} = v_{x,\mathrm{batt}} \frac{\mathscr{R}_c}{n^2} + \frac{1}{\mathscr{R}_c} i_{\mathrm{M}} \frac{d}{dt}\mathscr{R}_c. \tag{15}$$

From the perspective of R_{sense}, m_1 can be found by solving (15) for saturation at the end of the positive $i_{\mathrm{DAB,batt}}$ plateau and by substituting $v_{x,\mathrm{batt}} = V_{\mathrm{batt}}$

$$m_1 = V_{\mathrm{batt}} \frac{\mathscr{R}_{c,1}}{n^2} + \frac{1}{\mathscr{R}_{c,1}} i_{\mathrm{M},1} \frac{d}{dt}\mathscr{R}_{c,1} \tag{16}$$

and similarly for m_2. Δm is subsequently expressed as

$$\Delta m = \frac{d}{dt} i_{\mathrm{DAB,batt,sat},1} - \frac{d}{dt} i_{\mathrm{DAB,batt,sat},2}. \tag{17}$$

The substitution of (16) and similar for m_2 into (11) results in

$$\begin{aligned} \Delta m = &V_{\mathrm{batt}} \frac{\mathscr{R}_{c,1}}{n^2} + \frac{1}{\mathscr{R}_{c,1}} i_{\mathrm{M},1} \frac{d}{dt}\mathscr{R}_{c,1} \\ &- V_{\mathrm{batt}} \frac{\mathscr{R}_{c,2}}{n^2} - \frac{1}{\mathscr{R}_{c,2}} i_{\mathrm{M},2} \frac{d}{dt}\mathscr{R}_{c,2}. \end{aligned} \tag{18}$$

The application of assumption 3 simplifies (18) to

$$\Delta m = \frac{1}{\mathscr{R}_{c,1}} i_{\mathrm{M},1} \frac{d}{dt}\mathscr{R}_{c,1} - \frac{1}{\mathscr{R}_{c,2}} i_{\mathrm{M},2} \frac{d}{dt}\mathscr{R}_{c,2}. \tag{19}$$

The reluctance, $\mathscr{R}_{c,1}$ changes only under positive saturation while $\mathscr{R}_{c,2}$ only changes under negative saturation. Therefore, under a negative B_{dc}, $\frac{d}{dt}\mathscr{R}_{c,1} \approx 0$ and Δm is given by

$$\Delta m \approx -\frac{1}{\mathscr{R}_{c,2}} i_{\mathrm{M},2} \frac{d}{dt}\mathscr{R}_{c,2}. \tag{20}$$

Under a positive B_{dc}, $\frac{d}{dt}\mathscr{R}_{c,2} \approx 0$ and Δm is given by

$$\Delta m \approx \frac{1}{\mathscr{R}_{c,1}} i_{\mathrm{M},1} \frac{d}{dt}\mathscr{R}_{c,1}. \tag{21}$$

The magnitude of Δm is expressed as

$$|\Delta m| \approx \frac{1}{\mathscr{R}_c} i_{\mathrm{M}} \frac{d}{dt}\mathscr{R}_c \tag{22}$$

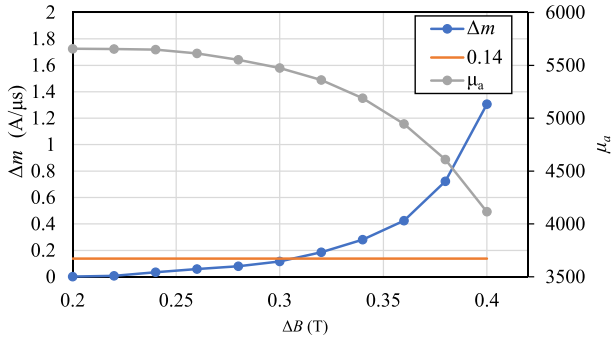

Fig. 9. Permeability μ_a and calculated Δm corresponding to ΔB.

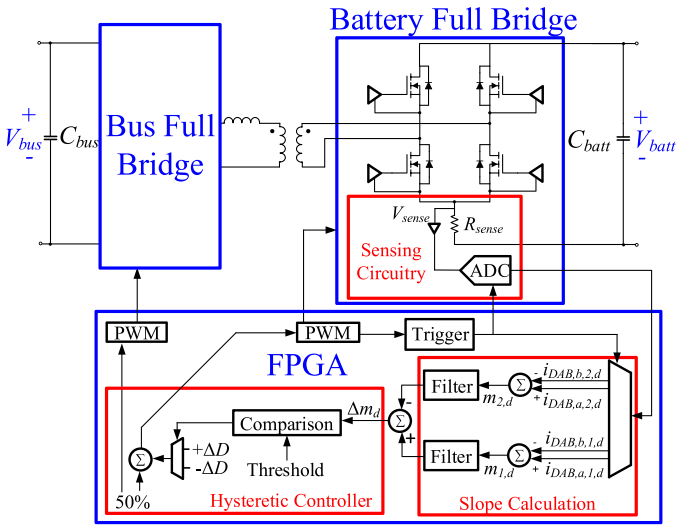

Fig. 10. DAB converter and SPA architecture.

where

$$i_{\mathrm{M}} = \frac{\mathscr{R}_c}{n^2} \int_{t+\frac{T_S}{4}}^{t} V_{\mathrm{batt}} dt. \tag{23}$$

Δm is shown in Fig. 9 for $\Delta B > 200$ mT, for an ETD49, N97 core.

V. SPA and Implementation

A simplified diagram of the digital controller and the respective flow chart are shown in Figs. 10 and 11.

A sense resistor at the base of $\mathrm{FB_{batt}}$ is used to measure i_{batt}, as shown in Fig. 4. Samples of i_{batt} are taken two times every switching cycle and stored in an array, $i_{\mathrm{DAB},d}\{\}$ using a 12-bit analog-to-digital converter (ADC), as shown in step A of Fig. 11. The samples are taken synchronous to the gating signal of $\mathrm{FB_{batt}}$, $\mathrm{FB_{batt,gating}}$, with a constant offset in time t_{samp} and a periodic offset in time Δt as shown in Fig. 12. After converter start-up has passed, the samples, which are denoted $i_{\mathrm{DAB},a,1,d}$, $i_{\mathrm{DAB},a,2,d}$, $i_{\mathrm{DAB},b,1,d}$ and $i_{\mathrm{DAB},b,2,d}$ are paired and subtracted to approximate m_1 and m_2 in the digital domain as shown in step B of Fig. 11. The subscripts a and b denote the cycle where the sample was taken, the subscripts 1 and 2 are as defined in Section IV, and

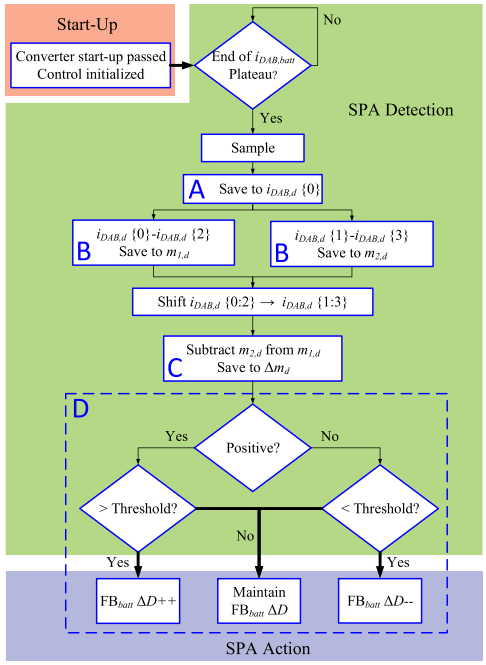

Fig. 11. SPA flowchart from converter start-up to FB$_{batt}$ duty-cycle correction ΔD.

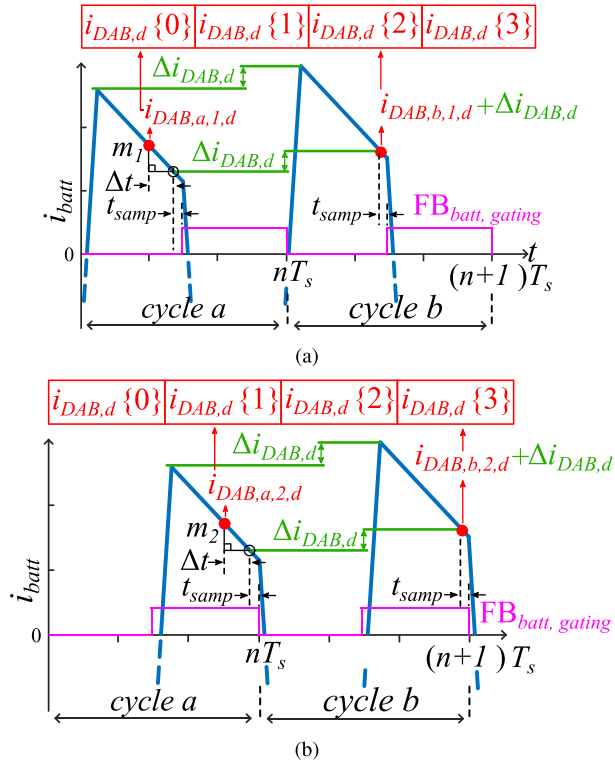

Fig. 12. Samples of i_{batt} are taken at the instances marked with solid red circles, along the (a) positive plateau and (b) negative plateau. The samples are stored in the $i_{DAB,d}\{\}$ array that is shifted.

the subscript d signifies the digital domain. The approximations of m_1 and m_2 are given as $m_{1,d}$ and $m_{2,d}$ in the digital domain. The slopes m_1 and m_2 are approximated by

$$m_1 \approx \frac{m_{1,d}}{\Delta t} \tag{24}$$

and

$$m_2 \approx \frac{m_{2,d}}{\Delta t} \tag{25}$$

where $m_{1,d}$ and $m_{2,d}$ are given by

$$m_{1,d} = i_{\text{DAB},a,1,d} - i_{\text{DAB},b,1,d} \tag{26}$$

and

$$m_{2,d} = i_{\text{DAB},a,2,d} - i_{\text{DAB},b,2,d} \tag{27}$$

where the calculation of $m_{2,d}$ accommodates the commutation of i_{batt} with respect to $i_{\text{DAB,batt}}$.

The two samples used in the calculation of each slope are separated in time by a minimum $T_s - \Delta t$ seconds. To calculate $m_{1,d}$ and $m_{2,d}$, an ADC with a sample rate that is inversely proportional to $\frac{T_s}{2} - \Delta t$ is required. For example, to approximate the instantaneous slope at a specific point in a 125-kHz waveform, with a Δt of 150 ns, a low-cost ADC with a sample rate that is slightly more than 250 ksps is required.

Since $V_{\text{dc-link}}$ and V_{batt} have negligible ripple between successive switching cycles, $\frac{d}{dt} i_{\text{DAB,batt}}$ and its digital approximations, $m_{1,d}$ and $m_{2,d}$, do not fluctuate under steady-state operation, as suggested by (10). Furthermore, small fluctuations can be measured and accommodated by the SPA accordingly in the controlled environment of an EV OBC. L_{DAB} also does not contribute to fluctuations in $\frac{d}{dt} i_{\text{DAB,batt}}$ as it is external from the transformer. A digital filter removes high frequency noise from $m_{1,d}$ and $m_{2,d}$ prior to the calculation of Δm_d, which is the digital approximation of Δm, as shown in step C of Fig. 11. The relation between Δm_d and Δm is given by

$$\Delta m_d = K \times \Delta m \tag{28}$$

where K is the gain associated with Δt and the sampling and sensing circuitry. A change in t_{ps} simultaneously effects $m_{1,d}$ and $m_{2,d}$, thereby not impacting Δm_d as given by

$$\begin{aligned}\Delta m_d &= m_{1,d} - m_{2,d} \\ &= (i_{\text{DAB},a,1,d} - (i_{\text{DAB},b,1,d} + \Delta i_{\text{DAB},d})) \\ &\quad - (i_{\text{DAB},a,2,d} - (i_{\text{DAB},b,2,d} + \Delta i_{\text{DAB},d})) \\ &= (i_{\text{DAB},a,1,d} - i_{\text{DAB},b,1,d}) \\ &\quad - (i_{\text{DAB},a,2,d} - i_{\text{DAB},b,2,d})\end{aligned} \tag{29}$$

where $\Delta i_{\text{DAB},d}$ is the change in current attributed to the change in phase-shift. The state of saturation in both sign and magnitude are detected using Δm_d, as shown in step D of Fig. 11.

The magnitude of Δm_d and the ADC resolution dictate the SPA resolution. The high-bandwidth amplifier senses the voltage across the shunt resistor R_{sense} with a high fidelity. The ADC resolution defines the least significant bit voltage LSB_v and the corresponding sensed current LSB_I by

$$LSB_I = \frac{\frac{LSB_v}{G}}{R_{\text{sense}}} \tag{30}$$

where G is the amplifier gain, and R_{sense} is the shunt resistance. LSB_I is the smallest detectable change in current and

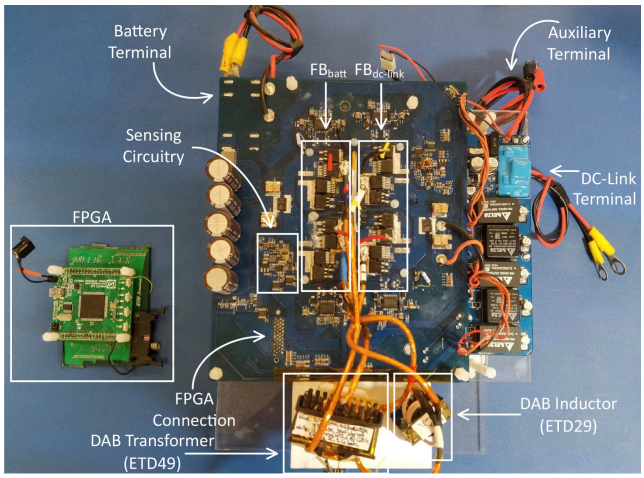

Fig. 13. 6.6-kW EV charger DAB converter prototype.

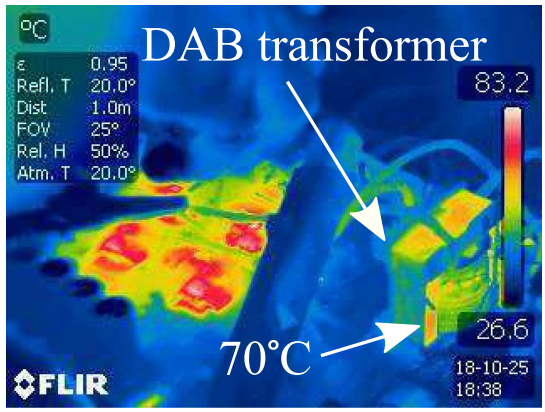

Fig. 14. Thermal image of DAB converter with prototype air cooling. At 6.6 kW, the transformer reaches 70 °C.

subsequently, the smallest Δm_d for a given Δt. A large LSB_v increases the minimum Δm_d and decreases the detectable range of ΔB.

For the transformer design described in Table I, corrective action is taken when $|\Delta m_d| > 20$, which corresponds to $\Delta B > 0.38$ T. Upon detecting the onset of saturation, the hysteretic controller applies a constant positive or negative ΔD to FB_{batt}, which results in a mitigating volt-second offset. The limited control range of the hysteretic controller results in bounded oscillations of B that increase in amplitude with decreasing V_{batt} and subsequent ΔB. Large amplitude oscillations can have an impact on core loss as outlined in [22].

VI. Experimental Verification

The DAB converter prototype is shown in Fig. 13. The design of the liquid cooling system has been validated through finite element simulations, which are calibrated experimentally. In [23], the use of liquid cooled potting has been compared against the use of forced air in an enclosed environment, for a different version of this converter. In [23], a feasible design is achieved for a similar transformer with similar losses using a liquid cooling system. Simulations of the proposed liquid cooling system and transformer cooling pot (see Table I) result in a peak MOSFET temperature of approximately 90 °C and a peak transformer core temperature of approximately 86 °C in steady state at 6.6-kW operation. The SPA controlled converter is initially verified using forced air cooling. The semiconductor devices and the magnetic components are both cooled using separate fans operating with a maximum flow rate of 1.08 m^3/min. As this converter is designed for use with a liquid cooled chill plate, the MOSFET thermal limits allow for a short duration air-cooled test. Through a 6.6-kW, 50-s operation, the transformer reaches 70°C, as shown in Fig. 14.

SPA functionality is demonstrated through measurements of $i_{DAB,batt}$ and real-time slope approximations. A close representation of the transformer B is measured through the analog integration of the induced voltage across a wire loop around the transformer core. The DAB converter and SPA specifications are shown in Table II.

Using a 12-bit, 3.3-V ADC, with an amplifier with G = 2.6, the LSB_I is 0.021 A, which corresponds to the smallest detectable Δm_d. Given a $\Delta t = 150$ ns, the smallest detectable Δm is given by

$$\Delta m = \frac{\Delta m_d}{\Delta t} = 0.14 A/\mu s \tag{31}$$

which corresponds to approximately $\Delta B = 0.3$ T. An increase in Δt, reduces the minimum detectable slope. The gradual change in permeability (soft saturation) in ferrites, as a function of ΔB, allows the controller to detect ΔB over a large range, as shown in Fig. 9.

A. SPA Experimental Results

Using the transformer with specifications defined in Table I, a ΔD of $+0.072\%$ and -0.072% is applied to $FB_{dc\text{-}link}$ at two different instances to induce saturation at a low power level. The resulting positive and negative saturation are seen in Fig. 15(a). With a positive ΔD and saturation, only $i_{DAB,a,1,d}$ and $i_{DAB,b,1,d}$ diverge with increasing m_1, which implies that $m_{1,d}$ tracks m_1, as shown in Fig. 15(b). Similar divergence occurs for $i_{DAB,a,2,d}$ and $i_{DAB,b,2,d}$, for a negative ΔD and saturation. The effect of saturation is captured with $|\Delta m_d| > 20$, which implies that $|B| > 0.38$ T, as shown in Fig. 15(c).

At 2.5 kW, the inherent component mismatches result in obvious signs of saturation in the DAB transformer. Upon activation of the SPA, the spikes in current attributed to saturation are mitigated, as seen in Fig. 16.

At 5.8 kW, the hysteretic controller produces small controlled B oscillations of approximately 30 mT. This is expected as the transformer ΔB of 0.37 T is very close to the set threshold, $B = 0.38$ T. The resulting current ripple of 3 A at a frequency of approximately 1 kHz, results in a voltage ripple of 0.25 V at the 900 μF bus port and 1.5 V at the 300 μF battery port. This ripple is 0.4% of the dc voltage, even at the lowest battery voltage. The lack of large spikes in $i_{DAB,batt}$, seen in Fig. 17(a) show that saturation has been controlled. A closer look at $i_{DAB,batt}$

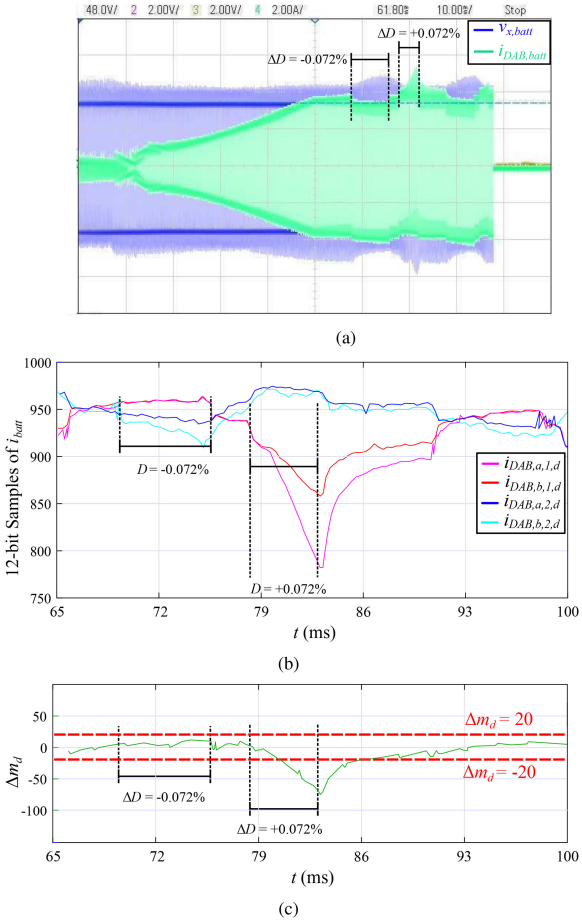

Fig. 15. (a) Measured $i_{\text{DAB,batt}}$ under momentarily forced $\Delta D = \pm 0.072\%$. (b) 12-bit samples of i_{batt}. (c) Calculated Δm_d.

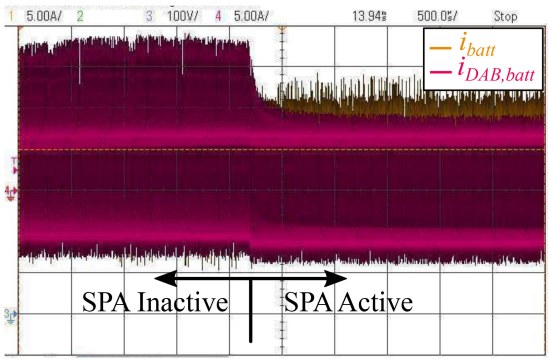

Fig. 16. Measured $i_{\text{DAB,batt}}$ and i_{batt} at 2.5 kW with both an active and inactive SPA. Saturation is present prior to activation.

and B in Fig. 17(b) reveal that the hysteretic corrections are applied accurately. With a constant correction, B_{dc} rises at a constant rate until the set threshold is reached. Large spikes in the positive plateau of $i_{\text{DAB,batt}}$ identify the positive bound of saturation. Once saturation is detected, the controller applies the necessary ΔD to decrease B_{dc} and mitigate saturation, as seen in Fig. 17(c).

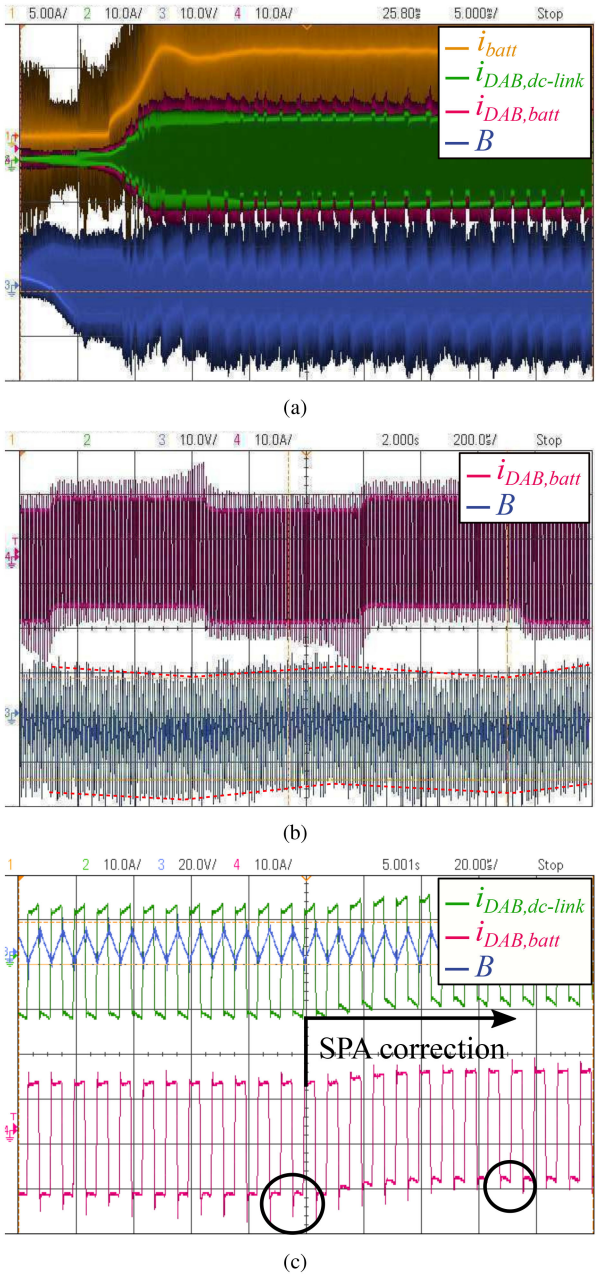

Fig. 17. (a) Measured $i_{\text{DAB,batt}}$, $i_{\text{DAB,dc-link}}$, i_{batt}, and transformer B under steady-state operation with SPA at 5.8 kW. (b) Zoom of $i_{\text{DAB,batt}}$ and B waveforms. (c) Zoom of DAB waveforms during SPA correction. The effect of saturation is present on $i_{\text{DAB,batt}}$ and not present on $i_{\text{DAB,dc-link}}$. The spikes associated with saturation are reduced during SPA correction, as circled in black.

A virtual I/O program is used to probe the i_{batt} ADC sample, $m_{1,d}$, $m_{2,d}$, and Δm_d registers of the FPGA. The i_{batt} samples taken under 5.8-kW operation, shown in Fig. 18, track the positive and negative plateaus of $i_{\text{DAB,batt}}$ as expected. With the corrective actions of the SPA, $m_{1,d}$ and $m_{2,d}$ track each other, as shown in Fig. 19. An artifact from the slope calculation immediately after a SPA duty cycle correction results in spikes, as shown in Figs. 19 and 20. These measurement artifacts do not impact the hysteretic SPA, as the artifacts do not change in polarity and as they occur immediately after an SPA corrective

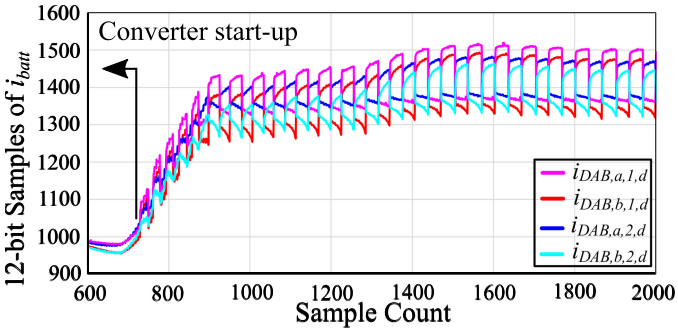

Fig. 18. Probed $i_{\mathrm{DAB},d}\{\}$ registers in FPGA, which contain 12-bit samples of i_{batt} at 5.8-kW operation.

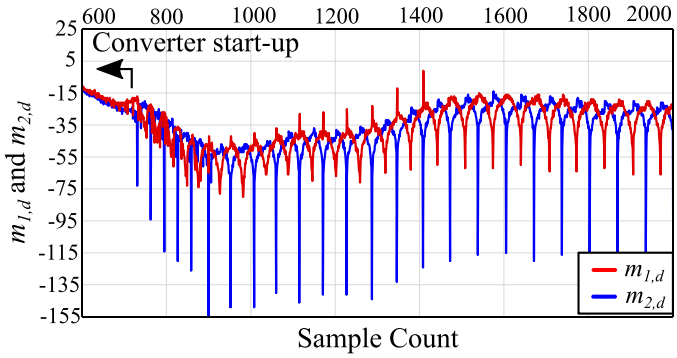

Fig. 19. Probed $m_{1,d}$ and $m_{2,d}$ registers in FPGA at 5.8-kW operation.

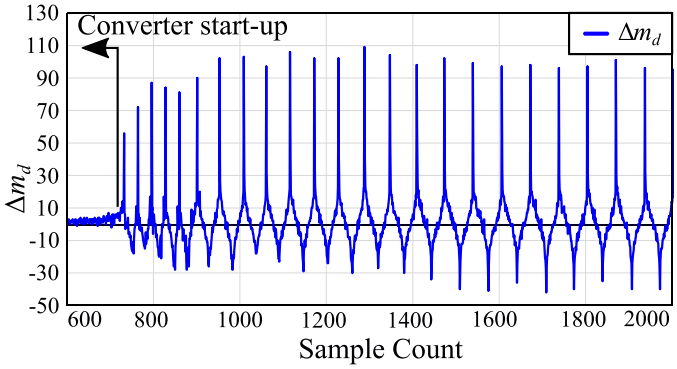

Fig. 20. Probed Δm_d registers in FPGA at 5.8-kW operation.

action. The artifacts are avoided by applying postprocessed calculations to the probed ADC samples to obtain $m_{1,d}$ and $m_{2,d}$, as seen in Fig. 21.

To verify the SPA operation, Δm_d is calculated through postprocessing, as shown in Fig. 22. With the SPA activated, the average of Δm_d is stable and small, while the hysteretic control results in a triangle waveform that remains between the control threshold of ± 20, and the subsequent ΔB bounds, as shown in Fig. 22.

B. Converter Efficiency With SPA

To precisely measure the converter efficiency, the Agilent 34401A is used to measure V_{batt} and $V_{\mathrm{dc-link}}$, in addition to

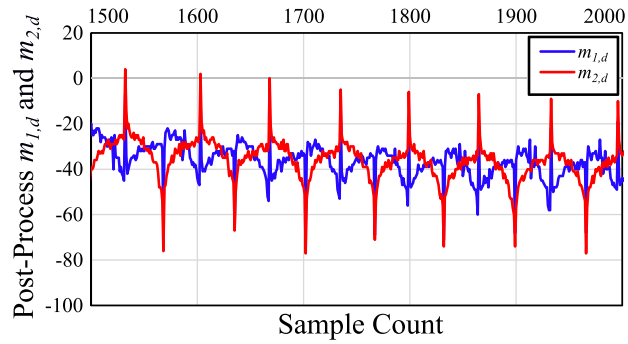

Fig. 21. Calculated $m_{1,d}$ and $m_{2,d}$ in postprocessing, at 5.8-kW operation. Calculation artifacts are no longer visible.

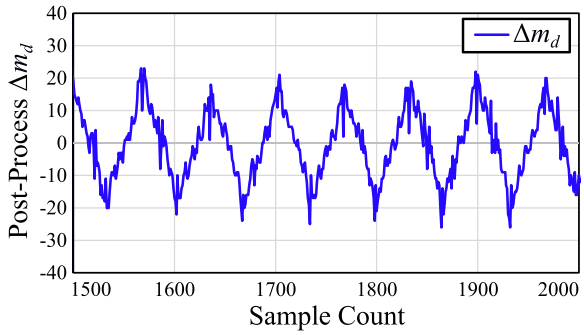

Fig. 22. Calculated Δm_d in postprocessing, at 5.8-kW operation. Calculation artifacts are no longer visible.

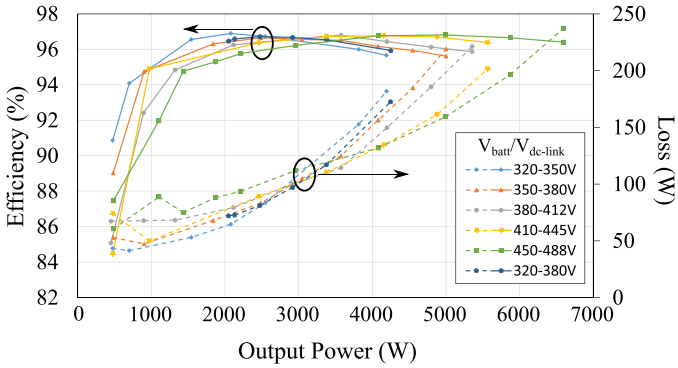

Fig. 23. Measured DAB efficiency and loss under varied ratios of $V_{\mathrm{batt}}/V_{\mathrm{dc-link}}$.

the input and output current through 3.3-mΩ sense resistors. Corresponding to the range of EV battery SOC, V_{batt} is varied from 320 to 450 V. Corresponding to the limits of the dc–ac stage, $V_{\mathrm{dc-link}}$ is varied from 380 to 480 V. For a battery voltage above 350 V, $V_{\mathrm{dc-link}}$ tracks with the transformer turns ratio, while for battery voltages below 350 V, $V_{\mathrm{dc-link}}$ is fixed at 380 V.

The converter efficiency at 6.6 kW reaches a peak value of 96.8%, as shown in Fig. 23. The lower efficiency is attributed to the ΔB that is slightly out of the design region shown in Section III-E and the lack of a sophisticated transformer thermal management system during initial testing of the SPA. The dc

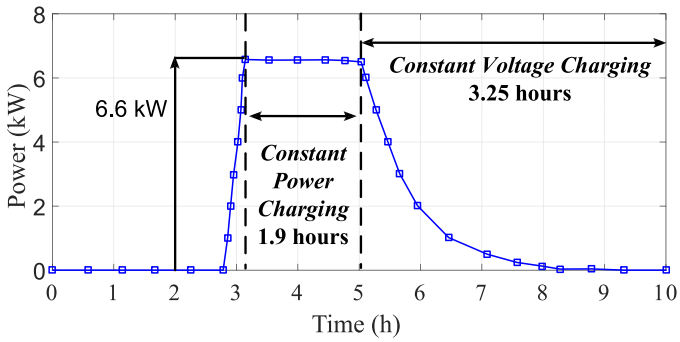

Fig. 24. Measured typical charging profile of a Level-2 6.6-kW EV charger in a 2015 Nissan Leaf.

TABLE III
DAB BENCHMARK COMPARISONS

Comparable	This Work	[24]	[25]
Core box volume: Transformer + L_{DAB} =	40.3 cm^3 49.9 cm^3	93.8 cm^3 -	- $\approx$ 127.1 cm^3
Peak efficiency	96.8%	96.3%	97.8%
Switching device	SiC 65 mΩ	Si 28 mΩ	GaN 25 mΩ
Operation frequency	125 kHz	120 kHz	500 kHz
Topology	DAB	DAB	CLLC
Power	6.6 kW	3.3 kW	6.6 kW

symmetry of the DAB ensures that the efficiency curves for both directions of power flow are similar.

OBCs operate for extended periods of time in constant voltage mode, where the charging power is asymptotically ramped down to maintain constant battery voltage. The typical power profile for a 2015 Nissan Leaf with a 6.6-kW OBC demonstrates the significant portion of time spent in constant voltage charging, and, subsequently, the significance of low power efficiency, as shown in Fig. 24.

C. Benchmark Comparison

A comparison of the SPA-enabled DAB prototype with comparable bidirectional converters is given in Table III. As winding and cooling system volume are not readily available, only total core box volume is compared. When compared against the GaN resonant converter of [25], the combined box volume of the proposed transformer and inductor with the SPA is smaller, operates at 25% of the frequency, and uses cheaper SiC devices, with comparable efficiency. Furthermore, compared to [24], the DAB transformer operates at twice the power, similar frequency, with half of the volume.

VII. CONCLUSION

An SPA has been demonstrated for a DAB converter. The SPA is implemented using the minimal number of sensors required for DAB converter operation. For complete converter loss and volume analysis, the full range of ΔB up to B_{sat} is safely considered due to the protection provided by the SPA. For a target efficiency of approximately 97%, the converter f_s, transformer ΔB, and core volume are analyzed to find the smallest feasible transformer core. In a 96.8% efficient, 6.6-kW DAB prototype, the ETD49 core is the smallest possible core with a design space spanning ΔB from 0.2 T to B_{sat} and f_s from 75 to 170 kHz. MOSFET cooling limitations restrict the maximum operable frequency and result in a converter with $f_s = 125$ kHz, and a transformer $\Delta B = 0.37$ T. Despite the very low saturation safety margin in the particular prototype, saturation mitigation is experimentally validated through the measurement of transformer current and approximate core B. The synchronous sampling of the SPA is validated through the probing of digital current samples, calculated slope approximations, and calculated slope differences. Compared to the presented benchmark converters, the SPA-enabled DAB has a smaller transformer, with a comparable or better efficiency.

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Seyed Amir Assadi (S'18) received the B.A.Sc. and M.A.Sc. degrees in electrical engineering from the University of Toronto, ON, Canada, in 2016 and 2019, respectively. He is currently working toward the Ph.D. degree at the University of Toronto.

His research interests include power electronics and control of high-density EV battery chargers.

Hirokazu Matsumoto (M'09) was born in Ehime, Japan, in 1977. He received the M.S. degree in electrical and electronic systems engineering and the Dr. Eng. degree in engineering from Kyushu University, Fukuoka, Japan, in 2001 and 2004, respectively.

In 2004, he was a Researcher of the 21st Century Center of Excellence Program. From 2005 to 2007, he worked on design of servo systems for factory automation at Mitsubishi Electric Company, Tokyo, Japan. From 2008 to 2019, he worked with the Department of Electrical Engineering, Fukuoka University, Fukuoka. In 2017, he was a Visiting Professor with The Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto. Since 2019, he has been working with the Department of Electrical Engineering and Electronics, Aoyama Gakuin University, Tokyo, Japan, as an Associate Professor. His research interests include power inverters, wireless power transfer systems, electric motors, and their control.

Mazhar Moshirvaziri (M'11) received the B.Sc. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 2010, and the master's degree in the electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 2012. His M.A.Sc. dissertation dealt with ultracapacitor and battery-based hybrid energy storage systems for electric vehicles.

He is currently a Senior Member of the Technical Staff at Advanced Micro Devices (AMD), Toronto, where he is responsible for power and performance definition of discrete graphics processing units. His research interests include electric vehicles, battery management systems in electric vehicles, and high-efficiency power electronics converter designs.

Miad Nasr received the B.A.Sc and M.A.Sc degrees in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 2015 and 2017, respectively.

He is currently a Research Associate with the University of Toronto Electric Vehicle (UTEV) Research Centre, where he performs research on high-density power electronics for automotive applications.

Mohammad Shawkat Zaman (S'07) was born in Dhaka, Bangladesh. He received the B.A.Sc. and M.A.Sc. degrees in electrical engineering from the University of Toronto, ON, Canada, in 2010 and 2013, respectively, where he is currently working toward the Ph.D. degree. He has received the NSERC Canada Graduate Scholarship (CGS) and the Ontario Graduate Scholarship (OGS) during both his M.A.Sc. and Ph.D. degrees.

He was an Intern with Analog Devices Inc. and NXP Semiconductors in 2008 and 2012, respectively. In 2013, he joined NXP Semiconductors in Eindhoven, The Netherlands, where he worked on integrated power converters for low-power applications. His research interests include monolithic integration and mixed-signal control techniques for high-density power conversion.

Olivier Trescases (SM'13) received the Ph.D. degree from the University of Toronto, Toronto, ON, Canada.

From 2007 to 2008, he was a Concept Engineer and mixed-signal IC Designer with Infineon Technologies, Graz, Austria, focusing on safety-critical automotive applications. While on sabbatical in 2016, he was at the Texas Instruments Kilby Labs, Santa Clara, CA, USA, and then at NXP Semiconductor in Eindoven, Holland. Since 2016, he has been the Director of University of Toronto Electric Vehicle (UTEV) Research Centre. He is currently a Professor with the Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto. His group conducts research on advanced power electronic converters.

Dr. Trescases has been an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS since 2015. He is a Canada Research Chair in Power Electronic Converters and serving as the Chair of the IEEE Toronto Section. He has served on various IEEE conference technical committees, including the Applied Power Electronics Conference, the Custom Integrated Circuits Conference, and the International Symposium on Power Semiconductors and ICs.