A Novel Single-Phase Three-Level Dual-Buck Inverter

Tien-The Nguyen, *Student Member, IEEE*, Honnyong Cha, Bang Le-Huy Nguyen, and Heung-Geun Kim, *Senior Member, IEEE*

***Abstract*—This article proposes a new single-phase three-level dual-buck inverter. The topology is derived from a simplified neutral-point clamped inverter that includes fewer active switches. The advantages of the proposed inverter are no shoot-through worries and no reverse recovery issue of the body diode of the power metal-oxide-semiconductor field-effect transistor compared with the conventional inverter; therefore, a high-reliability inverter can be achieved. The operation modes and pulsewidth modulation technique are analyzed in detail. Additionally, a switching scheme is proposed to balance and reduce the direct-current-link capacitance. A 1.4-kW prototype was built and tested to validate the theoretical analysis of the proposed converter.**

***Index Terms*—.**

I. Introduction

A THREE-LEVEL half-bridge is shown in Fig. 1. A bidirectional switch S_3 is connected between the middle point of the dc-link capacitors and the phase leg (S_1 and S_2), which generates three-level output voltages $V_{\rm dc}$, $V_{\rm dc}/2$, and 0. The half-bridge can be configured with two switches with common source/drain terminals in series, which is known as a T-type NPC branch, or with one switch and four external diodes, which is known as the simplified NPC, as depicted in Fig. 1(b). The high-side and low-side switches (S_1 and S_2) block the full dc-link capacitor voltage. However, the switch S_3 only blocks half of the input voltage; thus, it can be selected with a lower voltage rating and shows low switching and conduction loss [1]–[3]. Compared with diode NPC (DNPC), flying capacitor (FC), and active NPC, the number of switches of simplified NPC is reduced considerably [3]. Additionally, the simplified NPC is one of the best options for low-voltage application among conventional multilevel inverters, especially grid-tied inverters. Compared with conventional three-level pulsewidth modulation (PWM) inverter, although simplified NPC has lower efficiency (approximately <4%), it gives lower total harmonic distortion of the output waveforms [4], [5].

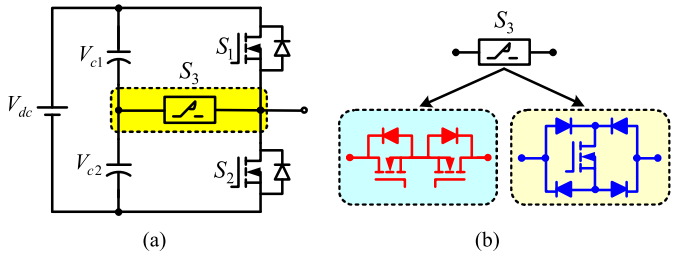


Fig. 1. (a) Three-level half-bridge inverter. (b) Configuration of switch S_3.

The significant advantages of power metal–oxide semiconductor field-effect transistors (MOSFETs) are fast switching, resistive conduction voltage drop, and no turn-OFF tail current, which provides lower switching and conduction losses than the insulated-gate bipolar transistor. However, power MOSFETs are not typically used in high-voltage applications ($V_{\rm dc} > 250$ V) because a large reverse recovery current flows through the body diode of power MOSFETs, which is related to significant losses [6]–[8]. It is well-known that the dual-buck structure can eliminate the reverse recovery problem of the body diode of power MOSFET. The concept of the dual-buck structure was first introduced in [9]. It has been researched and applied in a wide range of power converters, such as dc–ac inverters [10]–[14], ac–ac converters [15]–[19], and multilevel converters [20]–[22].

The derivation of dual-buck structures for the three-level half-bridge was presented in [22]–[24], as shown in Fig. 2. The series-switch (SS) DBI is derived from the DNPC depicted in Fig. 2(a). When the active switches S_1–S_4 and diodes D_1–D_4 are replaced by the diodes and switches, respectively, the SS DBI is converted into a series-diode (SD) DBI, as shown in Fig. 2(b). The NPC and FC DBI are shown in Fig. 2(c) and (d), respectively. In these configurations, four active switches and four diodes (two diodes for the FC DBI) are required.

One of the problems of the three-level inverter is the unbalanced dc-link capacitor voltages, which can reduce the quality of the output voltage and current, increase the voltage stress

Manuscript received December 20, 2018; revised April 25, 2019 and June 25, 2019; accepted July 28, 2019. Date of publication August 1, 2019; date of current version January 10, 2020. This work was supported in part by the Korea Institute of Energy Technology Evaluation and Planning, in part by the Ministry of Trade, Industry, and Energy of the Republic of Korea under Grant 20194030202310, and in part by the National Research Foundation of Korea (NRF) Grant funded by the Korean government (MSIT) (NRF-2019R 1A2C1006367). Recommended for publication by Associate Editor P. Barbosa. *(Corresponding author: Honnyong Cha.)*

T.-T. Nguyen, H. Cha, and B. L.-H. Nguyen are with the School of Energy Engineering, Kyungpook National University, Daegu 1370, South Korea (e-mail: nguyenthetien93@gmail.com; chahonny@knu.ac.kr; bang.lh.nguyen@gmail.com).

H.-G. Kim is with the Department of Electrical Engineering, Kyungpook National University, Daegu 1370, South Korea (e-mail: hgkim@knu.ac.kr).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2019.2932890

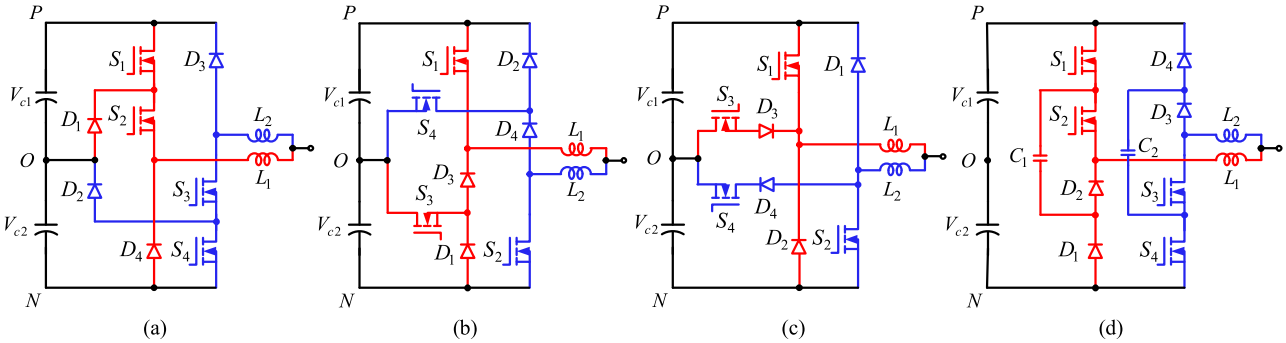


Fig. 2. Three-level half-bridge DBI. (a) SS. (b) SD. (c) NPC. (d) FC.

on the switches, damage the dc-link capacitor, and eventually kill the switching devices. The main cause of voltage balancing is the unequal charged and discharged currents at the middle point of the dc-link capacitor. The neutral-point self-balancing of five-level inverters is related to the modulation index, which is mentioned in [22]. When the modulation index is low, the additional neutral-point balancing method is employed. However, a large dc-link capacitance is needed to maintain the constant voltage on the capacitors. For these reasons, the motivation of this article is to obtain a high-reliability inverter, use less switching devices, and reduce the capacitance of the dc-link capacitor.

This article proposes a new single-phase three-level DBI that uses fewer active switches and has all the advantages of the DBI and three-level inverter. Compared with the conventional simplified NPC inverter, the proposed inverter achieves high reliability because of the absence of shoot-through and high efficiency because there is no reverse recovery of the body diode of the MOSFETs. Additionally, the converter can operate at a high switching frequency by using MOSFETs; therefore, the volume of the passive component and the current stress of the switching devices are reduced considerably. Furthermore, voltage balancing of the dc-link capacitor is discussed, and the PWM scheme is proposed to balance and reduce the capacitor size greatly.

This article is organized as follows. In Section II, the derivation of the proposed inverter is presented. The operation modes are analyzed in Section III. In Section IV, the neutral-point voltage control and the PWM switching pattern for controlling the dc-link capacitor voltage are described. A comparison with the conventional inverter and other DBIs is presented in Section V. Simulation and experimental results are presented in Section VI. Power loss of the proposed inverter is discussed in Section VII and Section VIII concludes the article.

II. Proposed Three-Level DBI

Fig. 3 shows the topology of the proposed three-level half-bridge DBI. It is developed from the conventional three-level half-bridge inverter using auxiliary switches [3], which is known as the simplified NPC inverter. The phase-leg S_{a1}, S_{a2} is extended to two legs: leg 1 including (S_{a1}, D_{a1}, L_{a1}) and leg 2 including (S_{a2}, D_{a2}, L_{a2}). The two diodes (D_{a4} and D_{a6}) connected to point A are spread into two points A_1 and A_2. L_{a1} and L_{a2} are connected to points A_1 and A_2, respectively. Fig. 4 shows three cases of shoot-through when overlap time occurs between the pair of switches of the proposed inverter. When the S_{a1} and S_{a2} turn ON simultaneously, L_{a1} and L_{a2} oppose the increase of the current, as depicted in Fig. 4(a). When the S_{a1} and S_{a3} turn on simultaneously, L_{a1} and L_{a2} oppose the increase of the current, as depicted in Fig. 4(b). Similarly, when overlap time occurs at S_{a2} and S_{a3}, L_{a1} and L_{a2} oppose the increase of the current, as depicted in Fig. 4(c). Hence, the high reliability of the inverter can be achieved.

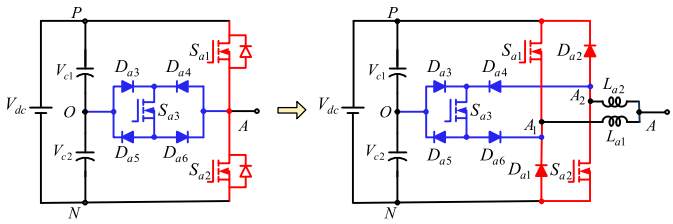


Fig. 3. Conversion of the proposed three-level half-bridge DBI.

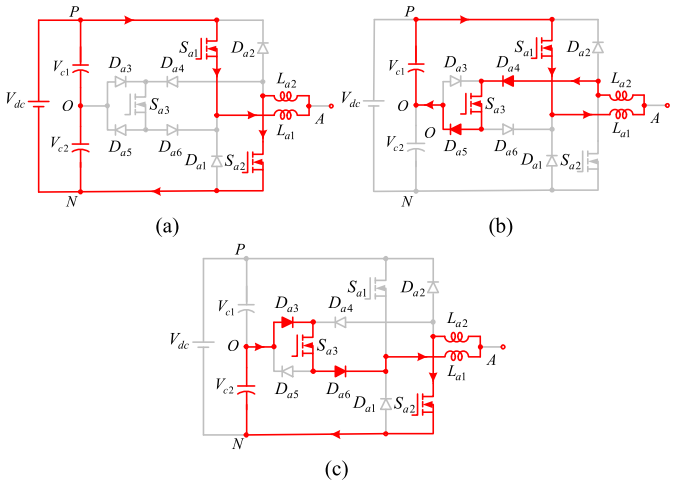


Fig. 4. Shoot-through during the overlap time of (a) S_{a1} and S_{a2}, (b) S_{a1} and S_{a3}, and (c) S_{a2} and S_{a3}.

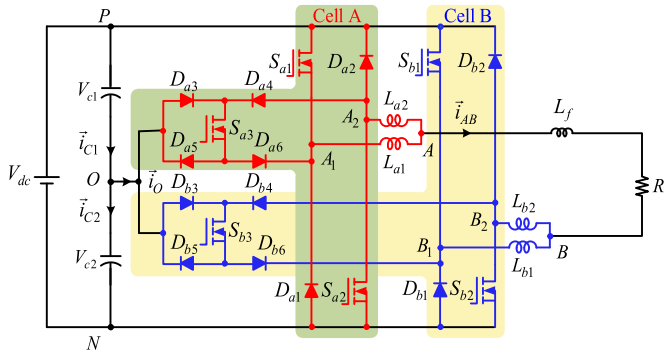


Fig. 5. Proposed single-phase three-level DBI.

Fig. 5 shows the proposed single-phase three-level DBI, which is analyzed in this article. It combines two proposed three-level half-bridge DBIs, i.e., cells *A* and *B*. The inverter is composed of six active switches (S_{x1}–S_{x3}), 12 external diodes (D_{x1}–D_{x6}), and four inductors (L_{x1}–L_{x2}), where $x = \{a, b\}$. L_{x1}–L_{x2} protect against a short-circuit and are called current-limiting inductors. They also serve as filter inductors. The inductor current flows through D_{x1}–D_{x6} instead of the body diode of S_{x1}–S_{x3} owing to current-limiting inductors (L_{x1}–L_{x2}).

III. Analysis of the Proposed Inverter

The number of switching states for the three-level inverter is expressed as 3^n, where n is the number of half-bridge legs. Hence, the proposed inverter has $3^2 = 9$ switching states, as shown in Fig. 6. Nine switching states are formed by the connections of point *A* to terminals (*P*, *O*, *N*) and point *B* to terminals (*P*, *O*, *N*), which generate five-level output voltages v_{AB}: $+V_{\rm dc}$, $+V_{\rm dc}/2$, 0, $-V_{\rm dc}/2$, and $-V_{\rm dc}$. The output voltage v_{AB} can be calculated as follows:

$$v_{AB} = V_{AN} - V_{BN}. \tag{1}$$

1) *Mode 1:* S_{a1} and S_{b2} are ON, while the other switches are OFF. Point *A* is connected to *P*, and point *B* is connected to *N*, as shown in Fig. 6(a). This mode obtains $v_{AB} = +V_{\rm dc}$. When the current path is positive (red path from point *A* to *B*), the switches S_{a1} and S_{b2} and the inductors L_{a1} and L_{b2} conduct. When the current path is negative (blue path from *B* to *A*), the current flows through the freewheeling diodes D_{a2}, D_{b1} and the inductors L_{a2}, L_{b1}.
2) *Modes 2 and 3:* These modes generate $v_{AB} = +V_{\rm dc}/2$. In mode 2, S_{a1} and S_{b3} are ON, while the other switches are OFF. Point *A* is connected to *P*, and point *B* is connected to *O*, as shown in Fig. 6(b). When the current path is positive, the current flows through S_{a1}, L_{a1}, L_{b2}, D_{b4}, S_{b3}, and D_{b5} in sequence, and capacitor C_1 discharges. When the current path is negative, D_{b3}, S_{b3}, D_{b6}, L_{b1}, L_{a2}, and D_{a2} conduct, and capacitor C_1 is charged. In mode 3, S_{a3} and S_{b2} are ON, while the other switches are OFF. Point *A* is connected to *O*, and point *B* is connected to *N*, as shown in Fig. 6(c). When the current path is positive, the current flows through D_{a3}, S_{a3}, D_{b4}, L_{a1}, L_{b2}, and S_{b2} in sequence, and capacitor C_2 discharges. When the current path is negative, D_{b1}, L_{b1}, L_{a2}, D_{a4}, S_{a3}, and D_{b3} conduct, and capacitor C_2 is charged.
3) *Modes 4–6:* These modes generate $v_{AB} = 0$. In mode 4, S_{a1} and S_{b1} are ON, while the other switches are OFF, as shown in Fig. 6(d). When the current path is positive, the current flows through S_{a1}, L_{a1}, L_{b2}, and D_{b2} in sequence. When the current path is negative, the current flows through S_{b1}, L_{b1}, L_{a2}, and D_{a2} in sequence. In mode 5, S_{a3} and S_{b3} are ON, while the other switches are OFF, as shown in Fig. 6(e). When the current path is positive, the current flows through D_{a3}, S_{a3}, D_{a6}, L_{a1}, L_{b2}, D_{b4}, S_{b3}, and D_{b5} in sequence. When the current path is negative, the current flows through D_{b3}, S_{b3}, D_{b6}, L_{b1}, L_{a2}, D_{a4}, S_{a3}, and D_{a5} in sequence. In mode 6, S_{a2} and S_{b2} are ON, while the other switches are OFF, as shown in Fig. 6(f). When the current path is positive, the current flows through D_{a1}, L_{a1}, L_{b2}, and S_{b2} in sequence. When the current path is negative, the current flows through S_{a2}, D_{b1}, L_{b1}, and L_{a2} in sequence.
4) *Modes 7 and 8:* These modes generate $v_{AB} = -V_{\rm dc}/2$. In mode 7, S_{a2} and S_{b3} are ON, while the other switches are OFF. Point *A* is connected to *N*, and point *B* is connected to *O*, as shown in Fig. 6(g). When the current path is positive, the current flows through D_{b3}, S_{b3}, D_{b6}, L_{b1}, L_{a2}, and S_{a2} in sequence, and capacitor C_2 discharges. When the current path is negative, D_{a1}, L_{a1}, L_{b2}, D_{b4}, S_{b3}, and D_{b5} conduct, and capacitor C_2 is charged. In mode 8, S_{a3} and S_{b1} are ON, while the other switches are OFF. Point *A* is connected to *O*, and point *B* is connected to *P*, as shown in Fig. 6(h). When the current path is positive, the current flows through D_{a3}, S_{a3}, D_{a6}, L_{a1}, L_{b2}, and D_{b2} in sequence, and capacitor C_1 is charged. When the current path is negative, S_{b1}, L_{b1}, L_{a2}, D_{a4}, S_{a3}, and D_{a5} conduct, and capacitor C_1 discharges.
5) *Mode 9:* This mode generates $v_{AB} = -V_{\rm dc}$. S_{b1} and S_{a2} are ON, while the other switches are OFF. Point *A* is connected to *N*, and point *B* is connected to *P*, as shown in Fig. 6(i). When the current path is positive, the current flows through D_{a1}, L_{a1}, L_{b2}, and D_{b2} in sequence. When the current path is negative, S_{b1}, L_{b1}, L_{a2}, and S_{a2} conduct.

The switching states of the proposed inverter are given in Table I. States *PN* and *NP* generate voltage levels $+V_{\rm dc}$ and $-V_{\rm dc}$, respectively, while states *PO* and *ON* produce the voltage level $+V_{\rm dc}/2$. States *NO* and *OP* produce the voltage level -$V_{\rm dc}/2$, and states *PP*, *OO*, and *NN* generate the voltage level 0. To balance the dc-link capacitor voltage and reduce the number of commutations, these redundant states are used and combined alternatively.

In order to reduce the magnetic volume, coupled inductors are formed between L_{a1} and L_{b2}, and between L_{a2} and L_{b1}. Two coupled inductors are integrated in one magnetic core as shown in Fig. 7. In positive half cycle, the current i_{AB} flows through L_{a1} and L_{b2} which are coupled each other. Similarity,

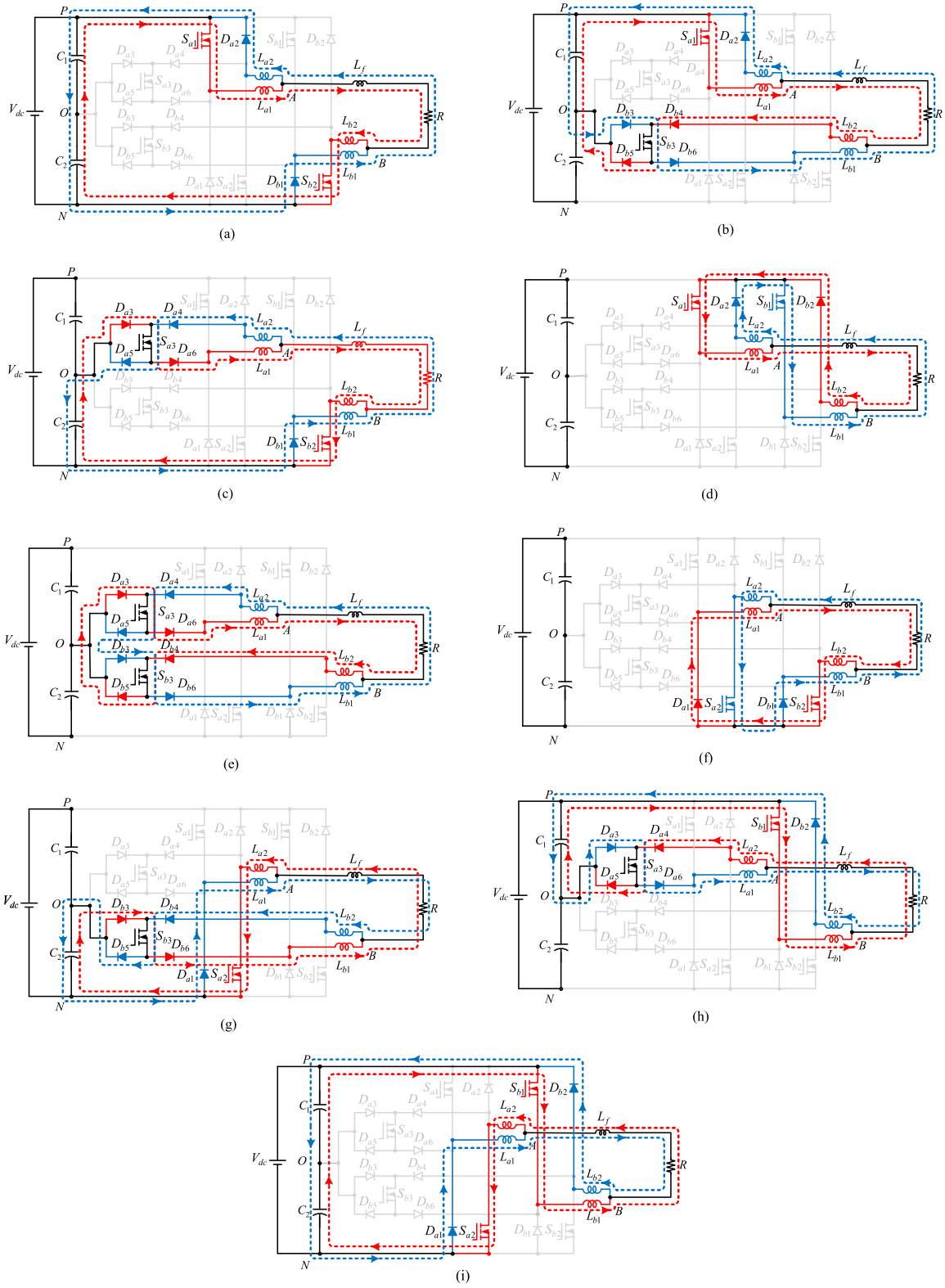


Fig. 6. Equivalent circuit of the operation modes. (a) Mode 1—state *PN*. (b) Mode 2—state *PO*. (c) Mode 3—state *ON*. (d) Mode 4—state *PP*. (e) Mode 5—state *OO*. (f) Mode 6—state *NN*. (g) Mode 7—state *NO*. (h) Mode 8—state *OP*. (i) Mode 9—state *NP*.

TABLE I
SWITCHING STATES AND OUTPUT VOLTAGE LEVELS

Mode	States	Conduction states						V_{AN}	V_{BN}	v_{AB}
		S_{a1}	S_{a2}	S_{a3}	S_{b1}	S_{b2}	S_{b3}			
1	*PN*	1	0	0	0	1	0	V_{dc}	0	$+V_{dc}$
2	*PO*	1	0	0	0	0	1	V_{dc}	$V_{dc}/2$	$+V_{dc}/2$
3	*ON*	0	0	1	0	1	0	$V_{dc}/2$	0	$+V_{dc}/2$
4	*PP*	1	0	0	1	0	0	V_{dc}	V_{dc}	0
5	*OO*	0	0	1	0	0	1	$V_{dc}/2$	$V_{dc}/2$	0
6	*NN*	0	1	0	0	1	0	0	0	0
7	*NO*	0	1	0	0	0	1	0	$V_{dc}/2$	$-V_{dc}/2$
8	*OP*	0	0	1	1	0	0	$V_{dc}/2$	V_{dc}	$-V_{dc}/2$
9	*NP*	0	1	0	1	0	0	0	V_{dc}	$-V_{dc}$

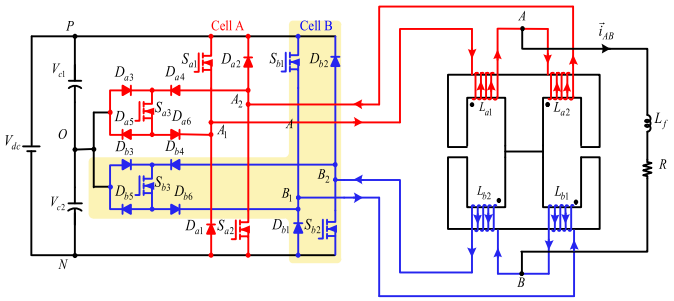


Fig. 7. Integrated magnetic of two coupled inductors.

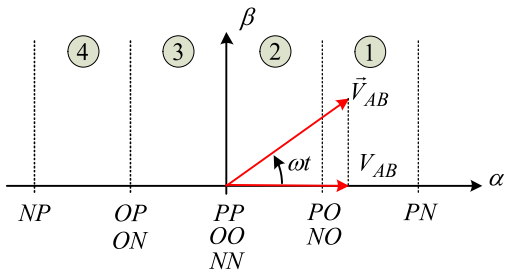


Fig. 8. Distribution of output voltage on the complex plane $\alpha\beta$.

the coupled inductor is formed between L_{a2} and L_{b1} in negative half cycle. The linkage flux of the coupled inductor L_{a1} and L_{b2} does not affect to L_{b1} and L_{a2} because of different operation mode and air gaps. By using coupled inductor and integrating them into one magnetic core, the volume of magnetic component can be reduced considerably.

IV. MODULATION STRATEGY FOR THE PROPOSED INVERTER

In this section, neutral-point voltage balancing is discussed, and the PWM pattern for the proposed inverter is presented for controlling the dc-link capacitor voltage.

A. Neutral-Point Voltage Control

Neutral-point voltage control was mentioned in [25]. The desired output voltage is sinusoidal waveform $v_{AB}(t) = V_{AB}\sin(\omega t)$ and represented on the complex plane $\alpha\beta$ as the modulus V_{AB} and phase ωt, which is shown in Fig. 8. The real component of modulus V_{AB} in α-axis locates in each sector, which is synthesized by the combination of switching states in one switching period. The duty ratios are defined as d_x, with x corresponding to one of nine switching states. The real component of modulus V_{AB} over one switching period is expressed as follows:

$$\frac{V_{AB}}{V_{\rm dc}} = d_{PN} - d_{NP} + \tfrac{1}{2}d_{PO} + \tfrac{1}{2}d_{ON} - \tfrac{1}{2}d_{NO} - \tfrac{1}{2}d_{OP} + 0 \times (d_{PP} + d_{OO} + d_{NN}) \tag{2}$$

with $\sum d_x = 1$.

Duty ratios d_A and d_B are defined as the set of switching states $\{PO, NO\}$ and $\{OP, ON\}$ in one switching period, respectively. These switching states are responsible for the capacitor voltage balance

$$d_A = d_{PO} + d_{NO} \tag{3}$$

$$d_B = d_{OP} + d_{ON}. \tag{4}$$

Applying Kirchoff's current law to node O, as shown in Fig. 6, yields the following equations:

$$i_{C1} - i_{C2} = i_O \tag{5}$$

$$C\frac{d\,(V_{C1} - V_{C2})}{dt} = (d_A - d_B) \times i_{AB}. \tag{6}$$

To balance the voltages V_{C1} and V_{C2}, d_A–d_B should be equal to zero; i.e., $d_A = d_B$. The combination of two sets of switching states $\{PO, NO\}$ and $\{OP, ON\}$ regulates the charged and discharged currents in the capacitors when an unbalanced voltage occurs. The difference $\Delta = d_A$–d_B also depends on the sign of the output current i_{AB} and the value of $V_{\rm diff} = V_{C1}$–V_{C2}

$$\Delta = d_A - d_B = kV_{\rm diff}\,\text{sign}\,(i_{AB}) \tag{7}$$

where $k > 0$.

The value of the constant k should be small to keep the value of Δ in the range of $[-1, 1]$.

B. PWM Strategy for the Proposed Inverter

The reference voltage $V_{\rm ref} = m * \sin(\omega t)$ is compared with one carrier waveform to produce the five-level output voltages, as shown in Fig. 9. The switching scheme is divided into four sectors. Sector 1 is defined as the voltage gain of $V_{\rm ref}$ in the range of $0.5 < m \leq 1$. The output voltage v_{AB} commutates between $+V_{\rm dc}$ and $+V_{\rm dc}/2$, and three switching states (*PN*, *PO*, and *ON*) are used in this sector. Sectors 2 and 3 are defined as the voltage gain of $V_{\rm ref}$ in the ranges of $0 < m \leq 0.5$ and $-0.5 < m \leq 0$, respectively. The output voltage v_{AB} commutates between $+V_{\rm dc}/2$ and 0 in sector 2 and between 0 and $-V_{\rm dc}/2$ in sector 3. Five switching states cooperate in these two sectors. Sector 4 is defined as the voltage gain of $V_{\rm ref}$ in the range of $-0.5 < m \leq -1$. The output voltage v_{AB} commutates between $-V_{\rm dc}/2$ and $-V_{\rm dc}$, and three switching states (*OP*, *NO*, and *NP*) are used in this sector.

As in (1), the output voltage v_{AB} is the differential between V_{AN} and V_{BN} which are expressed as

$$V_{AN} = \frac{mV_{\rm dc}}{2}\sin(\omega t) + \frac{V_{\rm dc}}{2} \tag{8}$$

$$V_{BN} = \frac{mV_{\rm dc}}{2}\sin(\omega t - \pi) + \frac{V_{\rm dc}}{2}. \tag{9}$$

TABLE II
DUTY-RATIO CALCULATION AND SWITCHING SEQUENCE OF THE PROPOSED INVERTER

Sector	Duty-ratio calculation			Switching sequence
	d_O	d_A	d_B	
1	$d_{PN} = -1 + 2m$	$d_{PO} = 1 - m + \Delta/2$	$d_{ON} = 1 - m - \Delta/2$	A. *PO→PN→ON→PN*
				B. *PN→ON→PN→PO*
2	$d_{OO} = 1 - 2m$	$d_{PO} = m + \Delta/2$	$d_{ON} = m - \Delta/2$	A. *PO→OO→ON→OO*
				B. *OO→ON→OO→PO*
3	$d_{OO} = 1 + 2m$	$d_{NO} = -m + \Delta/2$	$d_{OP} = -m - \Delta/2$	A. *NO→OO→OP→OO*
				B. *OO→OP→OO→NO*
4	$d_{NP} = -1 - 2m$	$d_{NO} = 1 + m + \Delta/2$	$d_{OP} = 1 + m - \Delta/2$	A. *NO→NP→OP→NP*
				B. *NP→OP→NP→NO*

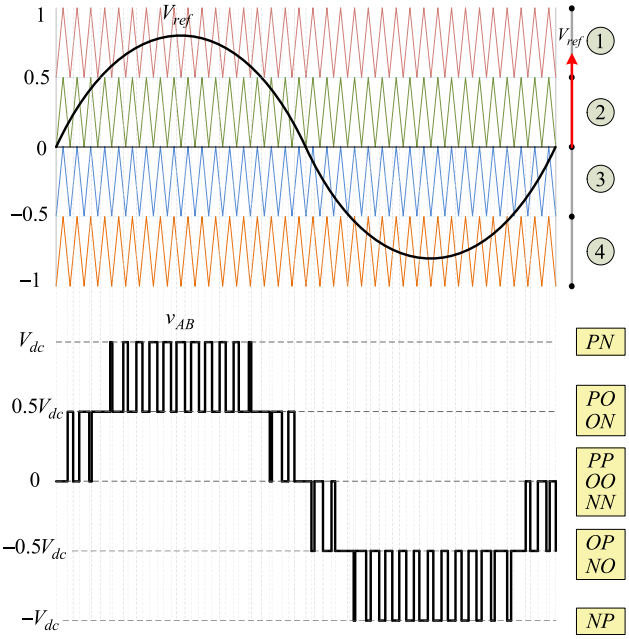


Fig. 9. Operation of PWM and the output voltage waveforms v_{AB}.

Hence, the voltage gain of the proposed inverter is presented as

$$v_{AB} = mV_{\rm dc}\sin(\omega t). \tag{10}$$

The duty ratios of the switching states according to the position of $V_{\rm ref}$ and the commutation sequence are given in Table II. The duty ratios d_1–d_3 represent the three switching states in each sector. The selection of the switching sequence balances the charged and discharged currents of the capacitor. It also minimizes the number of commutations in one sampling period to reduce the switching loss and avoid sudden changes in the output voltage.

The optimal switching patterns are presented in Fig. 10. Three control signals d_u, d_v, and d_t are compared with one carrier waveform to generate control signals, which can be calculated as follows:

$$\begin{aligned} d_u &= d_O + d_B \\ d_v &= d_O/2 + d_B \\ d_t &= d_O/2. \end{aligned} \tag{11}$$

Sector 1: The output voltage v_{AB} commutates between $+V_{\rm dc}$ and $+V_{\rm dc}/2$. The switching pattern is *PO-PN-ON-PN-PN-ON-PN-PO*, as depicted in Fig. 10(a). The switches S_{a2} and S_{b1} are OFF, while the other switches commutate. The control signal d_u regulates two complimentary switches S_{b2} and S_{b3}, while d_v and d_t are responsible for switches S_{a1} and S_{a3}.

Sector 2: v_{AB} commutates between $+V_{\rm dc}/2$ and 0. The switching pattern is *PO-OO-ON-OO-OO-ON-OO-PO*, as depicted in Fig. 10(b). Switches S_{a2} and S_{b1} are OFF, and the other switches commutate. The control signal d_u controls two complimentary switches S_{a1} and S_{a3}, while d_v and d_t are responsible for switches S_{b2} and S_{b3}.

Sector 3: v_{AB} commutates between 0 and $-V_{\rm dc}/2$. The switching pattern is *NO-OO-OP-OO-OO-OP-OO-NO*, as depicted in Fig. 10(c). Switches S_{a1} and S_{b2} are OFF, while the other switches commutate. The control signal d_u controls two complimentary switches S_{a2} and S_{a3}, while d_v and d_t are responsible for switches S_{b1} and S_{b3}.

Sector 4: v_{AB} commutates between $-V_{dc}/2$ and $-V_{\rm dc}$. The switching pattern is *NO-NP-OP-NP-NP-OP-NP-NO*, as depicted in Fig. 10(d). Switches S_{a1} and S_{b2} are OFF, and the other switches commutate. The signal d_u controls two complimentary switches S_{b1} and S_{b3}, while d_v and d_t are responsible for switches S_{a2} and S_{a3}. The process of the controller is briefly described in Fig. 11.

C. DC-Link Capacitor Reduction

From Fig. 6, assuming that $C_1 = C_2 = C$, the voltages of capacitors C_1 and C_2 are expressed follows:

$$V_{C1}(t) = V_{C2}(t) = \frac{1}{C}\int_0^t i_C(t)\,dt. \tag{12}$$

Four switching states *PO*, *OP*, *ON*, and *NO* affect the charged and discharged currents of the capacitors C_1 and C_2, which are depicted in Fig. 12. When the current i_{C1} discharges, the voltage V_{C1} decreases in the interval t_0–t_1 and does not change in the interval t_1–t_2. Then, i_{C1} is charged, and V_{C1} increases in the interval t_3–t_4 and remains unchanged in the interval t_3–t_4. The reverse process occurs in the rest of the sampling period. The voltage variation of capacitor C_1 can be calculated as

$$\Delta V_{C1} = \frac{\Delta Q_{1t}}{C} = \frac{i_{C1} \times d_x \times T_s}{C} \tag{13}$$

where d_x is the duty ratio of the switching states, and T_s is the sampling period.

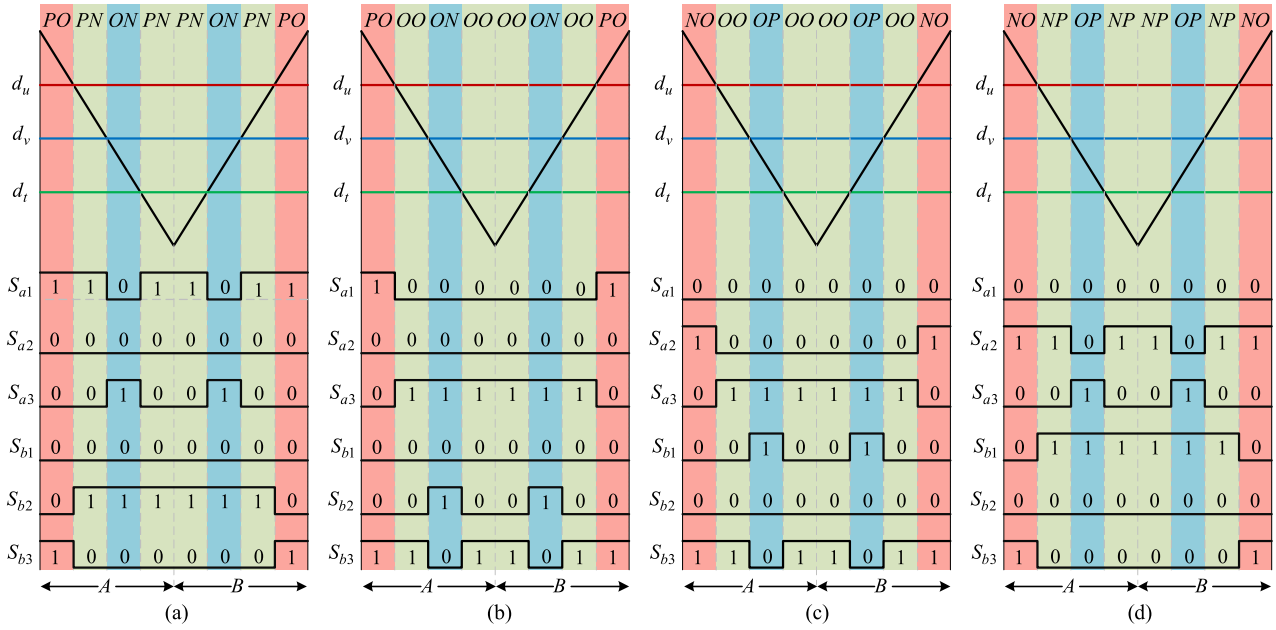


Fig. 10. Proposed PWM switching patterns. (a) Sector 1. (b) Sector 2. (c) Sector 3. (d) Sector 4.

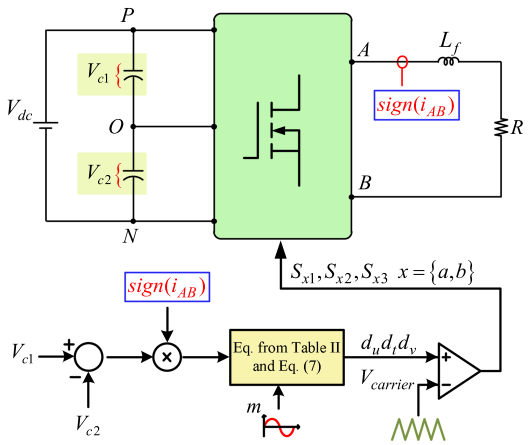


Fig. 11. Control diagram.

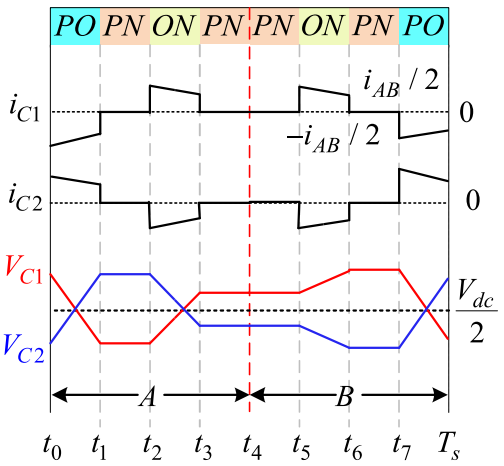


Fig. 12. Current and voltage of capacitors C_1 and C_2.

As indicated by (13), one way to reduce the capacitance C or voltage ripple is to reduce the interval of the switching states *PO*, *OP*, *ON*, and *NO* or increase the number of alternating current charging and discharging processes in one period. In the half-cycle A, the voltage variation of capacitor C_1 when C_1 discharged is $\Delta V_{C1} = 0.5 \times i_{C1} \times d_{PO} \times T_s/C$, and that when C_1 charged is $\Delta V_{C1} = 0.5 \times i_{C1} \times d_{\mathrm{ON}} \times T_s/C$. The current is charged and discharged twice in one period. Hence, the capacitance is reduced by half.

V. Comparison of Three-Level Half-Bridge DBI

Table III compares the three-level half-bridge among the conventional simplified NPC, the proposed, and other DBIs. Compared with the conventional inverter, two more external fast diodes and two inductors are required. However, owing to the current-limiting inductors, the reliability of the inverter is enhanced. The proposed inverter has no shoot-through problem and no reverse-recovery problem of the MOSFET body diode, because of the two external fast diodes. In addition, the PWM dead-time among the three switches is reduced or can be eliminated. Hence, the quality of the output waveforms is improved. Compared with other DBIs, the number of switches is reduced.

Table IV presents a comparison of the voltage stress on the switches. As shown, the voltage stress on the switches equal to V_{dc}, while it is equal to half of V_{dc} for the SD DBI and SS DBI.

However, the voltage stress on D_3 and D_4 of the proposed leg is reduced to a quarter of V_{dc}, while it is V_{dc} for the other DBIs.

VI. Simulation and Experimental Results

A. Simulation Results

PSIM simulation software was used to verify the operation of the proposed inverter. Table V gives the parameters of the

TABLE III
COMPARISON AMONG THE CONVENTIONAL INVERTER, THE PROPOSED DBI AND OTHER DBIS

Parameter	Inverters					
	SS DBI [22]	SD DBI [22]	NPC DBI [22]	FC DBI [23]	Conventional	Proposed
No. of switches	4	4	4	4	3	3
No. of diodes	4	4	4	2	4	6
No. of limiting inductors	2	2	2	2	0	2
Shoot-through worries?	no	no	no	no	yes	no
Reverse recovery issue on MOSFET's body diode	no	no	no	no	yes	no
Dead time between gate signals	can be eliminated	can be eliminated	can be eliminated	can be eliminated	cannot be eliminated	can be eliminated

TABLE IV
VOLTAGE STRESS AMONG THE CONVENTIONAL INVERTER, THE PROPOSED DBI, AND OTHER DBIS

	SD DBI	SS DBI	NPC DBI	FC DBI	Conventional	Proposed
V_{S1}, V_{S2}	V_{in}	$0.5V_{in}$	V_{in}	$0.5V_{in}$	V_{in}	V_{in}
V_{S3}, V_{S4}	$0.5V_{in}$	$0.5V_{in}$	$0.5V_{in}$	$0.5V_{in}$	$0.5V_{in}$ (S_3)	$0.5V_{in}$ (S_3)
V_{D1}, V_{D2}	$0.5V_{in}$	$0.5V_{in}$	V_{in}	$0.5V_{in}$	-	V_{in}
V_{D3}, V_{D4}	V_{in}	V_{in}	$0.5V_{in}$	-	$0.25V_{in}$	$0.25V_{in}$
V_{D5}, V_{D6}	-	-	-	-	$0.25V_{in}$	$0.25V_{in}$

TABLE V
SIMULATION AND EXPERIMENTAL SPECIFICATIONS

Input voltage	400 V
Output power	1.4 kW
Switching frequency (f_{sw})	30 kHz
Reference frequency (f)	60 Hz
MOSFET	IPW60R040C7
Freewheeling diode	RHRG3060
Capacitors C_1, C_2	272 µF
Inductors (L_{a1}, L_{a2}, L_{b1}, L_{b2})	100 µH
Inductance L_f	1.2 mH
Resistance R	35 Ω
Dead time	0.3 µs

proposed inverter. Fig. 13 shows the simulation results for the proposed inverter. The output voltage v_{AB} exhibits five levels: ±400 V, ±200 V, and 0 V. The output current (i_{AB}) is sinusoidal at 60 Hz with a 9-A peak. Each current-limiting inductor conducts in each half-cycle, where positive and negative currents flow through L_{a1}, L_{b2} and L_{a2}, L_{b1}, respectively. The capacitor voltages V_{C1} and V_{C2} are balanced and approximately equal to half of the input voltage 200 V.

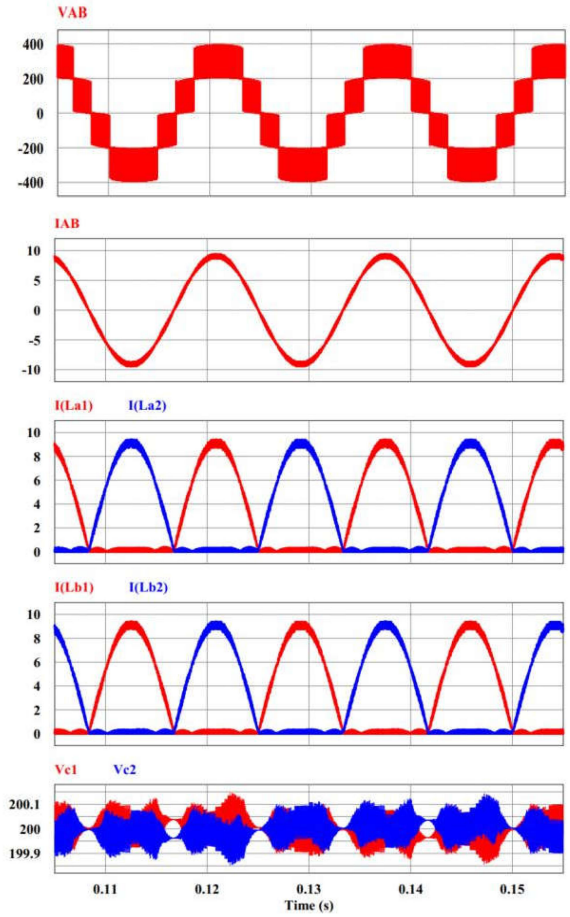


Fig. 13. Simulation results with $m = 0.8$. From top to bottom: Output voltage v_{AB}, output current i_{AB}, inductor currents i_{La1} and i_{La2}, inductor currents i_{Lb1} and i_{Lb2}, capacitor voltages V_{C1} and V_{C2}.

B. Experimental Results

The 1.4-kW prototype shown in Fig. 14 was implemented with the same simulation parameters. A microcontroller (F28335, Texas Instruments) was used to process the capacitor voltages, current signals and calculate the duty cycles. A field-programmable gate array implemented the PWM scheme for the proposed inverter. The gate signals are depicted in Fig. 15.

Fig. 16 presents the experimental results with resistive load $R = 35\ \Omega$ when $m = 0.8$. The output voltage v_{AB} exhibits five levels: ±400 V, ±200 V, and 0 V, as shown in Fig. 16(a). The output current i_{AB} has a peak at approximately 9 A and sinusoidal waveforms at 60 Hz. In Fig. 16(b), the capacitor

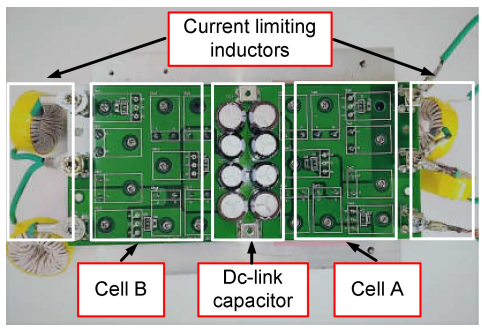


Fig. 14. Photograph of the proposed inverter.

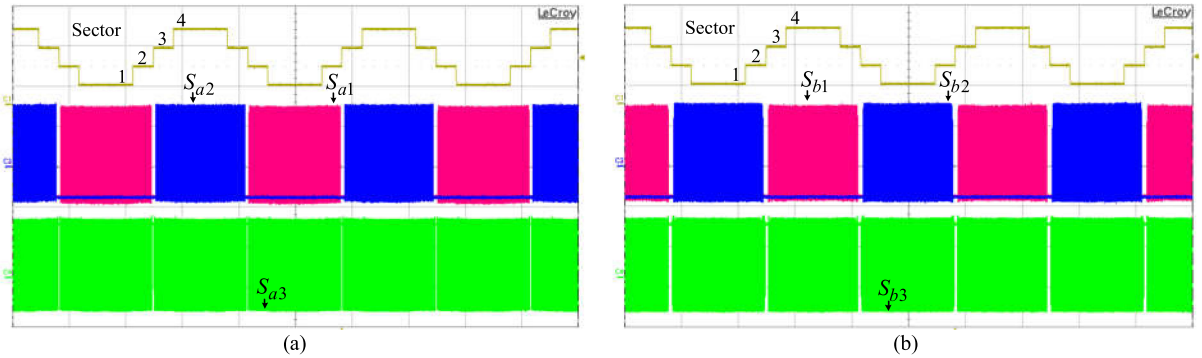


Fig. 15. Gate signals with $m = 0.8$. (a) S_{a1}, S_{a2}, and S_{a3}. (b) S_{b1}, S_{b2}, and S_{b3}.

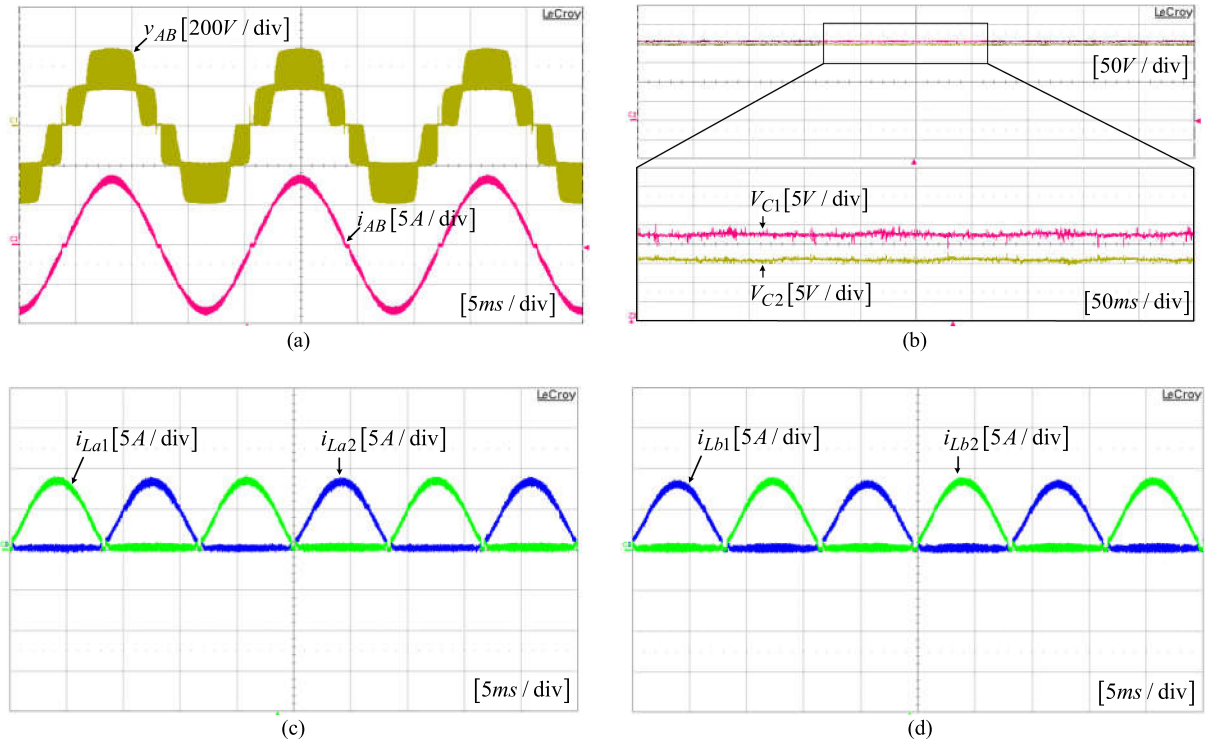


Fig. 16. Experimental waveforms of the proposed inverter with resistive load. (a) Output voltage v_{AB} and output current i_{AB}. (b) Magnified waveforms of capacitor voltages V_{C1} and V_{C2}. (c) Inductor currents i_{La1} and i_{La2}. (d) Inductor currents i_{Lb1} and i_{Lb2}.

voltages V_{C1} and V_{C2} are constant and approximately equal to 200 V in the steady state, $V_{C1} = 202$ V and $V_{C2} = 196$ V. The voltage ripples on capacitors C_1 and C_2 are low. Four current-limiting inductor currents are shown in Fig. 16(c) and (d). In Fig. 16(c), the currents i_{La1} and i_{La2} are phase-shifted by 180°. Each inductor only conducts in each half-cycle. The current amplitudes of i_{La1} and i_{La2} are 9 A. The current waveforms on inductors L_{b1} and L_{b2} are shown in Fig. 16(d). The peak currents are 9 A.

Fig. 17 presents the experimental waveforms with inductive load (power factor cos $\varphi = 0.88$), $R = 35\ \Omega$, $L = 50$ mH. The current i_{AB} lags the voltage v_{AB} as shown in Fig. 17(a). The two capacitor voltages are balanced and approximately equal to 200 V as shown in Fig. 17(b). The current waveforms on the shoot-through inductors are shown in Fig. 17(c) and (d). Fig. 18 shows the efficiency measured using a Yokogawa WT1600 power meter at different output powers. The maximum (97.05%) and minimum (95.5%) efficiency were achieved at 1 kW and 0.1 W, respectively.

VII. Power Loss of the Proposed Inverter

The body diode of MOSFET does not conduct in this topology; therefore, its power loss can be ignored. The main total power loss of the inverter includes the following: conduction loss and switching loss of the MOSFET and freewheeling diode. The power loss equations were mentioned in application note of Infineon [26]. Fig. 19 shows the percentage of conduction and switching

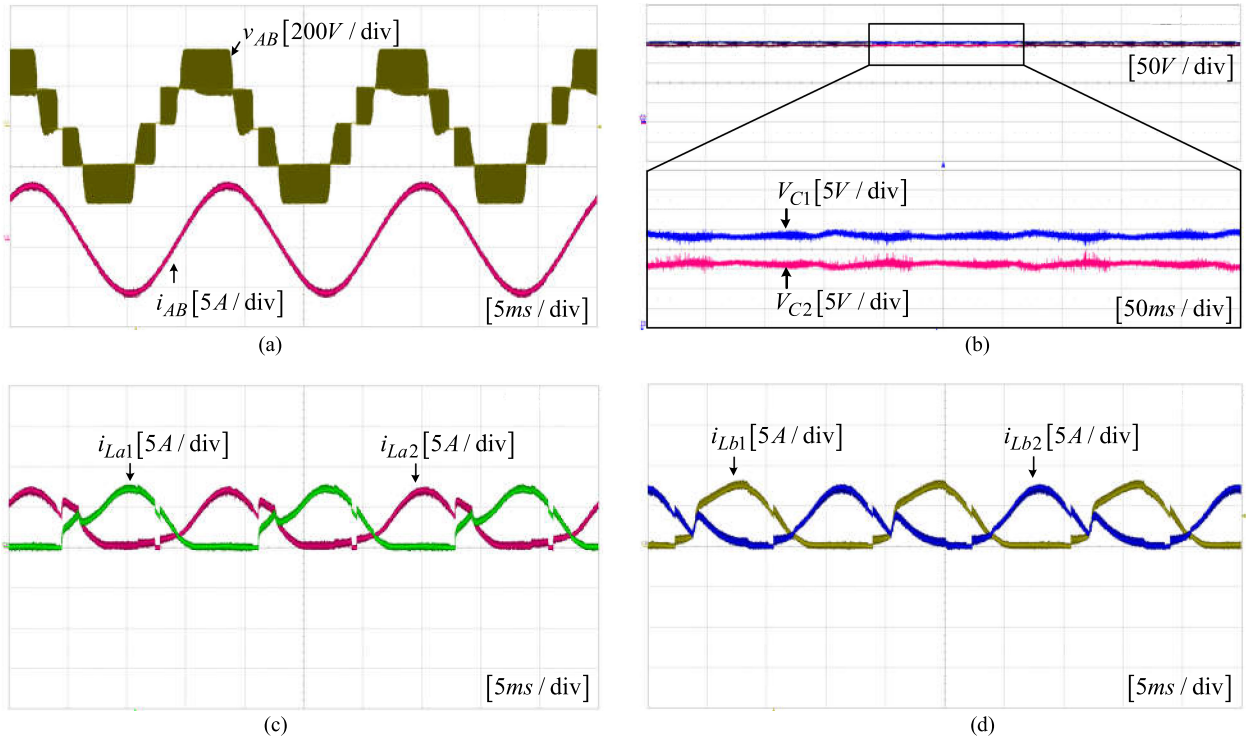


Fig. 17. Experimental waveforms of the proposed inverter with inductive load. (a) Output voltage v_{AB} and output current i_{AB}. (b) Magnified waveforms of capacitor voltages V_{C1} and V_{C2}. (c) Inductor currents i_{La1} and i_{La2}. (d) Inductor currents i_{Lb1} and i_{Lb2}.

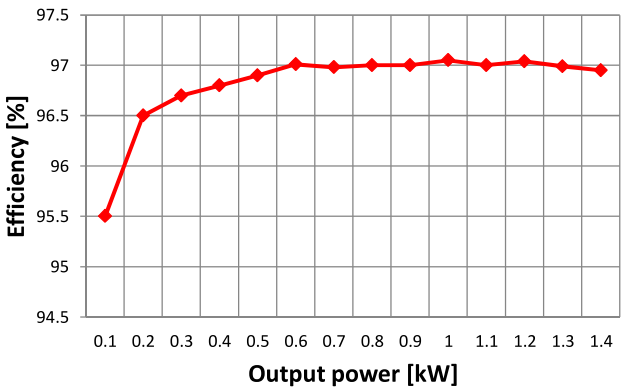


Fig. 18. Efficiency and output power of the proposed inverter.

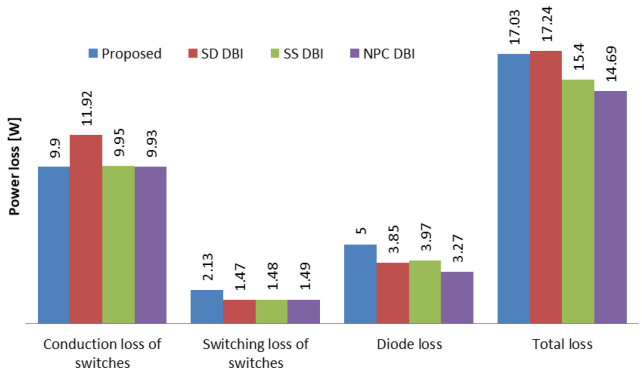


Fig. 20. Comparison of power loss between the proposed and other single-phase three-level DBIs.

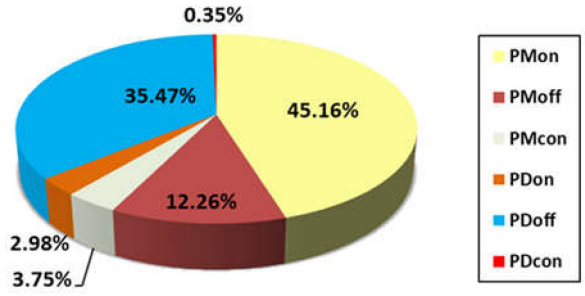


Fig. 19. Power loss of MOSFET and freewheeling diode.

loss of the MOSFET and freewheeling diode. *PMon*, *PMoff* , and *PMcon* are the turn ON, turn OFF, and conduction loss of MOSFET, respectively. *PDon*, *PDoff,* and *PDcon* are the turn-on, turn-off and conduction loss of the freewheeling diode respectively. The theoretical calculation of total power loss is 35.85 W compared to experimental measurement is about 42 W at the power 1.4 kW. The most losses come from turn-on loss of MOSFET and turn-OFF loss of freewheeling diode.

Fig. 20 shows the comparison of power loss between the proposed and other single-phase three-level DBIs in the same condition $V_{\rm in} = 400$ V, $P_{\rm o} = 1$ kW, $f_{\rm sw} = 30$ kHz with SPWM

method using Thermal Module of PSIM software. The conduction loss of the proposed inverter is the lowest because of less active switches while diode loss is larger. This is because the two diodes in series at the middle leg operate at high frequency in one period. Hence, the conduction loss of diode increases. The total loss of NPC is the lowest while SD DBI is the highest compared to other inverters.

VIII. Conclusion

A single-phase three-level DBI and novel PWM switching scheme are presented. The advantages of the proposed inverter are as follows: high reliability owing to no shoot-through worries; no reverse-recovery issue of the body diode of the MOSFET; a high switching frequency; therefore, the passive components can be reduced; reduction in the dc-link capacitance; and less active switches. The operational modes and circuit analysis of the proposed inverter are presented, and switching strategies are discussed for balancing the dc-link voltage. A 1.4-kW hardware prototype of the proposed topology is fabricated. The experimental results are presented to verify the performance of the proposed inverter.

References

[1] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level T-type converter for low-voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899–907, Feb. 2013.

[2] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative evaluation of advanced three-phase three-level inverter/converter topologies against two-level systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5515–5527, Dec. 2013.

[3] G. Ceglia, V. Guzman, C. Sanchez, F. Ibanez, J. Walter, and M. I. Gimenez, "A new simplified multilevel inverter topology for DC–AC conversion," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1311–1319, Sep. 2006.

[4] N. A. Rahim and J. Selvaraj, "Multistring five-level inverter with novel PWM control scheme for PV application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2111–2123, Jun. 2010.

[5] J. Selvaraj and N. A. Rahim, "Multilevel inverter for grid-connected PV system employing digital PI controller," *IEEE Trans. Ind. Electron.*, vol. 56, no. 1, pp. 149–158, Jan. 2009.

[6] L. Saro, K. Dierberger, and R. Redl, "High-voltage MOSFET behavior in soft-switching converters: Analysis and reliability improvements," in *Proc. 20th IEEE Telecom. Energy Conf.*, 1998, pp. 30–40.

[7] X. D. Huang, H. J. Yu, J.-S. Lai, A. R. Hefner, and D. W. Berning, "Characterization of paralleled super junction MOSFET devices under hard and soft-switching conditions," in *Proc. 32nd IEEE Power Electron. Spec. Conf.*, 2001, vol. 4, pp. 2145–2150.

[8] A. Huang, "Hard commutation of power MOSFET OptiMOS FD 200V/250V," Infineon, Neubiberg, Germany, Mar. 2014, pp. 1–13.

[9] N. R. Zargari, P. D. Ziogas, and G. Joos, "Two switch high performance current regulated DC/AC converter module," in *Proc. Conf. Rec. IEEE Ind. Appl. Soc. Annu. Meet.*, 1995, pp. 929–934.

[10] B. Gu, J. Dominic, J. Lai, C. Chen, T. LaBella, and B. Chen, "High reliability and efficiency single-phase transformerless inverter for grid-connected photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2235–2245, May 2013.

[11] P. Sun, C. Liu, J. Lai, C. Chen, and N. Kees, "Three-phase dual-buck inverter with unified pulse width modulation," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1159–1167, Mar. 2012.

[12] A. A. Khan and H. Cha, "Dual-buck-structured high-reliability and high-efficiency single-stage buck–boost inverters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3176–3187, Apr. 2018.

[13] B. L. Nguyen, H. Cha, and H. Kim, "Single-phase six-switch dual-output inverter using dual-buck structure," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7894–7903, Sep. 2018.

[14] A. A. Khan, H. Cha, H. F. Ahmed, J. Kim, and J. Cho, "A highly reliable and high-efficiency quasi single-stage buck–boost inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4185–4198, Jun. 2017.

[15] A. A. Khan, H. Cha, and H. Kim, "Three-phase three-limb coupled inductor for three-phase direct PWM AC–AC converters solving commutation problem," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 189–201, Jan. 2016.

[16] A. A. Khan, H. Cha, H. F. Ahmed, and H. Kim, "Elimination of filter inductor in switching cell AC–AC converters using magnetic integration," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6317–6326, Sep. 2016.

[17] A. A. Khan, H. Cha, and H. F. Ahmed, "High-efficiency single-phase AC–AC converters without commutation problem," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5655–5665, Aug. 2016.

[18] A. A. Khan, H. Cha, and H. F. Ahmed, "An improved single-phase direct PWM inverting buck–boost AC–AC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5384–5393, Sep. 2016.

[19] A. A. Khan, H. Cha, and H. F. Ahmed, "A new reliable three-phase buck-boost AC–AC converter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1000–1010, Feb. 2018.

[20] P. Sun, C. Liu, J. Lai, and C. Chen, "Cascade dual buck inverter with phase-shift control," *IEEE Trans. Ind. Electron.*, vol. 27, no. 4, pp. 2067–2077, Apr. 2012.

[21] A. A. Khan, H. Cha, J. Baek, J. Kim, and J. Cho, "Cascaded dual-buck AC–AC converter with reduced number of inductors," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7509–7520, Oct. 2017.

[22] L. Zhang, K. Sun, Y. Xing, and J. Zhao, "A family of five-level dual-buck full-bridge inverters for grid-tied applications," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7029–7042, Oct. 2016.

[23] M. Liu, F. Hong, and C.-H. Wang, "A novel flying-capacitor dual buck three-level inverter," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, USA, Mar. 17–21, 2013, pp. 502–506.

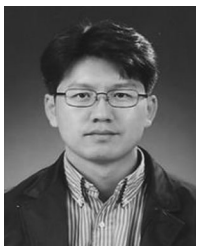
[24] N. Sun, Li Zhang, Y. Xing, M. Xu, Y. Fang, and X. Ma, "A five level dual buck full bridge inverter with neutral point clamp for grid connected PV application," in *Proc. 37th Annu. Conf. IEEE Ind. Electron. Soc.*, 2011, pp. 1041–1045.

[25] J. Salaet, A. Gilabert, J. Bordonau, S. Alepuz, A. Cano, and L. M. Gimeno, "Nonlinear control of neutral point in three-level single-phase converter by means of switching redundant states," *Electron. Lett.*, vol. 42, no. 5, pp. 304–306, Mar. 2006.

[26] G. Dusan, P. Macro, and K. Andreas, "MOSFET power losses calculation using the datasheet parameters," Infineon, Neubiberg, Germany, Jul. 2006.

Tien-The Nguyen (S'XX) was born in Vietnam. He received the B.S degree in electrical and electronics engineering from Bach Khoa University (HCMUT), Ho Chi Minh City, Vietnam, in 2016. He is currently working toward the Ph.D. degree at the School of Energy Engineering, Kyungpook National University, Daegu, South Korea.

He was a Laboratory Technician with International University—VNU-HCM. His current research interests include power converter topology, integrated magnetic design, Z-source converters, and control for power converters and power conversion for electric vehicles.



Honnyong Cha received the B.S. and M.S. degrees in electronics engineering from Kyungpook National University, Daegu, South Korea, in 1999 and 2001, respectively, and the Ph.D. degree in electrical engineering from Michigan State University, East Lansing, MI, USA, in 2009.

From 2001 to 2003, he was a Research Engineer with the Power System Technology (PSTEK) Company, An-san, South Korea. From 2010 to 2011, he was a Senior Researcher with the Korea Electrotechnology Research Institute, Changwon, South Korea. In 2011, he was with the School of Energy Engineering, Kyungpook National University. In 2017, he was with the Future Energy Electronics Center, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, as a Visiting Scholar. His current research interests include high-power dc–dc converters, dc–ac inverters, Z-source inverters, and power conversion for electric vehicles and wind power generation.

Bang Le-Huy Nguyen received the B.S. and M.S. degrees in electrical and electronics engineering from Bach Khoa University, Ho Chi Minh City, Vietnam, in 2010 and 2013, respectively. He is currently working toward the Ph.D. degree with the School of Energy Engineering, Kyungpook National University, Daegu, South Korea.

In 2015, he was with the School of Engineering, Eastern International University, Binh Duong New City, Vietnam, as a Lecturer. His current research interests include power converter topology, integrated magnetic design and control for power converters, and renewable energy systems.

Heung-Geun Kim (S'82–M'88–SM'12) was born in South Korea in 1956. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1980, 1982, and 1988, respectively.

Since 1984, he has been with the Department of Electrical Engineering, Kyungpook National University, Daegu, South Korea, where he is currently a Full Professor and the Director of the Microgrid Research Center. From 1990 to 1991, he was a Visiting Scholar with the Department of Electrical and Computer Engineering, University of Wisconsin-Madison, and from 2006 to 2007, he was with the Department of Electrical Engineering, Michigan State University, East Lansing, MI, USA. His current research interests are ac machine control, PV power generation, and micro grid system.