A High Efficiency and Fast Transient Digital Low-Dropout Regulator With the Burst Mode Corresponding to the Power-Saving Modes of DC–DC Switching Converters

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***Abstract*—The proposed digital low-dropout regulator uses nonlinear switching control (NLSC) technique to suppress voltage ripple to less than 6 mV when the switching noise voltage of a switching regulator operating in a power-saving mode is greater than 50 mV. In addition, the NLSC technique improves the current efficiency by reducing the quiescent current to less than 10 μA and reduces the switching power loss through variable switching frequency control. With a load step of 1–20 mA, the transient response time is 1.3 μs and the peak current efficiency is 99.8% at heavy loads.**

***Index Terms*—Digital low-dropout regulator (DLDO), nonlinear switch control (NLSC) technique, power-saving mode, variable switching frequency control.**

I. Introduction

INTEGRATED power management solutions are an integral part of the system-on-a-chip (SoC) systems [1]. The integrated power management is composed of the high-efficiency switching regulator and multiple cascaded low-dropout (LDO) regulators [2], [3] for providing distributive voltages and currents to different functional blocks. In order to achieve high performance and high efficiency in SoC, the dynamic voltage scaling (DVS) technology is adopted to scale up the supplying voltage for high-performance operation and scale down the supplying for high efficiency. Conventional analog LDO regulators can suppress the noise of switching regulator, but they are either unsuitable for low-voltage operation [4], [5], or have a limited gain-bandwidth product [6], [7]. Cascaded multiple digital LDO (DLDO) regulators withstand low-voltage operation and provide a wide range of $V_{\rm OUT}$ (0.5–1 V) for DVS technology [8]–[15]. Fig. 1(a) shows the structure of the switching regulator with the cascaded barrel-shifter DLDO regulator [8]. However, DLDO regulators have some limitations. When the switching regulator operates in a power-saving mode, such as skip mode or pulse frequency modulation (PFM), the induced large output voltage ripple $\Delta V_{\rm SWR}$ deteriorates the current conversion efficiency of DLDO regulators and reduces the output voltage regulation capability. A large $\Delta V_{\rm SWR}$ can also cause severe limit cycle oscillation (LCO) problems, resulting in a large voltage ripple $\Delta V_{\rm OUT}$ at the output of the DLDO regulator, as shown in Fig. 1(b). $\Delta V_{\rm SWR}$ is considered as the line voltage disturbance

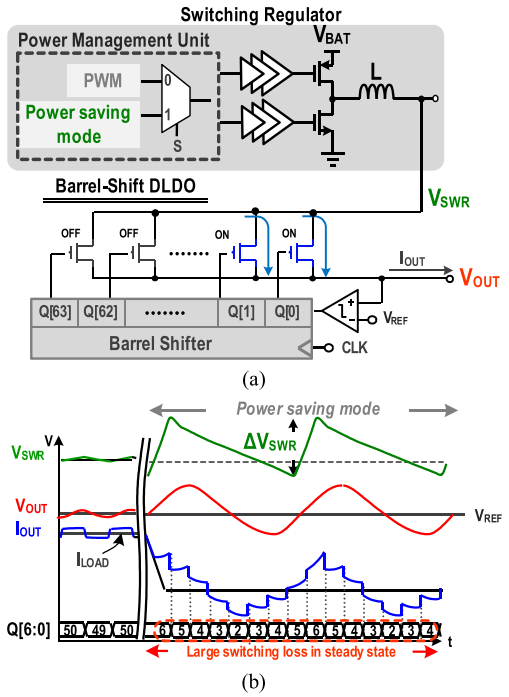

Fig. 1. (a) Structure of the DLDO regulator based on the barrel-shifter register. (b) Effects of the ripple of $V_{\rm SWR}$ at $V_{\rm OUT}$.

Manuscript received March 20, 2019; revised July 2, 2019; accepted August 26, 2019. Date of publication September 3, 2019; date of current version January 10, 2020. This work was supported by the Ministry of Science and Technology under Grants 108-2622-E-009-007-CC2, 106-2221-E-009-165-MY3, 106-2221-E-009-095-MY3, and 107-2321-B-468-001. Recommended for publication by Associate Editor W.-H. Ki. *(Corresponding author: Ke-Horng Chen.)*

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Digital Object Identifier 10.1109/TPEL.2019.2939415

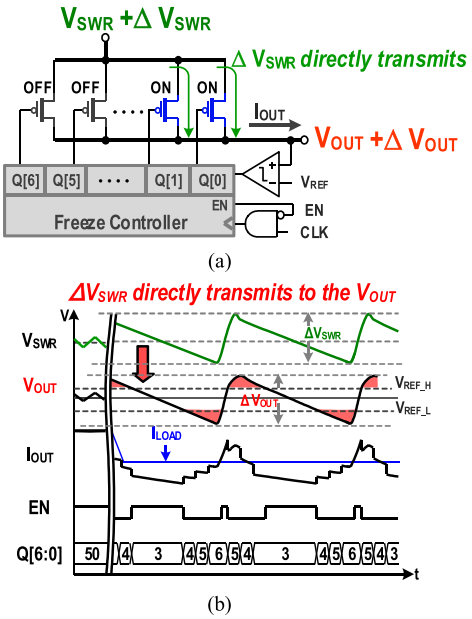

Fig. 2. (a) Structure of the DLDO regulator with freeze mode. (b) Effect of the ΔV_{SWR} on the V_{OUT} in the freeze mode.

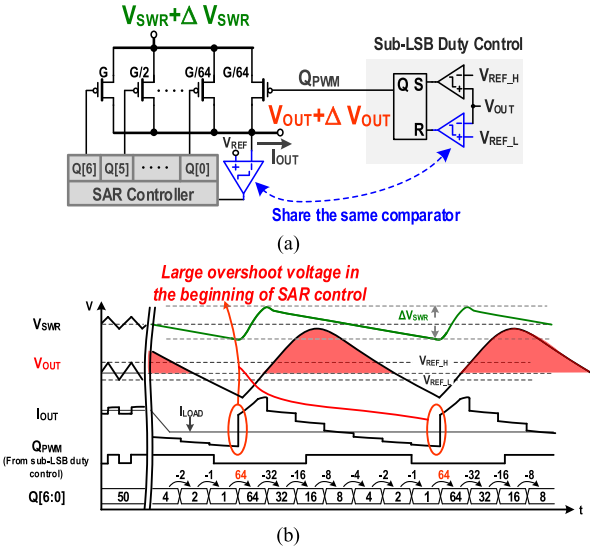

Fig. 3. (a) Architecture of the recursive DLDO regulator. (b) Operation waveforms of recursive DLDO regulator.

of the DLDO regulator. As a result, the steady state is interrupted, causing the DLDO regulator to quickly turn ON or OFF a large number of p-type power MOSFETs to provide more or less output current to regulate the V_{OUT}. Therefore, even if the switching regulator remains stable, the DLDO regulator will experience a large switching power loss, reducing the overall efficiency.

To reduce the aforementioned problem, the structure of a DLDO regulator with the freeze mode shown in Fig. 2(a) [13] is proposed. This DLDO is composed of a comparator, a p-type power MOSFET array, a barrel shifter with freeze mode, and clock gate logic. Freeze mode can decrease power loss and reduce output voltage ripple but it is achieved at the expense of losing output voltage regulation ability. Q[63:0] turns off the power switches during initialization and settles to a load current corresponding value during the regulation process. The switching signals are frozen in steady state to minimize loss. Unfortunately, the output voltage V_{OUT} is inherently exposed to large voltage fluctuations and ΔV_{SWR} is transparent to the V_{OUT} without any regulation by the DLDO regulator. Fig. 2(b) illustrates the effect of ΔV_{SWR} on the V_{OUT} in freeze mode. When the ΔV_{SWR} causes V_{OUT} to reach the boundary of the hysteresis window $(V_{\mathrm{REF\_}H}, V_{\mathrm{REF\_}L})$, the DLDO regulator changes from a steady state to a transient state and leaves the freeze mode to regulate V_{OUT}, causing large power losses, negating the power saving achieved by the switching regulator. Similar disadvantages occur in the DLDO regulator with the anti-process, voltage, and temperature (PVT)-variation technique [15].

Another approach, shown in Fig. 3(a), features a recursive DLDO regulator [15] consisting of a 7-bit binary-weighted P-type power switch array, coarsely tuned by a proportional-derivative successive-approximation recursive algorithm to quickly find the final array conductance value V_{OUT} and V_{REF}. The pulsewidth modulation (PWM) control signal Q_{PWM} will be set to 1 if V_{OUT} is greater than $V_{\mathrm{REF\_}H}$, and 0 if V_{OUT} is less than $V_{\mathrm{REF\_}L}$ as shown in Fig. 3(b). At the next clock, if the comparator detects that V_{OUT} is greater than V_{REF}, then, the p-channel metal-oxide-semiconductor (PMOS) array is consequently switched OFF from the (MSB-1) to the LSB during the other six cycles. When ΔV_{SWR} is greater than its hysteresis window, the transient process is still susceptible to additional switching loss and large output voltage ripple.

In this article, the DLDO using burst mode technique to reduce ΔV_{OUT} and increase the overall light load efficiency corresponding to the power saving modes in switching regulators is proposed. The DLDO utilizes the nonlinear switching control (NLSC) technique, which is capable of simultaneously achieving both reduced output voltage ripple and enhanced efficiency by decreasing the number of ON/OFF power switches and changes the switching frequency corresponding to the ΔV_{SWR} of the switching regulator. Moreover, the proposed transient enhancement technique decreases the response time when the DLDO leaves the burst mode.

The organization of this article is shown as follows. Section II shows the operation of the burst mode technique in the proposed DLDO regulator, which reduces the output voltage ripple and improves efficiency. Also, the advantages and drawbacks of the linear switching control technique are discussed, followed by the improved NLSC technique which features both reduced output voltage ripple and increased efficiency. Section III shows the circuit implementation. Experimental results prove this work in Section IV. Finally, conclusions are made in Section V.

II. Proposed DLDO Regulator With the Burst Mode Technique and the NLSC Technique

Fig. 4 shows the architecture of the proposed DLDO regulator featuring both the burst mode technique and transient enhancement technique. The differences between large ΔV_{SWR} ripple

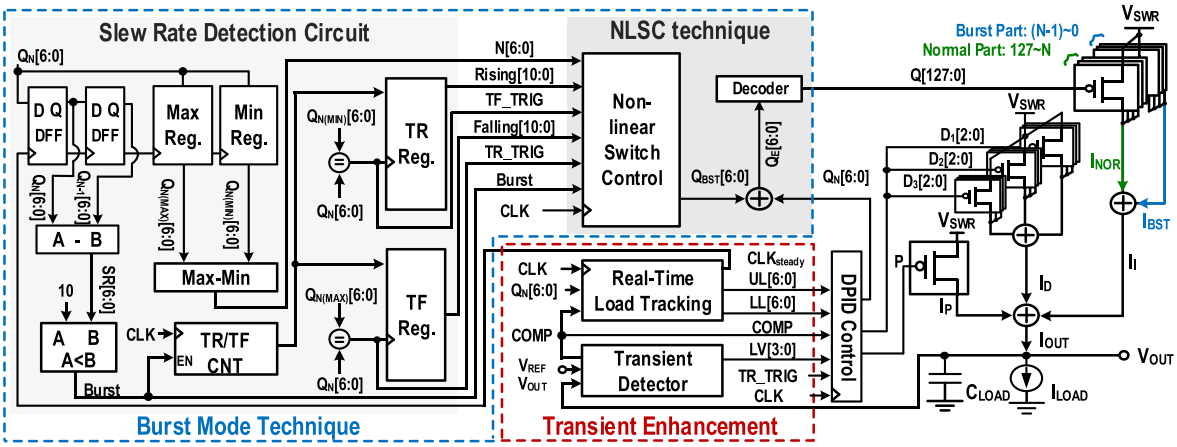

Fig. 4. Overall architecture of the DLDO with the burst mode technique controlled by the proposed NLSC technique.

and transient perturbance on V_{OUT} are distinguished with the slew rate detection circuit featured within the burst mode technique. The number of ON-switches of the current state is denoted as Q_N and the previous state is denoted as Q_{N-1}. When the difference between Q_N and Q_{N-1} is less than or equal to a predefined value *K*, the DLDO regulator enters the burst mode. The key component of this mode includes a slew rate detection circuit that features the NLSC technique, which is designed to further reduce ΔV_{OUT} by changing the switching frequency according to the ΔV_{SWR} falling and rising time periods to turn the switches ON and OFF, respectively, thereby reducing the switching losses of the DLDO regulator. Compensation is achieved with a digital proportional-integral-derivative (DPID) compensator including a proportional (P) compensator, a derivative (D) compensator ($D_{1\text{-}3}$[2:0]), and an integral (I) compensator (I [127:0]). By default, the DLDO regulator is solely controlled by the DPID compensator to reduce the ΔV_{OUT} by controlling normal part (127∼N) and setting current quantization error to one. On the other hand, the burst mode technique controls the burst part (N∼1) to reduce ΔV_{OUT} at light loads in the burst mode.

The transient enhancement technique consists of a transient detector circuit and a real-time load-tracking circuit to control P, I, and D signals and accelerate transient response speed. The output of the transient detector LV[3:0] is the digital equivalent of the difference between the V_{OUT} and the reference voltage V_{REF}. LV[3:0] is then fed into the digital PID compensator to generate the currents I_P and I_D by turning ON and OFF the transistor P and the grouped transistors through D_1[2:0], D_2[2:0], and D_3[2:0] with the proposed controller. By using this technique, voltage variations are decreased and load transient response is accelerated. Finally, the real-time load-tracking circuit minimizes current quantization error to one by setting the difference between the current upper limit signal UL [6:0] and the current lower limit signal LL [6:0] to one.

A. Slew Rate Detection Technique

The slew rate detection technique shown in Fig. 5(a) involves checking the signal SR[6:0] that stores the difference between

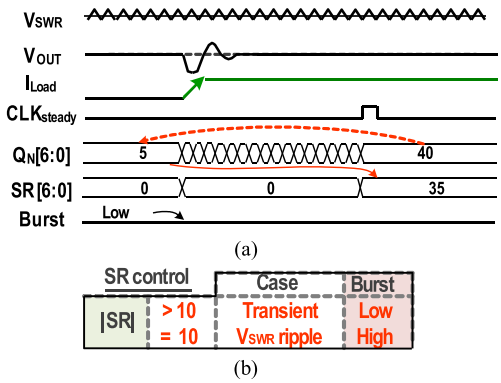

Fig. 5. (a) Operating waveform of slew rate detection during the transient response. (b) Decision of burst mode by the value of SR.

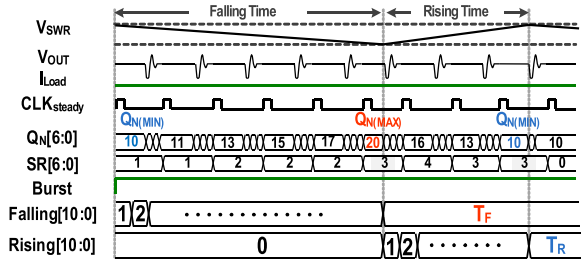

Fig. 6. Timing diagram of the proposed slew rate detection.

the current value $Q_N[6:0]$ and the previous value of $Q_{N-1}[6:0]$. If the absolute value of SR[6:0] is greater than *K* [$K = 10$ in Fig. 5(b) in this article], the system determines that a transient perturbation has occurred.

On the other hand, when the switching regulator enters the power-saving mode, the value of SR[6:0] is less than or equal to *K*. To compensate for the increased ΔV_{SWR}, the DLDO regulator enters the burst mode by setting the signal "Burst" to high, as shown in Fig. 6. During the burst mode, the slew rate detection records the number of turn-ON power switches during the falling time (T_F) of V_{SWR} at the positive edge of

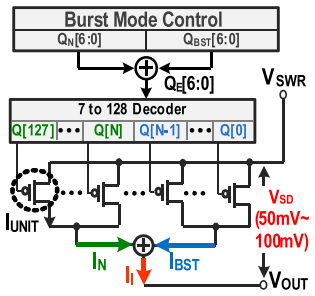

Fig. 7. Structure of I control part.

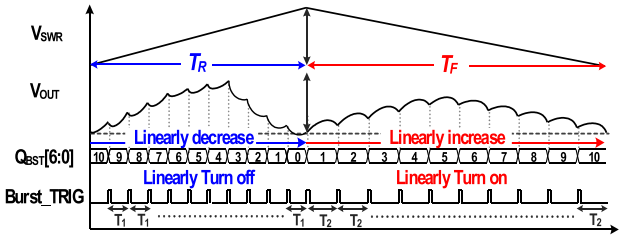

Fig. 8. Operation waveform of the linear switching control technique.

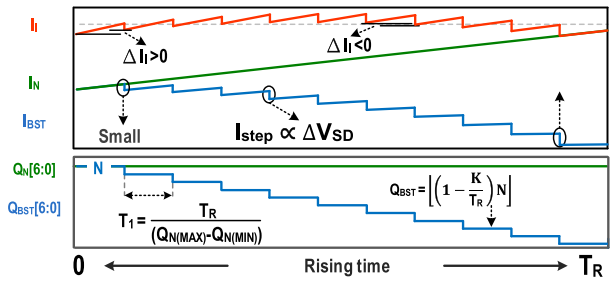

Fig. 9. Disadvantages caused by the nonideal effect of the V_{SD} variations.

the clock signal $(\mathrm{CLK})_{\mathrm{steady}}$. Thus, T_F and the maximum number $Q_{N(\mathrm{MAX})}$ of turn-ON switches are recorded in the signals Falling[10:0] and $Q_{N(\mathrm{MAX})}[6:0]$, respectively when V_{SWR} reaches the lower bound. On the contrary, the rising time (T_R) and the minimum number $Q_{N(\mathrm{MIN})}$ of turn-ON switches are stored to the signals Rising[10:0] and $Q_{N(\mathrm{MIN})}[6:0]$ separately when V_{SWR} reaches the upper bound.

B. Linear Switch Control Technique

To understand NLSC, conventional linear switching control technique must be discussed. Fig. 7 shows the integral (I) control part consisting of $Q_N[6:0]$ and the burst part Q_{BST}[6:0], which represents the number of ON power switches in burst mode. The sum of $Q_N[6:0]$ and Q_{BST}[6:0] is recorded as $Q_E[6:0]$ with a 7-bit register. A 7-to-128 decoder converts $Q_E[6:0]$ into the Q[127:0] thermometer code, with the ON/OFF of each power transistor. The combined current I_I is represented by (1), which is the sum of the nominal part (127∼0) I_N in (2) and the burst part (N∼1) I_{BST} in (3), where I_{UNIT} is the unit current of each unit power transistor

$$I_I = I_N + I_{\mathrm{BST}} \tag{1}$$

$$I_N = Q_N \times I_{\mathrm{UNIT}} \tag{2}$$

$$I_{\mathrm{BST}} = Q_{\mathrm{BST}} \times I_{\mathrm{UNIT}}. \tag{3}$$

The power switch array is operated in the triode region to minimize dropout voltage across V_{SD}. To suppress the noise from the switching regulator, the linear switching control technique suppresses output voltage ripple in burst mode by linearly reducing the number of ON/OFF switches. On the rising slope of V_{SWR} during T_R, V_{SD} increases, and both I_{BST} and I_N increase accordingly. During the falling slope, the linear switching control linearly increases Q_{BST}[6:0] and adds the burst current I_{BST} to the current I_I of the I part. In contrast, during the falling slope T_F of V_{SWR}, the linear switching control linearly reduces Q_{BST}[6:0] to subtract the burst current I_{BST} from I_I. The operation waveform is shown in Fig. 8.

A power switch is turned on at every T_1 time period during T_F at the positive edge of Burst_TRIG, which is defined by (4), and the number of ON-state power switches changes from $Q_{N(\mathrm{MIN})}$ to $Q_{N(\mathrm{MAX})}$

$$T_1 = T_F/(Q_{N(\mathrm{MAX})} - Q_{N(\mathrm{MIN})}). \tag{4}$$

Meanwhile, a power switch is turned off at every T_2 time period during T_R at the positive edge of Burst_TRIG, which is defined by (5), and the number of ON-state power switches changes from $Q_{N(\mathrm{MAX})}$ to $Q_{N(\mathrm{MIN})}$

$$T_2 = T_R/(Q_{N(\mathrm{MAX})} - Q_{N(\mathrm{MIN})}). \tag{5}$$

Fig. 9 shows that during the rise time of V_{SWR}, the I_{BST} must be reduced to maintain the I_I current so that I_I is close to load current. Therefore, linear switching control reduces Q_{BST}[6:0] from N to 0 to reduce I_{BST}, as shown in the following:

$$0 \le K \le T_R \tag{6}$$

$$Q_{\mathrm{BST}} = \left\lfloor \left(1 - \frac{K}{T_R}\right) N \right\rfloor. \tag{7}$$

However, when V_{SD} increases, I_{step} of I_{BST} and I_N gradually increase. Initially, the value of the I_I current rises much higher than I_{step}, the current that is reduced when a power switch is turned off at every T_1 time period. The overall response results in ΔI_I larger than zero at the beginning and produces an unwanted overshoot voltage. On the other hand, ΔI_I is less than zero at the end of the rise time of V_{SWR} rise. In contrast, as shown in (8) and (9), during the fall time of V_{SWR}, the I_{BST} needs to increase by increasing Q_{BST}[6:0] from 0 to N. The overall response results in ΔI_I less than zero at the beginning, and a large undershoot voltage occurs, but ΔI_I is larger than zero at the end of the fall time of V_{SWR}. Hence, the perturbation caused by ΔI_I results in an increase of ΔV_{OUT}

$$0 \le K \le T_F \tag{8}$$

$$Q_{\mathrm{BST}} = \frac{KN}{T_F}. \tag{9}$$

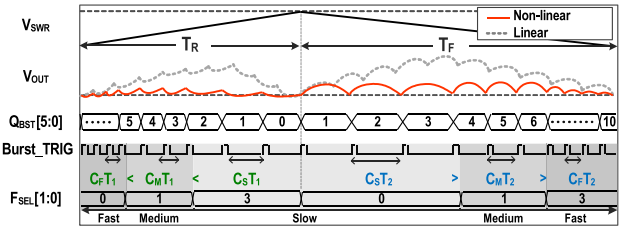

Fig. 10. Operation waveform of the NLSC technique.

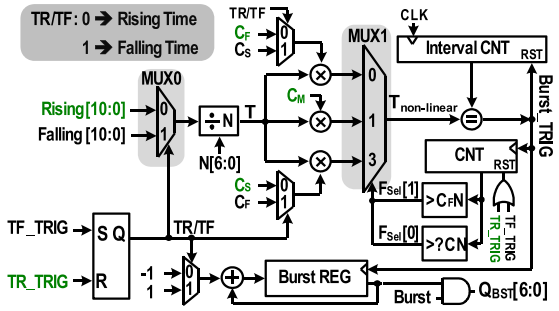

Fig. 11. Structure of the proposed NLSC technique.

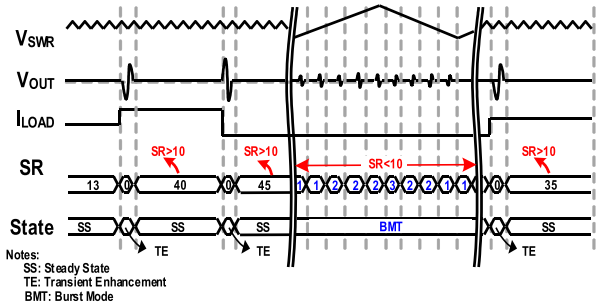

Fig. 12. Sequence of TE and burst mode technique.

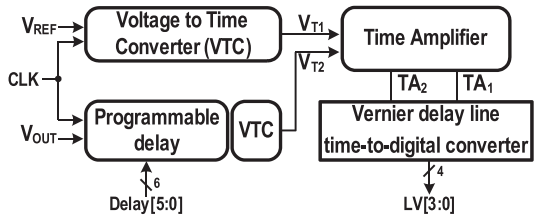

Fig. 13. Structure of the transient detector.

In summary, the linear switching control technique is capable of slightly reducing $\Delta V_{\rm OUT}$, but at the expense of doubling the frequency of the switching noise in comparison to clock frequency, causing extra power loss and unwanted high-frequency interferences. The NLSC technique is improved upon linear switching control and modifies the switching frequency to further suppress $\Delta V_{\rm OUT}$ and reduce power loss.

C. Proposed NLSC Technique

To avoid the aforementioned problems, a nonlinear approach to switch control, NLSC, is adopted where T_1 and T_2 are weighted with multiple time coefficients, C_F (fast), C_M (medium), and C_S (slow), to best suit the increase or decrease rate of $Q_{\rm BST}[6:0]$. In Fig. 10, Rising[10:0] is divided into three time segments, fast, medium, and slow to turn OFF the power switch array during T_R. The turn-OFF frequency is adjusted by the selection signal $F_{\rm SEL}[1:0]$. The operation initiates with a fast frequency for a time period of $C_F T_1$, and the value of $Q_{\rm BST}[6:0]$ is rapidly decreased. On the second segment, the turn-OFF frequency is decreased for a time period of $C_M T_1$, and eventually slows down the switching frequency to the minimum speed for a $C_S T_1$ time period. From empirical simulation results, C_F, C_M, and C_S are optimized to ⅔, 1, and 1⅓.

Fig. 11 shows the circuit implementation of the NLSC technique. During T_F, TR_TRIG is set to 1 and the output signal TR/TF of SR latch is set to 0. Therefore, Rising[10:0] is selected from MUX0 and is divided by N[6:0] (equivalent to $Q_{N({\rm MAX})} - Q_{N({\rm MIN})}$) to obtain the time interval T for turning off the power switches. In order to achieve nonlinear time interval switching control, T is divided into $C_F T$ and $C_S T$. At the initial segment of T_F, MUX1 sets $T_{\rm non\text{-}linear}$ to $C_F T$, Burst_TRIG is triggered every $T_{\rm non\text{-}linear}$ time period, and the counter is incremented by one. If the counter is greater than the difference between the coefficients ΔC, the $Fsel[0]$ is set to 1 to operate at $C_M T$. The sequence finalizes by setting to $C_S T$ to slow down the switching frequency.

To conclude, the slew rate detection technique detects the difference of PMOS array between the previous state and the current state to be the criteria to determine which mode needs to be operated. Even if the front-end dc–dc converter enters the power-saving mode and the presented circuit operates the burst mode technique, the circuits responsible for TE still monitor the output voltage to prevent the large voltage droop when sudden load transient occurs, as shown in Fig. 12. Therefore, both transient enhancement and burst mode technique works in conjunction to enhance the overall performance of the DLDO.

III. Circuit Implementations

A. Transient Detector

Fig. 13 shows the architecture of a transient detector consisting of a voltage-to-time converter (VTC), a time amplifier (TA), and a Vernier delay line time-to-digital converter. The VTC circuit converts $V_{\rm REF}$ and $V_{\rm OUT}$ to V_{T1} and V_{T2}, which are PWM signals with pulsewidth proportional to the analog input voltage. A time amplifier is used to magnify the time difference between V_{T1} and V_{T2} to T_{A1} and T_{A2}. This implementation increases the effective resolution of the Vernier delay line time-to-digital converter to generate LV[3:0], which indicates the difference between $V_{\rm REF}$ and $V_{\rm OUT}$. Programmable delays can be inserted to avoid the overflow or a cycle miss of the transient enhancement.

A VTC in Fig. 14(a) is used to map a voltage signal to a time domain signal. The VTC consists of a current-starved inverter, which is a static inverter whose charge or discharge current is

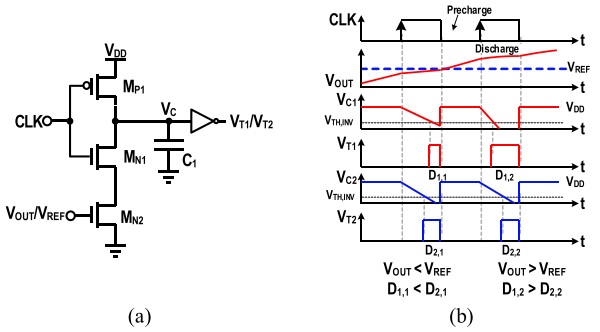

Fig. 14. Circuit implementation of VTC. (a) Schematic. (b) Timing diagram.

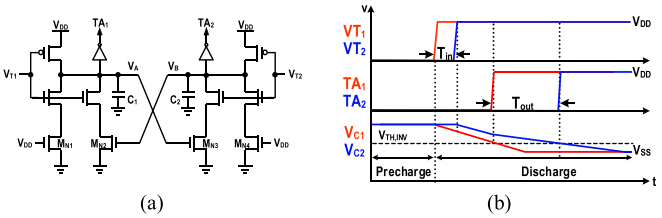

Fig. 15. Circuit implementation of time amplifier. (a) Schematic. (b) Timing diagram.

controlled by the current source, the load capacitor C_1, and the static inverter. The operation waveform is shown in Fig. 14(b). When CLK is low, the voltage V_C is precharged to V_{DD}. When CLK is high, V_C discharges to zero. The discharge rate of V_C is determined by changing the discharge current of transistor M_{N2} through the control of $V_{\rm IN}$. Finally, V_C is applied to the inverter and $V_{\rm OUT}$ is set high when V_C is less than the threshold voltage of the inverter ($V_{\rm TH,INV}$). Therefore, the pulsewidth of the output voltage $V_{\rm OUT}$ is proportional to the analog input voltage $V_{\rm IN}$. If $V_{\rm IN}$ is large, $V_{\rm OUT}$ has a higher duty cycle. The time difference between the two duty ratios, which are generated by the VTC with $V_{\rm REF}$ input and the VTC with $V_{\rm OUT}$ input (represented by V_{T1} and V_{T2}, respectively), are used to generate an error signal through the time amplifier circuit.

Structure and timing diagram of the time amplifier is shown in Fig. 15(a) and (b), respectively. During the precharge phase, V_{T1} and V_{T2} are low, and nodes V_A and V_B are initially precharged to V_{DD}. The output of the time amplifier is determined by the discharge time of V_A and V_B corresponding to the capacitors C_1 and C_2, respectively when the rising transitions of the inputs are applied. Discharging of the capacitor C_1 (or C_2) is performed by a pull-down path of the inverter controlled by the current source M_{N1} (or M_{N4}). In addition, another cross-coupled discharge path is controlled by M_{N2} (or M_{N3}). The strength of one cross-coupled discharge path is determined by the discharging status of the counterpart node, resulting in an enlarged time difference.

Fig. 16(a) shows the structure of the Vernier delay line time-to-digital converter composed of two identical delay lines and flip-flops. Each delay unit has the delay time t_1 and t_2 for upper and lower delay lines, respectively. Each conversion has two phases: 1) the sampling phase and 2) the pulse propagation phase. During the sampling phase, the D flip flop (DFF) acquires

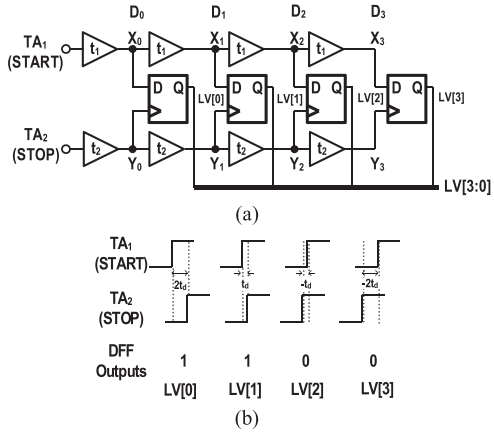

Fig. 16. Circuit implementation of Vernier delay line time-to-digital converter. (a) Schematic. (b) Timing diagram.

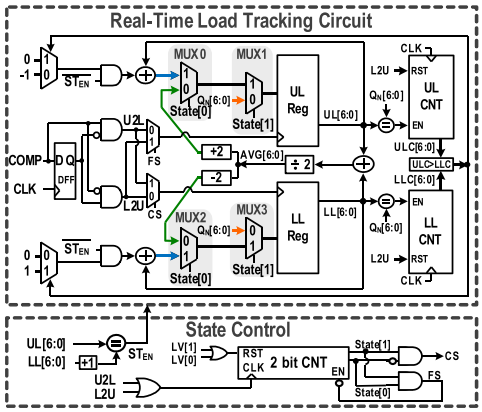

Fig. 17. Structure of real-time load-tracking technique.

new samples and all buffers are reset to "0." The operation of pulse propagation phase is shown in Fig. 16(b). During this phase, a rising edge is sent into "START" and propagates along the delay line. After t_d (equivalent to "$t_1 - t_2$") time, "STOP" goes high and triggers the trigger sampling delay line, generating a thermometer code, such as "1…1100…0." The number of "1"s in the code word provides a measure of the delay between "Start" and "Stop," and the resolution is the delay for each buffer.

B. Real-Time Load-Tracking Circuit and State Control

Fig. 17 shows the real-time load-tracking circuit and state control in the transient enhancement circuit. When the State[1:0] is 0, MUX1 stores $Q_N[6:0]$ to the upper limit (UL) current register; when the State[1:0] is 1, MUX3 stores $Q_N[6:0]$ to the lower limit (LL) current register. Therefore, the maximum and minimum values of $Q_N[6:0]$ are recorded in UL[6:0] and LL [6:0], respectively. When the State[1:0] is equal to 2, the DLDO regulator operates in the fast coarse mode. Meanwhile, MUX0 and MUX2 will be selected to switch to 0. UL and LL are set to "average value (Avg.) + 2" and "average value (Avg.) − 2," respectively. Finally, the State[1:0] is set to 3, and MUX0 and MUX2 are selected to switch to 1. Simultaneously, 2-bit counter

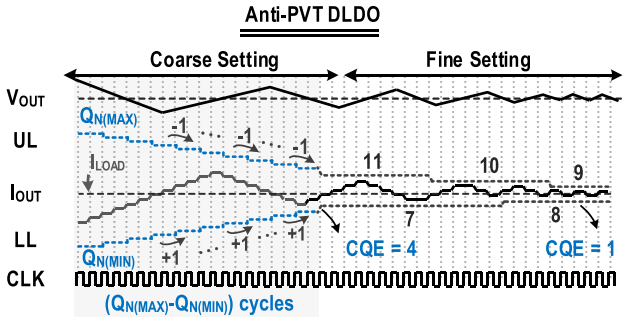

Fig. 18. Operation waveform of the anti-PVT-variation DLDO regulator [15].

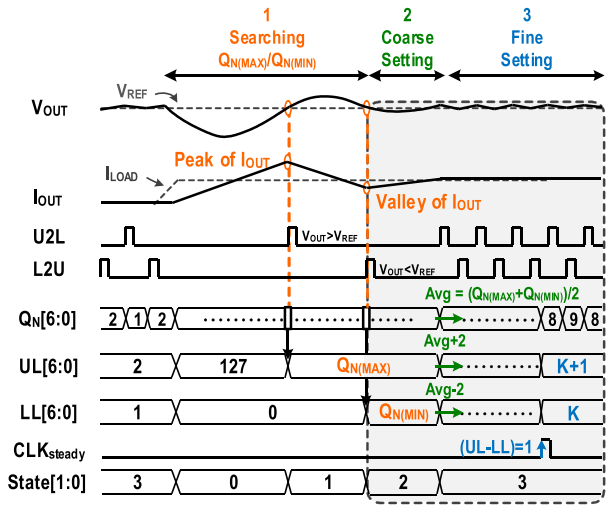

Fig. 19. Operation waveform of the proposed real-time load-tracking circuit.

(CNT) is disabled. Therefore, the state enters the fine-tuning mode, eventually reducing the difference between UL and LL to one.

C. Operation of Fast-Setting Current Limit

The real-time load-tracking operation consists of three parts: 1) searching the value of $Q_{N(\mathrm{MAX})}$ and $Q_{N(\mathrm{MIN})}$; 2) coarse setting; and 3) fine setting. In the coarse setting of the anti-PVT-variation DLDO regulator [15] in Fig. 18, the setting of UL and LL registers requires $(Q_{N(\mathrm{MAX})} - Q_{N(\mathrm{MIN})})$ cycles until "UL−LL" is equal to three. The disadvantage is that if $Q_{N(\mathrm{MAX})}$ is much larger than $Q_{N(\mathrm{MIN})}$, the coarse setup time will increase significantly. In other words, the overall response time also increases.

Fig. 19 shows the operation of the transient enhancement technique, which adds the searching mode at the start of the transient response to capture the peak and valley values of I_{OUT} in $Q_{N(\mathrm{MAX})}$ and $Q_{N(\mathrm{MIN})}$, respectively. In the following coarse setting step, the advantage is that it only takes one cycle to store Avg., Avg.+2, and Avg.−2 in Q_N, UL, and LL, respectively, where the Avg. is equal to $(Q_{N(\mathrm{MAX})} + Q_{N(\mathrm{MIN})})/2$. After the coarse setting, the difference between UL and LL is equal to four, which means that the current quantization error is reduced

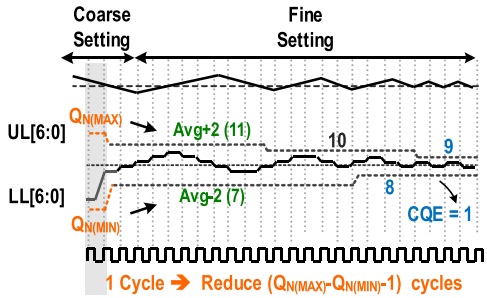

Fig. 20. Timing diagram of the real-time load-tracking operation.

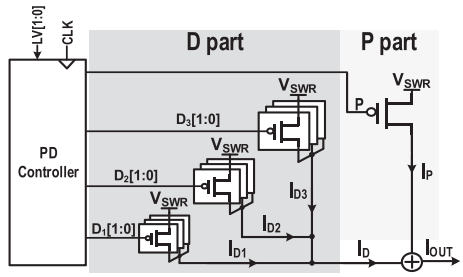

Fig. 21. Proposed PD controller.

to four. Finally, during the fine setting as depicted in Fig. 20, UL counter (ULC) and LL counter (LLC) record the number of times Q_N reaches UL and LL, respectively. In addition, the trigger signals L2U and U2L are generated to represent $V_{\mathrm{OUT}} > V_{\mathrm{REF}}$ and $V_{\mathrm{OUT}} < V_{\mathrm{REF}}$, respectively.

On each rising edge of L2U, if the value of ULC is greater than the value of LLC, LL increases by one, ULC or LLC is reset to zero, and the number of times that Q_N reaches UL or LL is recorded again. In contrast, if the value of the ULT is less than the value of LLT, the UL decreases by one. When the value of (UL−LL) decreases to one, it means that current quantization error is equal to one and ΔV_{OUT} is minimized. $\mathrm{CLK}_{\mathrm{steady}}$ is set high to indicate that the DLDO regulator is in a steady state.

D. PD Control

Fig. 21 shows the PD control section consisting of a PD controller and a power switch array divided into P-part (P) and D-part (D_{1-3}[2:0]). During transients, the PD controller determines the number of turn-ON power P-type power switches via LV[3:0]. In the case of heavy loads, the signal P is set to zero to turn ON the P-part transistor and provide the P-part current (I_P) to prevent large droop voltage. The transistor of D-part is used to increase the current resolution at light loads. When the error signal is nonzero, the path trigger sets the trigger signal to a high level based on different voltage levels and introduces a dynamic transient enhancement current to the output.

Fig. 22(a) shows the proposed PD controller. The proportional part (P-part) is controlled by the trigger signal P which is set high when LV[1:0] ≥ 1, thereby inducing a proportional current to the output. In order to reduce power consumption, proportional

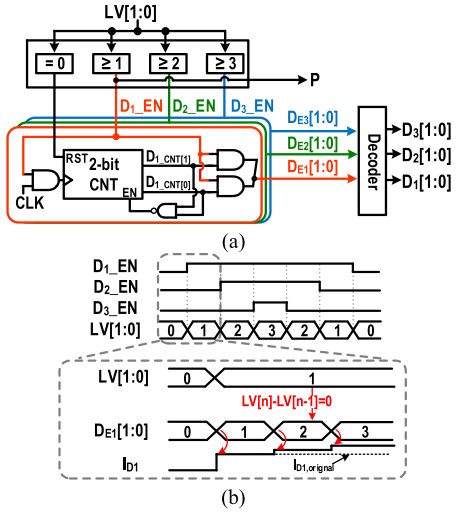

Fig. 22. Proposed PD control in DPID controller. (a) Block diagram. (b) Timing diagram.

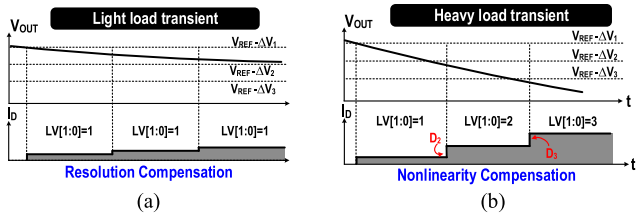

Fig. 23. Resolution compensation methodologies for DPID controller. (a) Resolution compensation. (b) Nonlinearity compensation.

control is implemented by one bit. Fig. 22(b) shows a timing diagram of the path trigger. Derivative control is divided into three parts: 1) D_1-*part* (D_1[1:0]); 2) D_2-*part* (D_2[1:0]); and 3) D_3-*part* (D_3[1:0]), which are enabled by trigger signals D_{1-3}_EN, for generating I_{D1}, I_{D2}, and I_{D3} to achieve derivative action. When LV[1:0] ≥ 2, the trigger signal D_2_EN is set high, and when LV[1:0] ≥ 3, the trigger signal D_3_EN is set high. As a result, the trigger signals are used to implement digital proportional and derivative actions. In the conventional digital derivative action, the derivative current remains at a constant value in the same error range, which means that the current error signal ER[n] equals the previous error signal ER[$n-1$].

The transient performance is determined by the resolution of the error signal. In low-power digital circuit design, resolution and power consumption are a tradeoff. Therefore, the proposed resolution compensator generates a derivative control signal D_{E1-3} and keeps counting within the same error range, and thus, the derivative current I_D slightly increases at the same LV[1:0] value. When $V_{\rm OUT}$ goes from $V_{\rm REF}$-ΔV_1 to $V_{\rm REF}$-ΔV_3, the error detector changes LV[1:0] from 1 to 3. Due to the resolution compensator, the dynamic transient boosts current $I_{\rm TRANSIENT}$ increases slightly at the same error interval as shown in Fig. 23(a). Although the difference shown in Fig. 23(b) is the same, since D_1-part, D_2-part, and D_3-part have different

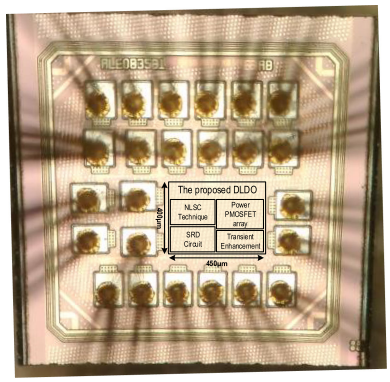

Fig. 24. Chip micrograph.

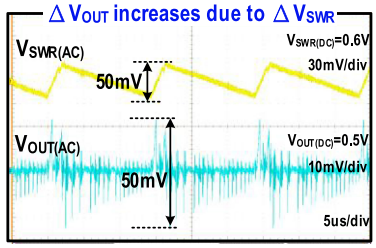

Fig. 25. Measured $\Delta V_{\rm OUT}$ of conventional barrel-shift DLDO regulator.

gains, I_D is still increased to combine the proportional actions in a lower power-consumption manner.

Both of the above-mentioned mechanisms help reduce the setup time and transient voltage drop. Therefore, if LV[1:0] changes from 1 to 3 within a short time, the D_1-*part*, the D_2-*part,* and the D_3-*part* are triggered simultaneously to provide a transient boost current. Conversely, if LV[1:0] remains within the same region, the proposed derivative control can also increase I_D to help $V_{\rm OUT}$ quickly return to the setpoint due to the compensation current.

IV. Experimental Results

The DLDO regulator using slew rate detection technique and NLSC technique is fabricated in a 40-nm Taiwan Semiconductor Manufacturing Company (TSMC) process and has an effective area of 0.18 mm^2, as shown in Fig. 24. The input voltage range is from 0.6 to 1.1 V and the output voltage range is from 0.5 to 1 V. The clock signal (CLK) sampling frequency is 100 MHz and the 4.7-nF load capacitor can ensure that the output voltage ripple less than 6 mV when $\Delta V_{\rm SWR}$ ranges from 0 to 50 mV.

In Fig. 25, the steady state of barrel-shift DLDO regulator shows poor power supply rejection capability. In the power-saving mode, $\Delta V_{\rm SWR}$ is approximately 50 mV at light loads, directly penetrating to the $V_{\rm OUT}$. There, the barrel-shift DLDO regulator suffers from $\Delta V_{\rm SWR}$, causing $\Delta V_{\rm OUT}$ to increase.

Fig. 26 shows the steady state of the DLDO regulator when linear switching control technique is enabled where Q_N is frozen and $Q_{\rm BST}$ is enabled. During switching regulator operation in PFM mode, $\Delta V_{\rm OUT}$ is reduced from 50 to 15 mV, and the

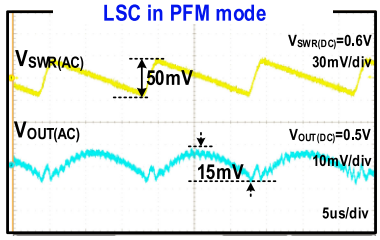

Fig. 26. Measured steady state ΔV_{OUT} of the proposed DLDO with linear switching control when ΔV_{SWR} is 50 mV.

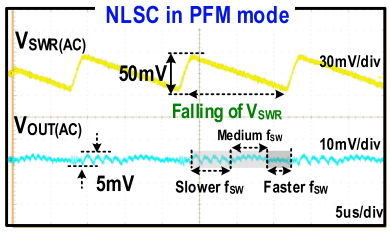

Fig. 27. Measured steady state ΔV_{OUT} of the proposed DLDO with the NLSC when the switching regulator operates in the PFM mode with the ΔV_{SWR} is around 50 mV.

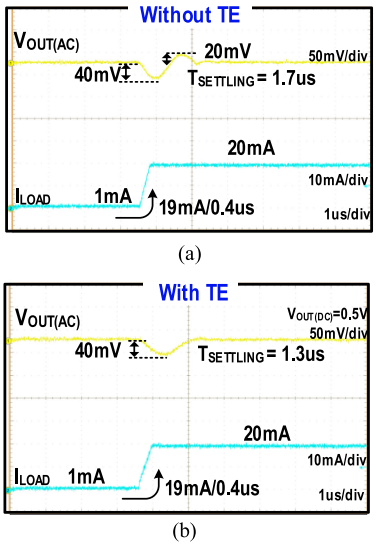

Fig. 28. Measured transient response of the proposed DLDO. (a) Without transient enhancement. (b) With transient enhancement.

switching frequency is also reduced. In contrast, the measurement results in Fig. 27 show the steady state of DLDO regulator using the NLSC technique. The NLSC technique can further suppress ΔV_{OUT} from 15 to 5 mV when the switching regulator operates in the PFM mode and the ΔV_{SWR} varies from 0 to 50 mV. The proposed DLDO regulator achieves a quiescent current of less than 10 μA.

Fig. 28(a) shows the transient response of the proposed DLDO regulator without the transient enhancement technique when the load current changes from 0.4 to 20 mA. Undershoot and overshoot voltages are 40 and 20 mV, respectively, and the settling time T_{SETTLING} is around 1.7 μs. In contrast, Fig. 28(b)

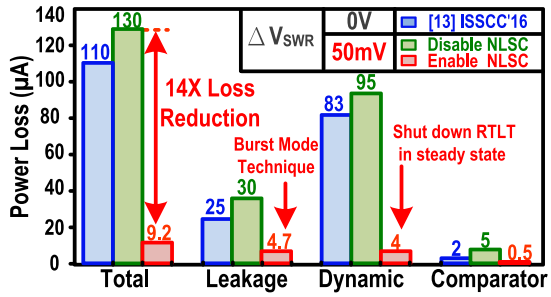

Fig. 29. Power loss comparison between the DLDO with freeze mode operation and the proposed DLDO including enabling and disabling NLSC.

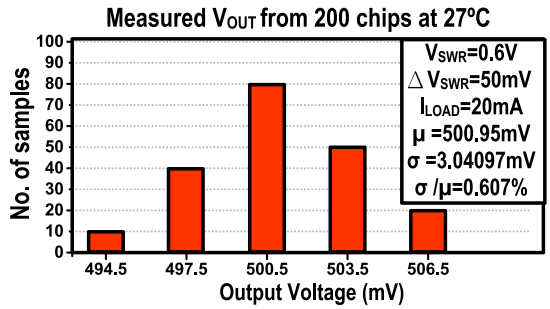

Fig. 30. Measured V_{OUT} from 200 samples.

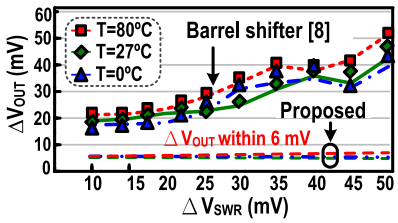

Fig. 31. Measured ΔV_{OUT} of the proposed DLDO and the barrel-shift DLDO when ΔV_{SWR} is 50 mV.

shows the transient performance of the proposed DLDO regulator when the transient enhancement technique is activated. Undershoot and overshoot voltages are decreased to 40 and 0 mV, respectively. T_{SETTLING} decreases to 1.3 μs.

Fig. 29 shows the power loss comparison between the DLDO with the freeze mode [15] and the proposed DLDO. The total power consumption is reduced to 9.2 μA due to the variable switching frequency and disabled real-time load tracking in steady state. From Fig. 30, it can be seen that the average V_{OUT} from the 200 samples at 27 °C is 500.95 mV and the sigma value is 3.04097 mV. Therefore, the proposed DLDO is affected by the PVT variations by less than 0.6% when V_{OUT} is 0.5 V under V_{SWR} from 0.6 to 1.1 V and I_{LOAD} is 20 mA.

ΔV_{OUT} of the proposed DLDO regulator is compared with a barrel shifter DLDO regulator with different temperatures and different ΔV_{SWR}, as shown in Fig. 31. A large ΔV_{OUT} in the barrel shifter DLDO regulator is the result of a high ΔV_{SWR} value, leading to a worst case of ΔV_{OUT} up to 50 mV at light loads. In contrast, the proposed DLDO regulator reduces it to

TABLE I
COMPARISON OF OTHER DLDO METHODOLOGIES

	[13] ISSCC'16	[14] ISSCC'16	[15] ISSCC'17	[16] ISSCC'17	[17] TCASII'16	[18] TPE'16	[19] TPE'16	[20] JSSC'17	This Work
Type	Digital	Digital	Digital	Digital	Digital	Digital	Digital	Digital	Digital
Process	28 nm	65 nm	40 nm	65 nm	65 nm	0.13μm	0.13 μm	65 nm	40 nm
V_{in} [V]	1.1	0.5–1	0.6–1.1	0.5–1	0.6–0.1.1	0.5–1.2	0.45–1.2	0.6–1	0.6–1.1
V_{out} [V]	0.9	0.45–0.95	0.5–1	0.3–0.45	0.4–1	0.45–1.14	0.35–1.15	0.55–0.95	0.5–1
$I_{LOAD,MAX}$ [mA]	200	3.511	210	2	100	4.6	1.5	500	20
Max. F_{SAMPLE} [MHz]	N.A.	N.A.	N.A.	240	N.A.	<100	10	N.A.	100
Load capacitor C_L [nF]	23.5	0.4	20	0.4	1	0.9	1	1.5	4.7
Load regulation [mv/mA]	<0.01	<0.05	<0.0175	<5.6	0.06	<10	0.6	0.25	<0.1
Transient ΔV_{OUT} @ΔI_{LOAD}	120 mV @180 mA	22 mV @0.2 mA	36 mV @200 mA	40 mV @1.06 mA	360 mV @100 mA	210 mV@ 1.4 mA	300 mV@ 1.48 mA	50 mV @100 mA	40 mV@19 mA
Settling time @ΔI_{LOAD}	<40 μS @180 mA	<80 μS @0.2 mA	<1.3 μS @200 mA	15 ns @1.06 mA	<14 μS @100 mA	5.8 μS @1.4 mA	1.5 μS @1.48 mA	25 ns @100 mA	<1.3 μs@19 mA
Output voltage ripple [mV]	20–40	-	2.3–3	20–40	55	10	2.6	5	ΔV_{SWR} = 50: 3 ΔV_{SWR} = 0: <6
I_Q [µA]	110	12.5–216	22.6–98.5	14	82	78.2	8.9	300	ΔV_{SWR} = 50: 19.6 ΔV_{SWR} = 0: <10
FOM_1 [ps]	7.76	155	1.61	56	2.95	698	119 × 10^3	0.09	9.21
FOM_2 [V]	0.196	127	1.54 × 10^{-3}	0.528×10^{-3}	2.76	4.54	0.18	0.25×10^{-3}	3.58×10^{-3}

Notes:
FOM_1 is defined as $K_T(\Delta V_{\rm OUT} I_Q/\Delta I_{\rm LOAD})$ [6]
FOM_2 is defined as $(\Delta V_{\rm OUT}/I_{\rm LOAD,MAX})(I_Q/I_{\rm LOAD,MAX})C_{\rm LOAD}$ [7]
where I_Q is the quiescent current, $\Delta I_{\rm LOAD}$ is the transient current, $C_{\rm LOAD}$ is the load capacitor, K_T is the response time ratio of each work compared to [16], $\Delta V_{\rm OUT}$ is the droop voltage, and $I_{\rm LOAD,MAX}$ is the maximum current load.

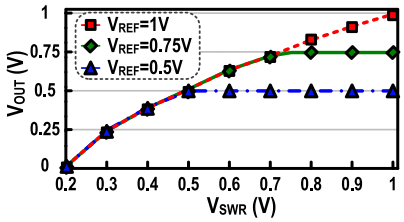

Fig. 32. Measured line regulation of with $V_{\rm OUT}$ ranging from 0.5 to 1V.

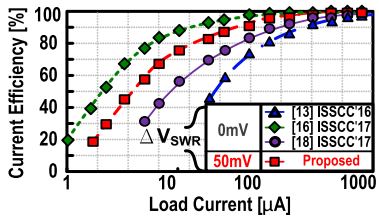

Fig. 34. Measured current efficiency of the proposed and others design.

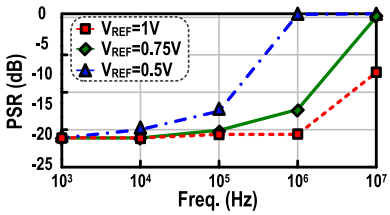

Fig. 33. Measured power supply rejection performance with $V_{\rm OUT}$ ranging from 0.5 to 1V with NLSC.

less than 6 mV with the same $\Delta V_{\rm SWR}$ value of 50 mV. The load regulation performance measured ranging from 0.5 to 1 V is shown in Fig. 32 with respect to reference voltages 0.5, 0.75, and 1 V, and the power supply rejection is plotted in Fig. 33 with the same reference voltages and NLSC.

Fig. 34 shows the current efficiency at different $\Delta V_{\rm SWR}$, temperature, and load currents when $V_{\rm OUT}$ is regulated at 0.5 V. The current efficiency of the proposed method is 99.8%. In addition, the current efficiency at light loads is 90.2%.

Compared with the prior arts, Table I lists the advantages of the proposed DLDO regulator.

1) The NLSC technique can make $\Delta V_{\rm OUT}$ less than 6 mV when the line voltage disturbance $\Delta V_{\rm SWR}$ is 50 mV.
2) Due to decreasing switching frequency in the burst mode operation, the lowest quiescent current is less than 10 μA.
3) The transient response time is 1.3 μs due to DPID compensation and the transient enhancement technique while the undershoot voltage is less than 40 mV in case of 1 to 20 mA load step.
4) Load regulation is less than 0.1 under the condition from 0.4 to 20 mA.

In summary, the proposed DLDO regulator performs with the lowest output voltage ripple and quiescent current even under a large $\Delta V_{\rm SWR}$.

V. Conclusion

Due to poor power supply rejection capability, conventional DLDO regulators always suffer from input voltage ripple, which reduces the current efficiency and increases the quiescent current. The proposed DLDO regulator uses the slew rate detection technique to distinguish between transient response and power saving modes. The NLSC technique adjusts the switching frequency in the falling/ramping time of the V_{SWR} to turn ON/OFF to reduce the quiescent current. The NLSC technique suppresses the voltage ripple to less than 6 mV when the switching noise voltage is larger than 50 mV from the switching regulator in the power-saving mode. The current efficiency is improved by decreasing the quiescent current to less than 10 μA. The switching power loss is reduced by variable switching frequency control. Moreover, during the transient period, the proposed transient enhancement technique improves load transient performance. In the case of 1-to-20 mA load step, the transient response time is 1.3 μs and the peak current efficiency is 99.8% at heavy loads.

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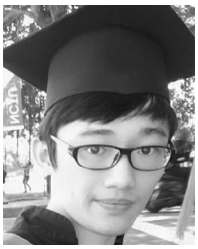

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