A Dual-Switch Discontinuous Current-Source Gate Driver Overcoming the Current Diversion Problem for a Buck VRM

Iman Abdali Mashhadi, *Student Member, IEEE*, and Majid Pahlevani, *Senior Member, IEEE*

***Abstract*—In this article, a novel dual-switch discontinuous current-source gate driver (CSD) suitable for driving the high-side MOSFET (HS MOSFET) of buck voltage regulator module (VRM) is presented. The proposed gate driver completely solves the gate current diversion problem, which most of the previous CSDs suffer from, during turn-OFF transition. Thus, in comparison to most of the previous CSDs, the proposed gate driver achieves to turn-OFF the power MOSFET considerably faster and with much higher effective gate current, which leads to significant reduction of turn-OFF losses. Whereas, turn-ON losses of buck VRM HS MOSFET driven by the proposed CSD and the previous CSDs are equal. Furthermore, the introduced gate driver consists of the minimum number of control switches and circuit elements, compared to previous CSDs. The proposed gate driver is analyzed and a prototype of the driver operating at 1 MHz is implemented in order to validate the theoretical analysis.**

***Index Terms*—Buck voltage regulator module (VRM), current diversion problem, current-source gate driver (CSD), switching losses, voltage-source driver (VSD).**

I. Introduction

ON THE basis of Moore's law, it has been predicted that the number of transistors per chip will double every 18 months [1]. As a result of the increase in the numbers of transistors on microprocessors, the current demand of new-generation CPUs keeps increasing while the operating voltage is reducing to subvolt [1].

Voltage regulator modules (VRMs) are used to supply CPUs in computers. Most of today's VRM topologies are based on the multiphase buck converters owing to their simplicity, low component-count, and low cost [2]. The switching frequency of VRMs has increased to MHz range in order to enhance the power density, reduce the size of passive components, and reach ultrafast dynamic response [2]–[5]. From the performance point of view, classical buck VRMs with conventional voltage-source drivers (VSDs) are no longer appropriate for MHz VRMs [6].

Manuscript received November 14, 2018; revised February 28, 2019 and July 4, 2019; accepted August 22, 2019. Date of publication September 1, 2019; date of current version January 10, 2020. Recommended for publication by Associate Editor M. Rodriguez. *(Corresponding author: Iman Abdali Mashhadi.)*

The authors are with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON K7L 3N6, Canada (e-mail: 18iam@queensu.ca; majid.pahlevani@queensu.ca).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2019.2938827

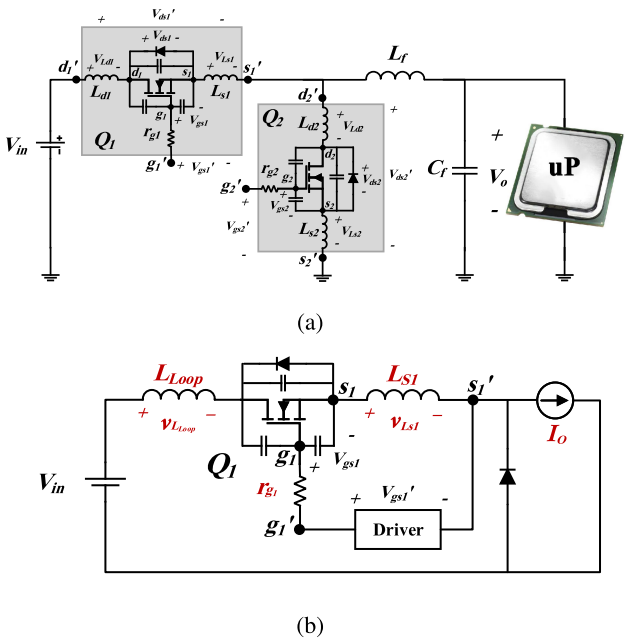


Fig. 1. (a) Synchronous buck VR with parasitic inductances. (b) Equivalent circuit for HS MOSFET.

Since by increasing the switching frequency, buck converters with conventional VSDs have two main problems.

1) *High gate drive losses:* The gate drive losses of VSDs is $Q_g.V_{c_{gs}}.f_{sw}$, where Q_g is the total gate charge, $V_{c_{gs}}$ is the applied gate–source voltage, and f_{sw} is the switching frequency.
2) *High turn-OFF switching losses:* Turn-OFF losses of the high-side MOSFET (HS MOSFET) of buck VRMs are a great challenge in high frequency buck VRMs. Fig. 1(a) shows a circuit diagram of a buck VRM including parasitic inductances (created by bonding wires within the MOSFET's package and by printed circuit board (PCB) traces). The equivalent circuit for the HS MOSFET is illustrated in Fig. 1(b). The loop inductance (i.e., $L_{\text{loop}} = L_{d1} + L_{d2} + L_{S2}$) tends to reduce the effective drain voltage, v_{ds1}, during turn-ON transitions, hence it reduces the turn-ON losses. However, as it creates an over voltage during turn-OFF, it increases turn-OFF losses [7]–[9]. Thus, the turn-OFF losses are much higher than the turn-ON

losses [7]–[9]. Additionally, the output inductor current ripple effectively reduces the current at turn-ON instants and increases the current at turn-OFF instants. This further reduces the turn-ON switching losses and increases the turn-OFF switching losses [10]. Therefore, the turn-OFF losses mainly contribute to efficiency degradation and are the focus of this article.

In the HS MOSFET of buck VRM with VSD, the common source inductance, L_{s_1}, and the gate resistance, r_{g_1}, contribute to the turn-OFF switching losses (turn-ON switching losses are negligible) [11]–[13]. The induced voltage across L_{s_1} and r_{g_1} decreases the effective gate current (and in turn the effective gate drive voltage) of the power MOSFET during switching intervals. It leads to reduced switching speed (increased turn-OFF losses) of the MOSFET using VSD [11]–[13].

Resonant gate drivers (RGDs) have been proposed in order to recover the gate drive losses in VSDs [14]–[19]. Although RGDs considerably reduce the gate drive losses, they are unable to decrease the switching losses [11]. These drivers are suitable for applications where the switching losses are not dominant (e.g., synchronous rectifiers in buck VRMs) [12].

In order to reduce both switching losses and gate drive losses, current-source gate drivers (CSDs) have been proposed [11]–[13], [20], [21]. In CSDs, the input capacitance of power MOSFETs is charged/discharged by a nearly constant current [12]. Therefore, CSDs reduce the turn-ON/turn-OFF transition times and consequently have a considerable reduction in the switching losses [12]. The CSDs are classified into the continuous CSDs [22]–[26] and the discontinuous CSDs [11]–[13], [27]–[29] based on the type of the inductor's current of the CSDs. Compared to the continuous CSDs, discontinuous ones show very low circulating losses, much smaller inductance, and better transient performance (against step changes in the duty cycle) [30]. However, continuous current-source gate drivers require fewer control switches [30].

A study between the performance of a buck VRM with CSDs and that of other architectures (e.g., TI buck [31], soft-switching phase shift buck converter [32], and self-driven soft-switching buck derived converter [33]) has been performed in [22]. According to this study, the buck VRM with CSDs has the same structure as today's VRMs, featuring low cost and simple control, while improving the efficiency in a cost-effective manner [21], [22]. Whereas, coupled inductor based approaches [31]–[33] need extra magnetic components leading to high cost and high complexity of the control circuits, and reduced power density [21], [22]. Thus, the buck VRMs with CSDs are appropriate for MHz VRMs to power microprocessors.

In VSDs, the gate drive current depends on the gate drive supply voltage. In addition, r_{g_1} and the induced voltage across L_{s_1} decrease the effective gate current and increase the turn-OFF losses [11]. Whereas, in ideal CSDs, the gate current of the power MOSFET is merely determined by the current-source independent of L_{s_1} and r_{g_1} [11], [34]. Fig. 2(a) shows a power MOSFET driven by an ideal CSD during the turn-OFF times. The gate terminal voltage of the MOSFET (and in turn the voltage across the ideal current-source) can have any reasonable values. Therefore, the voltage drop across L_{s_1} and r_{g_1} can be compensated by changing

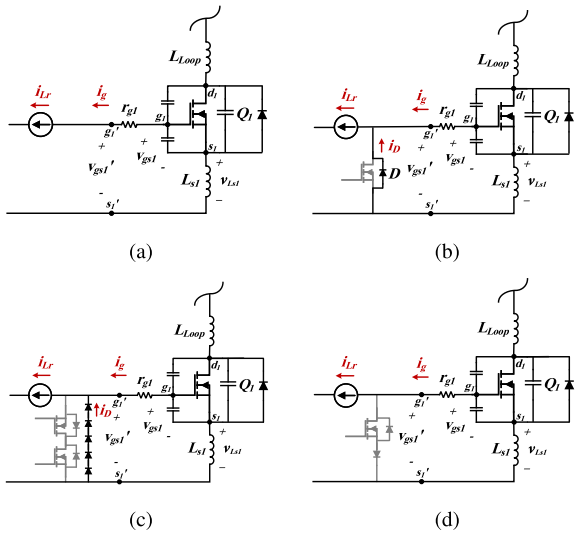


Fig. 2. Equivalent circuit of CSDs during turn-OFF. (a) Ideal CSD. (b) CSDs introduced in [20]–[27], [29], and [35]–[39]. (c) CSD introduced in [12] and [13]. (d) CSD introduced in [11].

the voltage across the ideal current-source. However, in many CSDs [20]–[27], [29], [35]–[39], the voltage drop across L_{s_1} and r_{g_1} adversely affects the switching speed. As illustrated in Fig. 2(b), a portion of the driver current is diverted through body diode, D, instead of discharging the gate capacitance of the power MOSFET. The gate terminal voltage used in [20]–[27], [29], and [35]–[39] (the CSDs with current diversion problem) cannot vary freely as in the ideal CSD and it is clamped to the ground during turn-OFF times. This is referred to as the current diversion problem or body diode clamping [11]–[13]. The current diversion problem increases the turn-OFF switching losses.

In [12], five diodes have been used to create a negative gate voltage (-3.5 V) in order to deal with the current diversion problem. However, a portion of the inductor's energy is dissipated in the diodes. Although the proposed circuit in [12] can mitigate the current diversion problem compared to the CSDs with current diversion problem, it is not able to completely rectify the issue. This is because the gate voltage of the power MOSFET (and the voltage across current-source produced by an inductor) is clamped to -3.5 V during turn-OFF instants. Thus, the current diversion effect happens as shown in Fig. 2(c). Furthermore, it requires many extra components (five control switches and five diodes). In [11], the current diversion problem has been studied and a circuit has been proposed, which can solve this problem completely. The performance of this CSD is similar to the ideal CSD during turn-OFF transitions as shown in Fig. 2(d) and the gate current is determined by the inductor current. However, additional conduction losses are produced owing to the undesired resonance between the gate resistance, the gate drive inductor, and the gate capacitances. Also, this resonance may lead to undesired triggering of the power MOSFETs. Additionally, this method utilizes several components (four switches and two diodes).

The main objective of this article is to introduce a new driver circuit, which operates as an ideal CSD (does not have the current diversion problem) during turn-OFF transitions, and uses minimum number of extra components. A new gate drive circuitry is proposed for driving the HS MOSFET of buck VRMs, which is able to overcome the aforementioned difficulties. The main idea behind the proposed drive circuit is to combine the current-source structure (i.e., CSD) with the resonant gate drive circuitry (i.e., RGD). This combination can drastically reduce the turn-OFF losses (the turn-ON losses of HS MOSFET are insignificant) of buck VRM. Basically, the proposed gate drive circuit discharges the gate capacitance of the MOSFET with an approximately constant current without being influenced by L_{s_1} and r_{g_1} (the idea of ideal CSDs) and charges the gate capacitance with zero initial inductor current (the idea of RGDs). Generally, the RGD structure is suitable where switching losses are not dominant and the CSD structure is useful where switching losses are considerable. It is noted that one important limitation of this driver is, similar to [39], that it can only be used for narrow on-time. The main features of the proposed gate drive circuitry are listed as follows.

1) It is able to perform as an ideal CSD (solve the current diversion problem completely) during turn-OFF transitions.
2) Turn-ON losses of buck VRM HS MOSFET driven by the proposed CSD and the previous CSDs are equal.
3) It has discontinuous inductor current.
4) It includes only two control switches and one inductor.
5) It tremendously reduces the gate drive losses.
6) It can achieve a negative gate drive signal which improves the reliability of VRMs.

In Section II, the topology and the operation principles of the proposed CSD are presented. Section III describes the procedures to calculate the losses along with the optimal design of the CSD inductor. The advantages of the proposed CSD are elaborated in Section IV. Section V presents the experimental results, and finally the conclusion is presented in Section VI.

II. Proposed Gate Drive Circuit

In this section, the proposed current-source gate drive circuit is described in detail. Fig. 3(a) shows the proposed gate drive circuit, and a buck VRM driven with the proposed CSD is illustrated in Fig. 3(b). According to Fig. 3, the proposed driver includes two control switches, S_1 (n-channel), S_2 (p-channel), and a small inductor L_r. V_{CC} is the drive supply voltage, switch Q_1 is the HS MOSFET of the buck VRM, L_{s_1} is the common source inductance, and $L_{\text{loop}} = L_{d_1} + L_{d_2} + L_{S_2}$ is the loop inductance. Fig. 4(a) shows the key waveforms of the drive circuit including the signals for the control switches S_1 and S_2, the power MOSFET gate–source voltage v_{gs_1}, the inductor current i_{Lr}, the drain–source voltage of HS MOSFET v_{ds_1}, and the drain–source current of HS MOSFET i_{ds_1}, and the simulation waveforms are given in Fig. 4(b).

There are two main assumptions considered in analyzing the proposed gate driver. The first assumption is related to the nonlinear behavior of the MOSFET's parasitic capacitances, which are described in [9] (the nonlinear equations given in [9] are used in the analysis). The output capacitance, c_{ds_1}, and the gate–drain capacitance, c_{gd_1}, are given by [9]

$$c_{\text{ds}_1} = \frac{C_{j1}}{\sqrt{1 + \frac{v_{\text{ds}_1}}{\phi_1}}} \tag{1}$$

$$c_{\text{gd}_1} = \frac{1}{\frac{1}{C_{\text{gd}-0V}} + \frac{v_{\text{ds}_1}^{x}}{C_{j2}}}. \tag{2}$$

The coefficients C_{j1}, ϕ_1, x, $C_{\text{gd}-0V}$, and C_{j2} can be extracted from the nonlinear capacitor's curves given in the datasheets. It is noted that other parasitic capacitors (i.e., the gate–source capacitance, c_{gs_1}) can be accurately estimated as a constant value [9]. The second assumption is related to the fact that the main difficulties with driving the HS MOSFET is related to its turn-OFF switching losses and the current division problem (that is generally a drawback of CSD drive circuits).

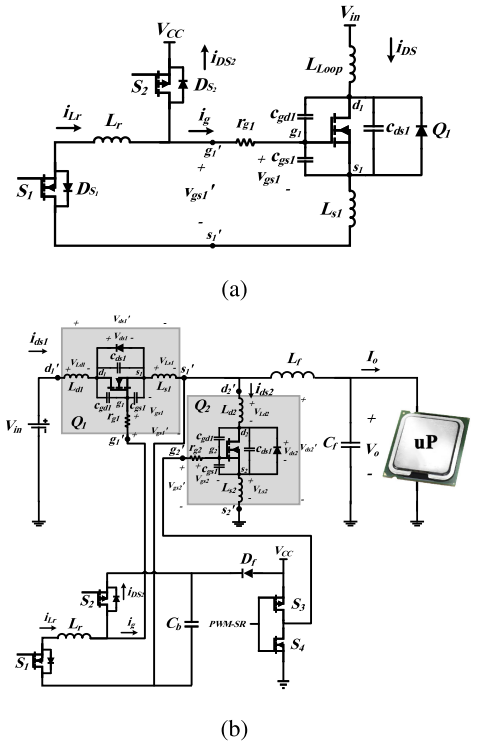


Fig. 3. (a) Proposed gate driver. (b) Buck VRM with the proposed gate driver.

According to Fig. 5, the operation of the proposed drive circuit can be described in 11 modes. These modes are described as follows.

1) Mode 1 ($t_0 \le t < t_1$) [see Fig. 5(a)] (Turn-ON delay): This mode starts at the beginning of the turn-ON process. It is assumed that before t_0 and beginning of the turn-ON process, a negative voltage is applied to the gate–source of power MOSFET ($v_{\text{gs}_1}(t_0) = v_{\text{gs}_1}(t_{10})$) and $|v_{\text{gs}_1}(t_0)| > V_{CC} + V_{fd2}$, where V_{fd2} is the body diode forward voltage of S_2. When it is desired to turn ON the power MOSFET (at t_0), S_1 turns on under zero current switching. Then, the input capacitance C_{iss_1}, which is composed of c_{gs_1} and c_{gd_1} charges from $-|v_{\text{gs}_1}(t_0)|$ to the threshold voltage V_{th} in a resonant manner. This interval ends

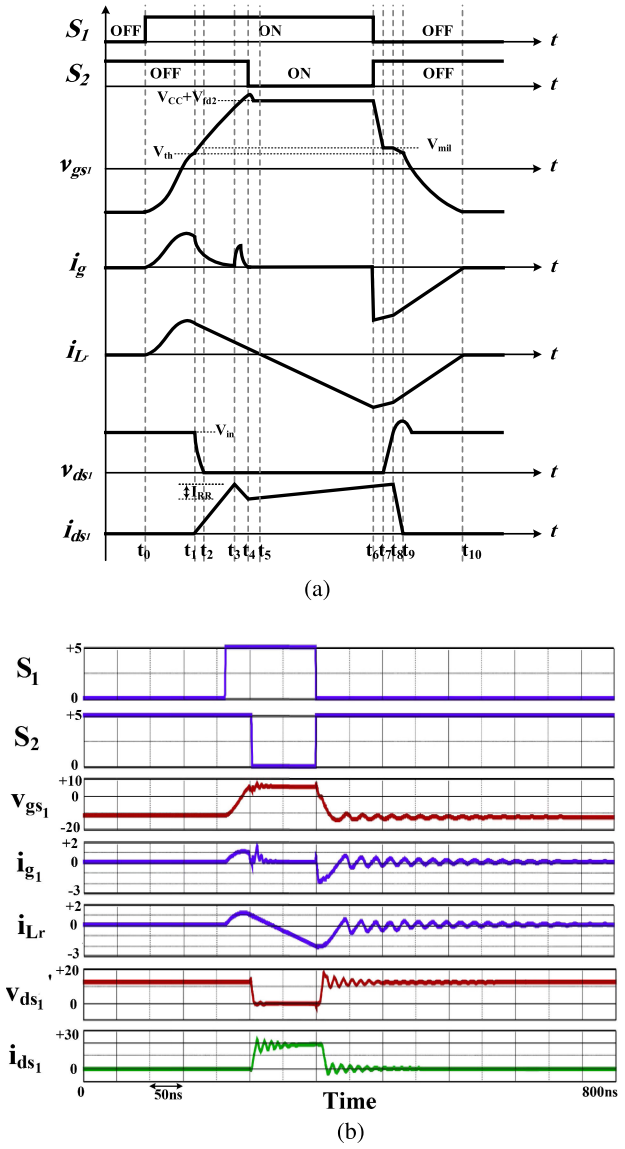


Fig. 4. Key waveforms of the proposed CSD. (a) Theoretical waveforms. (b) Simulation waveforms.

when $v_{\rm gs1}$ reaches $V_{\rm th}$. The gate–source voltage $v_{\rm gs1}$ and the gate current i_g are derived by

$$v_{\rm gs_1}(t) = e^{-\alpha_0 t}\left(A_0\cos\sqrt{\omega_0^2-{\alpha_0}^2}t + B_0\sin\sqrt{\omega_0^2-{\alpha_0}^2}t\right)$$

$$i_g(t) = (c_{\rm gs_1}+c_{\rm gd_1})\frac{d}{dt}v_{\rm gs_1}(t)$$

$$A_0 = v_{\rm gs_1}(t_0),\quad B_0 = \frac{A_0\alpha_0}{\sqrt{\omega_0^2-{\alpha_0}^2}} \tag{3}$$

$$\alpha_0 = \frac{R_{\rm on}}{2(L_r+L_{s_1})}$$

$$R_{\rm on} = r_{g_1}+R_{\rm ds(on),S_1}+R_{\rm ac}$$

$$\omega_0 = \frac{1}{\sqrt{(L_r+L_{s_1})(c_{\rm gs_1}+c_{\rm gd_1})}} \tag{4}$$

where r_{g_1} is the gate resistance of the power MOSFET, $R_{\rm ds(on),S1}$ is the ON-resistance of S_1, and $R_{\rm ac}$ is the ac resistance of the inductor. Drain–source current $i_{\rm ds_1}$ is equal to zero during this mode, because $v_{\rm gs_1}$ is lower than the threshold voltage $V_{\rm th}$. Therefore, there is no switching losses during this interval (the load current still circulates through the body diode of the synchronous rectifier Q_2.)

2) Mode 2 ($t_1 \le t < t_2$) [see Fig. 5(b)] (Transition Period): At t_1, $v_{\rm gs_1}$ reaches $V_{\rm th}$. During this mode, the drain–source current $i_{\rm ds_1}$ starts to increase, and the drain–source voltage $v_{\rm ds_1}$ begins to fall. The voltage drops across L_{s_1} (i.e., $v_{L_{s_1}} = L_{s_1}\frac{d(i_{\rm ds_1}+i_{Lr})}{dt}$) and r_{g_1} are large enough to force the body diode of S_2 to turn ON. Therefore, the gate terminal of the HS MOSFET is clamped to $V_{CC}+V_{fd2}$, where V_{fd2} is the body diode forward voltage of S_2. Then, the proposed CSD operates similar to a VSD with power supply voltage equal to $V_{CC}+V_{fd2}$, and the gate current is equal to $i_g(t) = \frac{V_{CC}+V_{fd2}-v_{L_{s_1}}(t)-v_{c_{\rm gs_1}}(t)}{r_{g_1}}$.

During this mode, two different operating modes may occur as shown in Fig. 6.

1) $v_{\rm gs_1}-V_{\rm th}$ remains lower than $V_{\rm in}-v_{L_{\rm loop}}-v_{L_{s_1}}$ [see Fig. 6(a)], and the power MOSFET operates in the saturation region during this state.
2) If the induced voltages across $L_{\rm loop}$ and L_{s_1} are large enough, $v_{\rm ds_1}$ reduces dramatically to a voltage value lower than $v_{\rm gs_1}-V_{\rm th}$ [see Fig. 6(b)], and it causes the power MOSFET to enter the ohmic region before $i_{\rm ds_1}$ reaches $I_o-\frac{\Delta i_L}{2}$, where Δi_L is the output inductor current ripple of the buck converter.

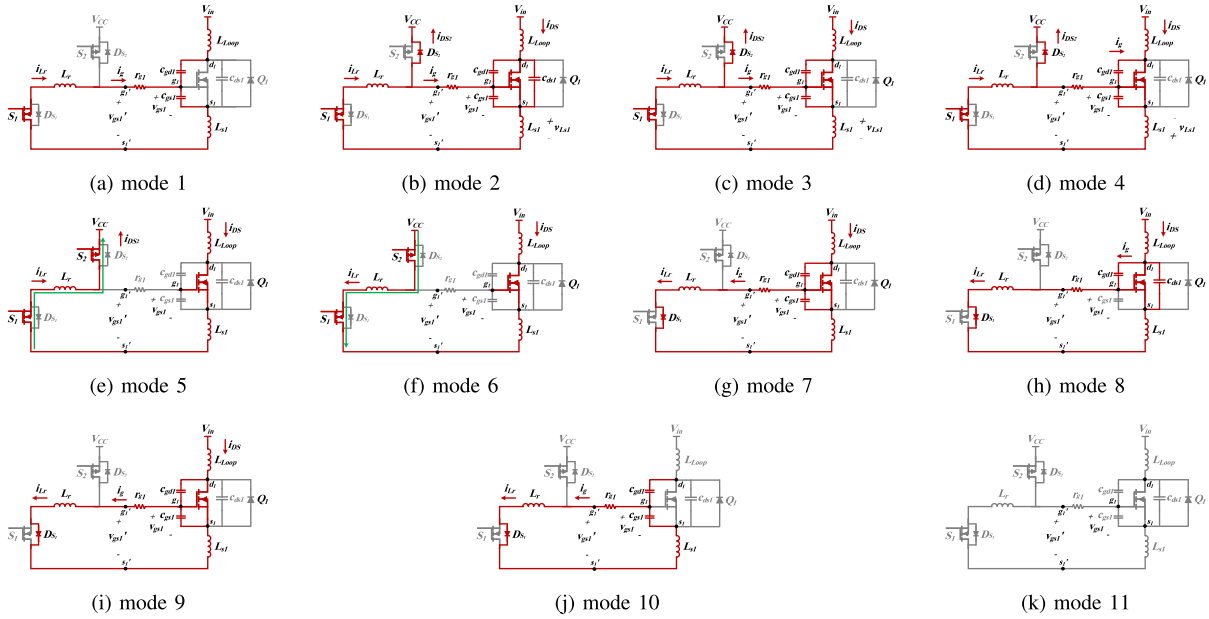
In buck VRMs, with low input voltage and high output current, $v_{\rm ds_1}$ is likely to enter the ohmic region within a short time and normally drops to zero before $i_{\rm ds_1}$ reaches its peak value [9]. With this assumption, Case B is described as follows.

The accurate equations of $v_{\rm gs_1}$, $i_{\rm ds_1}$, and $v_{\rm ds_1}$ in this state are given in [9]. This mode ends when the power MOSFET enters the ohmic region.

3) Mode 3 ($t_2 \le t < t_3$) [see Fig. 5(c)] (Continuing the Increase of Drain Current): At the beginning of this mode, the power MOSFET has entered the ohmic region and $i_{\rm ds_1}$ will continue to increase until it reaches its peak value, which is larger than the load current (due to the reverse recovery of the SR body diode [40], [41]). During this interval, the induced voltage across L_{s_1} keeps the body diode of the control switch S_2 forward biased. Thus, the proposed gate driver still behaves similar to a VSD, and VSD circuit equations still apply to this state, and $v_{\rm gs_1}$ rises.

4) Mode 4 ($t_3 \le t < t_4$) [see Fig. 5(d)] (Reverse Recovery Current Falling): At t_4, $i_{\rm ds_1}$ reaches its peak value. The SR body diode starts to block the SR drain–source capacitance voltage [41]. Then, $i_{\rm ds_1}$ decreases to reach $I_o-\frac{\Delta i_L}{2}$.

During this interval, a negative voltage is inducted across L_{S_1}, and the gate current charges the gate capacitance to a voltage higher than $V_{CC}+V_{fd2}$. When the reverse recovery is complete, $v_{\rm gs_1}$ drops back to $V_{CC}+V_{fd2}$. Effects of resonance between the SR output capacitance and parasitic inductances are neglected in the analysis.

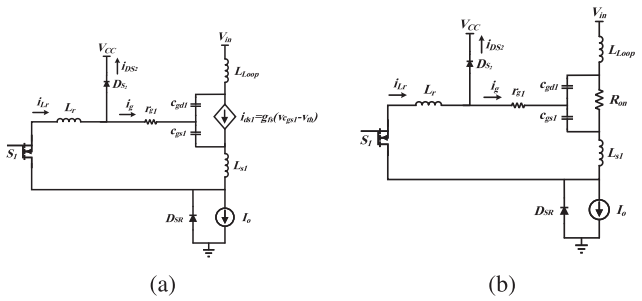


(a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4

(e) mode 5 (f) mode 6 (g) mode 7 (h) mode 8

(i) mode 9 (j) mode 10 (k) mode 11

Fig. 5. Operating modes of the proposed CSD. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8. (i) Mode 9. (j) Mode 10. (k) Mode 11.



(a) (b)

Fig. 6. Equivalent circuits of mode 2. (a) Saturation region. (b) Ohmic region.

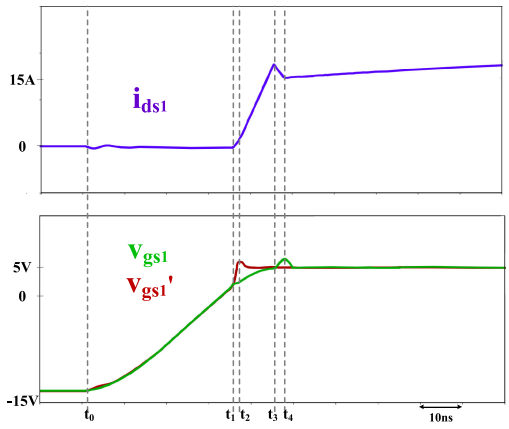


Fig. 7. Magnified simulation waveforms of mode 1 to mode 4.

The magnified simulation waveforms of mode 1 to mode 4 is illustrated in Fig. 7 to achieve a better understanding of the operating modes of the proposed CSD.

5) Mode 5 ($t_4 \le t < t_5$) [see Fig. 5(e)] (Energy Recovery Interval): When v_{gs_1} reaches $V_{CC} + V_{fd2}$, the body diode of S_2, D_{S_2}, continues to conduct. Afterwards, S_2 can be turned on under zero-voltage switching (ZVS) condition. During this mode, the remaining energy in the inductor L_r is fed back to V_{CC}, and i_{Lr} linearly decreases to reach zero at the end of this interval. It should be noted that during mode 2 to mode 4, a portion of the energy stored in L_r is recovered back to V_{CC}.

6) Mode 6 ($t_5 \le t < t_6$) [see Fig. 5(f)] (Inductor Current Precharge Interval): During this interval, i_{Lr} increases in the opposite direction ($i_{Lr} = -\frac{V_{CC}}{L_r}t$), and the gate of power MOSFET Q_1 is clamped to V_{CC}. Duration of this mode is determined by the on-time of the HS MOSFET.

7) Mode 7 ($t_6 \le t < t_7$) [see Fig. 5(g)] (Turn- OFF Delay): At t_6, the switches S_1 and S_2 are turned off under ZVS condition (due to the conduction of body diode and the gate capacitance C_{iss_1}, respectively), which allows i_{L_r} to discharge the MOSFET gate capacitance. This interval ends when v_{gs_1} reaches $V_{\mathrm{th}} + \frac{I_o}{g_{fs}}$. The equations of v_{gs_1} and the gate current during this mode are given by

$$i_g(t) = (c_{\mathrm{gs}_1} + c_{\mathrm{gd}_1})\frac{d}{dt}v_{\mathrm{gs}_1}(t) \tag{5}$$

$$v_{\mathrm{gs}_1}(t) = V_{fd1} + e^{-\alpha_1 t}\left(A_0 \cos\left(\sqrt{\omega_0^2 - {\alpha_1}^2}t\right) + B_0 \sin\left(\sqrt{\omega_0^2 - {\alpha_1}^2}t\right)\right)$$

$$A_0 = V_{CC} - V_{fd1}, \quad B_0 = \frac{A_0\alpha_1 + \frac{I_{\mathrm{pre}}}{(c_{\mathrm{gs}_1}+c_{\mathrm{gd}_1})}}{\sqrt{\omega_0^2 - {\alpha_1}^2}} \tag{6}$$

$$\alpha_1 = \frac{r_{g_1} + R_{\mathrm{ac}}}{2(L_r + L_{s_1})}. \tag{7}$$

The initial condition for this mode is $v_{\mathrm{gs}_1}(t_6) = V_{CC}$, and $i_g(t_6) = -\frac{V_{CC}}{L_r}(t_6 - t_5) = I_{\mathrm{pre}}$. According to the power MOSFET parameters, the equations are obtained for $\omega_0 > \alpha_1$.

8) Mode 8 ($t_7 \le t < t_8$) [see Fig. 5(h)] (Miller Plateau): During this mode, v_{gs_1} remains fixed at the Miller plateau voltage, V_{mil}. The gate drive current discharges c_{gd_1}, and v_{ds_1} increases accordingly. This interval ends when v_{ds_1} reaches the buck converter input voltage V_{in}. During this interval, v_{ds_1}, and i_g are derived as

$$i_g(t) = \frac{V_{\mathrm{mil}} - V_{fd1}}{r_{g_1} + R_{\mathrm{ac}}} + \left(i_{G\text{-}T7} - \frac{V_{\mathrm{mil}} - V_{fd1}}{r_{g_1} + R_{\mathrm{ac}}}\right) e^{\frac{-(r_{g_1} + R_{\mathrm{ac}})}{L_r + L_{s_1}} t}$$

$$v_{\mathrm{ds}_1}(t) = v_{\mathrm{ds}_1}(t_7) + \frac{1}{c_{\mathrm{gd}_1}} \left[-\frac{V_{\mathrm{mil}} - V_{fd1}}{r_{g_1} + R_{\mathrm{ac}}} t + \left(\frac{i_{G\text{-}T7} - \frac{V_{\mathrm{mil}} - V_{fd1}}{r_{g_1} + R_{\mathrm{ac}}}}{\frac{-(r_{g_1} + R_{\mathrm{ac}})}{L_r + L_{s_1}}} \right) \left(1 - e^{\frac{-(r_{g_1} + R_{\mathrm{ac}})}{L_r + L_{s_1}} t}\right) \right]. \tag{8}$$

The initial condition for this mode is $v_{\mathrm{gs}_1}(t_7) = V_{\mathrm{mil}}$, $i_g(t_7) = i_g(t_7 - t_6) = i_{G\text{-}T7}$, and $v_{\mathrm{ds}_1}(t_7) = I_0 R_{\mathrm{ds-ON}}$.

9) Mode 9 ($t_8 \le t < t_9$) [see Fig. 5(i)] (Drain Current Falling): At t_8, v_{ds_1} reaches the buck converter input voltage. Then, the drain current starts to decrease, and the body diode of SR turns on. The power MOSFET operates in the saturation region during this interval, and $i_{\mathrm{ds}_1} = g_{fs}(v_{\mathrm{gs}_1} - V_{\mathrm{th}})$. During this interval, v_{ds_1} keeps increasing due to the induced voltage across L_{S_1} and L_{loop}. In this mode, the total current of the driver inductance i_{L_r} flows through the gate (i.e., $i_{L_r} = i_g$), and discharges the power MOSFET gate capacitance. In the proposed CSD, the induced voltage across L_{S_1} and r_{g_1} does not impact the gate current of the power MOSFET, and the proposed CSD operates as an ideal CSD. However, in the CSD circuits with current diversion problem, the CSD inductor current is diverted, which reduces the effective current to discharge the power MOSFET gate. This interval ends when v_{gs_1} reaches V_{th}. The equations of v_{gs_1}, i_{ds_1}, and v_{ds_1} during this interval are given by

$$v_{\mathrm{gs}_1}(t) = A_1 + B_1 e^{(-\alpha_2 - \sqrt{\alpha_2^2 - {\omega_0}^2})t} + C_1 e^{(-\alpha_2 + \sqrt{\alpha_2^2 - {\omega_0}^2})t}$$

$$A_1 = V_{fd1}$$

$$B_1 = \frac{(V_{\mathrm{mil}} - V_{fd1})(-\alpha_2 + \sqrt{\alpha_2^2 - {\omega_0}^2}) - \frac{i_{G\text{-}T8}}{(c_{\mathrm{gs}_1} + c_{\mathrm{gd}_1})}}{2\sqrt{\alpha_2^2 - {\omega_0}^2}}$$

$$C_1 = \frac{(V_{\mathrm{mil}} - V_{fd1})(\alpha_2 + \sqrt{\alpha_2^2 - {\omega_0}^2}) + \frac{i_{G\text{-}T8}}{(c_{\mathrm{gs}_1} + c_{\mathrm{gd}_1})}}{2\sqrt{\alpha_2^2 - {\omega_0}^2}} \tag{9}$$

$$i_{\mathrm{ds}_1}(t) = g_{fs}(v_{\mathrm{gs}_1}(t) - V_{\mathrm{th}}) \tag{10}$$

$$v_{\mathrm{ds}_1}(t) = V_{\mathrm{in}} - (L_{\mathrm{loop}} + L_{s_1})\frac{di_{\mathrm{ds}}}{dt} + L_{s_1}\frac{di_g}{dt} \tag{11}$$

$$\alpha_2 = \frac{(r_{g_1} + R_{ac})(c_{\mathrm{gs}_1} + c_{\mathrm{gd}_1}) + L_{s_1} g_{fs}}{2(L_r + L_{s_1})(c_{\mathrm{gs}_1} + c_{\mathrm{gd}_1})} \tag{12}$$

where g_{fs} is the MOSFET's transconductance. The initial condition for this interval is $v_{\mathrm{gs}_1}(t_8) = V_{\mathrm{mil}}$, and $i_g(t_8) = i_g(t_8 - t_7) = i_{G\text{-}T8}$. According to the power MOSFET parameters, the equations are obtained for $\omega_0 < \alpha_2$.

10) Mode 10 ($t_9 \le t < t_{10}$) [see Fig. 5(j)] (Remaining Gate Discharging): At t_9, v_{gs_1} reaches V_{th} and the power MOSFET turns off. Thus, v_{gs_1} keeps decreasing until it reaches zero. Then, the polarity of v_{gs_1} is inverted and the energy stored in L_r is transferred to the gate capacitance of the power MOSFET. This interval ends when the inductor current becomes zero, and v_{gs_1} reaches its negative peak value. During this interval, i_g and v_{gs_1} are derived as

$$v_{\mathrm{gs}_1}(t) = V_{fd_1} + e^{-\alpha_1 t}\left(A_2 \cos\left(\sqrt{{\omega_0}^2 - \alpha_1^2}\, t\right) + B_2 \sin\left(\sqrt{{\omega_0}^2 - \alpha_1^2}\, t\right)\right) \tag{13}$$

$$A_2 = V_{\mathrm{th}} - V_{fd1}$$

$$B_2 = \frac{A_2\alpha_2 + \frac{i_{G\text{-}T9}}{c_{\mathrm{gs}_1} + c_{\mathrm{gd}_1}}}{\sqrt{{\omega_0}^2 - \alpha_1^2}} \tag{14}$$

$$i_g(t) = (c_{\mathrm{gs}_1} + c_{\mathrm{gd}_1})\frac{d}{dt} v_{\mathrm{gs}_1}(t). \tag{15}$$

The initial condition for this interval is $v_{\mathrm{gs}_1}(t_9) = V_{\mathrm{th}}$, and $i_g(t_9) = i_g(t_9 - t_8) = i_{G\text{-}T9}$.

11) Mode 11 ($t_{10} \le t < t_{11}$) [see Fig. 5(k)] (Noise Immunity Interval): During this mode, i_{L_r} remains zero, and a negative voltage is applied to the gate–source of the power MOSFET, which protects it from unwanted triggering.

III. Loss Analysis and Design Procedure

In order to obtain a precise study of losses of buck VRM for various loads, and to indicate the significance of the turn-OFF losses at full load, the loss analysis of the buck VRM is presented with accurate mathematical equations. Then, the tradeoff between the switching losses and the gate drive losses yields the optimum gate drive inductor value.

A. Loss Analysis

1) Turn-OFF Losses: The turn-OFF switching losses of HS MOSFET greatly impact the buck VRM performance. Turn-OFF losses are calculated as follows:

$$P_{\mathrm{off}} = f_{\mathrm{sw}}\left(\int_{t_7}^{t_9} (i_{\mathrm{ds}_1} v_{\mathrm{ds}_1})dt - \frac{1}{2} Q_{oss\text{-SR}} V_{\mathrm{in}}\right) \tag{16}$$

where f_{sw} is the switching frequency, and the derivations for i_{ds_1} and v_{ds_1} are given in modes 8 and 9 (see Fig. 4).

The common-source inductance causes the current diversion problem and reduces the effective gate current during transition times. As shown in [13], the switching losses of the HS MOSFET almost proportionally increase to I_o^2.

2) Turn-ON Losses: At turn-ON transition times, during mode 2 where i_{ds_1} and v_{ds_1} waveforms overlap, the proposed gate driver operates similar to a VSD with the supply voltage of $V_{CC} + V_{fd2}$. Thus, the turn-ON losses can be calculated using

the equations presented in [9]. It is noteworthy that the turn-OFF losses of the HS power MOSFET is much higher than the turn-ON losses, due to the effect of the loop inductance and the high output inductor ripple of the buck converter.

It is noteworthy that, as shown in [9], the drain–source voltage of the HS MOSFET in low-voltage high-current high-frequency buck VRMs becomes zero before the current reaches the steady-state value. Therefore, the turn-ON losses of the HS MOSFET is independent of load (in a specific range).

3) Conduction Losses of HS MOSFET and SR MOSFET: As presented in [42], the conduction losses can be calculated as

$$P_{\text{on}-H} = \left[{I_o}^2 + \frac{(I_p - I_v)^2}{12} \right] R_{\text{ds}-\text{HS}} \frac{V_{\text{out}}}{V_{\text{in}}} \tag{17}$$

$$P_{\text{on}-L} = \left[{I_o}^2 + \frac{(I_p - I_v)^2}{12} \right] R_{\text{ds}-\text{SR}} \left(1 - \frac{V_{\text{out}}}{V_{\text{in}}} \right) \tag{18}$$

where $I_p = I_o + \frac{\Delta I_L}{2}$, $I_v = I_o - \frac{\Delta I_L}{2}$, and $\Delta I_L = \frac{V_{\text{in}} - V_{\text{out}}}{L_f f_{\text{sw}}} \times \frac{V_{\text{out}}}{V_{\text{in}}}$. $R_{\text{ds}-\text{HS}}$ and $R_{\text{ds}-\text{SR}}$ are ON resistance of HS and SR MOSFETS, respectively.

4) Switching Losses of SR MOSFET: Based on the work in [43], the switching losses of SR MOSFET are given by

$$P_{\text{sw}-\text{SR}} = \left(t_2 V_F + t_3 \frac{V_F + 1.1 I_o R_{\text{ds(on)}-\text{SR}}}{2} \right) I_o f_{\text{sw}} \tag{19}$$

$$t_{2R} = K_{2R}(R_{\text{driver}} + R_g) C_{iss}$$

$$K_{2R} = \ln\left(\frac{V_{CC}}{V_{CC} - V_{SP}} \right) - \ln\left(\frac{V_{CC}}{V_{CC} - V_{\text{th}}} \right) \tag{20}$$

$$t_{3R} = K_{3R}(R_{\text{driver}} + R_g) C_{iss}$$

$$K_{3R} = \ln\left(\frac{V_{CC}}{V_{CC} - 0.9 V_{\text{SPEC}}} \right) - \ln\left(\frac{V_{CC}}{V_{CC} - V_{SP}} \right) \tag{21}$$

$$t_{2F} = K_{2F}(R_{\text{driver}} + R_g) C_{iss}, \; K_{2F} = \ln\left(\frac{V_{SP}}{V_{\text{th}}} \right) \tag{22}$$

$$t_{3F} = K_{3F}(R_{\text{driver}} + R_g) C_{iss}, \quad K_{3F} = \ln\left(\frac{0.9 V_{\text{SPEC}}}{V_{\text{SP}}} \right) \tag{23}$$

where $V_{SP} = V_{\text{th}} + \frac{I_o}{g_{fs}}$, $t_2 = t_{2R} + t_{2F}$, $t_3 = t_{3R} + t_{3F}$, V_{SPEC} is the gate voltage for the highest specified $R_{\text{ds}}(\text{on})$ according to the datasheet, and R_{driver} is the driver circuit's output resistance.

5) Reverse Recovery Losses: Fig. 8 shows the characteristic current waveform during the reverse recovery effect of the body diode of SR MOSFET.

The reverse recovery losses of the SR MOSFET body diode can be derived as

$$P_{\text{rr}} = V_{\text{in}} Q_{\text{rr}} f_{\text{sw}} \tag{24}$$

where Q_{rr} is the reverse recovery charge of SR body diode which depends on $\frac{di}{dt}$ ratio and forward current of the SR diode. Generally, a single measurement point for Q_{rr} is given in datasheet of the MOSFET. The accurate equation of Q_{rr} based on $\frac{di}{dt}$ ratio and forward current of the SR diode is presented in [44]. It

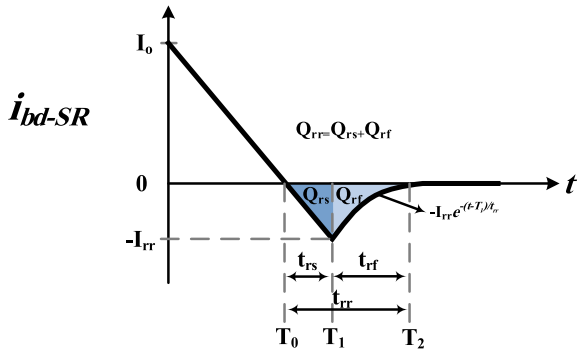


Fig. 8. Characteristic current during the reverse recovery effect of the SR body diode.

should be noted that, as shown in [9], Q_{rr} of the body diode of SRs lower than 30 V, when loop inductance L_{loop} is higher than 3 nH, has low sensitivity to the variations of $\frac{di}{dt}$. Therefore, Q_{rr} is assumed to be independent of $\frac{di}{dt}$ for calculating the reverse recovery losses, and it only changes with the forward current of the diode.

6) MOSFET Output Capacitance Losses: The output capacitance losses of SR MOSFET are given by

$$P_{Coss-\text{SR}} = \frac{1}{2} Q_{oss-\text{SR}} V_{\text{in}} f_{\text{sw}} \tag{25}$$

where $Q_{oss-\text{SR}}$ is the output charge of SR MOSFET.

For calculating the output capacitance losses of the HS MOSFET, a portion of the energy is stored in the output capacitance of HS MOSFET after the turn-OFF transition ends. This energy is dissipated when the HS MOSFET turns on. Thus, the equations of the switching losses for the HS MOSFET cover the output capacitance losses as well.

7) Dead Time Losses: The dead time losses occur when both the HS MOSFET and the SR MOSFET are OFF, and it can be calculated according to [43]

$$P_{\text{dead time}} = t_{\text{dead time}} f_{\text{sw}} V_F I_o \tag{26}$$

$$t_{\text{dead time}} = t_{\text{delay}} + \frac{Q_{\text{gs}}(r_{g_2} + R_{\text{driver}})}{V_{CC} - \frac{V_{\text{th}}}{2}} \tag{27}$$

where V_{th} is the gate threshold voltage of SR MOSFET, and $Q_{\text{gs}} \simeq 2Q_g(\text{th})$.

8) Gate Drive Losses: The total losses of the proposed gate drive circuit include the conduction losses of the control switches $P_{\text{cond-switch}}$, the conduction losses of the body diodes of the control switches P_{body}, the total conduction losses ($P_{\text{cond-total}} = P_{\text{cond-switch}} + P_{\text{body}}$), the gate resistance losses of the power MOSFET $P_{r_{g_1}}$, the gate driver inductance losses P_{ind}, and the gate losses of the control switches. Since, the control switches S_1, S_2 operate under soft-switching condition, no additional switching losses are considered for S_1 and S_2.

The power absorbed from the driver power supply is equal to the summation of $P_{\text{cond-switch}}$, P_{body}, $P_{r_{g_1}}$, and P_{ind}. Thus, the total power dissipated in the proposed gate driver is expressed

as

$$P_{\text{CSD}} = V_{CC} I_{\text{avg}} + P_{\text{gate}} \tag{28}$$

where I_{avg} is the average current of the driver power supply and P_{gate} is the gate losses of the control switches S_1 and S_2, which is given by

$$P_{\text{gate}} = (Q_{\text{gs}_1} v_{c_{\text{gs}1}} + Q_{\text{gs}_2} v_{c_{\text{gs}2}}) f_{\text{sw}} \tag{29}$$

where Q_{gs_1} and Q_{gs_2} are the total gate charges of the control switches S_1 and S_2, respectively.

The gate drive losses of SR MOSFET with VSD is

$$P_{\text{drive-SR}} = Q_g V_{CC} f_{\text{sw}} \tag{30}$$

where Q_g is the total gate charge of the SR MOSFET. The gate drive losses of the HS MOSFET driven by the proposed CSD are calculated in [17], and the gate drive losses of the HS MOSFET with the CSD introduced in [39] and with the VSD are given in [39].

9) Operation Loss of IC: The power consumption of the control circuit is derived as

$$P_{\text{IC}} = V_{\text{IC}} I_{\text{IC}} \tag{31}$$

where V_{IC} is the supply voltage of the IC, and I_{IC} is the current consumption of the control IC.

10) Output Inductance Losses: The output inductance losses include the conduction losses and the core losses. The conduction losses of the inductor are given by [9], [13]

$$P_{\text{cond}-L_f} = R_{ac} {I_{L_f,\text{RMS}}}^2 = R_{ac} \left(I_o + \frac{{V_o}^2 (V_{\text{in}} - V_o)^2}{12 {L_f}^2 {V_{\text{in}}}^2 {f_{\text{sw}}}^2} \right). \tag{32}$$

The core losses can be obtained using [45]

$$P_{\text{core}} = K_1 {f_{\text{sw}}}^x B^y V_e \tag{33}$$

where K_1 is a constant for the core material, B is the peak flux density in the core, x is the frequency exponent, y is the flux density, and V_e is the effective core volume. Thus, the total losses of the output inductance are

$$P_{L_f} = P_{\text{cond}-L_f} + P_{\text{core}}. \tag{34}$$

11) Input and Output Capacitance Losses: As explained in [42], the input and output capacitance losses of buck VRMs are

$$P_{\text{Cin}} = \text{ESR}_{C\text{in}} {I_{C\text{in(RMS)}}}^2 \tag{35}$$

$$I_{C\text{in(RMS)}} = I_o \frac{\sqrt{(V_{\text{in}} - V_o) V_o}}{V_{\text{in}}} \tag{36}$$

$$P_{\text{Cf}} = \text{ESR}_{Cf} {I_{Cf\text{(RMS)}}}^2 \tag{37}$$

$$I_{Cf\text{(RMS)}} = \frac{\Delta I_L}{2\sqrt{3}} \tag{38}$$

where ESR is the equivalent series resistance of the capacitor.

With regards to the mathematical equations, power dissipation ratio for the buck VRM driven by the proposed CSD, the CSD in [39] and the VSD for different load currents are illustrated. Parameters of the buck converter are $V_{\text{in}} = 12$ V, $f_{\text{sw}} = 1$ MHz, $V_{CC} = 5$ V, HS MOSFET: IRF7811AV, low side (LS) MOSFET: IRF6691, and VSD: ISL6207. Since the dynamic response is improved with the reduction of the output inductance, the power dissipation ratio is presented for various output inductances including 200, 100, and 50 nH. The reason for choosing the CSD in [39] for the comparison study is that, as given in Table III, the proposed gate driver and the CSD presented in [39] are the only two switch discontinuous current CSD circuits.

The efficiency curve of buck VRM with different parameters versus load current is presented in Fig. 9.

Detailed power losses of buck VRM driven by the proposed CSD, the CSD in [39], and VSD with the following parameters are presented in Table I: $V_{\text{in}} = 12$ V, $V_{\text{out}} = 1.3$ V, $f_{\text{sw}} = 2$ MHz, $L_f = 200$ nH, and $I_o = 30$ A. As shown in Fig. 10 and Table I, the significant part of the total losses in a 12 V buck VRM at full load is related to the turn-OFF losses of the HS MOSFET.

B. Optimal Design

There is a tradeoff between the turn-OFF switching losses and the gate drive losses reduction. The design optimization of the gate driver inductor tries to optimize this tradeoff. Reducing the gate drive inductance (increasing the gate drive current) minimizes the turn-OFF transition time, which results in a noticeable reduction in the turn-OFF switching losses of HS MOSFET. However, it increases the inductor rms current, which leads to higher gate drive conduction losses [22]–[24].

In order to achieve the optimal design, the proposed CSD is used to drive the HS MOSFET of a buck VRM converter, as shown in Fig. 5(a). The parameters of the buck VRM driven by the proposed gate driver are: $V_{\text{in}} = 12$ V, $V_o = 1.3$ V, $V_{CC} = 5$ V, $I_O = 20$ A, $f_{\text{sw}} = 1$ MHz, $L_f = 200$ nH, HS MOSFET: IRF7811AV (gate resistance: $r_{g_1} = 1\ \Omega$), SR MOSFET: IRF6691, and control switches S_1: FDN335N (on resistance $= 55$ mΩ; total gate charge $= 3.5$ nC @ $V_{\text{gs}} = 5$ V), S_2: FDN342P (on resistance $= 62$ mΩ; total gate charge $= 6.3$ nC @ $V_{\text{gs}} = 5$ V).

Generally, the value of the power MOSFET parasitic inductance is measured by the semiconductor manufacturer in [46] and [47], and it ranges from 250 pH to 1 nH for power PAK SO-8 package [13]. Thus, it is assumed that $L_{s_1} = L_{s_2} = L_{d_1} = L_{d_2} = 1$ nH.

In order to find the optimal design point, the turn-OFF losses of the HS MOSFET P_{off}, and the gate drive losses P_{CSD} (along with their summation by using (8)–(12), (17), (18), $P_{\text{sum}} = P_{\text{off}} + P_{\text{CSD}}$) are derived for different values of the gate drive inductances as illustrated in Fig. 11(a). The summation of these losses, $P_{\text{sum}} = P_{\text{off}} + P_{\text{CSD}}$, has a U-shaped curve and the optimal point (i.e., the optimal inductance value) is at the minimum point. Fig. 11(b) illustrates I_{pre} based on L_r and maximum negative voltage of gate–source ($v_{\text{gs}_1(t)}$ at $t = t_{10}$).

The value of L_r is selected with respect to the minimum $P_{\text{sum}} = P_{\text{off}} + P_{\text{CSD}}$, and guaranteeing that $|v_{\text{gs}_1}(t_{10})|$ is lower than the maximum negative gate voltage rate that the power MOSFET can tolerate (i.e., $|v_{\text{gs}_1}(t_{10})| < |v_{\text{gs}_1(\text{max})}|$).

In order to minimize the delay of the control loop, t_{65} should be selected small. On the other hand, hardware limitations of

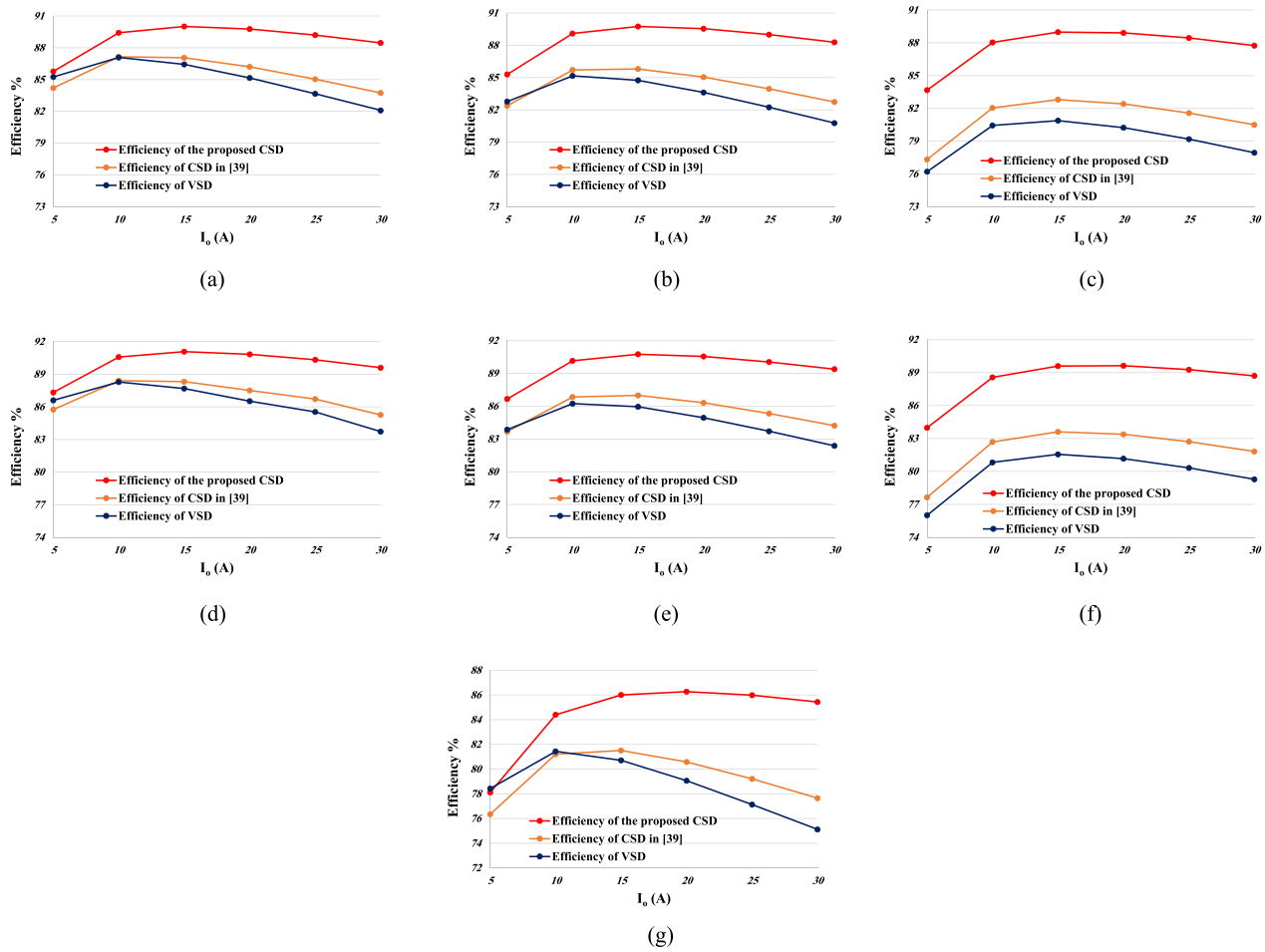


Fig. 9. Efficiency curve of buck VRM versus load current with different parameters. (a) $L_f = 200$ nH, $V_{\text{out}} = 1.3$ V, $f_{\text{sw}} = 1$ MHz. (b) $L_f = 100$ nH, $V_{\text{out}} = 1.3$ V, $f_{\text{sw}} = 1$ MHz. (c) $L_f = 500$ nH, $V_{\text{out}} = 1.3$ V, $f_{\text{sw}} = 1$ MHz. (d) $L_f = 200$ nH, $V_{\text{out}} = 1.5$ V, $f_{\text{sw}} = 1$ MHz. (e) $L_f = 100$ nH, $V_{\text{out}} = 1.5$ V, $f_{\text{sw}} = 1$ MHz. (f) $L_f = 50$ nH, $V_{\text{out}} = 1.5$ V, $f_{\text{sw}} = 1$ MHz. (g) $L_f = 200$ nH, $V_{\text{out}} = 1.3$ V, $f_{\text{sw}} = 2$ MHz.

TABLE I
DETAILED POWER LOSSES OF BUCK VRM DRIVEN BY DIFFERENT DRIVERS

Loss (mW)	Output capacitance	Input capacitance	Output inductor	Operation of IC	Gate drive	Dead time	MOSFET output capacitance	Reverse recovery of SR diode	Switching of low-side MOSFET	Switching of high-side MOSFET	Conduction of low-side MOSFET	Conduction of high-side MOSFET
VSD	0.7	171	720.56	12	650	944.7	420	170.935	551.6	7254.13	1143.89	878.18
CSD in [39]	0.7	171	720.56	12	960	944.7	420	170.935	551.6	5253.46	1143.89	878.18
Proposed CSD	0.7	171	720.56	12	960	944.7	420	170.935	551.6	680.5	1143.89	878.18

the complex programmable logic device (CPLD) on generating narrow pulses constraints the reduction of t_{65}. Thus, the duration of t_{65} is selected equal to 70 ns.

The optimal value of L_r that meets the aforementioned constraints is obtained: $L_r = 160$ nH; Hence I_{pre} at $t = t_6$ (see Fig. 4) is equal to $I_{\text{pre}}(t_6) = 2.12$ A, as shown in Fig. 11.

The logic circuit presented in Fig. 12(a) can be employed to generate the control signals for S_1 and S_2. Pulsewidth modulation (PWM) signal is generated by the converter controller to control the HS MOSFET. Fig. 12(b) illustrates the logic waveforms of the controller. Delay line D_1 delays the PWM signal as much as the time period from t_0 to t_4.

IV. COMPARATIVE ANALYSIS

A. Advantages of the Proposed CSD

In this section, the performance of the proposed gate driver is compared to that of previously proposed CSDs [11]–[13], [20]–[27], [29], [35]–[39] in order to show its superior performance. Some of the main advantages of the proposed gate driver are listed as follows.

1) Turn-OFF Losses: As illustrated in Fig. 4, during the turn-OFF transition, the overlap between the voltage and current waveforms occurs only at the Miller plateau interval (i.e., mode 8) and during the drain current falling interval (i.e., mode 9).

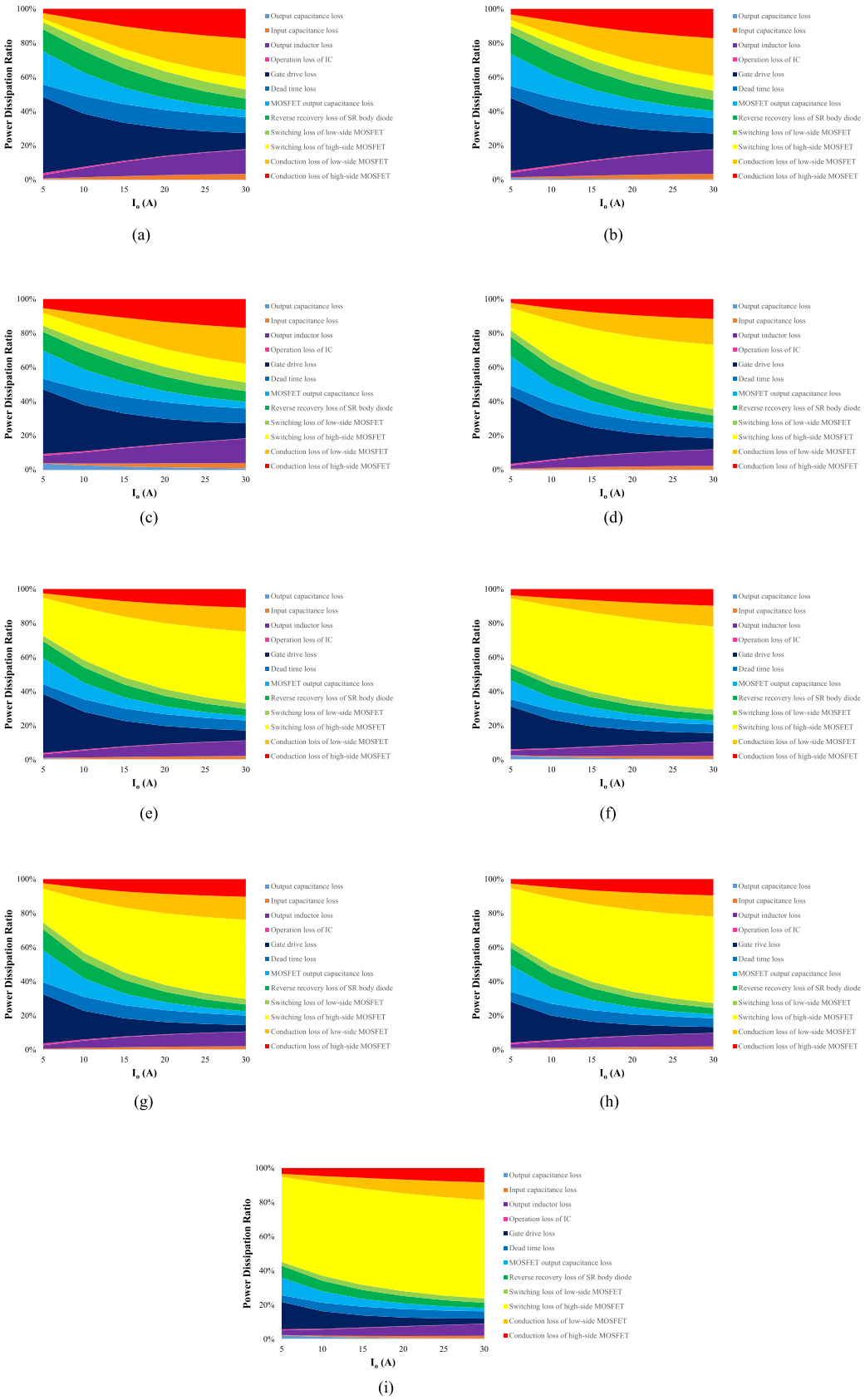


Fig. 10. Power dissipation ratio of buck VRM for various output currents. (a) Buck VRM with the proposed CSD—$L_f = 200$ nH. (b) Buck VRM with the proposed CSD—$L_f = 100$ nH. (c) Buck VRM with the proposed CSD—$L_f = 50$ nH. (d) Buck VRM with the CSD in [39]—$L_f = 200$ nH. (e) Buck VRM with the CSD in [39]—$L_f = 100$ nH. (f) Buck VRM with the CSD in [39]—$L_f = 50$ nH. (g) Buck VRM with VSD—$L_f = 200$ nH. (h) Buck VRM with VSD—$L_f = 100$ nH. (i) Buck VRM VSD—$L_f = 50$ nH.

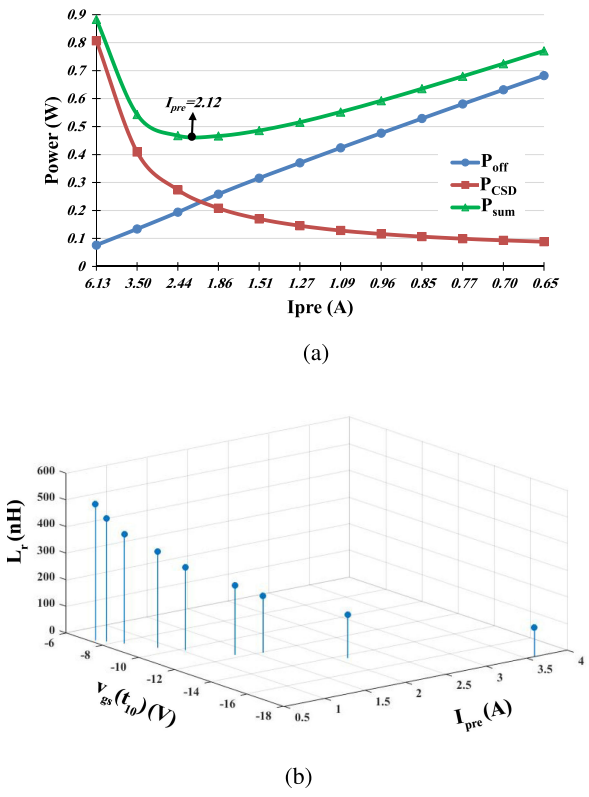


Fig. 11. Optimal design curves.

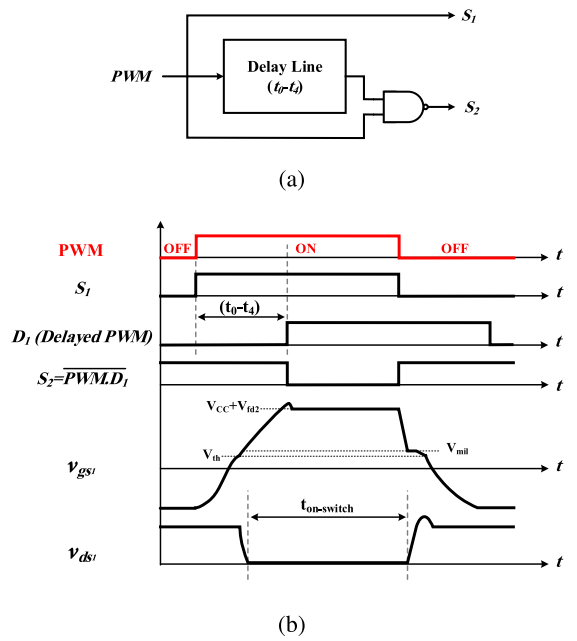


Fig. 12. Logic circuit and logic waveforms used to create the control switch gating signals of S_1 and S_2.

Thus, there are turn-OFF switching losses only during these two intervals. A comparison between the turn-OFF losses of the buck VRM HS MOSFET driven by the proposed gate driver, the CSDs with current diversion problem, the CSD proposed in [12], [13], the CSD proposed in [11], and the conventional VSD is presented as follows.

a) Miller plateau: During the Miller plateau interval, the drain–source current i_{ds_1} remains constant, hence there is no current diversion problem. For all CSD circuits and the proposed CSD, entire driver inductance current flows through the gate of the power MOSFET during this mode, and c_{gd_1} is charged with almost constant current. Therefore, in the CSD circuits and in the proposed CSD the Miller time is reduced, and in turn the turn-OFF switching losses are decreased compared to that of VSDs.

b) Drain current falling: During this interval, i_{ds_1} is decreasing and a voltage is induced across L_{s_1}, labeled as $v_{L_{s_1}}$. In VSDs, $v_{L_{s_1}}$ reduces the effective gate current (since $i_g = \frac{v_{\mathrm{gs}_1}(t) - v_{L_{s_1}}}{r_{g_1}}$), and increases the turn-OFF switching losses. As illustrated in Fig. 2(b) and in [12] and [13], $v_{L_{s_1}}$ causes the body diode, D, to turn ON in the CSDs with current diversion problem; and a portion of the gate drive current is diverted through the body diode, D, [see Fig. 2(b)] instead of discharging the gate capacitance of the power MOSFET. In fact, during this interval the CSDs with current diversion problem operate similar to a VSD with a negative driver voltage (approximately equal to the body diode voltage drop $-V_D$); and discharge the power MOSFET gate capacitance with a current equal to $i_g = \frac{v_{\mathrm{gs}_1}(t) + V_D - v_{L_{s_1}}}{r_{g_1}}$. Thus, the effective gate current of the CSDs with current diversion problem is slightly higher than the VSD gate current.

As shown in Fig. 2(c), the CSD proposed in [12] and [13] behaves similar to a VSD with driver voltage equal to $-nV_D$ by using the series diodes, where n is the number of series diodes and V_D is the voltage drop across the diode. The CSD proposed in [12] and [13] discharges the gate capacitance of the power MOSFET with a higher negative voltage compared to the CSDs with current diversion problem; which leads to smaller turn-OFF losses. The effective gate current of the CSD proposed in [32] is equal to $i_g = \frac{v_{\mathrm{gs}_1}(t) + nV_D - V_{L_{s_1}}}{r_{g_1}}$ during this interval.

The proposed CSD and the CSD presented in [11] [see Fig. 2(d)] operate as an ideal current-source during turn-OFF transition. Thus, the gate current of the HS MOSFET is determined only by the gate driver inductance current and it is not affected by L_{s_1}. It should also be noted that in [11], additional conduction losses are generated due to the undesired resonance between the gate driver inductance, the gate resistance, and the gate capacitance. This resonance may lead to undesired triggering of the power MOSFET.

The comparison between turn-OFF losses and average gate current of the proposed CSD, the CSDs with current diversion problem, the CSD proposed in [12] and [13], and the VSD by using derived equations is summarized in Table II. This comparison is performed for a buck VRM under the following parameters: $V_{\mathrm{in}} = 12$ V, $V_{\mathrm{out}} = 1.3$ V, $I_o = 30$ A, HS MOSFET: IRF7811AV. It is observed that the proposed gate driver achieves a turn-OFF losses reduction of 2.99 W in comparison with the VSD. Even compared to the CSDs with current diversion problem, the proposed bipolar CSD improves the losses by 2.08 W.

TABLE II
COMPARISON BETWEEN THE PROPOSED GATE DRIVER AND OTHER INTRODUCED CIRCUITS DURING TURN-OFF

Driver type	Turn-off losses of high-side MOSFET (W)	i_{g-avg} (A)
VSD	3.3	0.149
CSDs in [20]–[27], [29], [35]–[39]	2.39	0.239
CSD presented in [12], [13]	1.1	0.679
proposed gate driver	0.31	1.9

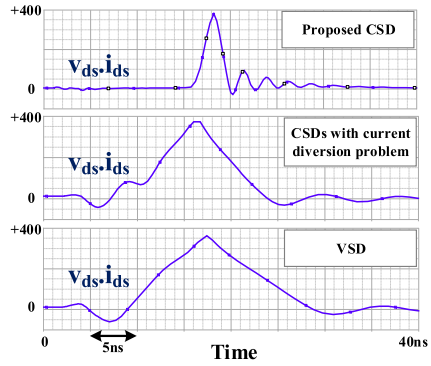


Fig. 13. Simulation waveforms of the turn-OFF losses for the proposed CSD, CSDs with current diversion problem, and for VSD.

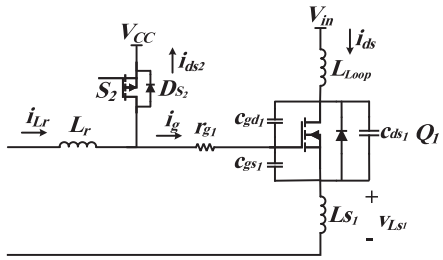


Fig. 14. Equivalent circuit of the proposed CSD and CSDs [20]–[27], [29], [35]–[39] during turn-ON.

Furthermore, the simulation waveforms of the turn-OFF losses that confirm the derived turn-OFF losses (given in Table II) are presented in Fig. 13.

2) Turn-ON Losses: The equivalent circuit for the proposed gate driver and the one for the CSDs with current diversion problem during the power MOSFET turn-ON time is shown in Fig. 14. During the interval where i_{ds_1} and v_{ds_1} waveforms overlap (i.e., the turn-ON losses), i_{ds_1} is increasing (see Fig. 4). The induced voltage across L_{s_1} causes D_{s_2} to conduct; and both the proposed CSD and the CSDs with current diversion problem operate similar to a VSD (during the overlap of i_{ds_1} and v_{ds_1}). Therefore, the turn-ON losses of the buck VRM HS MOSFET driven by the proposed CSD and the one driven by the CSDs with current diversion problem are equal. It is noted that during the turn-ON time, the parasitic inductances function as a current snubber given in [10]. Therefore, the turn-ON losses of the buck VRM HS MOSFET are negligible.

3) Number of Components: The proposed gate driver is consisted of only two control switches and a small inductor. Thus, it contains the lowest number of circuit components compared to the previously proposed CSDs. Furthermore, the proposed CSD operates in discontinuous mode (discontinuous CSD). Unlike continuous CSDs, discontinuous CSDs can achieve lower drive losses, and they are more suitable for driving the buck VRM HS MOSFETs as illustrated in [30]. Table III summarizes the comparison between the proposed gate driver and the CSDs proposed in [11]–[13], [23], [27], [29], [37], and [39].

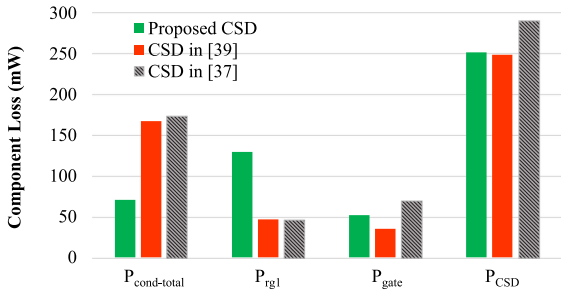


Fig. 15. Loss break-down and the total loss of the proposed CSD in comparison with the CSDs presented in [37] and [39].

4) Gate Drive Losses: Fig. 15 illustrates the loss break-down and the total losses of the proposed CSD in comparison with the CSDs presented in [37] and [39]. This comparison is performed for the proposed CSD with the parameters given in Section III.

According to Table II, the effective gate current of the proposed CSD is much higher than the one for the CSDs introduced in [37] and [39], which leads to higher gate resistance losses for the proposed CSD. However, a portion of the CSD inductance current flows through the diode D for the CSDs presented in [37] and [39] [see Fig. 2(b)]. This causes excessive diode conduction losses, which do not exist in the proposed CSD. Moreover, since the proposed CSD and the CSD presented in [39] contain lower number of control switches than the CSDs presented in [37], the gate losses of the control switches and the conduction losses are reduced. Also, the operating modes of the CSD introduced in [39] include a freewheeling mode, which imposes excessive conduction losses, and cause the CSD in [39] to have higher total conduction losses, $P_{\text{cond-total}}$, compared to the proposed CSD.

B. Disadvantages of the Proposed CSD

The disadvantages of the proposed CSD are listed as follows.

1) The proposed CSD and the CSD introduced in [39] are only suitable for narrow on-time applications such as buck VRM. While most of the discontinuous CSDs have wider applications. For example, the discontinuous CSD introduced in [27] is used as buck VRM and boost converter gate driver in [21] and [37], respectively.
2) Since the proposed CSD in unable to reduce the turn-ON losses of MOSFET, it is not suitable for applications where the turn-ON losses of MOSFET are dominant.

V. EXPERIMENTAL RESULTS

A. Key Waveforms

In order to verify the theoretical analysis, a buck VRM prototype with the proposed gate driver has been implemented. Fig. 16

TABLE III
COMPARISON BETWEEN THE PROPOSED GATE DRIVER AND OTHER INTRODUCED CIRCUITS

Driver circuit	CSD type	Number of switches	Number of capacitors	Number of diodes	Total number of circuit elements	Overcome the current diversion problem during turn-off
Proposed gate driver	Discontinuous	2	0	0	3	Completely overcome
CSDs in [27], [37]	Discontinuous	4	0	0	5	Unable to
CSD in [29]	Discontinuous	4	1	0	6	Unable to
CSD in [23]	Continuous	2	1	0	4	Unable to
CSD in [39]	Discontinuous	2	0	1	4	Unable to
CSDs in [12], [13]	Discontinuous	5	0	5	11	Improve
CSD in [11]	Discontinuous	4	0	2	7	Completely overcome

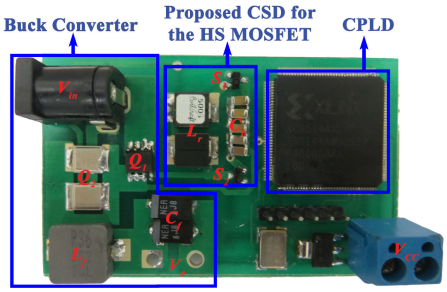


Fig. 16. Buck VRM prototype with the proposed gate driver.

TABLE IV
DESIGN PARAMETERS

Parameters	Value
Input voltage V_{in}	$12\,V$
Output voltage V_{out}	$1.3\,V$
Output current I_O	$20\,A$
Switching frequency f_{sw}	$1\,MHz$
Gate driver voltage V_{CC}	$5\,V$
HS MOSFET	$IRF7811AV$
SR MOSFET	$IRF6691$ (two parallel)
Output filter inductance L_f	$200\,nH$
Control switch S_1	$FDN342P$
Control switch S_2	$FDN335N$
Driver inductance L_r	$160\,nH$

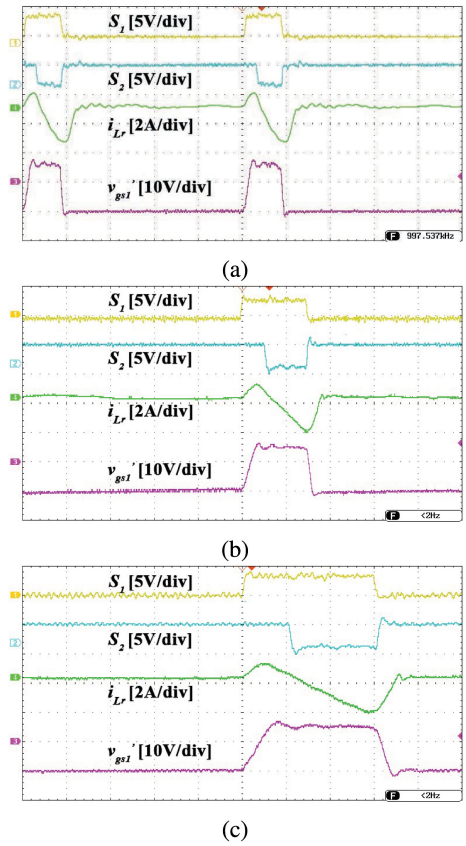


Fig. 17. Experimental waveforms of v_{gs_1} and i_{L_r} with control signals of S_1 and S_2. (a) Time/div = 200 ns. (b) Time/div = 100 ns. (c) Time/div = 50 ns.

shows the experimental prototype. According to Fig. 3(a), the proposed gate driver is applied to the HS MOSFET of the buck VRM, whereas the low-side SR MOSFET is driven with a conventional VSD.

The specifications of the buck VRM along with the selected components are presented in Table IV. The technique used to level-shift the signals and to drive switches S_1 and S_2 is quite similar to the one used in [12]. In order to drive the control switches S_1 and S_2 and to generate the gate signals, a CPLD (XC95144XL) along with the MOSFET gate drivers (ISL6207) is used. Gate signals generated by the CPLD are fed to the MOSFET drivers, which in turn deliver current pulses at 1 MHz to the gates of S_1 and S_2. The key waveforms of buck VRM are shown in Fig. 17. The two top waveforms in Fig. 17 illustrate the gate signals of S_1 and S_2, respectively; the third waveform illustrates i_{L_r}, and the gate–source voltage of the HS MOSFET (v_{gs_1}) is shown at the bottom of the figure. According to Fig. 17, the terminal gate–source voltage of the HS MOSFET (and in turn the voltage across the driver inductor) can have any appropriate values during the turn-OFF time (i.e., any value that does not damage the MOSFET gate). Therefore, the voltage drop across the common source inductance and the gate resistance can be compensated by changing the voltage across the inductor. In other words, the proposed gate driver behaves similar to an ideal CSD [see Fig. 2(a)] during the turn-OFF time. The experimental waveforms for the drain–source voltage and the gate–source voltage of the buck VRM are presented in Fig. 18.

It should be noted that the parasitic components of the differential probe will have an impact on the gate–source voltage of HS MOSFET. Thus, the experimental waveforms illustrated in Fig. 17 are slightly different from the actual waveforms.

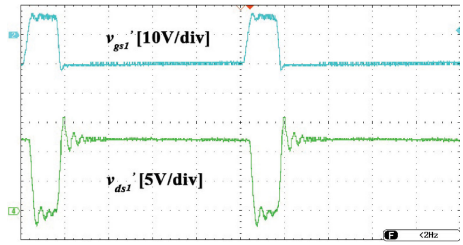
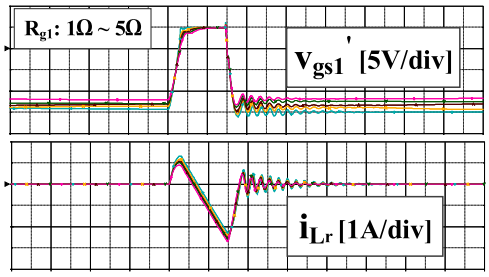
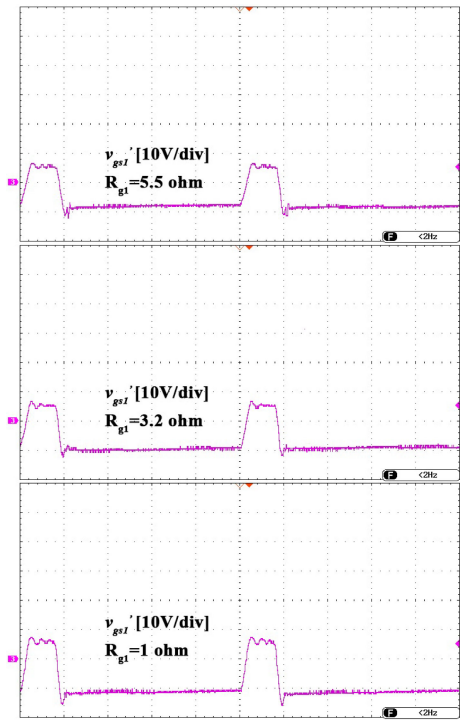


Fig. 18. Experimental waveforms of the drain–source voltage and the gate–source voltage (Time/div = 200 ns).



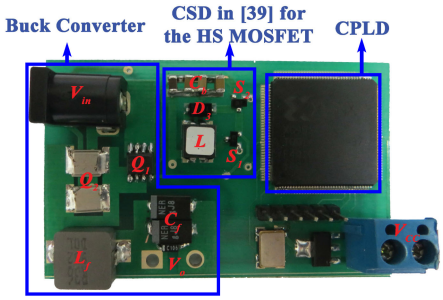
(a)



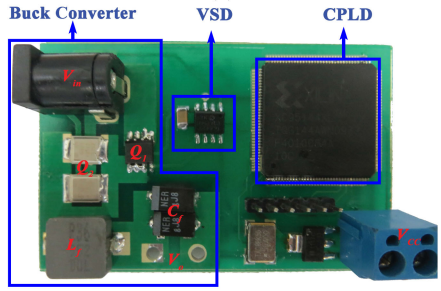
(b)

Fig. 19. Effect of gate resistance on performance of the gate driver. (a) Simulation results. (b) Experimental waveforms (Time/div = 200 ns.)

The experimental and simulation waveforms of v_{gs_1} for different gate resistances (that is obtained by adding external series resistors) are shown in Fig. 19. According to these waveforms, the proposed CSD has satisfactory performance for different values of the gate resistances. The reason for the difference between the experimental and simulation waveforms is related to the trace resistances and the resistance used to sense the current.



(a)



(b)

Fig. 20. Prototype of buck VRM (a) with the CSD in [39], (b) with VSD.

B. Comparison of the Proposed Gate Driver With VSD and the CSD Presented in [39]

In order to perform an accurate comparison study between the proposed gate driver, the CSD proposed in [39], and the VSD, three buck VRMs with the same specifications and different drivers have been implemented. The experimental prototypes of the three buck VRMs are shown in Figs. 16 and 20.

The operation of the CSD proposed in [39] is very similar to the ones with current diversion problem during the turn-OFF times [see Fig. 2(b)]. The reason for choosing it for the comparison study is that, as given in Table III, the proposed gate driver and the CSD presented in [39] are the only two switch discontinuous current CSD circuits. It is noteworthy to mention that, in order to achieve an accurate comparison the same PCB for power stage has been used.

As shown in [39], the terminal gate–source voltage of the CSD presented in [39] is unable to vary freely unlike the ideal CSD, and it is clamped to the voltage drop of the body diode ($\simeq -0.7$ V). Thus, in the CSD presented in [39], a portion of the driver current is diverted through the body diode instead of discharging the gate capacitance of the power MOSFET, whereas in the proposed CSD, the entire driver current flows through the gate.

Because measuring the gate current i_g would disturb the circuit operation, the measured waveform of i_g is not presented in this article.

Fig. 21 presents the efficiency comparison between the three buck VRMs driven by the proposed gate driver, by the CSD

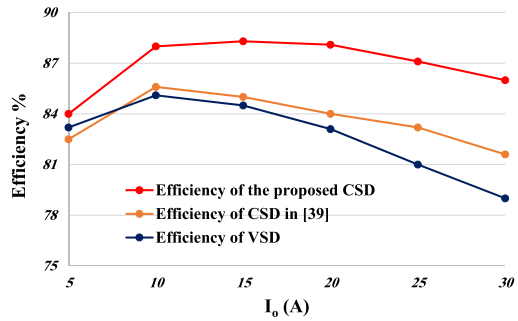


Fig. 21. Efficiency comparison.

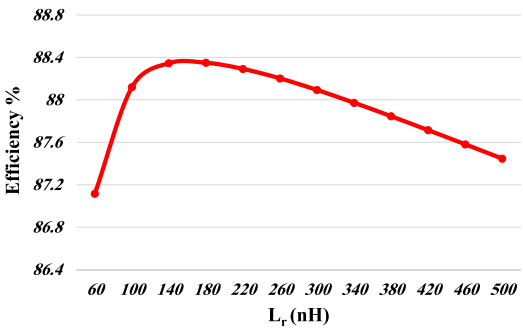


Fig. 22. Efficiency of buck VRM driven by the proposed CSD with different inductance values.

in [39], and by the VSD with the buck gate driver $ISL6207$. The buck VRMs operate with: $V_{\text{in}} = 12$ V, $V_o = 1.3$ V, $f_{\text{sw}} = 1$ MHz, and $L_f = 200$ nH. It should be noted that the values of the driver peak current and the driver inductance of the gate drivers are optimally designed for the efficiency comparison, as illustrated in Fig. 11 and in [39].

According to Fig. 21, the efficiency of the proposed CSD is improved by 4.4% compared to the one for the CSD proposed in [39], and it increase by 7% compared to the one for the VSD at 30 A output current. This is due to the fact that the buck VRM with the proposed gate driver has lower turn-OFF switching losses compared to the buck VRM with the CSD in [39], and the VSD.

The efficiency comparison of a buck VRMs driven by the proposed CSD with different inductance values are presented in Fig. 22 to confirm the optimal design of the proposed CSD. As can be observed, the efficiency of buck VRM with CSD inductance of 160 nH is highest at 20 A load.

VI. Conclusion

This article introduced a new discontinuous CSD with the ability to fully overcome the current diversion problem during the turn-OFF transitions, due to its performance as an ideal current-source. The presented gate driver uses minimum number of extra components, and also has attractive features such as gate energy recovery, high $C\frac{dv}{dt}$ immunity, and low circulating losses. Turn-OFF losses of the HS MOSFET of the buck VRM driven by the proposed gate driver is lower than most of existing CSDs [12], [13], [21]–[27], [29], [35]–[39], whereas its turn-ON losses are similar to the ones for the CSDs with current diversion problem. This article has also presented an optimal design for the reduction of turn-OFF losses and the gate drive losses. In order to verify the theoretical analysis, three 12 V buck VRM prototypes with the proposed gate driver, with the CSD in [39], and with the VSD have been implemented. It has been shown that the efficiency of the buck VRM with the proposed gate driver is significantly improved compared to the ones for the CSD in [39] and the VSD.

References

[1] Z. Zhang, "MOSFET current source gate drivers and topologies for high efficiency and high frequency voltage regulator modules," Ph.D. dissertation, Queen's University, Kingston, ON, Canada, Apr. 2009.

[2] Z. Zhang, W. Eberle, Y. Liu, and P. C. Sen, "A nonisolated ZVS asymmetrical buck voltage regulator module with direct energy transfer," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3096–3105, Aug. 2009.

[3] K. Jin, L. Gu, W. Cao, X. Ruan, and M. Xu, "Nonisolated flyback switching capacitor voltage regulator," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3714–3722, Aug. 2013.

[4] Z. Zhang, E. Meyer, Y. Liu, and P. C. Sen, "A 1-MHz, 12-V ZVS nonisolated full-bridge VRM with gate energy recovery," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 624–636, Mar. 2010.

[5] C. Fei, M. H. Ahmed, F. C. Lee, and Q. Li, "Two-stage 48V-12V/6V-1.8V voltage regulator module with dynamic bus voltage control for light-load efficiency improvement," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5628–5636, Jul. 2017.

[6] T. Lopez and E. Alarcón, "Power MOSFET technology roadmap toward high power density voltage regulators for next-generation computer processors," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 2193–2203, Apr. 2012.

[7] J. Sun, "Investigation of alternative power architectures for CPU voltage regulators," Ph.D. dissertation, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, Nov. 2008.

[8] D. C. Reusch, "High frequency, high power density integrated point of load and bus converters," Ph.D. dissertation, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, Apr. 2012.

[9] Y. Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical loss model of power MOSFET," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 310–319, Mar. 2006.

[10] W. Eberle, Z. Zhang, Y. Liu, and P. C. Sen, "A practical switching loss model for buck voltage regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 700–713, Mar. 2009.

[11] X. Zhou, Z. Liang, and A. Huang, "A high-dynamic range current source gate driver for switching-loss reduction of high-side switch in buck converter," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1439–1443, Jun. 2010.

[12] J. Fu, Z. Zhang, Y. Liu, P. C. Sen, and L. Ge, "A new high efficiency current source driver with bipolar gate voltage," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 985–997, Feb. 2012.

[13] J. Fu, Z. Zhang, Y. Liu, and P. C. Sen, "MOSFET switching loss model and optimal design of a current source driver considering the current diversion problem," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 998–1012, Feb. 2012.

[14] H. L. N. Wiegman, "A resonant pulse gate drive for high frequency applications," in *Proc. 7th Annu. Appl. Power Electron. Conf. Expo.*, Feb. 1992, pp. 738–743.

[15] I. D. de Vries, "A resonant power MOSFET/IGBT gate driver," in *Proc. APEC. 17th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2002, vol. 1, pp. 179–185.

[16] Y. Chen, F. C. Lee, L. Amoroso, and H.-P. Wu, "A resonant MOSFET gate driver with efficient energy recovery," *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 470–477, Mar. 2004.

[17] M. M. Swamy, T. Kume, and N. Takada, "An efficient resonant gate-drive scheme for high-frequency applications," *IEEE Trans. Ind. Appl.*, vol. 48, no. 4, pp. 1418–1431, Jul. 2012.

[18] H. Fujita, "A resonant gate-drive circuit capable of high-frequency and high-efficiency operation," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 962–969, Apr. 2010.

[19] H. Fujita, "A resonant gate-drive circuit with optically isolated control signal and power supply for fast-switching and high-voltage power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5423–5430, Nov. 2013.
[20] Z. Zhang, W. Cai, and P. Xu, "Adaptive continuous current source drivers to achieve efficiency improvement in wide load range," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2011, pp. 1196–1201.
[21] W. Eberle, Z. Zhang, Y. Liu, and P. C. Sen, "A high efficiency synchronous buck VRM with current source gate driver," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2007, pp. 21–27.
[22] Z. Zhang, W. Eberle, Z. Yang, Y. Liu, and P. C. Sen, "Optimal design of current source gate driver for a buck voltage regulator based on a new analytical loss model," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2007, pp. 1556–1562.
[23] I. A. Mashhadi, E. Ovaysi, E. Adib, and H. Farzanehfard, "A novel current-source gate driver for ultra-low-voltage applications," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 4796–4804, Aug. 2016.
[24] Z. Zhang, W. Eberle, P. Lin, Y. Liu, and P. C. Sen, "A 1-MHz high-efficiency 12-V buck voltage regulator with a new current-source gate driver," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2817–2827, Nov. 2008.
[25] Y. Ren, M. Xu, Y. Meng, and F. C. Lee, "12V VR efficiency improvement based on two-stage approach and a novel gate driver," in *Proc. IEEE 36th Power Electron. Spec. Conf.*, Jun. 2005, pp. 2635–2641.
[26] Z. Zhang and Y.-F. Liu, "Current-source gate driver," U.S. Patent 8 085 083B2, 2011.
[27] W. Eberle, Y. Liu, and P. C. Sen, "A new resonant gate-drive circuit with efficient energy recovery and low conduction loss," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 2213–2221, May 2008.
[28] R. Chen and F. Z. Peng, "A high-performance resonant gate-drive circuit for MOSFETs and IGBTs," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4366–4373, Aug. 2014.
[29] Z. Zhang, J. Fu, Y. Liu, and P. C. Sen, "Discontinuous-current-source drivers for high-frequency power MOSFETs," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1863–1876, Jul. 2010.
[30] Z. Zhang, J. Fu, Y. Liu, and P. C. Sen, "Comparison of continuous and discontinuous current source drivers for high frequency applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2010, pp. 2434–2440.
[31] K. Yao, M. Ye, M. Xu, and F. C. Lee, "Tapped-inductor buck converter for high-step-down DC-DC conversion," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 775–780, Jul. 2005.
[32] J. Wei and F. C. Lee, "Two novel soft-switched, high frequency, high-efficiency, non-isolated voltage regulators-the phase-shift buck converter and the matrix-transformer phase-buck converter," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 292–299, Mar. 2005.
[33] J. Zhou, M. Xu, J. Sun, and F. C. Lee, "A self-driven soft-switching voltage regulator for future microprocessors," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 806–814, Jul. 2005.
[34] X. Zhou, "Resonant gate driver design for high efficiency switching power converter," Ph.D. dissertation, North Carolina State University, Raleigh, NC, USA, May 2010.
[35] Z. Zhang, C. Xu, and Y. Liu, "A digital adaptive discontinuous current source driver for high-frequency interleaved boost PFC converters," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1298–1310, Mar. 2014.
[36] I. A. Mashhadi, R. R. Khorasani, E. Adib, and H. Farzanehfard, "A discontinuous current-source gate driver with gate voltage boosting capability," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5333–5341, Jul. 2017.
[37] W. Eberle, Z. Zhang, Y. Liu, and P. C. Sen, "A current source gate driver achieving switching loss savings and gate energy recovery at 1-MHz," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 678–691, Mar. 2008.
[38] Z. Zhang, J. Fu, Y. Liu, and P. C. Sen, "Adaptive current source drivers for efficiency optimization of high-frequency synchronous buck converters," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2462–2470, May 2012.
[39] I. A. Mashhadi, B. Soleymani, E. Adib, and H. Farzanehfard, "A dual-switch discontinuous current-source gate driver for a narrow on-time buck converter," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4215–4223, May 2018.
[40] J. Wang, H. S. Chung, and R. T. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 573–590, Jan. 2013.
[41] R. Li, J. Zhu, and M. Xie, "An improved analysis of dv/dt-induced low-side MOSFET false turn on in synchronous buck converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2018, pp. 2227–2234.
[42] *Efficiency of Buck Converter*, Application note from ROHM, USA, December 2016. [Online]. Available: www.rohm.com/
[43] J. Klein, *Synchronous Buck MOSFET Loss Calculations With Excel Model*, Applications note AN-6005, Fairchild Semiconductor, USA, Apr. 2006. [Online]. Available: www.fairchildsemi.com
[44] D. Christen and J. Biela, "Analytical switching loss modeling based on datasheet parameters for MOSFETs in a half-bridge," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3700–3710, Apr. 2019.
[45] N. Garcia, *Determining Inductor Power Losses*, Application note from Coil Craft, USA, 2005. [Online]. Available: www.coilcraft.com/appnotes
[46] M. Pavier *et al.*, *Understanding the Effects of Power MOSFET Package Parasitics on VRM Circuit Efficiency at Frequencies Above 1 MHz*, International Rectifier Application Note, USA, 2003. [Online]. Available: www.irf.com
[47] J. Lee, "Package parasitics influence efficiency," *Power Electron. Technol. Mag.*, vol. 31, pp. 14–21, Nov. 2005.

Iman Abdali Mashhadi (S'16) received the M.Sc. degree in electrical engineering from the Isfahan University of Technology, Isfahan, Iran, in 2017. He is currently working toward the Ph.D. degree in electrical engineering with Queen's University, Kingston, ON, Canada.

He was with the University of Calgary, Calgary, AB, Canada, for more than one year. His current research interests include dc–dc converters, wireless power-transfer circuits for biomedical implants, and novel gate drive techniques.

Mr. Mashhadi was the recipient of the Outstanding Master Thesis Award from IEEE Iran section, 2018.

Majid Pahlevani (S'07–M'12–SM'14) received the Ph.D. degree from Queen's University, Kingston, ON, Canada, in 2012.

He is currently an Assistant Professor with the Department of Electrical and Computer Engineering, Queen's University. Prior to Queen's, he was an Assistant Professor with the University of Calgary, Calgary, AB, Canada, from 2016 to 2019. He was also the Chief R&D Engineer and then the VP of Technology with SPARQ Systems Inc., from 2011 to 2016. At SPARQ, he invented multiple innovative power circuitry and digital control techniques for SPARQ's main product, QUAD microinverter. He collaborated with Freescale Semiconductor Inc., where he was the Leader of a research team working on the design and implementation of the power converters for a pure electric vehicle from 2008 to 2011. He has conducted more than 20 industrial projects in renewable energy systems, energy storage systems, electric vehicles, and LED lighting. He has authored more than 130 journals and conference proceeding papers and is the holder of 40 U.S. patents (issued/pending).

Dr. Pahlevani is the Associate Editor for the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS and a Member of the IEEE Power Electronics Society. He is also the recipient of numerous awards such as the Early Research Excellence Award from Alberta, Canada, Engineering and Applied Sciences Outstanding Thesis Award from Queen's University, Research Excellence Award from IEEE Canada, and Distinguished Research Award from the University of Calgary.