A Constant On-Time Buck Converter With Analog Time-Optimized On-Time Control

Yu-Chen Li, Ching-Jan Chen, *Senior Member, IEEE*, and Chieh-Ju Tsai

***Abstract*—A constant on-time buck converter with analog time-optimized on-time control (OTC) is proposed to achieve fast load-current step-up transient response for high slew-rate loads. The proposed control first implements a constant on-time converter embedded with analog time-optimized OTC and solves the prior art issues such as poor light-load efficiency, high quiescent current, and the dependence on the power stage parameters of OTC. The body diode control, which minimizes the overshoot with simple logic and capacitor-current sensor, is proposed for load current step-down. The proposed control was implemented into an integrated circuit using 0.18 μm CMOS process with a chip area of 1.423 mm^2, where OTC only occupies 0.054 mm^2. The simulation results show 51.3% and 55.5% reductions of voltage deviation after enabling the proposed control functions at load step-up and step-down, respectively. Measurement results show that the undershoot of output voltage improves 52.4% after enabling OTC for a 0.84 A load step-up.**

***Index Terms*—Buck converter, constant on-time (COT) control, load transient response, time-optimized on-time control (OTC).**

I. Introduction

BUCK converters with ripple-based constant on-time (COT) controls are widely used for high slew-rate loads due to the advantages of fast transient response and high light-load efficiency [1]–[5]. For high slew-rate loads such as system-on-chip (SoC) and the microprocessor, the ripple-based COT controls achieve fast transient response because the output voltage is directly sensed back for modulation without passing through an error amplifier (EA). Beside, COT control has a relatively constant switching frequency at continuous conduction mode and scaled switching frequency with load current at discontinuous conduction mode, which achieves high light-load efficiency. However, a ripple-based COT controlled buck converter has a stability issue with ceramic output capacitor [1].

Ripple-based COT control with virtual inductor current (VIC), as shown in Fig. 1, is one of the ripple-based COT control schemes to solve the stability issue; however, COT controls still have the potential to further improve transient response [2], [3]. The output capacitor is modeled as a capacitor C_o, an equivalent series resistor (ESR), and an equivalent series inductor (ESL). The ceramic capacitor is chosen as an output capacitor due to its small size, but the low ESR value of ceramic capacitor might cause subharmonics oscillation. Therefore, VIC is added for stability and is obtained by integrating the phase voltage, V_X, through the "$R_{VIC}C_{VIC}$ integrator" and removing the dc value by using the low pass filter, $R_{LPF}C_{LPF}$ as will be seen in Fig. 3 [3]. When the two input signals of the pulsewidth modulation (PWM) comparator, CMP_{PWM}, intersect, a COT is generated. However, minimum off-time restricts the maximum duty cycle and causes severer V_O undershoot at load step-up. Beside, there is usually a tradeoff between the stability and load transient response of ramp-compensated ripple-based COT control [6]. That is, adding the compensated ramp to output voltage V_O for stability slows down the transient response. Finally, the problem of ringing back is common after V_O undershoot is recovered.

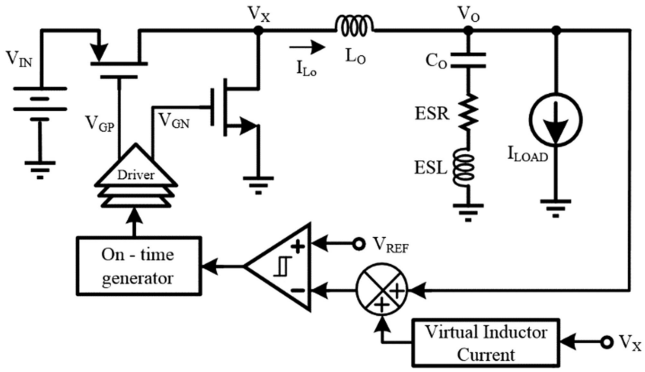

Fig. 1. Simplified circuit diagram of the ripple-based COT control with the VIC.

Another control scheme to solve instability was reported by inducing the concept of VIC compensation to RBCOT control [4]–[7]. With this VIC ripple compensation, the control-to-output transfer function is more straightforward to analyze because poles and zeros can be readily separated and simplified. Beside, no current sensor is required. However, RBCOT control with VIC may not achieve optimal load transient response design under the wide-range operations for power management integrated circuit (PMIC) applications. Take Intel APL PMIC as an instance [13]. The buck converter must support dynamic voltage scaling, i.e., the output voltage varies from 0.5 to 1.45 V depending on its definition of modes. The output load is from 0 to 20 A. Hence, the output power is from 0 to approximate

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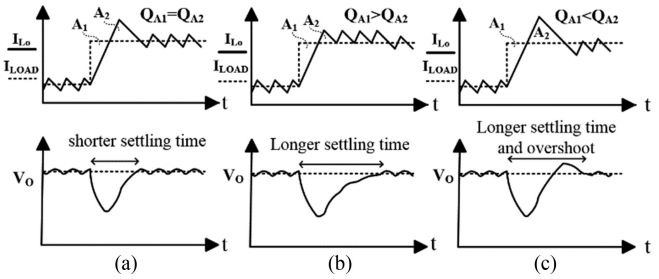

Fig. 2. Conceptual waveform of step-up load transient response. (a) With time-optimized control. (b) Without time-optimized control and $Q_{\rm A1} > Q_{\rm A2}$. (c) Without time-optimized control and $Q_{\rm A1} < Q_{\rm A2}$.

30 W. Plus, the input voltage also varies from 5 to 21 V. Under such a wide-range operation, a large ramp compensation is indispensable to avoid instability at worst case. Generally speaking, in such applications, the ripple compensation may not be the optimal design under different working conditions, since the transfer function varies with different operating points, especially for quality factor at half switching frequency in COT schemes.

To further improve the transient response of the ripple-based COT, some on-time extension methods are proposed as high slew-rate load current happens. The DCS control [7] was proposed to not only have the seamless transition between the power-save mode and the PWM mode but also directly sense the output voltage to modulate the on-time as the load current changes. However, the on-time is not turned ON immediately at load current step-up because the extended on-time in DCS is triggered by the signal when the output voltage is lower than a defined threshold. Therefore, the reduction of undershoot is not obvious. Ramp pulse modulation [8], dynamic on-time current mode [9], [10], and variable on-time control (OTC) [11], [12] also extend on-time at transient happening. However, the extended on-time of these techniques is not defined, which might cause ringing problem or cannot achieve the optimized transient response if the control loop is not well designed. Moreover, the transient response of these techniques depends on the response of the comp voltage produced by the EA, which is restricted by the closed-loop bandwidth and phase margin.

Time-optimized controls were proposed to achieve the theoretically fastest transient response [13]–[18]. The time-optimized control is only activated after a transient event is detected and go back to the original control scheme after that. The main concept is to calculate an extended on-time as load transient happens to achieve minimum settling time and undershoot/overshoot without ringing back. Fig. 2(a) shows the time-domain waveforms of an optimized light-to-heavy load transient response. On-time is instantly turned ON as load transient happens and keeps providing the power to output after the inductor current exceeds the load current. Thus, the decreased charge $Q_{\rm A1}$ on the output capacitor is minimized, which results in a minimal undershoot. Then, on-time is turned OFF at the well-controlled time to ensure that the area of $\rm A_1$ and $\rm A_2$ are equal, which implies that the excess charge, $Q_{\rm A2}$, is used to compensate the decreased charge, $Q_{\rm A1}$. Thus, the settling time will be minimized. By doing this, the output capacitor charge is balanced when the load current steps up. Fig. 2(b) and (c) shows that if the extended on-time is shorter or longer, respectively. With the time-optimized control, minimal undershoot, minimal settling time, and nonovershoot are achieved.

Various time-optimized controls were proposed; however, they have some drawbacks. Beside, there is no COT control embedded with time-optimized control based on the author's knowledge. Time-optimized controls achieve optimized load-transient response [13]–[18]. However, the time-optimized control proposed in [13] is digitally realized by a field-programmable gate array with four off-chip discrete analog-to-digital converters (ADC), which require higher cost and larger board area. Thus, the analog implementations of time-optimized control were proposed [13]–[16]. However, the proposed hysteretic buck converter in [13] has poor light-load efficiency compared to the COT control. Beside, the derived time-optimized equation of hysteretic threshold is affected by the power stage's inductor, capacitor, and process mismatch. In [15] and [16], the time-optimized control is implemented in a voltage-mode buck converter, which also has poor efficiency at light load. Beside, the extended on-time is calculated by catching the information from the output capacitor current sensor and using a time-to-voltage converter and a square-rooting (SQR) circuit. However, the square root implemented by an SQR circuit is difficult and complicated to implement precisely in analog circuits.

Hence, a COT control embedded with an analog time-optimized OTC is proposed and fabricated in an integrated circuit (IC) to achieve fast transient response for COT control and solve the aforementioned issues. The proposed OTC is compact and independent of the power stage's inductor and capacitor variation. Beside, the OTC could be applied to any type of COT control, which is widely used to improve the light-load efficiency. The proposed control is illustrated in Section II. Section III shows the transistor level circuit implementation. Section IV shows the measurement results, and Section V concludes this article.

II. Proposed Control for COT Buck Converter

Fig. 3 shows the circuit diagram of a COT buck converter with proposed control. VIC circuit improves the system stability at ceramic capacitor by using a current-type adder (CTA) to add $V_{\rm O}$, $V_{\rm ACDC}$ together and subtract $V_{\rm DC}$. EA regulates the output voltage $V_{\rm O}$ to the reference voltage $V_{\rm REF}$ by generating the compensation voltage $V_{\rm C}$. The proposed OTC contains a CTA, $\Delta V_{\rm H}$ generator, threshold detector and logic, and capacitor-current sensor. The timing information of the load current step-up $V_{\rm LCSU}$ and passing zero of output capacitor current $V_{\rm PZ}$ are needed for the proposed OTC. The OTC circuit generates $V_{\rm H,F}$ as the threshold of the COT generator. Body diode control (BDC) is also proposed to improve transient response at load step-down. BDC is implemented by adding an AND logic before the driver and using the information of load current step-down $V_{\rm LCSD}$ generated from the threshold detector and logic. The power stage specifications for the implemented IC are $V_{\rm IN} = 3.3$ V,

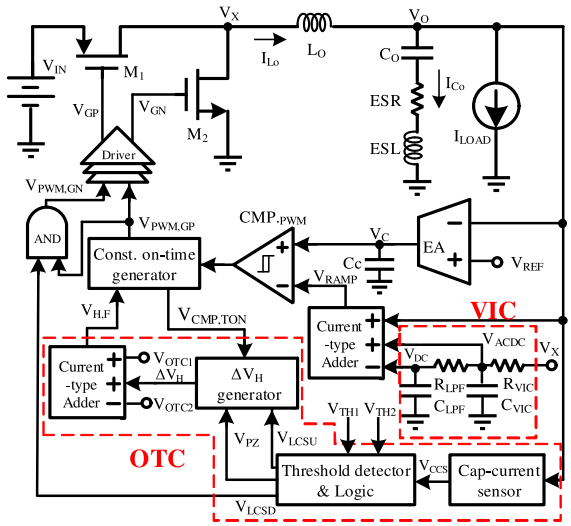

Fig. 3. Circuit diagram of the COT buck converter with proposed control.

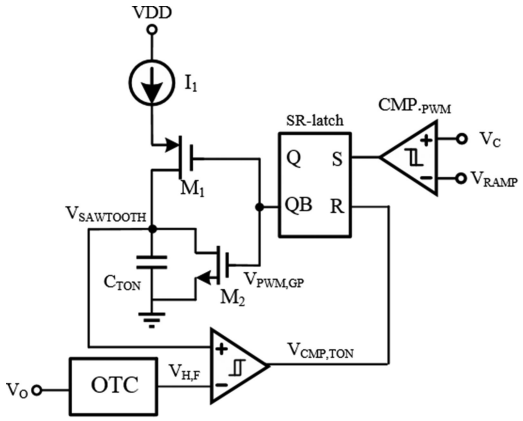

Fig. 4. Simplified circuit diagram of the COT generator with the proposed transient optimized OTC.

$V_{\rm O} = 1$ V, $L_{\rm O} = 1$ μH, $C_{\rm O} = 4.7$ μF, ESR $= 5.4$ mΩ, ESL $=$ 330 pH, and switching frequency $f_{\rm sw} = 1.5$ MHz.

A. Time-Optimized OTC for Load Current Step-Up

The proposed OTC, as shown in Fig. 4, is embedded within the COT generator and achieves the time-optimized control with minimum undershoot and settling time at load current step-up. As Fig. 4 shows, the circuit of proposed OTC is similar to the conventional COT generator except for the variation of threshold voltage, $V_{\rm H,F}$. When the two input signals of $\rm CMP_{PWM}$ intersect, an on-time is initiated and a sawtooth voltage $V_{\rm SAWTOOTH}$ starts to rise due to a current I_1 charging a capacitor $C_{\rm TON}$. When $V_{\rm SAWTOOTH}$ reaches $V_{\rm H,F}$, on-time is terminated. Unlike the fixed voltage $V_{\rm H,F}$ in the conventional circuit, the proposed OTC increases $V_{\rm H,F}$ with an appropriate voltage $\Delta V_{\rm H}$ as load transient steps up. Thus, the on-time is extended to achieve the time-optimized control.

Fig. 5 shows the conceptual load transient waveform of COT buck converter with the proposed OTC. The t_1 is the time from

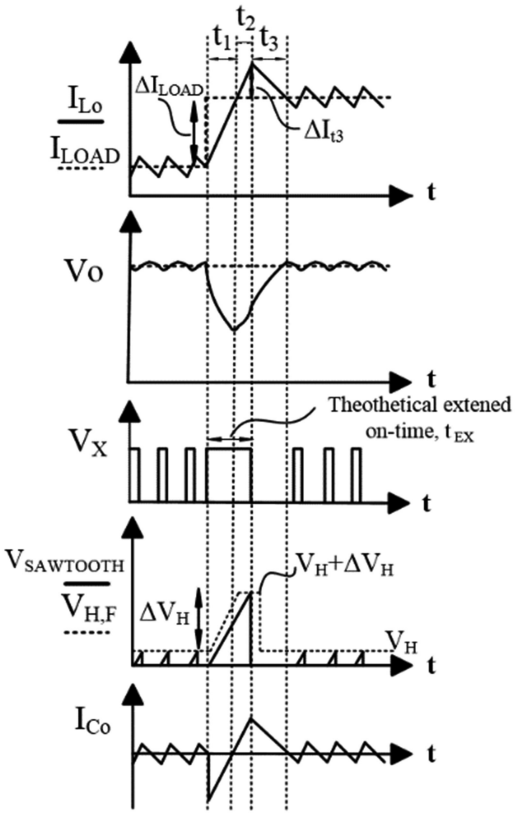

Fig. 5. Conceptual load transient waveform of the COT buck converter with the proposed OTC.

the load current step-up to the point of passing zero of output capacitor current $I_{\rm Co}$, which means that the inductor current is equal to the load current. The t_2 is followed by t_1 and stops at the end of extended on-time $t_{\rm EX}$. Finally, t_3 is followed by t_2 and ends at the point of passing zero again of the output capacitor current. $V_{\rm X}$ shows the duty cycle of the COT buck converter. $V_{\rm H,F}$ has a constant rising slope before reaching the calculated value of $(V_{\rm H} + \Delta V_{\rm H})$ during load current step-up. This is because the $V_{\rm H,F}$ is implemented by a current charging a capacitor, which will be illustrated in Section III. To achieve the concept mentioned above with time-optimized control, the derivation of $\Delta V_{\rm H}$ is needed.

The derivation of $\Delta V_{\rm H}$ is shown as follows. A high slew-rate load step, neglectable steady-state output voltage ripple, and inductor current ripple are assumed for the calculation of the time-optimized control, as shown in Fig. 5. The relationship between t_2 and t_3 is derived as follows by the inductor current slope equation and Fig. 5

$$\Delta I_{t3} = \frac{V_{\rm IN} - V_O}{L_O} \cdot t_2 = \frac{V_O}{L_O} \cdot t_3. \tag{1}$$

Based on the output capacitor's charge balance and $\rm A_1 = A_2$ from Fig. 2, the following equation can be derived

$$\frac{1}{2} \cdot \Delta I_{\rm LOAD} \cdot t_1 = \frac{1}{2} \cdot \Delta I_{t3} \cdot (t_2 + t_3). \tag{2}$$

Substituting ΔI_{LOAD} and ΔI_{t3} by inductor current slope equation, (2) is modified as

$$\left(\frac{V_{\mathrm{IN}}-V_O}{L}\cdot t_1\right)\cdot t_1=\left(\frac{V_O}{L}\cdot t_3\right)\cdot(t_2+t_3)\,. \tag{3}$$

The relationship between t_1 and t_2 is derived by substituting t_3 into (3) to t_2 into (1) and is expressed as

$$t_2=\left(\sqrt{\frac{V_O}{V_{\mathrm{IN}}}}\right)\cdot t_1. \tag{4}$$

Inductor current slope equation, as shown in (5) is used to substitute t_1 into (4). Thus, t_2 is expressed as (6).

$$t_1=\frac{L_O}{V_{\mathrm{IN}}-V_O}\cdot\Delta I_{\mathrm{LOAD}} \tag{5}$$

$$t_2=\frac{L_O}{V_{\mathrm{IN}}-V_O}\left(\sqrt{\frac{V_O}{V_{\mathrm{IN}}}}\right)\cdot\Delta I_{\mathrm{LOAD}}. \tag{6}$$

Therefore, the theoretical extended on-time $t_{\mathrm{EX,theory}}$, which is equal to t_1 plus t_2, is expressed as

$$t_{\mathrm{EX,theory}}=\left(1+\sqrt{\frac{V_O}{V_{\mathrm{IN}}}}\right)\cdot\frac{L_O}{(V_{\mathrm{IN}}-V_O)}\cdot\Delta I_{\mathrm{LOAD}}. \tag{7}$$

Then, the key equation of added threshold voltage, $\Delta \mathrm{V_H}$, of the on-time generator is calculated based on the idea that ΔV_{H} needs to be generated to let V_{SAWTOOTH} meets $V_{\mathrm{H,F}}$ at the end of t_2 to achieve the time-optimized control. Thus, $V_{\mathrm{H,F}}$ is expressed as

$$V_{H,F}=V_H+\Delta V_H=\frac{I_1\cdot(t_1+t_2)}{C_{\mathrm{TON}}}. \tag{8}$$

Finally, two types of ΔV_{H} are derived as follows by substituting the different definition of t_2 from (4) and (6), respectively, into (8)

$$\Delta V_H=\frac{I_1}{C_{\mathrm{TON}}}\cdot\left(1+\sqrt{\frac{V_O}{V_{\mathrm{IN}}}}\right)\cdot t_1-V_H \tag{9}$$

$$\Delta V_H=\frac{I_1\cdot L_O}{C_{\mathrm{TON}}(V_{\mathrm{IN}}-V_O)}\cdot\left(1+\sqrt{\frac{V_O}{V_{\mathrm{IN}}}}\right)\cdot\Delta I_{\mathrm{LOAD}}-V_H. \tag{10}$$

In the proposed control, (9) is used to implement the time-optimized control because the derived equation is independent to the power stage's inductor and capacitor. This implies that the proposed control does not affected by the mismatch of power stage. The capacitor-current sensor is used to capture t_1 in (9) and will be introduced in Section III. In (9), a square root function appeared, which is a challenge to fulfill it precisely in the CMOS process. Therefore, a current digital-to-analog (I-DAC) implementation is proposed and elaborated in Section III to accomplish (9). Although the value of ΔI_{LOAD} in (10) could be calculated immediately when load transient happens, inductor value affects the accuracy of extended on-time.

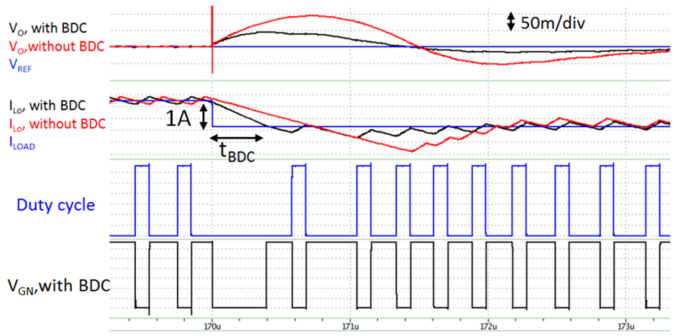

Fig. 6. Simulated transient response of the COT buck converter with and without proposed BDC.

B. BDC For Load Current Step-Down

BDC is proposed to reduce the overshoot when the load current steps down. As shown in Fig. 3, the power MOSFET, M_2, is turned OFF using an AND logic controlled by the V_{LCSD} signal during load current step-down. Thus, the current passes through the body diode of M_2 and generates a diode forward voltage drop V_{D} across M_2. Then, the inductor current falling slope at load current step-down is higher and can be expressed as

$$-V_D-V_O=L_O\frac{di_{Lo}}{dt}. \tag{11}$$

By implementing BDC control, the slope of the inductor current is deeper. V_{LCSD} is logic zero from the load current step-down to the point of passing zero of the output capacitor current by using the capacitor-current sensor and threshold detector and logic. The implementation of V_{LCSD} will be illustrated in Section III. Compared to the detecting output voltage and turning OFF the M_2 if the output voltage exceeds a certain threshold, M_2 is turned OFF immediately as load transient happens with the proposed technique, which is more effective to minimize the overshoot.

Fig. 6 shows the MOSFET-level simulated transient response of the COT buck converter with and without the proposed BDC. t_{BDC} is the time period that the BDC is working. The simulation result shows a 55.5% reduction of voltage deviation at the load step-down after enabling the proposed BDC. It can also be seen that the proposed control achieves deeper inductor current slope and reduced settling time by turning OFF M_2 during t_{BDC}.

C. State Diagram and Detection Mechanism

Figs. 7–9 show the conceptual transient response waveform, the state diagram of the proposed control, and the circuit diagram of the threshold detector and logic block, respectively. The proposed control includes three modes. First, the control starts with linear control, as shown in Fig. 8, which means V_{C} and V_{RAMP} in Fig. 3 decides the duty as the conventional ripple-based COT control. The operation state changes to the time-optimized OTC as V_{LCSU} is logic high and gets back to the state of linear control as $V_{\mathrm{CMP,TON}}$ is logic high. In Fig. 9, V_{LCSU} is the output of a comparator and is logic high when V_{CCS}

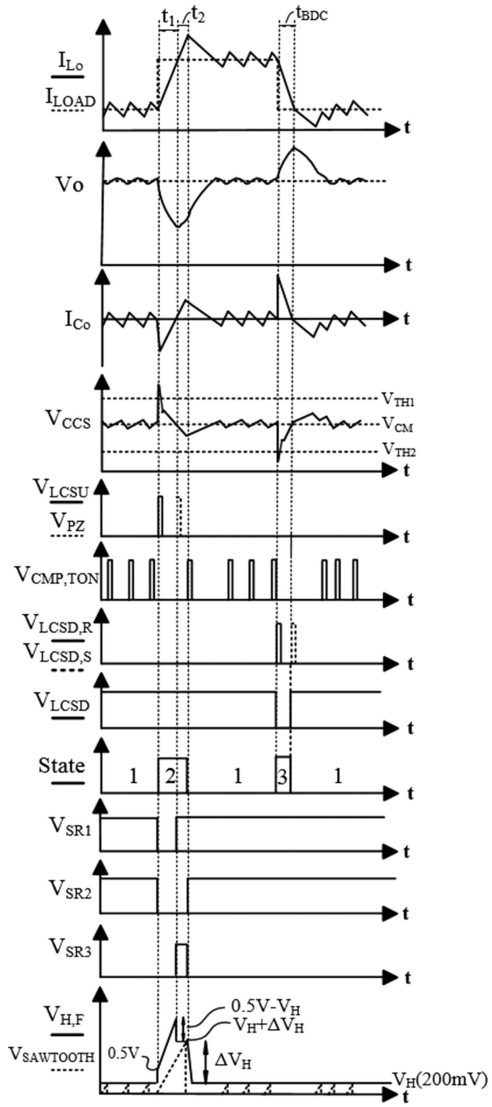

Fig. 7. Conceptual transient response waveform of the OTC.

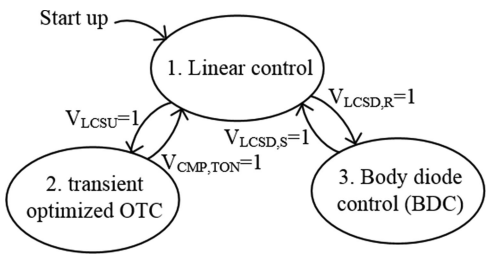

Fig. 8. State diagram of the buck converter with the proposed control.

is larger than the defined threshold voltage, V_{TH1}. This means the load current step-up condition happens. V_{CCS} is the output of the capacitor-current sensor which will be introduced in Section III. $V_{\mathrm{CMP,TON}}$ in Fig. 4 is logic high when V_{SAWTOOTH} reaches $V_{\mathrm{H,F}}$, which means the on-time finishes. V_{PZ} is needed for the proposed OTC to obtain the properly extended on-time. V_{PZ} is set to logic high when V_{CCS} equals the common-mode voltage

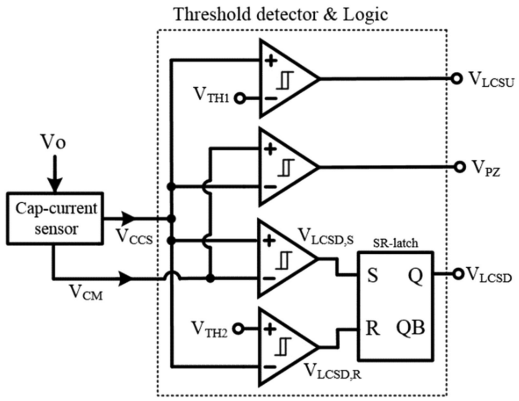

Fig. 9. Circuit diagram of the threshold detector and logic block of Fig. 3.

V_{CM} of capacitor-current sensor which means the I_{Co} is zero. The detail operation and the waveforms of OTC circuit will be introduced in Section III.

On the other hand, the operation state changes to the BDC as $V_{\mathrm{LCSD,R}}$ is logic high and gets back to linear control as $V_{\mathrm{LCSD,S}}$ is logic high. $V_{\mathrm{LCSD,R}}$, as shown in Figs. 7 and 9, is the output of a comparator and is logic high when V_{CCS} is smaller than the defined threshold voltage, V_{TH2}, which means the load current step-down condition happens. $V_{\mathrm{LCSD,S}}$ is also the output of a comparator and is logic high when V_{CCS} exceeds V_{CM}, which implies the output capacitor current goes from a positive value to a negative value. In Fig. 9, an SR-latch is used to define V_{LCSD} used to turn OFF the M_2 by using an AND logic, as shown in Fig. 3. In the proposed circuit, a slight ringing back might happen when operation mode changes from the OTC to the linear control. To overcome this problem, transient-hold technique could be implemented to hold compensator output voltage V_{C} during the OTC mode [14].

III. Circuit Implementation

A. Implementation of Time-Optimized OTC

To implement the proposed $V_{\mathrm{H,F}}$, (9) is rewritten as

$$V_{H,F} = V_H + \Delta V_H = V_H + \frac{I_1}{C_{\mathrm{TON}}} \cdot \left(1 + \sqrt{\frac{V_O}{V_{\mathrm{IN}}}}\right) \cdot t_1 - V_H. \quad (12)$$

$V_{\mathrm{H,F}}$ in (12) is used to generate the correct on-time for the time-optimized OTC. Three terms in the right part of (12) are added by the CTA circuit which will be introduced in Section III-C. The middle part of (12) is taken apart into three elements, which contains the capacitance, C_{TON}, the time duration, t_1, and a current. The value of the current is expressed as

$$I_2 = I_1 \cdot \left(1 + \sqrt{\frac{V_O}{V_{\mathrm{IN}}}}\right). \quad (13)$$

Thus, (12) is rewritten as

$$V_{H,F} = V_H + \frac{I_2}{C_{\mathrm{TON}}} \cdot t_1 - V_H. \quad (14)$$

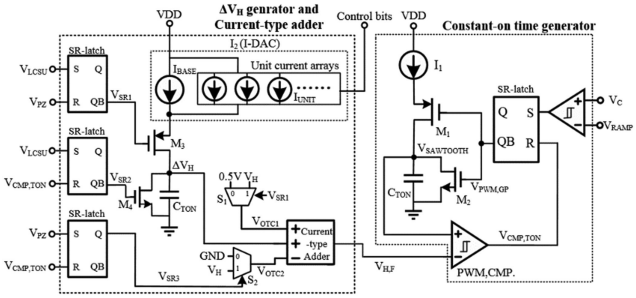

Fig. 10. Circuit diagram of the $\Delta V_{\rm H}$ generator embedded with COT generator.

Fig. 10 shows the circuit diagram of the $\Delta V_{\rm H}$ generator embedded with a COT generator. The implementation of the middle part in (12) is implemented by a capacitor, $C_{\rm TON}$, charged by the current, I_2, from the time of transient happening detected by $V_{\rm LCSU}$ to the time instant of passing zero of the output capacitor current detected by $V_{\rm PZ}$, which is known as t_1. That is, the middle part of (12) is implemented simply by a circuit similar to the conventional on-time generator, which is easy to implement in IC. M_3 is turned ON to let current source I_2 charge $C_{\rm TON}$ during the time duration t_1 defined by $V_{\rm LCSU}$ and $V_{\rm PZ}$. M_4 is turned OFF at the load current step-up until $V_{\rm SAWTOOTH}$ reaches $V_{\rm H,F}$. Then, M_4 is turned ON to tie $\Delta V_{\rm H}$ to the ground, which means the OTC mode is finished and $V_{\rm H,F}$ resets to the nominal voltage $V_{\rm H}$ to obtain COT in linear mode.

Fig. 7 shows the detailed waveform of $V_{\rm SR1}$, $V_{\rm SR2}$, $V_{\rm SR3}$, and $V_{\rm H,F}$. Switch S_1 is used to change the threshold voltage from $V_{\rm H}$ to 0.5 V immediately as load transient happens. Therefore, a larger noise margin between $V_{\rm H,F}$ and $V_{\rm SAWTOOTH}$ is achieved to prevent comparator mistriggering before $V_{\rm H,F}$ reaching its final value. Switch S_2 is used to subtract $V_{\rm H}$ when the output capacitor current passes zero to implement the rightmost part of (12).

An I-DAC implementation is proposed to realize current source I_2 in Fig. 10 with the compact circuit and good power efficiency. As shown in (13), square root function appeared, which is a challenge to implement it precisely with the compact circuit in the CMOS process. The value of I_2 is between one and two times I_1 because $V_{\rm IN}$ is larger than $V_{\rm OUT}$ for a buck converter. Therefore, I-DAC is used to realize I_2 in Fig. 10 to achieve (13). Base current $I_{\rm BASE}$ is always connected for $C_{\rm TON}$ charging while the number of unit current source in the unit-current arrays is determined by control bits.

Table I tabulates the examples of I-DAC design for implemented IC. The specifications for the tested chip are $V_{\rm IN} = 3.3$ V, $V_{\rm O} = 1$ V, $I_3 = 31$ μA, $I_{\rm BASE} = 29$ μA, $I_{\rm unit} = 0.2$ μA, and M = 10. In the example of the implemented IC, 16-unit array of an I-DAC is chosen, and $I_{\rm UNIT}$ or least significant bit (LSB) is 0.2 μA. Therefore, the quantization error is 0.2 μA. The latter terms in (15) are neglected if the value is under 0.2 μA. I_3 is the current generated by I-DAC. $I_{\rm BASE}$ is the base current which is always turned ON when the OTC is working. $I_{\rm DIFF}$ is the difference between I_3 and $I_{\rm BASE}$. The value of $I_{\rm DIFF}$ is implemented by unit current arrays, which are controlled by

TABLE I
I-DAC DESIGN EXAMPLES FOR IMPLEMENTED IC

$V_{\rm IN}$ (V)	$V_{\rm O}$ (V)	I_2 (μA)	I_3 (μA)	$I_{\rm DIFF}$ (μA)	$I_{\rm UNIT}$ (μA)	M	Error ($(I_3-I_2)/I_2$)
3.3	0.8	29.847	29.8	0.8	0.2	4	-0.16%
3.3	1	31.009	31	2		10	-0.03%
3.3	1.2	32.061	32	3		15	-0.19%

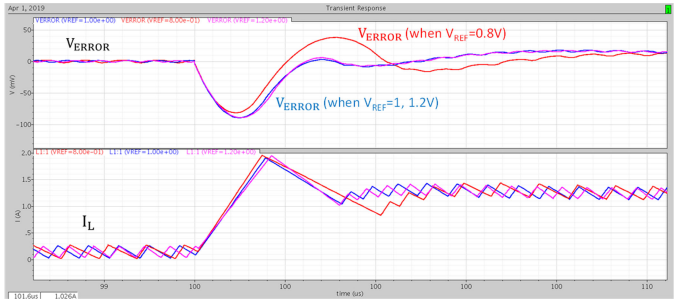

Fig. 11. Simulated load transient responses of COT buck converter at various $V_{\rm O}$ conditions.

control bits. $I_{\rm UNIT}$ is chosen as 0.2 μA in the implemented IC, and M is the number showing that how many units current needs to be turned ON when the OTC is working. According to Table I, the error between (13) and the I-DAC generated I_3 is lower than 0.2%.

In here, a simple and low-cost method to adjust the I-DAC setting for various duty cycle conditions is implemented and verified by simulation. We will analyze the variation of I_2 in (13) due to duty cycle change first. Then, the proposed solution will be implemented and verified by the simulation.

First, we derive the variation of I_2 due to duty cycle change from (13) as follows. It can be seen that the variation of I_2 is relatively more severe at low-duty-cycle condition

$$\frac{\partial\left(\frac{I_2}{I_1}\right)}{\partial D} = \frac{1}{2\sqrt{D}}. \tag{15}$$

Considering the common application of COT control for a modern digital SoC processor supply with input voltage equals 3.3 V and the output voltage ranges from 0.8 to 1.2 V. If the I_2 design is based on $V_{\rm o} = 1$ V condition, the gain of (15) is around 0.9. That is, there is about 5.4% maximum I_2 error deviated from the optimized design for the worst case, where $V_{\rm o}$ changes to 0.8 V.

Fig. 11 shows the simulated load transient responses of COT buck converter at various $V_{\rm o}$ conditions. $V_{\rm ERROR}$ is defined as $(V_{\rm o} - V_{\rm REF})$ with 50 mV/div. Various output voltage conditions (0.8, 1, 1.2 V) are tested by setting different reference voltages. Vin = 3.3 V. I_2 is designed based on $V_{\rm o} = 1$ V condition and is fixed at various $V_{\rm o}$ conditions. It can be seen that the optimized output voltage response is still achieved for $V_{\rm o} = 1.2$ V condition while a ringback exhibits for $V_{\rm o} = 0.8$ V condition. This verifies

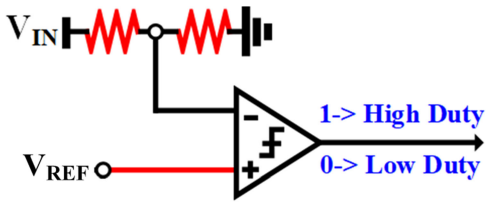

Fig. 12. Proposed low-duty-cycle detection circuit.

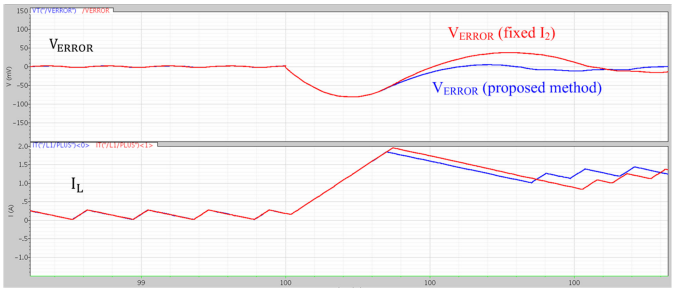

Fig. 13. Simulated load transient responses of the COT buck converter with proposed method ($V_{\rm o} = 0.8$ V).

the theoretical analysis that the variation of I_2 is more severe at low-duty-cycle condition. If this response is acceptable, a fixed I_2 design is enough for this application. If a further improvement in low-duty-cycle condition is required, we proposed a low-cost solution explained in the following paragraph.

A low cost and simple solution to achieve near time optimal response is proposed and verified by simulation. Fig. 12 shows the proposed low-duty-cycle detection circuit to improve the response at low-duty-cycle condition. Input voltage $V_{\rm IN}$ passes through a resistor divider with voltage gain k and compares with $V_{\rm REF}$. The threshold duty cycle $D_{\rm TH}$ can be designed using (16). When the duty cycle is lower than $D_{\rm TH}$, comparator will output low level. Then, the I-DAC array is adjusted to set I_2 to another value for low-duty-cycle condition.

$$D_{\rm TH} = k. \tag{16}$$

The simulated load transient response, as shown in Fig. 13, proves the effectiveness of the proposed method to handle the 0.8 V output voltage scenario. When the low-duty-cycle condition is detected, I_2 is set to the value for $V_{\rm o} = 0.8$ V condition. It is shown that the near time optimal response is achieved for the proposed method. Thus, the proposed solution is robust for commercial application with low cost and simple implementation.

B. Capacitor-Current Sensor

Capacitor-current sensor plays an indispensable and vital role for the proposed time-optimized control. The challenge of the capacitor-current sensor is that it is unable to implement inductor directly in ICs and the sensed signal is distorted if a mismatch of resonant frequency exists between the output capacitor and the capacitor-current sensor. The noninvasive capacitor-current sensing [19]–[21] method was reported, where the sensor was

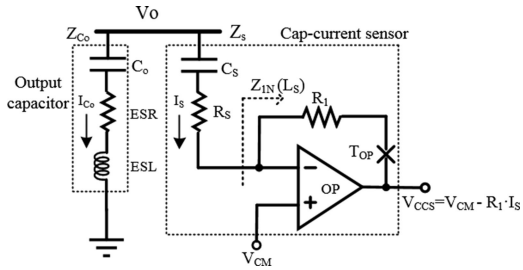

Fig. 14. Capacitor-current sensor.

implemented in the discrete circuit, which increases the board area. Huerta *et al.* [19]–[21] pointed out that the proper operation of the noninvasive capacitor-current sensor strongly depends on the relative position of the converter switching frequency $f_{\rm sw}$ and the output capacitor resonant frequency $f_{\rm res}$. When $f_{\rm sw}$ is smaller than $f_{\rm res}$, the impedance of the output capacitor is capacitive. The capacitor-current sensor should work in the capacitive side as well. That is, $f_{\rm sw}$ is smaller than the resonant frequency of sensor. If the capacitor-current sensor is designed at the inductive side, then $f_{\rm res}$ must always be lower than $f_{\rm sw}$ to guarantee the appropriate operation. That is, we need to confirm the both the output capacitor and the implemented capacitor-current sensor are operated at either inductive side or capacitive side related to the switching frequency. Then, the phase of the capacitor-current sensor is the same as the output capacitor current. This is one of the advantages of the noninvasive capacitor-current sensor because the mismatch of $\pm 10\%$ or more than $\pm 10\%$ is not the reason that the phase of the capacitor-current sensor drastically produces malfunctioning [19]–[21].

This article implements the capacitor-current sensing method of the article presented in [19]–[21] into IC and designs a wide bandwidth operational amplifier (OP) to ensure the proper operation of the capacitor-current sensor. Fig. 14 shows the implementation of the capacitor-current sensor, which is based on a parallel *RLC* network [19]–[21]. The target is to generate a current, $I_{\rm S}$, which is proportional to the actual output capacitor current $I_{\rm Co}$ by scaling the impedances to achieve the following:

$$|Z_S| = k \cdot |Z_{Co}| \tag{17}$$

where $Z_{\rm s}$ is the impedance of the capacitor-current sensor seen from $V_{\rm O}$. In our design, k is chosen as 20 000 to reduce the area and the quiescent power of the capacitor-current sensor. Therefore, $C_{\rm S}$ is chosen as 24 pF and is implemented by the metal–insulator–metal capacitor in the TSMC 0.18 μm CMOS process. $R_{\rm S}$ is made of the P+ poly w/o silicide resistor, and the value is chosen as 1 kΩ on account of the value of k and stability.

The consideration of loop stability is needed for the capacitor-current sensor because two left-half plane poles exist in the loop gain $T_{\rm OP}$ measured by breaking the point marked with $T_{\rm OP}$, as shown in Fig. 14. The OP generates the second pole, and the dominant pole frequency is expressed as follows:

$$f_{P1} = \frac{1}{2\pi \cdot (R_1 + R_S) \cdot C_s}. \tag{18}$$

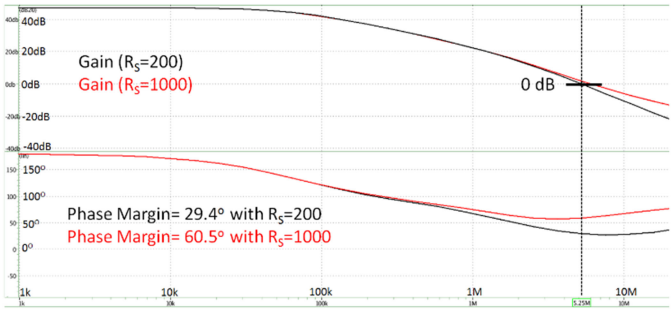

Fig. 15. Simulated loop gain T_{OP} with $R_{\mathrm{S}} = 200\ \Omega$ and $R_{\mathrm{S}} = 1\ \mathrm{k}\Omega$.

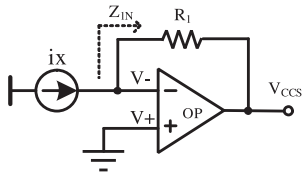

Fig. 16. Test circuit to derive the emulated inductance of the capacitor-current sensor.

Therefore, the frequency of the left-half plane zero, expressed as follows, is needed to be designed inside ten times crossover frequency for loop stability, and the value of R_{S} needs to be well considered

$$f_Z = \frac{1}{2\pi \cdot R_S \cdot C_S}. \tag{19}$$

Fig. 15 shows the simulated loop gain T_{OP} with $R_{\mathrm{S}} = 200\ \Omega$ and $R_{\mathrm{S}} = 1\ \mathrm{k}\Omega$, respectively. The phase margin increases from 29.4° to 60.5°, if R_{S} changes from 200 Ω to 1 kΩ. The accuracy of the loop gain T_{OP} derived in (18) and (19) is verified by transistor-level simulation and is not shown due to the page limit.

After the value of the capacitor and the resistor is chosen, the emulated inductance design is considered. Fig. 16 shows the test circuit to derive the emulated inductance of the capacitor-current sensor. According to Fig. 16 and [19]–[21], the impedance of emulated inductor, Z_{IN}, is derived as

$$Z_{\mathrm{IN}} = \frac{V_-}{ix} = \frac{\frac{R_1}{A_{\mathrm{DC}}} + \frac{R_1}{\mathrm{BW}}s}{1 + \frac{1}{A_{\mathrm{DC}}} + \frac{1}{\mathrm{BW}}s} \tag{20}$$

where A_{DC} is the dc gain of OP, W_{P} is the dominant pole of OP, and BW is the bandwidth of OP.

To let Z_{IN} acts as an inductor, it is assumed that BW is ten times larger than the switching frequency, and A_{DC} is much larger than one. Thus, the denominator in (20) is approximated as one and (20) can be approximated as

$$Z\mathrm{in} = -\left(\frac{R_1}{A_{\mathrm{DC}}} + \frac{R_1}{\mathrm{BW}}s\right). \tag{21}$$

It can be seen that an inductance in series with resistance is obtained. In addition, the value of V_{CCS} is expressed as

$$V_{\mathrm{CCS}} = V_{\mathrm{CM}} - R_1 \cdot I_S. \tag{22}$$

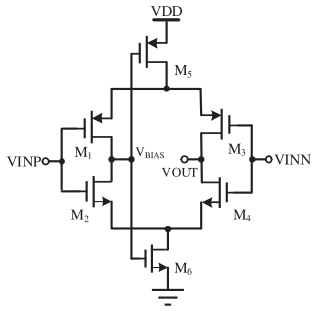

Fig. 17. Dynamic-bias OP circuit.

Therefore, R_1 is related to not only the inductor value, as shown in (20), but also the gain (A_{CCS}) of the capacitor-current sensor, which is shown as

$$A_{\mathrm{CCS}} = -\frac{R_1}{k}. \tag{23}$$

Based on the required A_{CCS}, R_1 is chosen as 100 kΩ and is made of a P+ poly w/o silicide resistor in the TSMC 0.18 μm CMOS process.

Fig. 7 shows the waveform of the capacitor-current sensor during transient and steady state. The phase difference is 180° between the output capacitor current and V_{CCS} as can be seen from (22). When the load current steps up and down, V_{CCS} has a deviation from V_{CM}, which is used to detect the start of t_1 and t_{BDC}. T_1 and t_{BDC} used for the time-optimized OTC and BDC, respectively, finishes at the time instant of passing zero of the output capacitor current.

Fig. 17 shows the implemented dynamic-biased OP circuit in Fig. 14 to achieve wider bandwidth. The transconductance of input pair is $(g_{\mathrm{m},1} + g_{\mathrm{m},2})$ instead of g_{m} due to the inverter-type input. Dynamic bias is used to enhance bandwidth by connecting the gate of MOSFET, M_5 and M_6 to V_{BIAS}. Thus, the bias current of OP varies with the input signals. The designed dynamic-biased OP has dc gain 51 dB, and bandwidth is 262 MHz with 500 f load, which has only one pole within the bandwidth. The bandwidth is large enough for Z_{IN} to act as an inductor, as shown in (20).

The sensed signal is distorted if a mismatch of resonant frequency exists between the output capacitor and the capacitor-current sensor; however, this distortion has less effect to the proposed time-optimized OTC and BDC. This is because the information we need in OTC and BDC is the time instant of passing zero of the output capacitor current instead of sensing the peak or valley values. The mismatch only changes the magnitude and the triangle wave to a slight arc triangle wave at the duty switching instead of the phase if both the output capacitor and the implemented capacitor-current sensor are operated at either the inductive side or the capacitive side related to the switching frequency. Fig. 18 shows the simulated load transient waveforms of the capacitor-current sensor having a mismatch with the output capacitor. A mismatch of ±10% of the output capacitor ESL and ESR is tested. The transistor-level simulation shows that the mismatch does not affect the t_1 used for the proposed

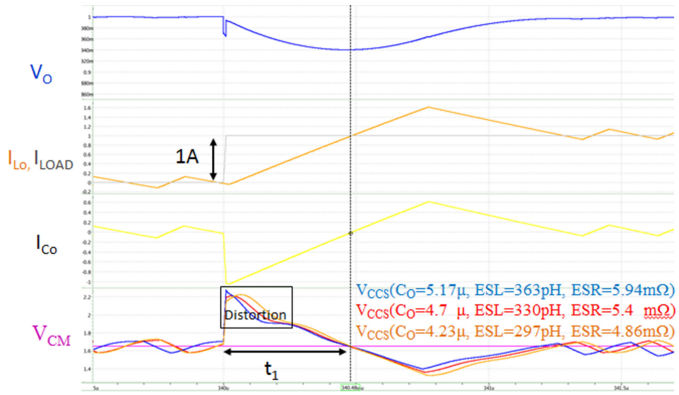

Fig. 18. Simulated load transient waveforms of the capacitor-current sensor having mismatch with the output capacitor.

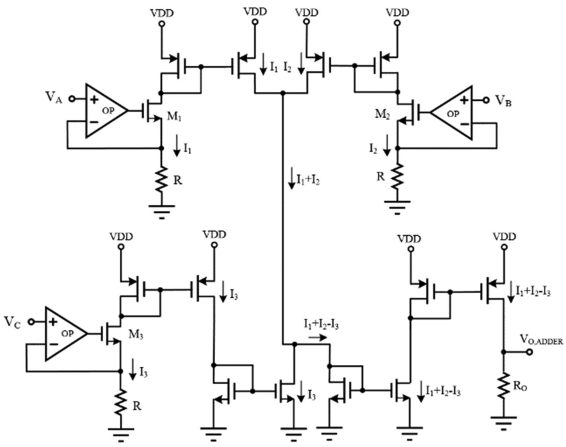

Fig. 19. Circuit diagram of CTA.

OTC, although the triangle wave becomes slight arc and the magnitude changes at the load current step-up.

C. Current-Type Adder

A CTA, as shown in Fig. 19, is used to realize adding function with reduced power consumption. In Fig. 3, an adder is required to add *Vo* and V_{ACDC} and subtract V_{DC}. The proposed OTC circuit needs an adder as well. The traditional method uses the summing amplifiers to add voltage signals; however, buffers are needed for each input signal due to the finite input impedance of summing amplifiers, which increases the area of the chip and the power consumption. Fig. 19 shows an example of a CTA. The negative feedback of OP is used to let the source of M_1 follow the input voltage V_{A} and transfer the voltage into a current by using a resistor R. By doing this, the voltages of V_{A}, V_{B}, and V_{C} are transformed into currents for addition or subtraction, and the high input impedance is also achieved. OP is implemented by PMOS-input two-stage OP because the input signal might be the ground in our application. The current mirror is widely used to duplicate the value of current in the current adder. Finally, the output voltage of the current adder is shown as

$$V_{O,\mathrm{ADDER}} = R_O \cdot (I_1 + I_2 - I_3). \tag{24}$$

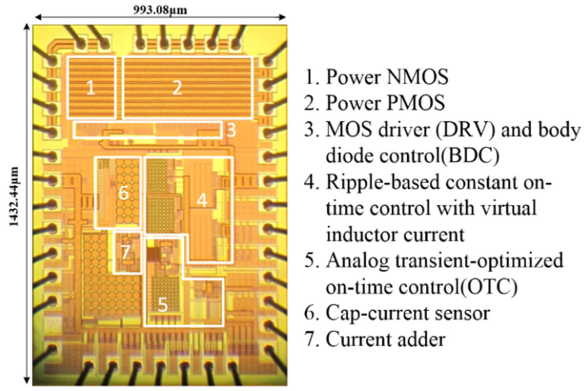

Fig. 20. Chip micrograph of the proposed circuit.

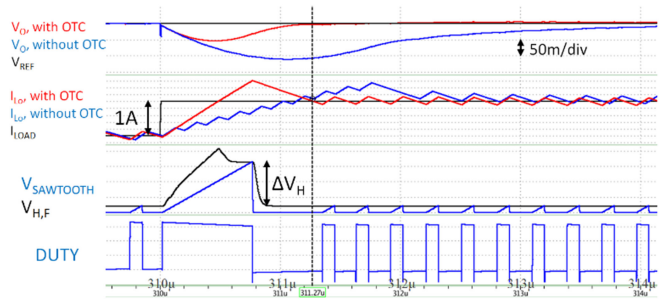

Fig. 21. Simulated transient responses of the COT buck converter with and without proposed OTC.

The jittering issue needs to be well considered especially the layout. This is because a lot of current mirrors are used in the CTA and the mismatch or noise is possible to influence the important signal of our circuit including threshold voltage, $V_{\mathrm{H.F}}$ and ramp voltage V_{RAMP}, as shown in Fig. 3.

IV. Simulation and Measurement Results

The proposed control was fabricated into an IC using TSMC 0.18 μm CMOS process. Fig. 20 presents the chip micrograph. The chip area including all bonding pads is 1.423 mm^2. The proposed OTC only occupies 0.054 mm^2 which is 3.8% of the chip area, and the quiescent current of the proposed OTC is 890 μA, which reduces 30% compared to the load transient optimizer proposed in [16]. Unless otherwise specified, the test condition is as follows. V_{IN} is 3.3 V, V_{O} is 1 V, the maximum I_{LOAD} is 1.25 A, f_{SW} is 1.5 MHz, $L_{\mathrm{O}} = 1$ μH, and $C_{\mathrm{O}} = 4.7$ μF. The bandwidth of linear control is 50 kHz, which is 1/30 of the switching frequency. Therefore, if the slew rate of the transient load is high enough, the nonlinear control will start. Otherwise, the circuit works in the slow linear loop.

Fig. 21 shows a MOSFET-level simulation of transient responses of the COT buck converter with and without the proposed OTC. It is shown that an appropriate ΔV_{H} is added to $V_{\mathrm{H,F}}$ to achieve the time-optimized control at the load step-up, which matches with Fig. 7. The target of charge balance is achieved at the time instant of dotted black line with minimum

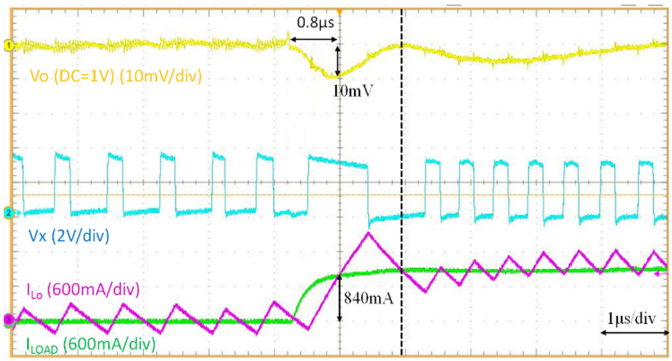

Fig. 22. Measured load step-up transient response with the OTC.

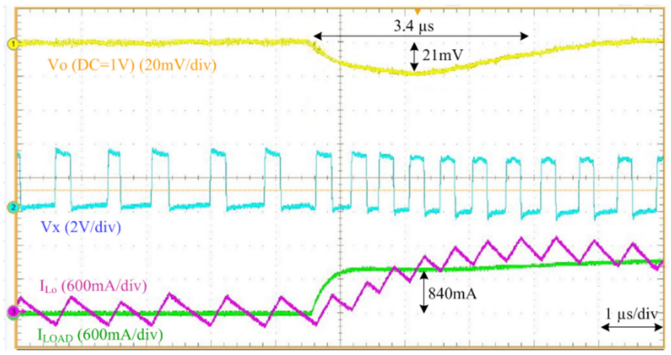

Fig. 23. Measured step-up load transient response without the OTC in 1 μs/div time scale.

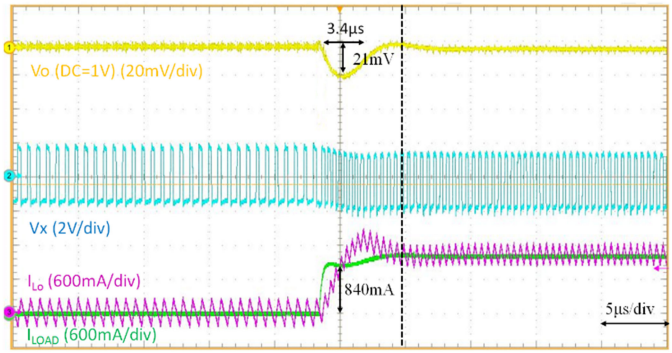

Fig. 24. Measured step-up load transient response without the OTC in 5 μs/div time scale.

undershoot and settling time and without $V_{\rm O}$ overshoot after the inductor current go back to target. The simulation result shows a 51.3% reduction of voltage deviation after enabling the proposed control function on the ripple-based COT control at the load step-up.

Figs. 22, 23, and 24 show the experimental load transient response with and without the proposed OTC, respectively, during load current step-up. To have a fair comparison, the load transients happen at relatively the same position in one switching cycle and the current change rates are kept the same using the same load transient tool. The transient load step is 840 mA.

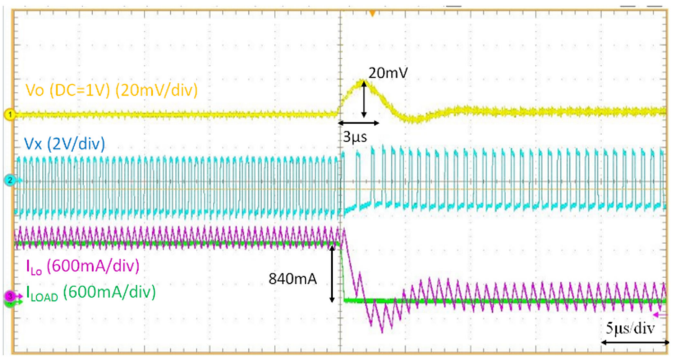

Fig. 25. Measured load transient response during load current step-down.

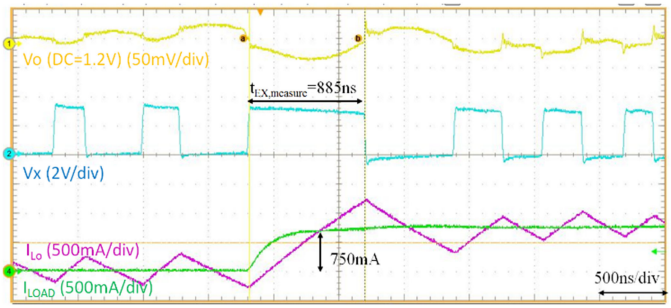

Fig. 26. Measured load transient response with the OTC with $V_{\rm o} = 1.2$ V, $C_{\rm O} = 2.2$ μF, $L_{\rm O} = 1.5$ μH, and M = 4.

The $V_{\rm O}$ undershoot improves 52.4% with the proposed OTC. The dotted black line in Fig. 22 shows the charge balance time instant of output capacitor, and the output voltage gets back to 1 V after a single extended on-time. The settling time to within 1% of $V_{\rm O}$ also reduces from 3.4 to 0.8 μs, as shown in Figs. 22 and 23, which improves 88%.

Fig. 25 shows the load current step-down with the linear control. The overshoot is 20 mV and the settling time to within 1% of $V_{\rm O}$ is 3 μs. Moreover, 90.2% peak efficiency is measured at 1 W output power.

The proposed analog time-optimized OTC achieves the time-optimized control at various duty cycle and power stage's inductor and capacitor value conditions. To prove this, the buck converter with different values of the capacitor, $C_{\rm O}$, and the inductor, $L_{\rm O}$, was tested. In Figs. 26–28, the $C_{\rm O}$ is changed from 4.7 to 2.2 μF, and the $L_{\rm O}$ is changed from 1 to 1.5 μH. Moreover, various output voltage conditions were tested to prove the effectiveness of the proposed I-DAC. The turned-ON number of unit current arrays in I-DAC at various output voltage conditions are given in Table I. The output voltage is 1.2, 1, and 0.8 V in Figs. 26, 27, and 28, respectively. The different measurement specification between Figs. 22 and 26 to Fig. 28 is organized as Table II . Table III shows the comparison between the theoretical extended on-time $t_{\rm EX,theory}$ calculated by (7) and the measured extended on-time $t_{\rm EX,measure}$. The error of the extended on-time is lower than 3.5%. Slightly ring back is happened because the slew rate of our measurement equipment is not higher enough as our assumption.

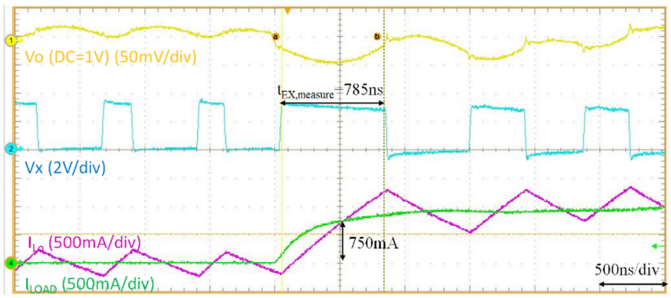

Fig. 27. Measured load transient response with the OTC with $Vo = 1$ V, $C_O = 2.2\ \mu$F, $L_O = 1.5\ \mu$H, and M = 10.

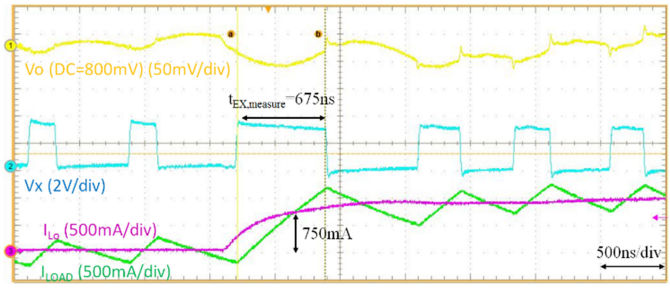

Fig. 28. Measured load transient response with the OTC with $Vo = 0.8$ V, $C_O = 2.2\ \mu$F, $L_O = 1.5\ \mu$H, and M = 15.

TABLE II
DIFFERENT MEASUREMENT SPECIFICATION BETWEEN FIGS. 22 AND 26 TO FIG. 28

Fig.	V_{IN} (V)	V_O (V)	L_O (μH)	C_O (μF)
Fig. 22	3.3	1	1	4.7
Fig. 26	3.3	1.2	1.5	2.2
Fig. 27	3.3	1	1.5	2.2
Fig. 28	3.3	0.8	1.5	2.2

TABLE III
COMPARISON BETWEEN $T_{EX,Theory}$ AND $T_{EX,MEASURE}$ IN FIGS. 26–28

Fig.	V_{IN} (V)	V_O (V)	M	$t_{EX,theory}$ (ns)	$t_{EX,measure}$ (ns)	t_{EX} Error
Fig. 26	3.3	1.2	4	859	885	3.0%
Fig. 27	3.3	1	10	758	785	3.5%
Fig. 28	3.3	0.8	15	672	675	0.4%

Table IV presents a performance comparison with other state-of-the-art single-phase buck converters [14], [22]–[25]. Compared to other state-of-the-art single-phase buck converters, the measurement results of the proposed time-optimized OTC embedded in the ripple-based COT achieves the lowest undershoot and the shortest settling time with the high slew-rate load current step-up. By improving the layout of power MOS and optimize its size, we may further improve the converter efficiency of the proposed circuit.

TABLE IV
PERFORMANCE COMPARISON WITH OTHER STATE-OF-THE-ART SINGLE-PHASE BUCK CONVERTER

		This Work	JSSC 2018 [23]	TPE 2017 [22]	JSSC 2015 [12]	JSSC 2014 [21]	TPE 2012 [20]
Implemented technique		Transient-optimized OTC	Hysteretic Quasi-V^2	Synchronous Double-Pumping	Transient-optimized feedback	DDA-Based Type-III Compensator	reconfigurable compensation
Technology (μm)		0.18 μm	0.35 μm	0.35 μm	0.35 μm	0.13 μm	0.35 μm
Inductor, L_O(μH)		1 μH	2.2 μH	4.7 μH	1 μH	0.33 μH	4.7 μH
Capacitor, C_O(μF)		4.7 μF	4.7 μF	4.7 μF	4.7 μF	3.3 μF	4.7 μF
Input Voltage, V_{IN}(V)		3.3 V	3.3 V	2.7-4.2 V	2.7-4.2 V	3.3 V	2.4-3.6 V
Output Voltage, V_O(V)		0.6-1.2 V	1.5-1.8 V	1.8 V	0.8-2.4 V	0.37-2.85 V	0.7-2.0 V
Load current, I_{LOAD}(mA)		<1250 mA	<700 mA	<600 mA	<2000 mA	<1500 mA	<1050 mA
Switching frequency (MHz)		1.5 MHz	2 MHz	1 MHz	1.25 MHz	10 MHz	0.2-1 MHz
Peak efficiency (%)		90.2%	92%	95%	96%	91.8%	96.3%
Load Transient Response	Transient step, ΔI_{LOAD}(mA)	840 mA	510 mA	400 mA	1000 mA	340 mA	1000 mA
	Settling Time(μs) Light → Heavy / Heavy → Light	0.4μs /3μs	2.5μs /2.6μs	2.4μs /2.6μs	1.6μs /1.4μs	9μs /9μs	85μs /140μs
	Undershoot / Overshoot (mV)	10 mV /20 mV	38 mV /20 mV	88 mV /76 mV	75 mV /65 mV	25 mV /20 mV	N.A.
Chip Area (mm^2)		1.423mm^2	0.913mm^2	2.242mm^2	0.88mm^2	0.75mm^2	3.2mm^2

V. CONCLUSION

This article proposed a COT converter embedded with the analog time-optimized OTC and BDC to increase load transient response at step-up and step-down, respectively. The proposed OTC is implemented in IC with the compact analog circuit and low quiescent current. According to the measurement results, the OTC improves V_O undershoot by 52.4% and settling time after load step-up by 88% as the load current steps up after enabling OTC. Beside, the proposed OTC achieves the time-optimized control independent of the power stage's inductor and capacitor values and output voltage. The proposed I-DAC simplifies the square root circuit and achieves the high accuracy of extended on-time with less than 3.5% error compared to the theoretical value.

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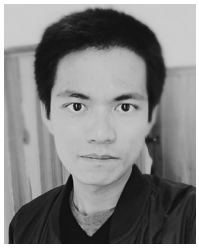
REFERENCES

[1] J. Li and F. C. Lee, "New modeling approach and equivalent circuit representation for current-mode control," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1218–1230, May 2010.
[2] R. Redl and J. Sun, "Ripple-based control of switching regulators—An overview," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2669–2680, Dec. 2009.
[3] Y. C. Lin, C. J. Chen, D. Chen, and B. Wang, "A ripple-based constant on-time control with virtual inductor current and offset cancellation for DC power converter," *IEEE Trans. Power Electron.*, vol. 27, no. 10, pp. 4301–4310, Oct. 2012.
[4] J. Sun, "Characterization and performance comparison of ripple-based control for voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 346–353, Mar. 2006.

[5] F. Yu and F. C. Lee, "Design oriented model for constant on-time V2 control," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 3115–3122.
[6] W. H. Yang *et al.*, "A constant-on-time control DC–DC buck converter with the pseudowave tracking technique for regulation accuracy and load transient enhancement," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6187–6198, Jul. 2018.
[7] C. Glaser, "High-efficiency, low-ripple DCS-control offers seamless PWM/power-save transitions," *Analog Appl. J.*, 3Q, 2013. [Online]. Available: http://www.ti.com/lit/an/slyt531/slyt531.pdf
[8] K. Lee and H. Zou, "Comparison between ramp pulse modulation (RPM) and constant frequency modulation for the beat frequency oscillation in voltage regulators," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 3101–3106.
[9] W. Qiu, G. Miller, and Z. Liang, "Dual-edge pulse width modulation scheme for fast transient response of multiple-phase voltage regulators," in *Proc. IEEE Power Electron. Spec. Conf.*, 2007, pp. 1563–1569.
[10] C.-F. Nien *et al.*, "A novel adaptive quasi-constant on-time current-mode buck converter," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 8124–8133, Oct. 2017.
[11] S. Zhen *et al.*, "Variable on time controlled buck converter for DVS applications," in *Proc. IEEE 43rd Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2017, pp. 1642–1648.
[12] S. Zhen *et al.*, "Transient response improvement of DC–DC converter by current mode variable on time control," in *Proc. IEEE 61st Int. Midwest Symp. Circuits Syst.*, 2018, pp. 603–606.
[13] S. Kapat and P. T. Krein, "Improved time optimal control of a buck converter based on capacitor current," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1444–1454, Mar. 2012.
[14] S. H. Chien, T. H. Hung, S. Y. Huang, and T.-H. Kuo, "A monolithic capacitor-current-controlled hysteretic buck converter with transient-optimized feedback circuit," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2524–2532, Nov. 2015.
[15] S.-Y. Huang, K.-Y. Fang, Y.-W. Huang, S.-H. Chien, and T.-H. Kuo, "Capacitor-current-sensor calibration technique and application in a 4-phase buck converter with load-transient optimization," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2016, pp. 228–229.
[16] Y. W. Huang, T.-H. Kuo, S. Y. Huang, and K. Y. Fang, "A four-phase buck converter with capacitor-current-sensor calibration for load-transient-response optimization that reduces undershoot/overshoot and shortens settling time to near their theoretical limits," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 552–568, Feb. 2018.
[17] G. Feng, E. Meyer, and Y.-F. Liu, "A new digital control algorithm to achieve optimal dynamic performance in DC-to-DC converters," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1489–1498, Jul. 2007.
[18] E. Meyer, Z. Zhang, and Y.-F. Liu, "An optimal control method for buck converters using a practical capacitor charge balance technique," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1802–1812, Jul. 2008.
[19] S. C. Huerta, P. Alou, J. A. Oliver, O. Garcia, J. A. Cobos, and A. Abou-Alfotouh, "Design methodology of a non-invasive sensor to measure the current of output capacitor for a very fast non-linear control," in *Proc. 24th IEEE Appl. Power Electron. Conf. Expo.*, 2009, pp. 806–811.
[20] S. C. Huerta, P. Alou, J. A. Oliver, O. Garcia, J. A. Cobos, and A. Abou-Alfotouh, "Non-linear control for DC–DC converters based on hysteresis of the COUT current with a frequency loop to operate at constant frequency," *IEEE Trans. Ind. Electron.*, vol. 58, no. 3, pp. 1036–1043, Mar. 2011.
[21] S. C. Huerta, A. Soto, P. Alou, J. A. Oliver, O. Garcia, and J. A. Cobos, "Advanced control for very fast DC–DC converters based on hysteresis of the COUT current," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 4, pp. 1052–1061, Apr. 2013.
[22] J.-M. Liu, P.-Y. Wang, and T.-H. Kuo, "A current-mode DC–DC buck converter with efficiency-optimized frequency control and reconfigurable compensation," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 869–880, Feb. 2012.
[23] L. Cheng, Y. Liu, and W.-H. Ki, "A 10/30 MHz fast reference-tracking buck converter with DDA-based type-III compensator," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2788–2799, Dec. 2014.
[24] K.-I. Wu, B.-T. Hwang, and C. C-P. Chen, "Synchronous double-pumping technique for integrated current-mode PWM DC–DC converters demand on fast-transient response," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 849–865, Jan. 2017.
[25] D.-H. Jung, K. Kim, S. Joo, and S.-O. Jung, "0.293-mm^2 fast transient response hysteretic quasi-V^2 DC–DC converter with area-efficient time-domain-based controller in 0.35-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1844–1855, Jun. 2018.



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