A 2-kV Charge-Based ZVS Three-Level Inverter

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***Abstract*—Industrial applications, e.g., semiconductor manufacturing equipment, require power converters providing high power with high precision and bandwidth. This article presents a three-level flying capacitor resonant pole inverter configuration that combines high output power and high switching frequency with reduced switch voltage stress. A multilevel modulation strategy is applied to minimize conduction losses, which, in addition, guarantees zero-voltage switching (ZVS) for the entire operating range to reduce switching losses. The proposed multilevel converter configuration is compared with an existing two-level configuration by simulation. Increasing the number of voltage levels results in lower total losses and increased linearity of the generated output current. Experimental results acquired with a hardware prototype validate the fast switching of high voltage, proper functioning of the multilevel modulation strategy, and achieving of ZVS. Improvements of the theoretical analysis are presented to compensate for delays in the system and deviating parameter values. Results obtained with a compensated system indicate a relatively high accuracy and linearity of the generated output current of the inverter.**

***Index Terms*—High voltage power converters, modulation strategy, multilevel converters, resonant converter, soft switching.**

I. INTRODUCTION

EQUIPMENT used in semiconductor manufacturing applies high-precision fast-moving stages for accurate positioning of wafers to fulfill tasks such as exposure, inspection, or dicing [1], [2] (see Fig. 1 [3]). The required positioning accuracy is in the nanometer range, which results in stringent requirements on the output current accuracy and bandwidth of the power converters driving the various types of actuators involved [4], [5]. At the same time, semiconductor manufacturers strive to minimize machine operating cost by maximizing machine throughput. As a result, the demand for mechanical power, and therefore, electrical power, is evermore increasing. Since the actuators of the moving stages operate in a dynamic environment, it is desirable to keep the weight and rigidity of the actuator cables low as the resulting disturbance forces are difficult to model and compensate. Therefore, increasing processed power by increasing operating voltage is favorable, compared to increasing operating current, which the converter should be capable of providing.

Current power converters used in semiconductor manufacturing equipment operate, for instance using a bus voltage of around 600 V and employ MOSFETs as switching devices. A resonant pole inverter topology using variable hysteresis control is implemented resulting in soft-switching behavior with a switching frequency range of 10–100 kHz [9]–[11]. In order to meet the requirements for future generation semiconductor manufacturing equipment, a bus voltage of 2 kV and switching frequency of ≥ 50 kHz across the entire operating range is proposed. Due to the stringent requirements on output current accuracy for high-precision industrial applications [2], [4], [5], [12], the required switching frequency of the power converter is several orders higher than that applied in common HV applications, such as electrical propulsion and grid-connected converters. This, however, imposes challenges for the power converter as reliable fast-switching devices are not available with blocking voltages ranging up to 2 kV [13].

Previous research conducted in this area has shown that the flying capacitor resonant pole inverter (FC RPI) is a suitable topology to reduce voltage stress on switches through a multilevel configuration [6]–[8], see Fig. 2. This enables the use of fast switches with a voltage rating lower than the bus voltage by dividing the voltage stress over multiple switches. The addition of two switches and a flying capacitor to a standard half-bridge results in a three-level converter. The presented half-bridge is often applied in two or three branches to drive single- or three-phase actuators, and such implementations are covered by this article as well.

Next to a (big) increase in output power, the industry further requires improved power density to not exceed existing weight and volume restrictions. Therefore, an increase in efficiency has to be realized. This can be achieved by actively using the available middle voltage level of the flying capacitor to shape the filter inductor current i_{Lf}, as was previously presented in [8]. With three different gradients for the filter inductor current, a trapezoidal shape is obtained, which has lower rms and peak values. A lower rms value of the current results in lower conduction losses in the switches and filter inductor. Lower peak values result in lower switching losses, lower core losses in the filter inductor L_{f}, and lower losses in the output filter capacitor C_{f}.

Previous implementations of the RPI topology applied additional resonant capacitors parallel to the switches and hysteresis current control to achieve zero-voltage switching (ZVS) across the entire operating range [7], [9]–[11], [14]. A more elaborate charge-based modulation strategy for a two-level converter discarding the additional resonant capacitors is proposed in [15]. Piecewise linear approximation of the filter inductor current is

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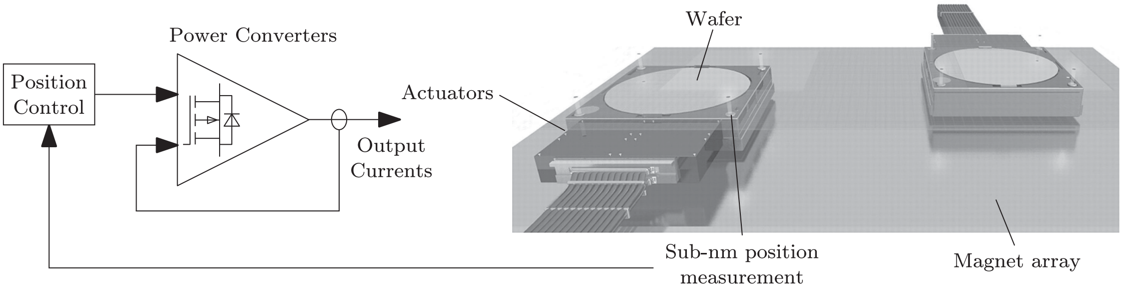


Fig. 1. Outline of a high-precision wafer positioning system as used in semiconductor manufacturing equipment. It comprises a moving stage with sub-nm position measurement for position control, which generates set points for the power converters that drive the actuators. (Courtesy of ASML [3].)

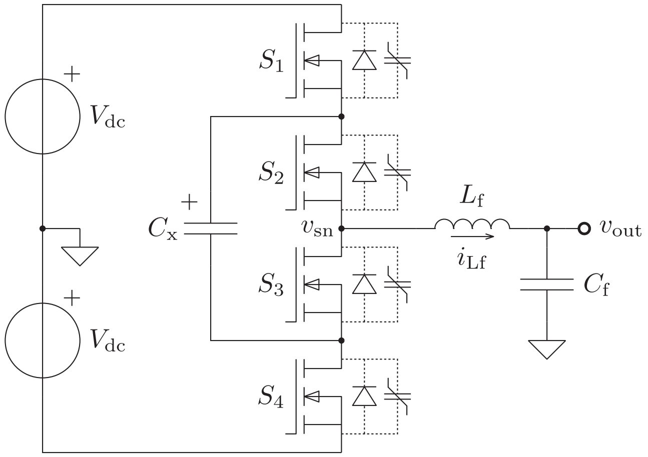


Fig. 2. Schematic of a three-level FC RPI. The flying capacitor is designated C_{x}, the filter inductor L_{f}, and the output filter capacitor C_{f}. For each MOSFET S_{1-4}, the internal body diode and nonlinear output capacitance C_{oss} are drawn with dashed lines [6]–[8].

applied, and the presented basic principles are adapted to a three-level FC RPI in [8]. This results in less required commutation current, a higher switching frequency due to faster commutation, and lower rms and peak values of the filter inductor current. This article presents various significant extensions of the three-level modulation strategy, and elaborate theoretical and experimental verification of the resulting performance.

Section II contains a summary of the previously presented analysis regarding charge-based ZVS of a three-level FC RPI with trapezoidal filter current [8]. The basic analysis of the modulation strategy is extended, and an optimization is described to limit the switching frequency within a desired range. In Section III, a loss break-down analysis and the comparison between the two-level modulation as presented in [7] and the three-level modulation described in Section II are given. The two corresponding simulation frameworks that were used are described in detail, from which a comparison between the achieved quality of the output current is made. The experimental results obtained from a hardware prototype of the three-level converter configuration are treated in Section IV, from which critical improvements of the theoretical analysis are deduced to match the characteristics of the actual converter. The results of the adapted theoretical analysis and simulations are presented next to the ideal and measured values. Finally, the conclusions drawn are presented in Section V.

TABLE I
SWITCH NODE VOLTAGE v_{sn} FOR MIDDLE LEVEL

v_{Cx} action	$i_{\mathrm{Lf}} >= 0$	$i_{\mathrm{Lf}} < 0$
Charge	$v_{\mathrm{sn}} = V_{\mathrm{dc}} - v_{\mathrm{Cx}}$	$v_{\mathrm{sn}} = -V_{\mathrm{dc}} + v_{\mathrm{Cx}}$
Discharge	$v_{\mathrm{sn}} = -V_{\mathrm{dc}} + v_{\mathrm{Cx}}$	$v_{\mathrm{sn}} = V_{\mathrm{dc}} - v_{\mathrm{Cx}}$

II. FLYING CAPACITOR RESONANT POLE INVERTER

In Fig. 2, the schematic of the FC RPI topology is shown with a symmetrical supply voltage V_{dc}. It consists of four switches S_{1-4}, flying capacitor C_{x}, filter inductor L_{f}, and output filter capacitor C_{f} to limit $\mathrm{d}v_{\mathrm{out}}/\mathrm{d}t$. For each MOSFET, the internal body diode and nonlinear output capacitance C_{oss} are drawn with dashed lines. The additional commutation/resonant capacitors, as used in previous implementations of RPIs [7], [9]–[11], [14], are discarded from the circuit. This results in a lower required commutation charge to achieve ZVS, resulting in lower rms and peak values of the filter inductor current i_{Lf}, and therefore, lower losses. Determining the actual required charge is more difficult since the output capacitor of a MOSFET is highly nonlinear. However, the nonlinearity of C_{oss} helps to obtain fast commutation and enables piecewise linear approximation of i_{Lf}, as followed from the analysis presented in [15].

The switch node sn can be directly connected to $+V_{\mathrm{dc}}$ or $-V_{\mathrm{dc}}$, or to a middle level of $V_{\mathrm{dc}} - v_{\mathrm{Cx}}$ or $-V_{\mathrm{dc}} + v_{\mathrm{Cx}}$. Depending on the respective switching state when selecting the middle level, the flying capacitor C_{x} can either be charged or discharged, see Table I [7]. By actively balancing v_{Cx} to V_{dc} and ensuring that one switch is always conducting, the voltage across all switches is limited to V_{dc} plus the (small) ripple voltage $\tilde{v}_{\mathrm{Cx}}$ of the flying capacitor. Self-balancing of the flying capacitor voltage v_{Cx}, as for instance described in [16], is insufficient as the converter has to generate both ac and dc currents. This does, however, require a differential voltage measurement circuit with a high common mode rejection ration (CMMR).

A. Trapezoidal Filter Current

In contrast to the triangular filter currents typically used in RPI topologies [7], [10] and, for instance, power factor correction (PFC) rectifier circuits [17], the additional voltage level provided by the flying capacitor enables the use of different filter current shapes. This may reduce the rms and peak values of the current flowing through the switches, filter inductor, and

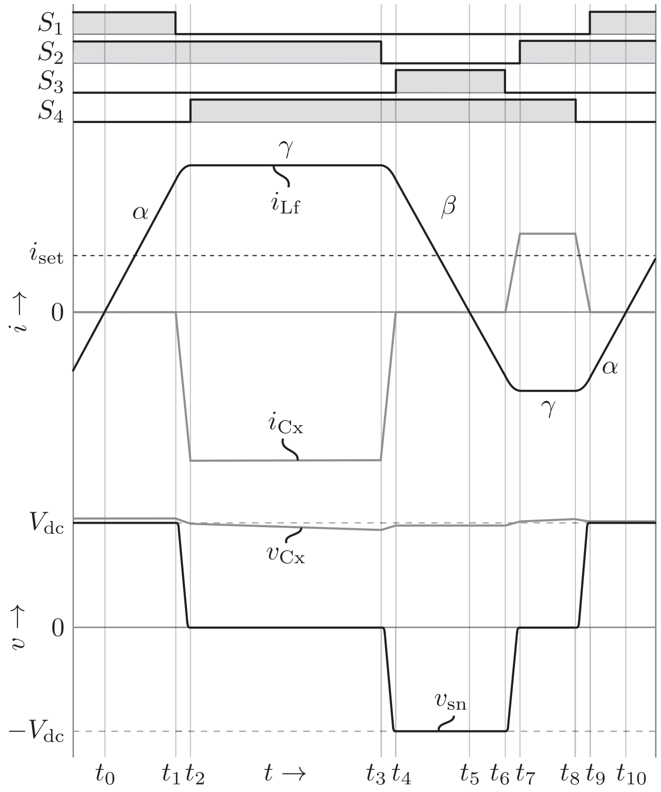


Fig. 3. Schematic representation of the i_Lf, i_Cx, v_Cx, and v_sn waveforms for a single switching period. The corresponding drive signals for switches S_{1-4} are shown at the top of the figure. The desired average current for this exemplary schematic representation is $i_\mathrm{set} > 0$ A, and $v_\mathrm{out} = 0$ V.

TABLE II
FC RPI SWITCHING STATES

	Floating C_x				Charge C_x				Discharge C_x			
interval	S_1	S_2	S_3	S_4	S_1	S_2	S_3	S_4	S_1	S_2	S_3	S_4
$[t_0, t_1]$	1	1	0	0								
$[t_1, t_2]$					1	0	0	0	0	1	0	0
$[t_2, t_3]$					1	0	1	0	0	1	0	1
$[t_3, t_4]$					0	0	1	0	0	0	0	1
$[t_4, t_5]$	0	0	1	1								
$[t_5, t_6]$	0	0	1	1								
$[t_6, t_7]$					0	0	0	1	0	0	1	0
$[t_7, t_8]$					0	1	0	1	1	0	1	0
$[t_8, t_9]$					0	1	0	0	1	0	0	0
$[t_9, t_{10}]$	1	1	0	0								

filter capacitor, and therefore, increase the converter's efficiency. Fig. 3 shows exemplary waveforms for one switching period of the filter inductor current i_Lf, flying capacitor current i_Cx and voltage v_Cx, and the voltage v_sn from the switch node sn to ground. The desired per-period average value of i_Lf, defined as i_set, is positive and the output voltage v_out is equal to 0 V, resulting in a flat middle part of the trapezoidal current shape. The corresponding switching states that result in the exemplary waveforms are shown at the top of Fig. 3 and given in Table II, where the distinction is made between charging or discharging the flying capacitor C_x. The negative part of i_Lf is required for each switching period to achieve ZVS for all turn-ON events of the switches.

The duration of each switching state can be adjusted to obtain the desired average filter current i_set, to minimize the rms value of the current through the filter inductor, to regulate the switching frequency, and to guarantee soft-switching at each switching instant. The latter requires the proper calculation of the corresponding time intervals and current values, in order for v_sn to completely commutate to the appropriate voltage level as indicated in Fig. 3 [8].

For each switching period, two time instants are available to choose between charging or discharging the flying capacitor in order to balance v_Cx around V_dc—at t_1 and t_6. The decision whether to charge or discharge C_x is based on a measurement of the actual voltage v_Cx, resulting in closed-loop control of the flying capacitor voltage. Balancing v_Cx to V_dc results in the switch node voltages for the respective states shown in Table I, depending on the sign of i_Lf. The three states for which v_sn is constant result in constant slopes of i_Lf which are indicated by α, β, and γ in Fig. 3. The corresponding equations for the slopes are

$$\alpha = \frac{V_\mathrm{dc} - v_\mathrm{out}}{L_\mathrm{f}} \tag{1}$$

$$\beta = \frac{-V_\mathrm{dc} - v_\mathrm{out}}{L_\mathrm{f}} \tag{2}$$

$$\gamma = \frac{v_\mathrm{sn} - v_\mathrm{out}}{L_\mathrm{f}}. \tag{3}$$

Assuming v_Cx is balanced properly around V_dc with relatively low variations, the approximation can be made that $v_\mathrm{sn} \approx 0$ V during intervals $[t_2, t_3]$ and $[t_7, t_8]$. However, the flying capacitor is actively delivering a significant amount of energy to the output of the converter. This means that the capacitor has to contain sufficient charge for its ripple voltage $\tilde{v}_\mathrm{Cx}$ to remain relatively low, and therefore, ensure that the assumption that $v_\mathrm{sn} \approx 0$ V continues to be valid.

B. Analytical Modeling of Charge-Based ZVS

The nonlinear output capacitance $C_\mathrm{oss}\,(v_\mathrm{ds})$ of a MOSFET can be used as a resonant component for the circulating filter current i_Lf and to achieve ZVS in a switching leg [15], [18]. Due to the high nonlinearity of C_oss, fast commutation of the switch node voltage is obtained. The charge model of $C_\mathrm{oss}\,(v_\mathrm{ds})$ enables the use of piecewise linear approximation of the trapezoidal shape of i_Lf, which is shown in Fig. 4 for $i_\mathrm{set} > 0$ A and $v_\mathrm{out} < 0$ V. The charge-based analysis presented in [15] was applied to a three-level FC RPI in [8]. In this article, the basic analysis is extended and an optimization to limit the switching frequency is presented.

To reduce the rms value of i_Lf, thereby increasing efficiency, the surface of the negative part of i_Lf (indicated with t_N), needed to achieve ZVS, is to be minimized. As a first step, a critical area underneath i_Lf is defined which has to contain at least the commutation charge Q_c of the output capacitance $C_\mathrm{oss}\,(v_\mathrm{ds})$ of a single MOSFET, assuming $v_\mathrm{ds} = V_\mathrm{dc}$. The critical area is indicated with Q_c in Fig. 4. From this area and the slope of

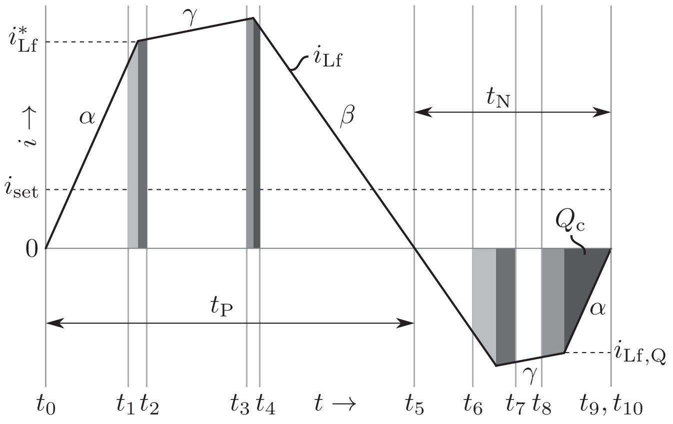


Fig. 4. Schematic representation of i_{Lf} for $i_{\mathrm{set}} > 0$ and $v_{\mathrm{out}} < 0$ with charge commutation areas to ensure ZVS indicated in gray. The corresponding minimum current $i_{\mathrm{Lf,Q}}$, desired per-period average current i_{set}, and set-point dependent i^*_{Lf} are indicated together with the switching state timing intervals. Note that $t_9 = t_{10}$ since $[t_9, t_{10}] = 0$ for this modulation state.

i_{Lf} for that section α, the corresponding minimum current $i_{\mathrm{Lf,Q}}$ needed to ensure ZVS can be calculated according to

$$i_{\mathrm{Lf,Q}} = -\sqrt{2Q_{\mathrm{c}}\alpha}. \tag{4}$$

In order to achieve ZVS for each switching instant, the charge present in the current for each of the commutation intervals, being $[t_1, t_2]$, $[t_3, t_4]$, $[t_6, t_7]$, and $[t_8, t_9]$, should be at least $2Q_{\mathrm{c}}$ [15]. This is indicated in Fig. 4 with areas in different shades of gray, each representing an area corresponding to Q_{c}. The indicated switching-state timing intervals correspond to Fig. 3. Note that $t_9 = t_{10}$ since $[t_9, t_{10}] = 0$ for this modulation state ($i_{\mathrm{set}} > 0$ A, $v_{\mathrm{out}} < 0$ V).

As followed from the analysis in [8], the resulting switching frequency for light-load operation is relatively high resulting in high switching losses. To mitigate this issue, the middle part of the trapezoidal filter inductor current can be extended. The interval $[t_7, t_8]$ is made dependent of i_{set} and v_{out} as a tuning parameter for the switching frequency, according to

$$[t_7, t_8] = t_{\mathrm{cx,min}} + t_{\mathrm{cx,ext}} \left(1 - \frac{|i_{\mathrm{set}}|}{i_{\mathrm{set,max}}}\right)^2 \left(1 - \frac{|v_{\mathrm{out}}|}{V_{\mathrm{dc}}}\right)^2 \tag{5}$$

where $t_{\mathrm{cx,min}}$ indicates a minimum time for the middle part of the trapezoid to allow for balancing of the flying capacitor C_{x}, $t_{\mathrm{cx,ext}}$ is a tuning parameter for the variable extension of the middle part depending on the load profile, and $i_{\mathrm{set,max}}$ and V_{dc} indicate the maximum output current and voltage, respectively. The values for $t_{\mathrm{cx,min}}$ and $t_{\mathrm{cx,ext}}$ are determined empirically as they depend on the output current requirements and load characteristics.

The area underneath the filter inductor current indicating the required commutation charge, has to be equal to Q_{c}. The integral of the first-order piecewise linear equations for i_{Lf} give second-order equations which can easily be solved analytically resulting in second-order equations. The subsequent derived equations are analogous to the calculations for the switching times and current presented in [15]. Given α, β, γ, the required commutation charge Q_{c}, $i_{\mathrm{Lf,Q}}$, and the above-defined interval $[t_7, t_8]$, all time values $t_5, ..., t_{10}$ and their respective current values for the negative part of i_{Lf} can be calculated numerically.

From the set of equations describing the negative part of filter inductor current, a total charge area A_{N} of i_{Lf} in the time interval $t_{\mathrm{N}} = [t_5, t_{10}]$ is obtained. Furthermore, the average value of i_{Lf} has to be equal to the desired current i_{set}. This gives for the total charge area A_{P} of the positive part of i_{Lf} in the time interval $t_{\mathrm{P}} = [t_0, t_5]$

$$A_{\mathrm{P}} = A_{\mathrm{N}} + i_{\mathrm{set}} \left(t_{\mathrm{N}} + t_{\mathrm{P}}\right). \tag{6}$$

However, the equations for both time and current values of i_{Lf} for the charge area of the positive part are still unbounded. To oppose this in a way to have simple calculations, i^*_{Lf}, as indicated in Fig. 4, is proposed to be made dependent of i_{set} and the minimum commutation current $i_{\mathrm{Lf,Q}}$ for the same slope α, and set to

$$i^*_{\mathrm{Lf}} = -i_{\mathrm{Lf,Q}} + i_{\mathrm{set}}. \tag{7}$$

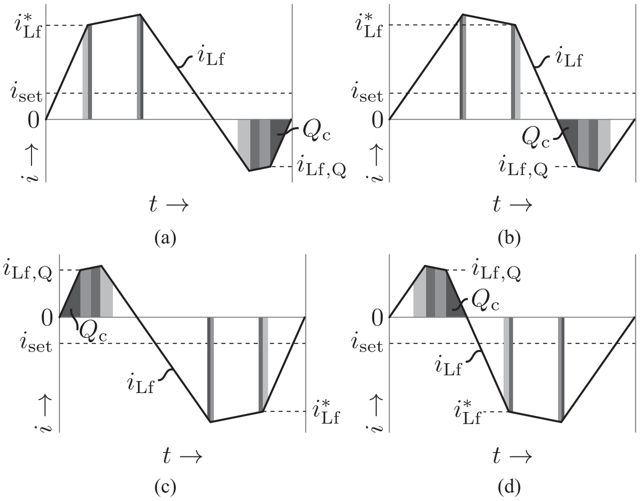
From the given slopes of i_{Lf}, defined current value i^*_{Lf}, commutation charge Q_{c}, area A_{N} and (6), the remaining time and current values for the positive part of i_{Lf} can be calculated. This results in a complete description of i_{Lf} and timing of the switching intervals for a single switching period that can be implemented in a controller. The extension of the middle part of the trapezoid for negative i_{Lf}, $[t_7, t_8]$, as defined in (5) is incorporated in A_{N}, and therefore, results in an extended middle part for positive i_{Lf}, $[t_2, t_3]$, as well.

The resulting numerical rms and peak values of the filter inductor current can be determined from the set of equations that describe a complete period of i_{Lf}. The corresponding values are then used for component dimensioning. Due to the second-order equations and sequential calculation process, it is not feasible to derive practical analytical expressions for the rms and peak current values of i_{Lf}. All parameters can however be calculated numerically. The actual filter inductor current profile is however strongly dependant on the load characteristics, input current profile, and design choices made (e.g., for $t_{\mathrm{cx,min}}$ and $t_{\mathrm{cx,ext}}$).

For a converter with a trapezoidal filter current operating in all four quadrants, corresponding piecewise linear approximations of i_{Lf} can be made and are shown in Fig. 5. The critical area of i_{Lf} with a minimum required charge Q_{c} is located differently for each modulation state, depending on the signs of i_{set} and v_{out}. However, the reasoning and calculations are analogous to the case discussed above. The result is four sets of ten equations to calculate the value of each switching time when the converter is operating in the corresponding quadrant.

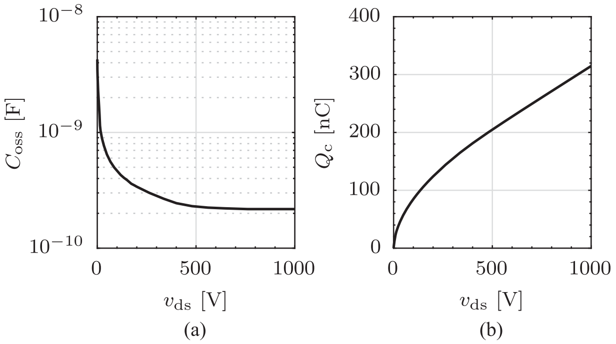
Zero-crossing detection of i_{Lf} is used to ensure that the calculated timing model remains in phase with the actual current. This means that no accurate measurement of i_{Lf} is necessary for proper operation of the converter; accuracy is determined by the clock frequency of the controller that generates the gate signals for the switches.

To determine a practical value for Q_{c}, a plot of the nonlinear output capacitance $C_{\mathrm{oss}}\left(v_{\mathrm{ds}}\right)$ is taken from the datasheet of a Wolfspeed C2M0025120D SiC MOSFET and shown in Fig. 6(a) [19]. The resulting charge Q_{c} as a function of v_{ds} is shown in



(a) (b) (c) (d)

Fig. 5. Schematic representation of i_{Lf} for four different modulation states depending on the signs of i_{set} and v_{out}: (a) $i_{\mathrm{set}} > 0$ A and $v_{\mathrm{out}} < 0$ V; (b) $i_{\mathrm{set}} > 0$ A and $v_{\mathrm{out}} < 0$ V; (c) $i_{\mathrm{set}} < 0$ A and $v_{\mathrm{out}} < 0$ V; and (d) $i_{\mathrm{set}} < 0$ A and $v_{\mathrm{out}} > 0$ V. Required commutation current $i_{\mathrm{Lf,Q}}$, set-point-dependent current i_{Lf}^{*} and i_{set} are indicated for each quadrant, as well as the commutation charges in gray.



(a) (b)

Fig. 6. (a) Plot of the nonlinear output capacitance C_{oss} as a function of v_{ds}, taken from the datasheet of a Wolfspeed C2M0025120D SiC MOSFET [19]. (b) Plot of the calculated charge Q_{c} in the output capacitance of a Wolfspeed C2M0025120D SiC MOSFET as a function of v_{ds}.

Fig. 6(b), which is calculated according to

$$Q_{\mathrm{c}}\left(v_{\mathrm{ds}}\right) = \int_{0}^{v_{\mathrm{ds}}} C_{\mathrm{oss}}(v)\mathrm{d}v. \tag{8}$$

C. Dimensioning of L_{f} and C_{x}

The inductance value of the filter inductor L_{f} has a significant impact on the shape of the current i_{Lf} as it determines the values of the slopes α, β, and γ. Under maximum load conditions with a high set-point current and output voltage, the inductance value determines the minimum switching frequency that can be achieved as the middle parts of the trapezoid are being minimized. The filter inductor current shape can then be approximated by a triangle which can be used to determine a boundary value for the inductance for a certain minimum desired switching frequency. The resulting limit for L_{f} is given by

$$L_{\mathrm{f}} \leq \frac{V_{\mathrm{dc}}^{2} - \hat{v}_{\mathrm{out}}^{2} - 4 f_{\mathrm{sw}} V_{\mathrm{dc}} t_{\mathrm{neg}}\left(V_{\mathrm{dc}} + \hat{v}_{\mathrm{out}}\right)}{4 f_{\mathrm{sw}} V_{\mathrm{dc}} \hat{\imath}_{\mathrm{set}}} \tag{9}$$

where $\hat{v}_{\mathrm{out}}$ is a defined maximum output voltage, f_{sw} is the desired minimum switching frequency, t_{neg} represents the time between the negative zero crossing of i_{Lf} and the end of the first commutation (corresponding to $[t_5, t_7]$ in Fig. 4), and $\hat{\imath}_{\mathrm{set}}$ is a defined maximum set-point current. The parameters $\hat{v}_{\mathrm{out}}$, $\hat{\imath}_{\mathrm{set}}$, and t_{neg} depend on the characteristics of the load and the applied set point current profile. While the equation gives an upper limit for L_{f}, the lower limit is defined by the desired output voltage ripple in combination with the value for C_{f}.

During the middle parts of the trapezoidal filter inductor current i_{Lf}, the flying capacitor C_{x} is actively delivering energy toward the output of the converter. For the piecewise linear approximation of i_{Lf} to remain valid, the ripple voltage $\tilde{v}_{\mathrm{Cx}}$ of the flying capacitor should be relatively small. The resulting relative charge error in the middle part of the trapezoidal current can be expressed by

$$\frac{\Delta Q}{Q_{\mathrm{middle}}} = \frac{t_{\mathrm{middle}}^{2}}{L_{\mathrm{f}} C_{\mathrm{x}}} \tag{10}$$

where ΔQ is the absolute charge error, Q_{middle} is the desired charge in the middle part, and t_{middle} is the time interval of the middle part (corresponding to $[t_2, t_3]$ in Fig. 4). For a defined worst case scenario depending on the characteristics of the load and the applied set-point current profile, a minimum value for the flying capacitor can be obtained.

III. TWO LEVEL VERSUS THREE LEVEL COMPARISON

In order to compare the three-level modulation scheme as presented in Section II with the existing two-level modulation strategy as presented in [7], [9], and [10], two different simulation frameworks were constructed using MATLAB Simulink and the Plexim PLECS blockset. The simulation models and parameters are discussed for both converter configurations, a loss breakdown analysis is presented, and the performance is compared using dc and ac analysis.

A. Two-Level Simulation Model

The existing two-level modulation strategy for a two-level converter as presented in [9] and [10] was applied to an FC RPI topology in [7] to achieve fast switching of voltages exceeding the maximum forward voltage of the switches used. The corresponding circuit schematic is shown in Fig. 7. The differences with the schematic presented in Fig. 2 are only marginal viz., the added resonance capacitors $C_{\mathrm{r1-4}}$. The applied modulation strategy as presented in [7] is summarized in this paragraph.

The modulation for the two-level converter is based on variable hysteresis control [9]. The high and low current levels for the circulating current to achieve ZVS are determined using

$$i_{\mathrm{Lf,min}} = \frac{2 V_{\mathrm{dc}}}{\sqrt{\frac{L_{\mathrm{f}}}{C_{\mathrm{res}}}}} \tag{11}$$

$$C_{\mathrm{res}} = 2\left(C_{\mathrm{r}} + C_{\mathrm{Qoss}}\right) \tag{12}$$

where C_{Qoss} is the charge equivalent capacitance of C_{oss} for a given V_{dc}. Depending on the sign of i_{set}, the high and low current levels are defined by the conditional equations as given

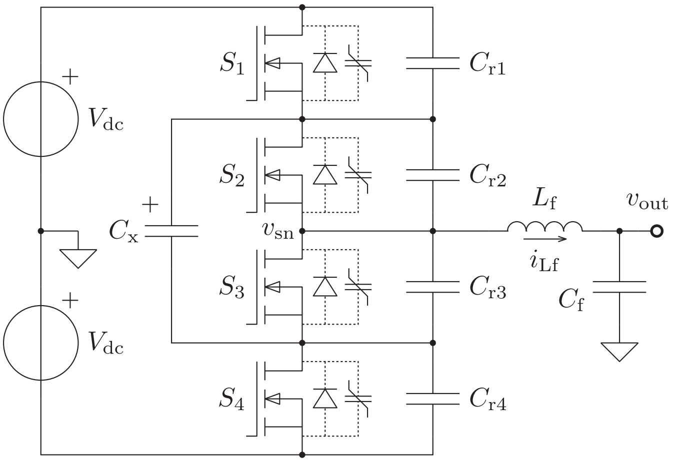


Fig. 7. Circuit schematic of the FC RPI used for two-level modulation. The resonance capacitors $C_{\mathrm{r1-4}}$ are added in comparison with the circuit schematic presented in Fig. 2.

TABLE III
CURRENT LEVELS FOR VARIABLE HYSTERESIS CONTROL

i_{set}	$>= 0$	< 0
i_{hi}	$2i_{\mathrm{set}} + i_{\mathrm{Lf,min}}$	$i_{\mathrm{Lf,min}}$
i_{lo}	$-i_{\mathrm{Lf,min}}$	$2i_{\mathrm{set}} - i_{\mathrm{Lf,min}}$

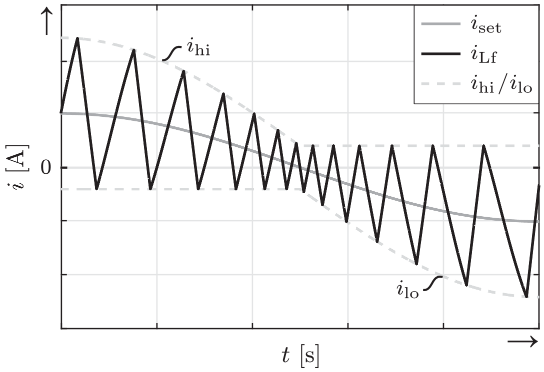


Fig. 8. Schematic representation of the desired per-period average current i_{set} (gray) and the resulting filter inductor current i_{Lf} (black), with the high and low current levels for the turn-OFF currents indicated with dashed lines [9].

TABLE IV
SWITCHING STATES FOR VARIABLE HYSTERESIS CURRENT CONTROL

	Floating C_{x}				Charge C_{x}				Discharge C_{x}			
interval	S_1	S_2	S_3	S_4	S_1	S_2	S_3	S_4	S_1	S_2	S_3	S_4
$[t_0, t_1]$	1	1	0	0								
$[t_1, t_3]$					1	0	0	0	0	1	0	0
$[t_3, t_5]$	0	0	0	0								
$[t_5, t_6]$	0	0	1	1								
$[t_6, t_8]$					0	0	0	1	0	0	1	0
$[t_8, t_{10}]$	0	0	0	0								

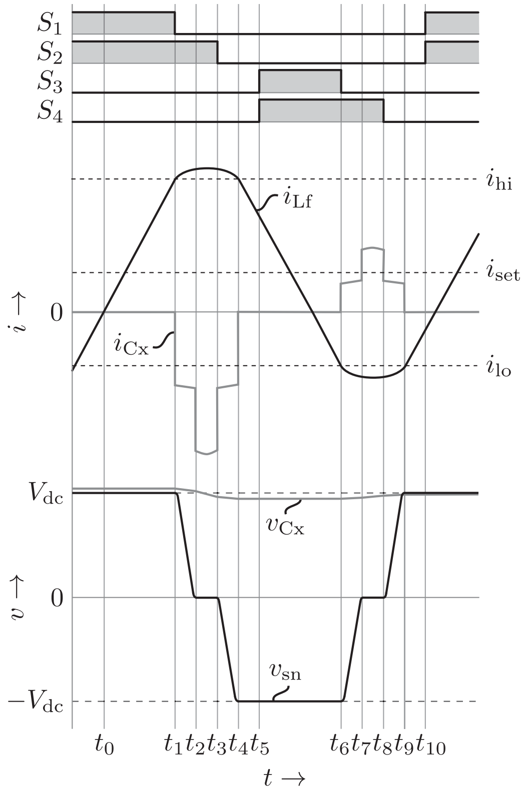


Fig. 9. Schematic representation of the i_{Lf}, i_{Cx}, v_{Cx}, and v_{sn} waveforms for a single switching period for two-level variable hysteresis control. The corresponding drive signals for switches S_{1-4} are shown at the top of the figure. The desired average current for this exemplary schematic representation is $i_{\mathrm{set}} > 0$ A.

in Table III [9]. A schematic representation of the resulting filter inductor current i_{Lf} for a given desired per-period average current i_{set} is shown in Fig. 8. The corresponding high and low levels for the turn-OFF currents are drawn with dashed lines.

The switching strategy for two-level modulation with variable hysteresis current control as presented in [7] is slightly different compared to the three-level modulation described in Section II. Since the middle-level voltage is not actively used, the flying capacitor is not directly connected to the switch-node during commutation. However, balancing the capacitor voltage by choosing either to charge or discharge the capacitor is still possible as the body diode of the corresponding switch starts conducting when the switch-node voltage is fully commutated. The resulting switching states are shown in Table IV, and a schematic representation of the i_{Lf}, i_{Cx}, v_{Cx}, and v_{sn} waveforms for a single switching period are shown in Fig. 9.

A fixed waiting time is applied for each commutation interval, being $[t_1, t_3]$, $[t_3, t_5]$, $[t_6, t_8]$, and $[t_8, t_{10}]$, which is calculated using [7]

$$t_{\mathrm{wait}} = \frac{C_{\mathrm{res}} V_{\mathrm{dc}}}{i_{\mathrm{Lf,min}}}. \tag{13}$$

Since t_{wait} is calculated for the longest commutation interval when $i_{\mathrm{set}} = 0$ A, and considering the actual switch turn-OFF delay and that there is a delay between i_{Lf} crossing the predetermined current levels as well, being either i_{hi} or i_{lo} (see Fig. 8), effectively a small time interval is available for either charging or discharging the flying capacitor. However, this small

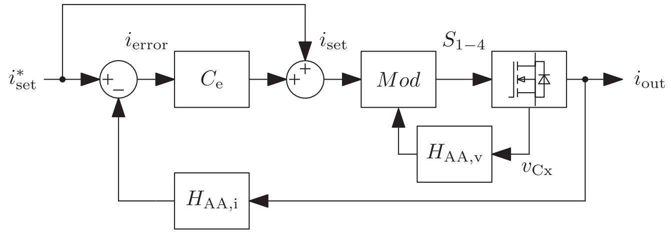


Fig. 10. Schematic overview of the simulation framework for the two-level converter configuration, with the electrical circuit depicted by the MOSFET block, modulator Mod, antialiasing filters $H_{\rm AA,i}$ and $H_{\rm AA,v}$, and output current controller $C_{\rm e}$.

TABLE V
SIMULATION SPECIFICATIONS

Parameter	Value	Unit	Parameter	Value	Unit
$V_{\rm dc}$	1	kV	$C_{\rm r}$	820	pF
$C_{\rm x}$	60	μF	$C_{\rm Qoss}$	335	pF
$L_{\rm f}$	20	μH	$R_{\rm o}$	75	Ω
$C_{\rm f}$	20	μF	$L_{\rm o}$	5	mH

time interval is sufficient to enable active balancing of the flying capacitor voltage for two-level modulation. An accurate determination of the actual flying capacitor voltage $v_{\rm Cx}$ is required and included in the simulation framework.

The resonant pole inverter can be seen as a current controlled converter, for which closed-loop output current control was implemented in the simulation framework [4], [20]. The open-loop bandwidth was tuned to 1 kHz, and antialiasing filters with a cutoff frequency of 100 kHz were added for the measurements of $i_{\rm out}$ and $v_{\rm Cx}$.

A schematic overview of the implemented simulation framework for the two-level converter configuration is shown in Fig. 10. The switching endstage and electrical circuit are depicted by the MOSFET block which has the gate signals for the four switches S_{1-4} as an input from the modulator Mod. The antialiasing filters are designated $H_{\rm AA,i}$ and $H_{\rm AA,v}$, and the output current controller $C_{\rm e}$. The parameters for the simulation framework are given in Table V. The load consists of a series connection of a resistor $R_{\rm o}$ and inductor $L_{\rm o}$, emulating an actuator. The values for $L_{\rm f}$, $C_{\rm r}$, and $C_{\rm Qoss}$ are chosen in accordance with the values given in [7]. The values for $C_{\rm x}$ and $C_{\rm f}$ are equal to the values used for the three-level simulations, which will be elaborated in the next section.

B. Three-Level Simulation Model

For the simulation model of the three-level converter configuration, the electrical circuit diagram shown in Fig. 2 is used. To obtain an equal comparison, the three-level simulation model is based on the same simulation specifications as used for the two-level simulation model, as shown in Table V. The values for $L_{\rm f}$ and $C_{\rm x}$ were determined using the reasoning presented in Section II-C and applying worst case parameters determined by simulation. The value of $C_{\rm f}$ determines the output voltage ripple $\tilde{v}_{\rm out}$ together with $L_{\rm f}$, which was chosen $\tilde{v}_{\rm out} \leq 5$ V, from which a minimum value for $C_{\rm f}$ can be calculated. Furthermore, with the generation of a hardware prototype in mind, the values for $C_{\rm x}$ and $C_{\rm f}$ were chosen from the set of components available on the market.

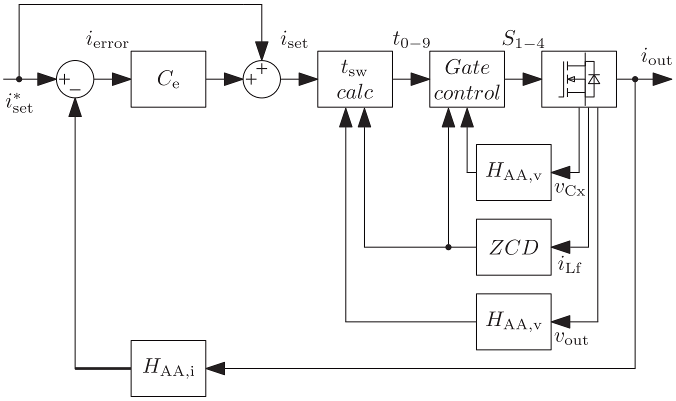


Fig. 11. Schematic overview of the simulation framework for the three-level converter configuration, with the electrical circuit depicted by the MOSFET block, switching times calculator $t_{\rm sw}$, $Gate\ control$ block, antialiasing filters $H_{\rm AA,i}$ and $H_{\rm AA,v}$, and output current controller $C_{\rm e}$.

Instead of the modulator used for the two-level simulations, the three-level simulation model contains a switching time calculator block, based on the trapezoidal filter inductor current and charge-based modulation as discussed in Section II, and a separate gate control block. A schematic overview of the resulting simulation framework based on the converter configuration as described in this article is shown in Fig. 11.

The switching time calculator block uses the desired per-period average current $i_{\rm set}$ and output voltage $v_{\rm out}$ to calculate the switching times according to the method described in Section II-B. The gate control block generates the gate signals from the switching times by means of a state machine derived from the possible switching states as given in Table II. The switching time calculator block ensures ZVS and output current control, and the gate control block adds $v_{\rm Cx}$ balancing.

The zero-crossing detection block (ZCD) is added to determine the zero crossings of the filter inductor current $i_{\rm Lf}$. The detected zero crossings are used by the gate control block to synchronize the calculated switching times with the actual current, and by the $t_{\rm sw}$ calculating block to trigger the start of the calculations at each zero crossing of a rising edge of $i_{\rm Lf}$. The three-level simulation model contains the same antialiasing filters with a cutoff frequency of 100 kHz and output current controller $C_{\rm e}$ tuned to an open-loop bandwidth of 1 kHz as used for the two-level simulations.

C. DC Analysis

To analyze the basic differences between the two-level and three-level converter configurations with the corresponding modulation strategies, the simulation platforms discussed in the previous paragraphs are excited with a $i^*_{\rm set} = 5$ A dc set-point current. The resulting waveforms for the filter inductor current $i_{\rm Lf}$, switch node voltage $v_{\rm sn}$, and flying capacitor voltage $v_{\rm Cx}$ zoomed in at two switching periods are shown in Fig. 12.

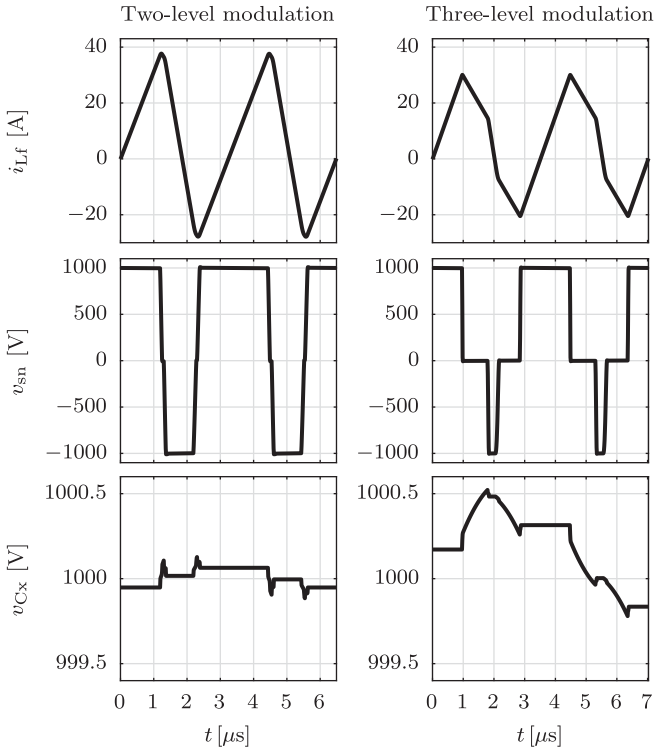


Fig. 12. Simulated waveforms for the filter inductor current i_{Lf}, switch node voltage v_{sn}, and flying capacitor voltage v_{Cx}. The results are obtained with the corresponding simulation frameworks for two- and three-level modulation, a set-point current of $i^*_{\mathrm{set}} = 5$ A, and zoomed in on two switching periods.

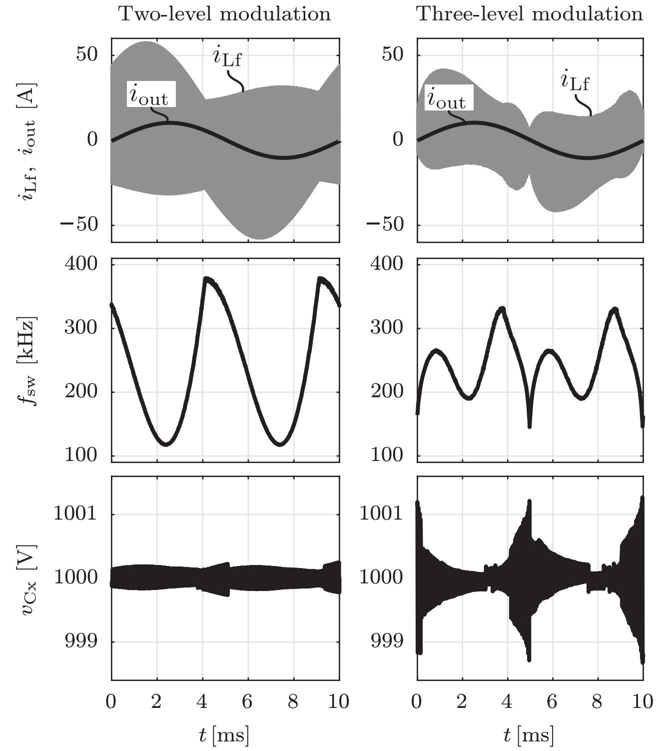


Fig. 13. Simulation results of the filter inductor current i_{Lf}, output current i_{out}, switching frequency f_{sw}, and flying capacitor voltage v_{Cx} for a single period of a 100-Hz sinusoidal set-point current for the two-level and three-level converter configurations.

TABLE VI
DC SIMULATION RESULTS

Parameter	Two-level	Three-level	Unit
$i_{\mathrm{Lf,rms}}$	20.6	16.8	$\mathrm{A_{rms}}$
$i_{\mathrm{Lf,pk,max}}$	37.9	30.0	A
$i_{\mathrm{Lf,pk,min}}$	−27.9	−20.5	A
f_{sw}	309	286	kHz
i_{error}	−2.66	−1.50	mA

The lower peak values of i_{Lf} obtained with the three-level converter configuration are clearly visible. The plots of the switch node voltages show the distinct two-level and three-level behavior, and the commutation of the switch node voltages during the resonance periods. A clear difference in the ripple voltages of the flying capacitors is shown in the bottom plots of Fig. 12, originating from the two-level versus three-level modulation. This is due to the flying capacitors having the same capacitance in the simulations for both converter configurations. In [7], the dimensioning of the flying capacitor is described analytically for triangular waveforms, which resulted in a significantly smaller capacitor value for equal voltage ripple requirements. The delay caused by the antialiasing filter for the v_{Cx} measurement results in an additional voltage ripple, as can be clearly observed in both the bottom plots of Fig. 12.

Specific characteristics derived from the simulation results of both converter configurations are shown in Table VI. The lower rms value of the filter inductor current $i_{\mathrm{Lf,rms}}$ for the three-level converter configuration will result in lower conduction losses in the switches S_{1-4} and filter inductor L_{f}, which are proportional to $i^2_{\mathrm{Lf,rms}}$. The lower peak value will result in lower turn-OFF losses of the switches, lower core losses in the filter inductor, and lower rms current through the filter capacitor C_{f}. This will be investigated further in the next paragraph. The switching frequencies are of the same order of magnitude; however, the three-level converter configuration contains additional freedom to tune the switching frequency to the desired specifications. The dc current error i_{error} is smaller for the three-level configuration, indicating that the per-period average generated current has a higher correspondence with the desired value.

D. AC Analysis

In order to compare the performance of the two-level and three-level modulation strategies for ac signals, simulations were performed for a sinusoidal set-point current with a frequency of $f_{\mathrm{i,set^*}} = 100$ Hz and amplitude $|i^*_{\mathrm{set}}| = 10$ A. An extensive loss breakdown analysis was performed for both modulation strategies on the simulation results obtained for the sinusoidal set-point current. In Fig. 13, the resulting filter inductor current i_{Lf}, output current i_{out}, switching frequency f_{sw}, and flying capacitor voltage v_{Cx} of both converter configurations are shown for a single period of the set-point current.

The plots in Fig. 13 show the different shapes of the filter inductor current and different range of the switching frequency as a result of the distinctive modulation strategies. The plots of the flying capacitor voltages indicate proper balancing of the capacitor voltages to V_{dc}. The difference in voltage ripple resulting from the active use of the additional voltage level for the three-level configuration is shown as well. However, the voltage ripple remains relatively low for the set-point current profile as used in the simulations.

1) Loss Breakdown Analysis: A loss breakdown analysis was performed on the obtained results, which incorporates the switching and conduction losses of the switches, core and conduction losses of the filter inductor, and the losses generated in the flying capacitor and filter capacitor.

In order to compare the switching losses $P_{\mathrm{loss,sw}}$ resulting from the different modulation strategies, the measurement results presented in [21] and [22] were used to derive an estimate of the losses for the switches used in this article. The results indicate a quadratic relation between the drain-source current at the turn-OFF moment $i_{\mathrm{sw,off}}$ and the corresponding switching energy $E_{\mathrm{sw,off}}$. A correction factor of 0.5 has been applied to the measured results to compensate for the difference in current handling between the SiC module used in the reference (∼200 A) and the SiC discrete component used in this article (∼100 A). This results in the following equation to give an estimation of the turn-OFF switching energy of a single switch:

$$E_{\mathrm{sw,off}} = \frac{1}{30} i_{\mathrm{sw,off}}^2 \;\; [\mu\mathrm{J}] \tag{14}$$

where $i_{\mathrm{sw,off}}$ is the current through the switch at the turn-OFF moment. The total switching losses for each converter configuration can be calculated by applying (14) for the turn-OFF current of each switch S_{1-4}, assuming ZVS is achieved and negligible turn-ON losses are generated. An estimate of the $R_{\mathrm{ds,on}}$ taken from the datasheet of the SiC discrete MOSFET used (Wolfspeed C2M0025120D [19]), and applied together with the currents through the switches, was used to determine the total conduction losses $P_{\mathrm{loss,cond}}$ in the switches.

To obtain estimates of the filter inductor losses, an extensive loss model was constructed which had the actual currents and voltages from the simulation frameworks as inputs. The modeled core losses $P_{\mathrm{loss,core}}$ are based on the improved generalized Steinmetz equation as presented in [23]. The wire losses $P_{\mathrm{loss,wire}}$ are based on the methods presented in [24] to obtain the estimated skin effect losses (including dc losses) and proximity effect losses. The parameters used in the models correspond to the inductor as it was designed for the hardware prototype, which will be detailed in Section IV.

To estimate the losses generated in the flying capacitor $P_{\mathrm{loss,Cx}}$ and filter capacitor $P_{\mathrm{loss,Cf}}$, the currents through the respective capacitors were extracted from the simulation frameworks. The ESRs of the capacitors as implemented in the hardware prototype were then used to calculate the corresponding losses.

Each individual loss component was determined for a single period of the 100 Hz set-point current, of which the results are summarized in Table VII. Due to the high switching frequency on which both converter configurations operate, the switching losses $P_{\mathrm{loss,sw}}$ and core losses $P_{\mathrm{loss,core}}$ are relatively high. Together with the conduction losses in the switches $P_{\mathrm{loss,cond}}$, these components dominate the loss breakdown. The almost two factor difference in losses between the two-level and three-level configurations is another important observation from the obtained results. Due to the lower rms and peak values of the current flowing through the switches, inductor, and filter capacitor, the corresponding losses are significantly smaller. Since the flying capacitor is actively delivering energy to the output in the three-level converter, the losses generated in the capacitor are higher. However, they remain insignificant compared to the losses generated in the switches and the inductor. From the loss breakdown analysis can be concluded that, applying three-level modulation results in a significant reduction in losses compared to two-level modulation.

TABLE VII
OVERVIEW OF LOSSES FROM AC SIMULATIONS

Parameter	Two-level	Three-level	HS	Unit
$P_{\mathrm{loss,sw}}$	38.9	12.4	44.3	W
$P_{\mathrm{loss,cond}}$	36.2	18.8	9.85	W
$P_{\mathrm{loss,core}}$	41.3	19.8	5.36	W
$P_{\mathrm{loss,wire}}$	18.1	8.58	3.40	W
$P_{\mathrm{loss,Cx}}$	0.149	0.430	0.270	W
$P_{\mathrm{loss,Cf}}$	1.66	0.792	0.365	W
$P_{\mathrm{loss,total}}$	136	60.8	63.5	W

The losses generated in the switches add up to 75.1 W for the two-level configuration and 31.2 W for the three-level configuration. In addition, simulation results were generated with three-level hard-switching modulation at $f_{\mathrm{sw}} = 200$ kHz, of which the results are aggregated in Table VII in column HS. The rms and peak values of the filter inductor current for the hard-switching configuration are lower than that for both soft-switching configurations, resulting in lower conduction losses and lower core and wire losses in the inductor. The switching losses have however increased significantly due to the included turn-ON losses of the switches, resulting in total switch losses of 54.1 W. Subsequently, the total losses of the three-level soft-switching configuration come out lower than that for the three-level hard-switching modulation.

2) Spectral Analysis: High-precision industrial applications require a high linearity of the generated output current [2], [4], [5], [12]. In order to analyze the performance improvement with respect to linearity of the three-level converter configuration when compared to the two-level configuration, spectral analysis is performed by exciting the respective simulation frameworks with a 100-Hz sinusoidal set-point current. The amplitudes of the harmonics of the 100-Hz base frequency are calculated using the Fourier coefficients of a single period of the 100-Hz sine wave. The resulting values for the first 20 harmonics are shown in Fig. 14. The amplitudes of the third and fifth harmonic are higher for the two-level configuration when compared to the three-level configuration, whereas the amplitudes for almost all other harmonics are higher for the three-level configuration. However, the amplitude of the third harmonic for the two-level configuration is the dominant frequency component.

To quantify the nonlinear characteristics for both two- and three-level modulation, the spurious free dynamic range (SFDR)

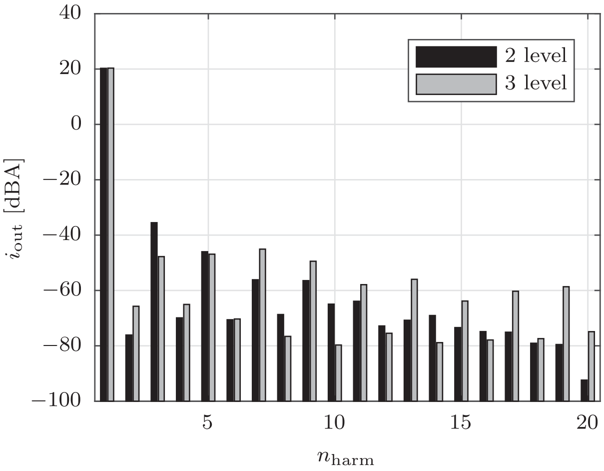


Fig. 14. Amplitudes of the first 20 harmonics of the 100-Hz base frequency calculated using Fourier coefficients of a single period of the 100-Hz sinusoidal set-point current for the two-level and three-level converter configurations.

TABLE VIII
CHARACTERISTICS FROM AC ANALYSIS

Parameter	Two-level	Three-level	Unit
SFDR	55.8	65.4	dB
THD	−55.4	−60.8	dB

and total harmonic distortion (THD) are calculated for the first 100 harmonics. The resulting values are gathered in Table VIII. From the spectral analysis can be concluded that, applying the three-level converter configuration results in an approximately 10-dB increase in SFDR and 5-dB decrease in THD. The performance of each converter configuration can be further improved by increasing the bandwidth of the output current control loop.

The position accuracy of a high-precision industrial application depends on the linearity of the output current generated by the power converter driving the actuators [4]. The increased linearity of the three-level converter configuration, as proposed by this article, with respect to the two-level converter configuration, which is based on an existing converter implementation, indicates potential performance improvement for a high-precision application.

IV. EXPERIMENTAL RESULTS

A hardware prototype setup was constructed of a three-level flying capacitor resonant pole inverter. The goal of the setup is to provide experimental results of the presented three-level modulation strategy, and validate the fast switching of high-voltage capabilities of the applied topology. A general description of the specifications of the prototype setup is given corresponding with the parameters used for the simulations performed in Section III. Measurements were performed to determine the actual required commutation charge Q_c, the delay incorporated in the zero-crossing detection, and dc and ac characteristics. The results of the measurements were used to improve the analytical description of the filter inductor current to better match the actual current.

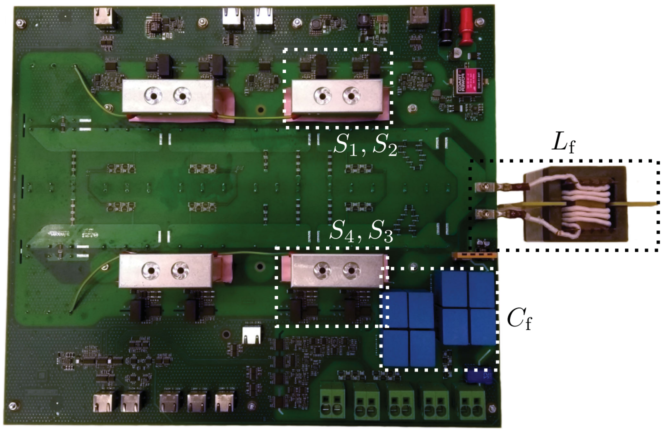


Fig. 15. Experimental setup with the four switches S_{1-4}, filter inductor L_f, and filter capacitor C_f indicated. The flying capacitor is located at the bottom of the PCB.

TABLE IX
SPECIFICATIONS OF PROTOTYPE SETUP

Parameter	Value	Unit
V_{dc}	1	kV
C_x	60	μF
L_f	18.9	μH
C_f	20	μF
R_o	73.5	Ω
L_o	2.28	mH

A. Prototype Setup

The three-level prototype, of which the circuit schematic is shown in Fig. 2, was constructed using Wolfspeed C2M0025120D SiC MOSFETs as switching devices. The circuit parameters of the prototype setup, as shown in Fig. 15, are summarized in Table IX. The value for C_x was determined using the reasoning presented in Section II-C, and selected from the restricted set of available components that can withstand the flying capacitor voltage equal to V_{dc} plus a certain margin. The filter inductor consists of four E-cores (TDK E70/33/32 N87) with eight turns of Litze wire and 3-mm air gaps, resulting in a measured inductance of 18.9 μH. A relatively large filter capacitor was chosen to limit the output voltage ripple. The resulting cutoff frequency of the L_f and C_f combination is around 8 kHz, leaving ample possibility to achieve the required bandwidth with sufficient phase margin.

The processor and field-programmable gate array (FPGA) of a dSpace Microlabbox were used to perform the calculation of the switching times and gate control, respectively. Closed-loop output current control was implemented for which the open-loop bandwidth was tuned to 1 kHz. The measured filter inductor current i_{Lf} was used for zero-crossing detection to synchronize the calculated switching times with the actual current. The control structure was set up according to the schematic overview given in Fig. 11. A differential voltage measurement circuit with a high CMMR was implemented to measure the flying capacitor voltage to facilitate active balancing of v_{Cx}.

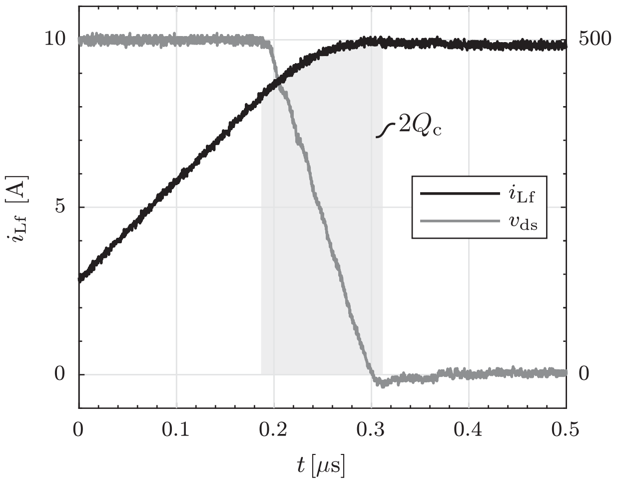
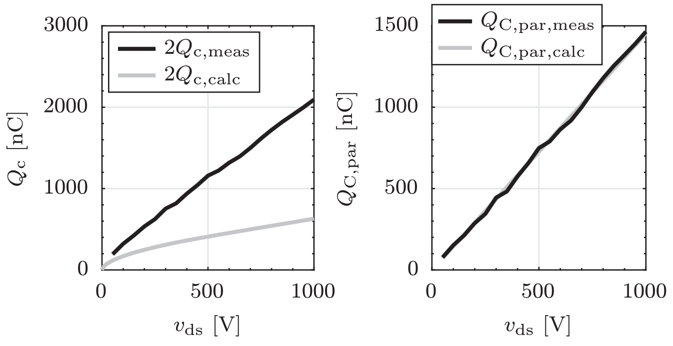


Fig. 16. Plot of the measurement results of the filter inductor current i_{Lf} (black) and the drain-source voltage v_{ds} (gray) of S_4 during commutation. The total commutation charge $2Q_{\mathrm{c}}$ is indicated with a light gray area underneath i_{Lf}. The supply voltage for this measurement was set to $V_{\mathrm{dc}} = 500$ V.



(a) (b)

Fig. 17. (a) Plot of the measured (black) and calculated (gray) total commutation charges $2Q_{\mathrm{c}}$ as a function of v_{ds}. (b) Plot of the measured (black) parasitic commutation charge $Q_{\mathrm{C,par,meas}}$, obtained by subtracting the calculated total commutation charge $2Q_{\mathrm{c,calc}}$ from the measured total commutation charge $2Q_{\mathrm{c,meas}}$ for the same voltage. The calculated (gray) parasitic commutation charge $Q_{\mathrm{C,par,calc}}$ represents a linear capacitance derived from $Q_{\mathrm{C,par,meas}}$.

B. Determination of Actual Required Commutation Charge

As indicated in [18], additional parasitic capacitance of the switch node may have a significant influence on the total charge required for complete commutation of the switch node voltage. This parasitic capacitance is expected to manifest itself, for instance, between printed circuit board (PCB) traces, and the parasitic capacitance of the filter inductor. Measurements were performed to investigate the actual charge required for commutation. The total commutation charge $2Q_{\mathrm{c}}$ was determined for a range of supply voltages V_{dc} by integrating the filter inductor current during commutation. An example of the resulting measurements of i_{Lf} and v_{ds} of S_4, and the resulting total commutation charge $2Q_{\mathrm{c}}$ for a supply voltage of $V_{\mathrm{dc}} = 500$ V, is shown in Fig. 16. The measurement procedure was repeated for a supply voltage range of $V_{\mathrm{dc}} = 50$–1000 V, and the resulting total commutation charge $2Q_{\mathrm{c,meas}}$ is shown in Fig. 17(a), together with the corresponding calculated values $2Q_{\mathrm{c,calc}}$.

As can be seen in Fig. 17(a), a significant difference exists between the measured total commutation charge $2Q_{\mathrm{c,meas}}$ and total commutation charge $2Q_{\mathrm{c,calc}}$ calculated from the datasheet of the MOSFET (see Fig. 6). This indicates a significant parasitic capacitance present in the hardware prototype. When the calculated total commutation charge is subtracted from the measured total commutation charge for the same voltage, the charge in the additional parasitic capacitance of the switch node is obtained, designated $Q_{\mathrm{C,par,meas}}$. Fig. 17(b) shows a plot of $Q_{\mathrm{C,par,meas}}$, which approximately represents a straight line and therefore, indicates a linear capacitance. When the average capacitance of all measurements is calculated and used to determine the corresponding charge in that capacitance, the line designated $Q_{\mathrm{C,par,calc}}$ in Fig. 17(b) is obtained. As can be concluded from the figure, the additional parasitic capacitance is indeed a linear capacitance, with value $C_{\mathrm{par}} = 1.45$ nF. This result is in line with the findings presented in [18] regarding the linearity of additional parasitic capacitance of the switch node. Moreover, the significant increase in required commutation charge will influence the peak and rms values of the filter inductor current.

C. DC Measurements

To verify the proper functioning of the proposed charge-based ZVS with trapezoidal filter current, measurements were performed with a dc set-point current of $i^*_{\mathrm{set}} = 0$ A and $i^*_{\mathrm{set}} = 5$ A. The resulting waveforms of the filter inductor current i_{Lf}, switch-node voltage v_{sn}, flying capacitor voltage v_{Cx}, and output voltage v_{out} are shown in Fig. 18 for two switching periods.

The measured waveform of v_{sn} shows the distinct three-level modulation resulting in the trapezoidal shape of i_{Lf}. The waveforms of v_{Cx} for both set-point currents indicate proper balancing of the flying capacitor voltage around V_{dc}. However, voltage spikes of v_{Cx} are clearly visible at switching instants which increase in magnitude for higher set-point currents. The prototype contains relatively large parasitic inductance loops between S_2, S_3, and C_{x}, and between S_1, C_{x}, S_4, and V_{dc}. The parasitic inductances result in ringing of v_{sn} during commutation, of which the amplitude increases with increased $\mathrm{d}v_{\mathrm{sn}}/\mathrm{d}t$, which in turn increases for higher i_{Lf}. The voltage spikes are visible in the waveforms of v_{out} and v_{sn} as well. The parasitic inductance can be greatly reduced by optimizing the PCB design to minimize the surface area of the loops.

To verify whether complete commutation of the switch-node voltage v_{sn} is achieved before turning ON a switch, the first commutation interval is investigated for $i^*_{\mathrm{set}} = 0$ A. In Fig. 19, a plot of the waveforms of i_{Lf}, $v_{\mathrm{gs,2}}$, $v_{\mathrm{gs,3}}$, and $v_{\mathrm{ds,3}}$ is shown for the interval corresponding with $[t_1, t_2]$ in Fig. 4. The plot shows that when $v_{\mathrm{gs,2}}$ decreases to below the MOSFET threshold voltage, commutation of $v_{\mathrm{ds,3}}$ from V_{dc} to 0 V is initiated. The waveform of $v_{\mathrm{gs,2}}$ shows that switch S_3 is turned-ON when $v_{\mathrm{ds,3}}$ is fully commutated and that zero-voltage turn-ON is achieved.

To verify complete commutation of the remaining intervals and for a nonzero set-point current, zoom-in plots are constructed around the commutation intervals as shown in Fig. 18. The filter inductor current i_{Lf} and switch-node voltage v_{sn} for the $i^*_{\mathrm{set}} = 0$ A set point are shown in Fig. 20, and the waveforms for

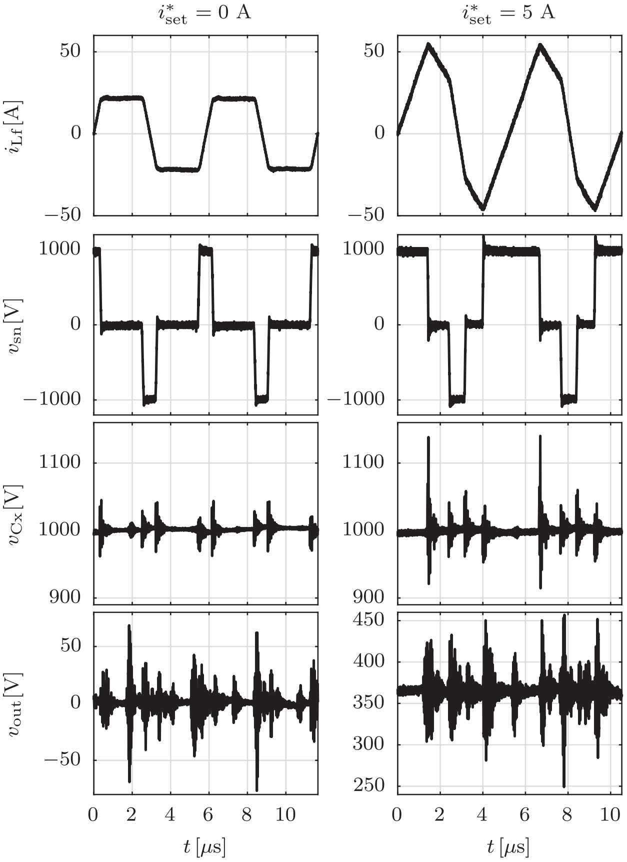


Fig. 18. Measurement results of the three-level FC RPI prototype for a set-point current of $i^*_{\rm set} = 0$ A (left) and $i^*_{\rm set} = 5$ A (right). For both set-point currents, the filter inductor current $i_{\rm Lf}$, switch node voltage $v_{\rm sn}$, flying capacitor voltage $v_{\rm Cx}$, and output voltage $v_{\rm out}$ are shown for two switching periods.

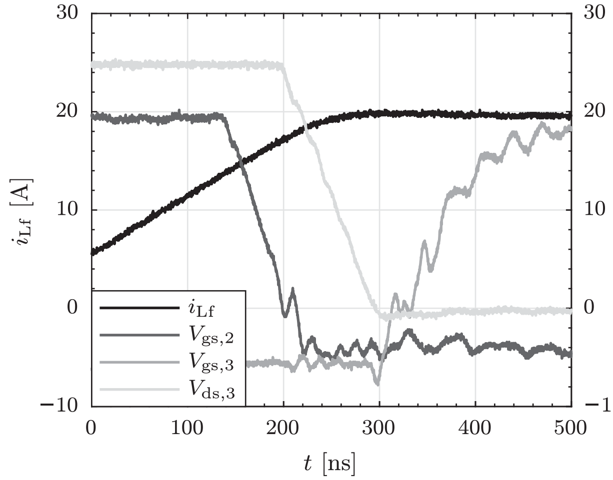


Fig. 19. Plot of $i_{\rm Lf}$, $v_{\rm gs,2}$, $v_{\rm gs,3}$, and $v_{\rm ds,3}$ during the first commutation interval, corresponding with $[t_1, t_2]$ in Fig. 4 for $i^*_{\rm set} = 0$ A. The waveform of $v_{\rm ds,3}$ is scaled down 40 times.

the $i^*_{\rm set} = 5$ A set point are shown in Fig. 21. The filter inductor current corresponds with the current flowing through a switch at turn-OFF, and the switch-node voltage corresponds with the drain-source voltage of the switch.

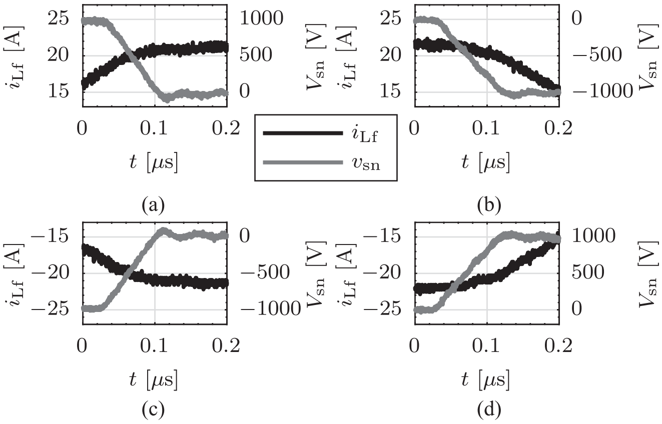


Fig. 20. Zoomed plots of the $i_{\rm Lf}$ (black) and $v_{\rm sn}$ (gray) waveforms for the commutation intervals as shown in Fig. 18 for $i^*_{\rm set} = 0$ A. (a) Commutation from $V_{\rm dc}$ to 0 V, (b) commutation from 0 V to $-V_{\rm dc}$, (c) commutation from $-V_{\rm dc}$ to 0 V, and (d) commutation from 0 V to $V_{\rm dc}$.

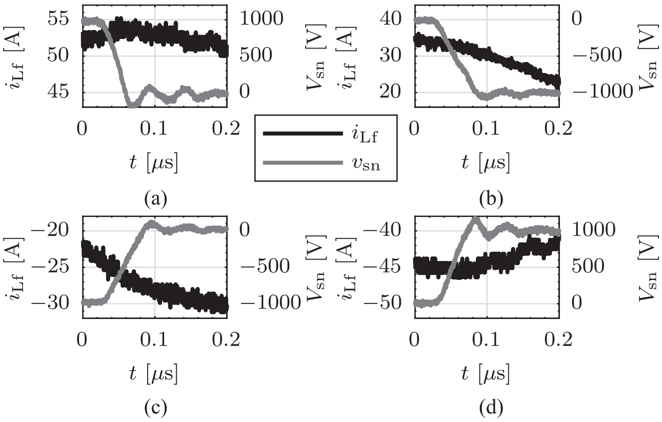


Fig. 21. Zoomed plots of the $i_{\rm Lf}$ (black) and $v_{\rm sn}$ (gray) waveforms for the commutation intervals as shown in Fig. 18 for $i^*_{\rm set} = 5$ A. (a) Commutation from $V_{\rm dc}$ to 0 V, (b) commutation from 0 V to $-V_{\rm dc}$, (c) commutation from $-V_{\rm dc}$ to 0 V, and (d) commutation from 0 V to $V_{\rm dc}$.

The zoomed plots of Fig. 20 show the complete commutation of the switch-node voltage $v_{\rm sn}$ for each of the commutation intervals for $i^*_{\rm set} = 0$ A. A small overshoot occurs at the end of the commutation intervals due to the parasitic inductance in the converter. When the commutation is complete, the body diode of the switch that is to be turned ON starts conducting and the oscillation is damped. The almost linear behavior of $v_{\rm sn}$ during commutation is due to the parasitic capacitance of the switch node, as was shown in Fig. 17. In the case where $i^*_{\rm set} = 0$ A, the circulating filter inductor current is minimal, resulting in the worst case ZVS realization scenario. From Fig. 20 can be concluded that, complete commutation of $v_{\rm sn}$ is achieved for all commutation intervals in the case of $i^*_{\rm set} = 0$ A.

The zoomed plots of Fig. 21 again show complete commutation of $v_{\rm sn}$ for higher circulating currents. Since the time scale of Figs. 20 and 21 are identical, the differences in duration of the commutation intervals, and therefore, slopes of $v_{\rm sn}$ are clearly visible. Due to the faster commutation of $v_{\rm sn}$ for higher $i_{\rm Lf}$ at turn-OFF of a switch, the overshoot of $v_{\rm sn}$ occurring at the

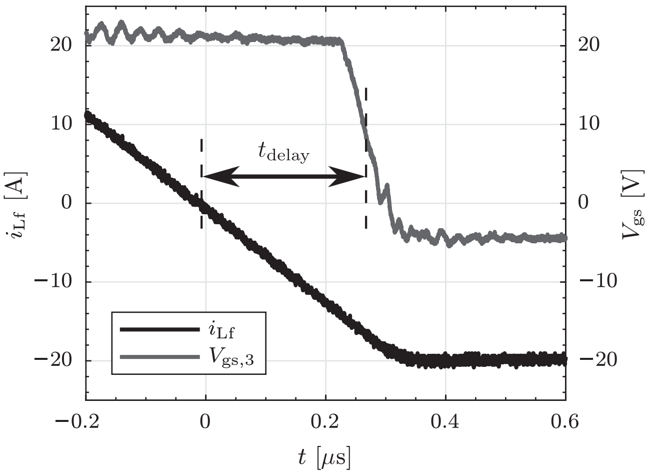


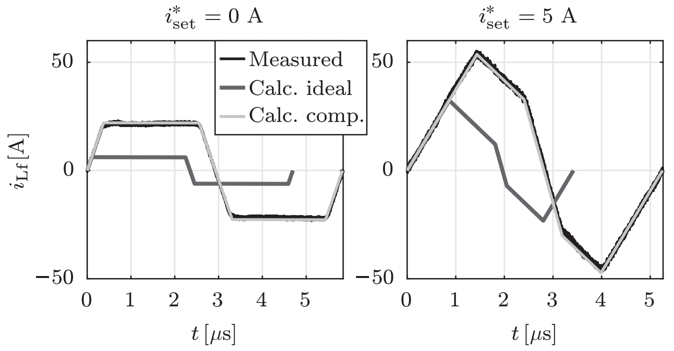
Fig. 22. Plots of the measured waveforms of i_{Lf} and $V_{\mathrm{gs,3}}$ at a negative zero crossing of i_{Lf}. The time delay between the zero crossing of i_{Lf} and the turn-OFF instant of S_3 when $V_{\mathrm{gs,3}}$ reaches the threshold voltage of the switch is indicated with t_{delay}.

end of the commutation interval increases significantly. This explains the voltage spikes shown in the plots of v_{Cx} and v_{out} of Fig. 18, which should remain limited to make sure the breakdown voltages of the components involved are not exceeded.

D. Compensation of Zero-Crossing Detection Delay

When comparing the measured waveforms of Fig. 18 with their equivalent obtained by simulation as shown in Fig. 12, the increased peak values for the filter inductor current stand out. The increased peak values originate to a small extent from the increased required commutation charge, as described in Section IV-B. However, the delay introduced in the detection of the zero crossing of the filter inductor current and the subsequent turn-OFF of the appropriate switch has a more significant impact. This is shown in Fig. 22, where the time delay t_{delay} between the zero crossing of i_{Lf} and the subsequent turn-OFF of S_3 is indicated. The total delay amounts to around $t_{\mathrm{delay}} = 310$ ns which should be 0 s for this particular scenario where $i^*_{\mathrm{set}} = 0$ A and $v_{\mathrm{out}} = 0$ V. The main causes for the delay are the analog front-end of the Microlabbox and the gate driver. The impact can be mitigated in future designs by discarding the Microlabbox by using local control, and a gate driver with minimal propagation delay.

The increased required commutation charge Q_{c} in the hardware prototype can be easily implemented in the calculations of the switching times. The results shown in Fig. 18 indicate that piecewise linear approximation of i_{Lf} is still valid, especially for higher circulating currents. However, it is not possible to eliminate the significant delay introduced between the zero crossing of i_{Lf} and actual turn-OFF of a switch. Nonetheless, it is possible to take the delay into account when calculating the switching times by setting a minimum time for the intervals $[t_0, t_1]$ and $[t_5, t_6]$ as indicated in Fig. 4. The minimum time for both intervals is set equal to t_{delay} and the calculation of the switching times progresses accordingly.



(a) (b)

Fig. 23. Waveforms of i_{Lf} for a single switching period with (a) $i^*_{\mathrm{set}} = 0$ A and (b) $i^*_{\mathrm{set}} = 5$ A. The measured waveforms are plotted in black, the calculated ideal waveforms in dark gray, and the compensated calculated waveforms in light gray.

The resulting waveforms of i_{Lf} for the compensated calculations are shown in Fig. 23 for both $i^*_{\mathrm{set}} = 0$ A and $i^*_{\mathrm{set}} = 5$ A. The corresponding measured waveforms are shown in black, the ideal calculated waveforms in gray, and the compensated calculated waveforms in light gray. The significant differences between the ideal calculated waveforms and measured waveforms are illustrated again in the figure. Nonetheless, the compensated calculated waveforms, including the increased commutation charge $Q_{\mathrm{c,meas}}$ and zero-crossing detection delay t_{delay}, show a significant correspondence with the measured waveform of i_{Lf}. Subsequently, the compensated calculated switching times are implemented in the hardware prototype and used to generate the measurement results.

E. AC Measurements

The ac performance of the three-level FC RPI was verified using a sinusoidal set point current with frequency $f_{\mathrm{i,set^*}} = 100$ Hz and amplitude $|i^*_{\mathrm{set}}| = 10$ A. The resulting waveforms of the output current i_{out}, output voltage v_{out}, filter inductor current i_{Lf}, and flying capacitor voltage v_{Cx} are shown in Fig. 24 for a single period of the 100-Hz sine wave.

The waveforms of i_{out} and v_{out} adopt the 100 Hz sinusoidal set point, with the addition of small spikes originating from the switching behavior, as was indicated in Fig. 18. The measured waveform of i_{Lf} shows similarities with its simulated counterpart shown in Fig. 13. However, due to the nonidealities explained in the previous paragraph, the envelope has a higher peak value. Moreover, a step in the envelope is clearly visible when the modulator switches between quadrants, due to the fact that the impact of the zero-crossing detection delay changes.

The waveform of v_{Cx} indicates proper balancing of the flying capacitor voltage around the reference voltage of 1 kV. The voltage spikes due to the switching behavior are visible in this plot as well, and are dominant with respect to the voltage ripple resulting from the voltage regulation. However, from the measured waveforms can be concluded that, a properly functioning converter is constructed.

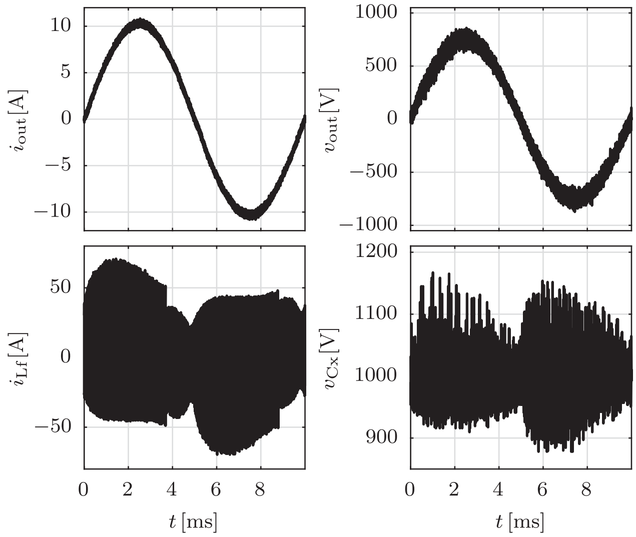


Fig. 24. Measurement results of the three-level FC RPI prototype for a sinusoidal set-point current with frequency $f_{\mathrm{i,set}^*} = 100$ Hz and amplitude $|i^*_{\mathrm{set}}| = 10$ A. The waveforms of the output current i_{out}, output voltage v_{out}, filter inductor current i_{Lf}, and flying capacitor voltage v_{Cx} are shown for a single period of the 100-Hz sine wave.

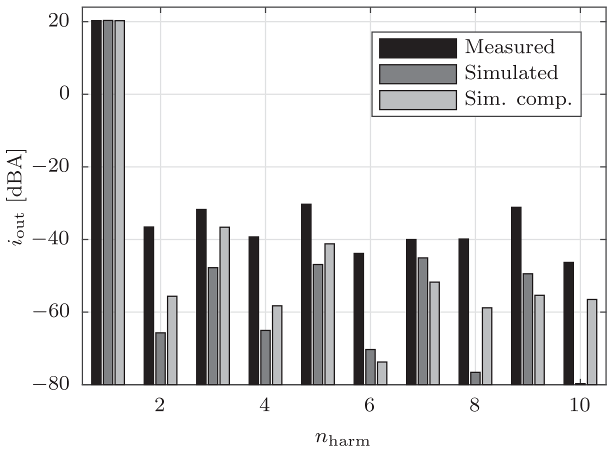


Fig. 25. Amplitude of the first ten harmonics of the measured and simulated output current i_{out} for a single period of the 100-Hz sinusoidal set-point current.

To investigate the linearity of the measured output current, the amplitudes of the harmonics are calculated using the Fourier coefficients of a single period of the 100-Hz sine wave of i_{out} with $|i^*_{\mathrm{set}}| = 10$ A. The resulting values for the first ten harmonics are shown in Fig. 25 for the measurements, ideal simulations, and simulations with the compensated switching time calculations. The SFDR and THD were calculated for the first 100 harmonics, and the resulting SFDR is 50.6 dB and THD is −43.4 dB for the measured i_{out}, which are significantly lower and higher, respectively, than the results obtained from the ideal simulations (respectively, 65.4 and −60.8 dB). The values for the results with the compensated switching time calculations are SFDR: 56.9 dB and THD: −54.8 dB, which still do not correspond with the measured values. This is also indicated by the bar plot in Fig. 25, where an increased correlation is visible only for the third harmonic.

The decreased linearity of the measured output current originates from several nonidealities that were not taken into account for the simulations. Sampling and quantization of the measured voltages and currents were not taken into account in the simulations performed in Section III. The simulations containing the compensated switching calculations did take sampling and quantization into account according to the values obtained with the hardware prototype. However, for instance delays and jitter in digital signal chains, and nonlinearity of the output current sensor and zero-crossing detection of the filter inductor current were not included in the simulation frameworks.

Furthermore, a suboptimal PCB layout of the converter introduced relatively large parasitic induction loops resulting in resonances on the switching nodes. Significant capacitive coupling inside the PCB between switching nodes and supply nodes, and outside the PCB between the flying capacitor and bus capacitors, result in the switching behavior being visible on the output voltage and output current measurements and on all other measurement signals.

However, from both the dc and ac measurements can be concluded that the proposed charge-based ZVS modulation scheme applied to a three-level FC RPI functions properly. The performance with respect to the quality of the generated output current is less than what was expected from the simulation results. Future work will incorporate the construction of a prototype specifically designed to mitigate the presented issues and to investigate further potential performance improvements.

V. CONCLUSION

A three-level flying capacitor resonant pole inverter configuration is described, to which a multilevel modulation strategy was applied. Charge-based analysis of the piecewise linear approximation of the filter inductor current was implemented to ensure ZVS across the entire operating range and minimize the total losses. The resulting three-level converter configuration has reduced voltage stress and generates a high output voltage with a high switching frequency.

An elaborate simulation framework has been constructed to compare the proposed three-level configuration with an existing two-level configuration. From the simulation results can be concluded that increasing the number of voltage levels results in significantly lower switch and inductor losses, and increased linearity of the generated output current. The latter indicates a potential performance improvement of a high-precision industrial application with respect to position accuracy. The extra computational resources required for the proposed multilevel modulation strategy with charge-based ZVS are readily available in modern FPGAs and system on chips (SoCs).

A hardware prototype of the three-level converter configuration has been constructed, and measurements obtained from the prototype verify the proper functioning of the multilevel modulation strategy with charge-based ZVS. However, a significant discrepancy was observed between the obtained measurement and simulation results. The divergence originated from an increased required commutation charge, and a delay between the zero crossing of the filter inductor current and the turn-OFF instant of a switch. Results obtained with compensated switching time calculations were presented, indicating a significant improvement. From the resulting measurements can be concluded that, fast switching of high voltage was achieved with a relatively high accuracy and linearity of the generated output current.

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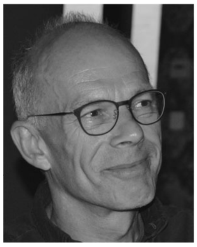

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