Topology and Control of a Four-Level ANPC Inverter

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***Abstract*—Four-level hybrid-clamped inverter is a newly proposed topology that can operate under a wide voltage range without switches connected in series. However, when it is applied in medium voltage high power conversions, the flying capacitors in each phase will occupy a huge volume and a high switching frequency is required to restrain the voltage ripples. In order to overcome this drawback, a four-level active neutral-point clamped inverter is discussed in this paper, which consists of only six switches and no diodes or flying capacitors are required. In order to balance the neutral-point voltages under the full power factor and modulation index range, a capacitor voltage balance method based on carrier-overlapped pulsewidth modulation is proposed in this paper. The upper and lower dc-link capacitor voltages are balanced by zero-sequence voltage injection and the central dc-link capacitor voltage is balanced by adjusting the duty cycles of switching signals slightly. Simulation and experimental results are presented to confirm the validity of this method.**

***Index Terms*—Active neutral-point clamped (ANPC), multilevel converter, pulsewidth modulation (PWM), voltage balance.**

I. Introduction

THREE-LEVEL neutral-point clamped (NPC) inverters are widely used in industry for its simple structure, low dv/dt and high power quality [1], [2]. In high-power applications, such as rolling mills, pumps, ship propulsion and conveyors, three-level NPC inverters allow a higher dc-link voltage over two-level converters and can avoid the series connection of active switches. However, when it is extended to higher voltage levels, not only the number of diodes increases rapidly, but also the dc-link neutral-point (NP) potentials are hard to be balanced with passive front-ends [3]–[5].

In order to improve the output voltage levels and reduce the number of devices, a five-level active NPC (ANPC) inverter is proposed in [6], which can be seen as the combination of a three-level ANPC inverter and a two-level cell. Its dc-link is divided into two parts and it is easy to balance the NP voltage [7], [8]. The main problem of this topology is the unequal voltage stresses of switches, which will bring the dynamic voltage-sharing problem of the series-connected switches in medium-voltage applications.

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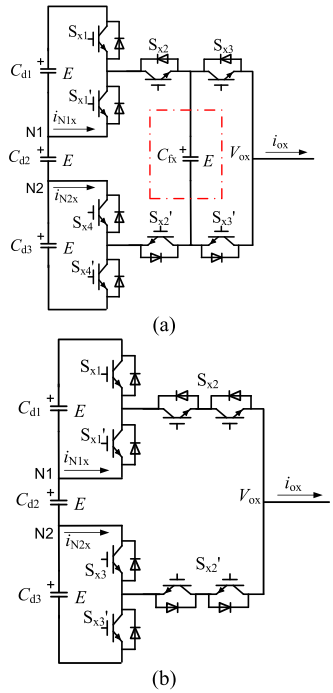


Fig. 1. Phase circuits of (a) four-level hybrid clamped inverter and (b) four-level ANPC inverter.

Based on the similar concept, a four-level hybrid-clamped inverter is proposed in [9], as shown in Fig. 1(a), which can avoid the series connection of switches. Although its dc-link is divided into three parts, it is easy to balance the NP voltages with phase-shifted pulsewidth modulation (PWM) due to the extra redundant switching states brought by the flying capacitor [10]. However, in high power medium voltage applications, a large flying capacitor is required due to the low switching frequency, which will lower the power density and increase the cost significantly.

Actually, the flying capacitor in the four-level hybrid-clamped inverter can be removed directly, as shown in Fig. 1(b) [11]. Since no diodes or flying capacitors are used, it can be regarded as a true four-level ANPC inverter. Similar with four-level NPC inverters, the main issue of this topology is still the NP voltage balance problem [12].

For the four-level NPC inverter, it has been proved that the NP potentials cannot be balanced under the full power factor and modulation index range with traditional phase-disposition PWM (PDPWM) or nearest three-vector (NTV) PWM [3]. The theoretical balance boundary also exists in this four-level ANPC inverter. Virtual-space-vector based PWM is a good method that can achieve the NP voltage balancing under the full modulation

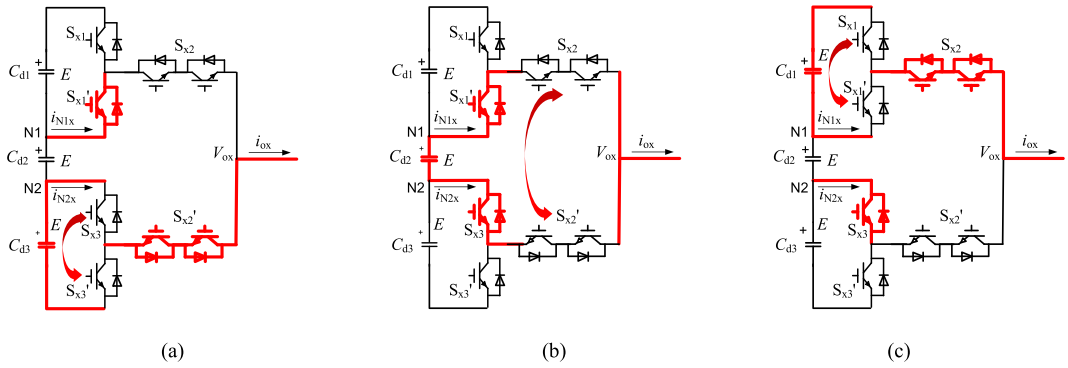


Fig. 2. Commutations between different voltage levels. (a) Commutation between 0 and E. (b) Commutation between E and $2E$. (c) Commutation between $2E$ and $3E$.

index and load power factor range [12]–[14]. Each virtual vector is generated by more than one switching state to guarantee that the average values of each NP current equal to zero in every switching period. The main shortcoming of this method is the complex modulation implementation. Model-predictive control (MPC) is another popular method to balance the capacitor voltages of various multilevel converters by optimizing a cost function [15]–[17]. However, the MPC also has many problems, such as large computation burden, uncertain weighting coefficient, and inconstant switching frequency.

Carrier-overlapped PWM (COPWM) is a newly proposed modulation method which satisfies the volt-second balance principle [18]. It provides a new idea to balance the NP voltages of neutral-point clamped multilevel converters. However, just like PDPWM for three-level NPC inverters, a closed-loop balance control is also required to get a better voltage balance performance under all operating conditions.

This paper is organized as follows. Section II introduces the operating principles and modulation method of the four-level ANPC converter. Section III introduces the NP voltage balance method based on COPWM in detail. Simulation and experimental results are presented in Sections IV and V. Finally, Section VI concludes this paper.

II. Operating Principles and Modulation Method

As shown in Fig. 1, the four-level ANPC inverter can be regarded as a four-level hybrid-clamped inverter without flying capacitors. Hence, the number of redundant switching states will be reduced and the voltage stresses of different switches will be different. The first problem will lead to the voltage imbalance of three dc-link capacitors and the second problem will lead to the uneven voltage-sharing of series connected switches.

Assuming that the dc-link voltage is $3E$ and equally divided among the upper, central, and lower dc-link capacitors, in order to output four voltage levels, the following operating rules should be obeyed.

1) Switches $S_{x1}-S_{x3}$ and S'_{x1}–S'_{x3} are complementary, respectively.
2) S_{x3} must be turned ON before S_{x2} is turned ON and S_{x2} must be turned ON before S_{x1} is turned ON. So that S_{x2} and S'_{x2} always bear a maximal voltage stress of $2E$. If S_{x1} and S'_{x3} are turned ON at the same time, S_{x2} or S'_{x2} will bear the total dc-link capacitor voltage.

TABLE I
Switching States of the 4L-ANPC Inverter

S_{x1}	S_{x2}	S_{x3}	S_{x1}'	S_{x2}'	S_{x3}'	i_{N1x}	i_{N2x}	V_{ox}	V_{ce2}
0	0	0	1	1	1	0	0	0	$2E$
0	**0**	**1**	**1**	**1**	**0**	**0**	$\boldsymbol{i_{ox}}$	$\boldsymbol{E}$	$\boldsymbol{E}$
0	**1**	**1**	**1**	**0**	**0**	$\boldsymbol{i_{ox}}$	**0**	$\boldsymbol{2E}$	**0**
1	1	1	0	0	0	0	0	$3E$	0

Based on the earlier operating principles, all the switching states are given in Table I, where i_{ox} is the phase current, i_{N1x} and i_{N2x} are the currents flowing out of neutral points N1 and N2, V_{ox} is the output voltage level and V_{ce2} is the voltage stress of S_{x2}. Subscript symbol x represents phase a, b, or c. The commutation processes between different voltage levels are also shown in Fig. 2.

It should be noticed that S_{x2} and S'_{x2} will bear a voltage stress of $2E$ at maximum, which is a shortcoming of this topology. In medium-voltage applications, in order to bear the doubled voltage stress, two switches need to be connected in series and turned ON or OFF synchronously, which will result in the dynamic voltage sharing problem. Generally speaking, due to the driver circuit delay or the dispersion of device characteristics, the switch turned ON later or turned OFF earlier will bear the total voltage stress, which may decrease the reliability of the whole system. However, this problem is not so severe in this topology. Because S_{x2} bears the voltage stress $2E$ only when the output voltage level is 0. When the output voltage transits between 0 and E, the voltage stress of S_{x2} will transit between $2E$ and E. During this process, S_{x2} is turned OFF all the time, as shown in Fig. 2(a). The static voltage sharing can be realized easily by parallel connected snubber capacitors or resistors. So the equalized voltage sharing in S_{x2} is easy to realize and there is no dynamic voltage sharing problem related to the switching transient in this condition. The switches S_{x2} and S'_{x2} act only when the voltage level transits between E and $2E$, as shown in Fig. 2(b). In this condition, the voltage stress of S_{x2} or S'_{x2} is only E. So S_{x2} and S'_{x2} can adopt two switches connected

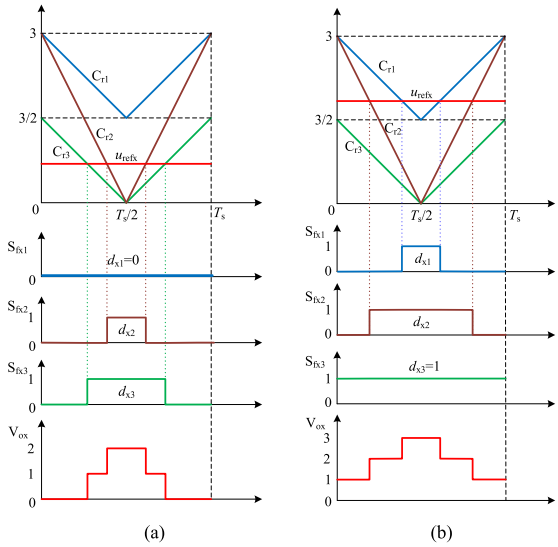


Fig. 3. Diagram of the four-level COPWM method. (a) $0 \le u_{\text{ref}x} < 3/2$. (b) $3/2 \le u_{\text{ref}x} \le 3$.

in series in medium-voltage applications and will not have the dynamic voltage sharing problem.

Another problem is the voltage imbalance of three dc-link capacitors. In order to solve this problem, a newly proposed four-level COPWM [18] can be used to control this inverter, as shown in Fig. 3. The negative pole of the dc-link is referred as the zero potential and 1/3 of the dc-link voltage is selected as the base value. Then, the range of the reference phase voltage $u_{\text{ref}x}$ is from 0 to 3. Three triangular carrier waves C_{r1}, C_{r2} and C_{r3} are phase synchronous and corresponding to switches S_{x1}, S_{x2} and S_{x3}, respectively.

Different from PDPWM, carriers C_{r1} and C_{r3} are level-shifted with the peak-to-peak value 3/2 while carrier C_{r2} overlaps both C_{r1} and C_{r3} with the peak-to-peak value 3.

Defining the switching functions of switches $S_{x1}-S_{x3}$ are $\mathrm{S}_{fx1}-\mathrm{S}_{fx3}$, then the duty cycles of $S_{fx1}-S_{fx3}$ in a carrier period can be written as follows [18]:

$$\left.\begin{aligned} d_{x1} &= 0 \\ d_{x2} &= \tfrac{1}{3}u_{\text{ref}x} \\ d_{x3} &= \tfrac{2}{3}u_{\text{ref}x} \end{aligned}\right\},\ 0 \le u_{\text{ref}x} \le \frac{3}{2} \tag{1}$$

$$\left.\begin{aligned} d_{x1} &= \tfrac{2}{3}\left(u_{\text{ref}x} - \tfrac{3}{2}\right) \\ d_{x2} &= \tfrac{1}{3}u_{\text{ref}x} \\ d_{x3} &= 1 \end{aligned}\right\},\ \frac{3}{2} \le u_{\text{ref}x} \le 3. \tag{2}$$

It is easy to obtain the average output voltage in a carrier period as follows:

$$u_{ox} = d_{x1} + d_{x2} + d_{x3} = u_{\text{ref}x} \tag{3}$$

which means the COPWM method satisfies the volt-second balance principle [18].

III. NP Voltage Balance Method

According to Table I, the load current flows out of neutral point N1 when the voltage level is $2E$ and out of N2 when the voltage level is E. Hence, the average NP currents of a single phase in a carrier period can be written as

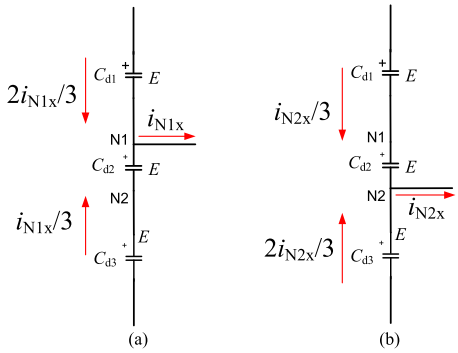


Fig. 4. Influences of NP currents to the dc-link capacitor voltages.

$$\begin{cases} \bar{i}_{\text{N1}x} = (d_{x2} - d_{x1}) \cdot i_{ox} \\ \bar{i}_{\text{N2}x} = (d_{x3} - d_{x2}) \cdot i_{ox} \end{cases} \tag{4}$$

where $\bar{i}_{N1x}$ and $\bar{i}_{N2x}$ are the average currents out of neutral points N1 and N2 in a carrier period. Assuming the dc-link capacitances are $C_{d1} = C_{d2} = C_{d3} = C_d$, then the distribution of NP currents among the dc-link capacitors is shown in Fig. 4.

Then, the influences of average NP currents to the dc-link capacitor voltages in a carrier period can be written as follows:

$$\Delta u_{d1x} = \frac{2}{3} \cdot \frac{\bar{i}_{N1x} \cdot T_s}{C_d} + \frac{1}{3} \cdot \frac{\bar{i}_{N2x} \cdot T_s}{C_d} \tag{5a}$$

$$\Delta u_{d2x} = -\frac{1}{3} \cdot \frac{(\bar{i}_{N1x} - \bar{i}_{N2x}) \cdot T_s}{C_d} \tag{5b}$$

$$\Delta u_{d3x} = -\frac{1}{3} \cdot \frac{\bar{i}_{N1x} \cdot T_s}{C_d} - \frac{2}{3} \cdot \frac{\bar{i}_{N2x} \cdot T_s}{C_d}. \tag{5c}$$

From (5) it can be seen, the three capacitor voltages are affected by the two NP currents at the same time. Although it has been proved that the COPWM can achieve the natural voltage balance of the three dc-link capacitors under ideal and steady states, it may diverge under nonideal and dynamic conditions if not controlled. Hence, a closed-loop control is required to regulate the three dc-link capacitor voltages. Assuming the total dc-link voltage is constant, and then the NP potential balance can be decoupled into the following two steps.

1) Voltage balancing between the upper and lower dc-link capacitors.
2) Voltage balancing of the central dc-link capacitor.

A. Voltage Balancing Between the Upper and Lower DC-Link Capacitors

For the upper and lower dc-link capacitors, the unbalanced voltage Δu_{Nx} caused by phase x can be written as follows:

$$\Delta u_{Nx} = \Delta u_{d3x} - \Delta u_{d1x} = -\frac{(\bar{i}_{N1x} + \bar{i}_{N2x}) \cdot T_s}{C_d} \tag{6}$$

which means that the deviation of the upper and lower dc-link capacitor voltages depends on the sum of the two NP currents. According to (1), (2), and (4), the total NP current $\bar{i}_{Nx}$ of a single

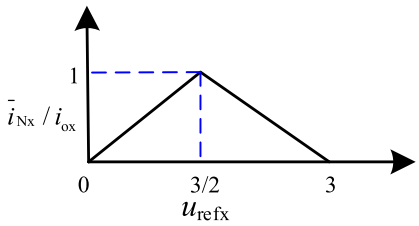


Fig. 5. Relationship between the total NP current and the reference phase voltage.

phase can be written as

$$\bar{i}_{Nx} = \bar{i}_{N1x} + \bar{i}_{N2x} = \begin{cases} \frac{2}{3}u_{\text{ref}x} \cdot i_{ox}, & 0 \le u_{\text{ref}x} < 3/2 \\ (2 - \frac{2}{3}u_{\text{ref}x}) \cdot i_{ox}, & 3/2 \le u_{\text{ref}x} \le 3 \end{cases} \tag{7a}$$

which can be further simplified as

$$\bar{i}_{Nx} = \left(1 - \left|\frac{2}{3}u_{\text{ref}x} - 1\right|\right) \cdot i_{ox}. \tag{7b}$$

From (7) it can be seen, the relationship between $\bar{i}_{Nx}$ and $u_{\text{ref}x}$ is a piecewise function that is similar with three-level NPC inverters [19], as shown in Fig. 5.

For a three-phase three-wire inverter system, there exists $i_{oa} + i_{ob} + i_{oc} = 0$, so the average total NP current can be written as follows:

$$\bar{i}_N = \bar{i}_{Na} + \bar{i}_{Nb} + \bar{i}_{Nc} = -\sum_{x=a,b,c}\left|\frac{2}{3}u_{\text{ref}x} - 1\right| \cdot i_{ox}. \tag{8}$$

In order to eliminate the voltage deviation of the upper and lower dc-link capacitors in a carrier period, according to (6), an average total NP current is expected to be injected into N1 and N2. The demanded total NP current can be written as

$$\bar{i}_{N,\text{ref}} = C_d\frac{(u_{d3} - u_{d1})}{T_s} \tag{9}$$

where u_{d1} and u_{d3} are the upper and lower dc-link capacitor voltages, C_d is the capacitance of three dc-link capacitors.

Since the total NP current depends on the reference voltage, classic zero-sequence voltage (ZSV) injection method can be used to regulate the total NP current. The actual reference modulation voltage after ZSV injection is defined as follows:

$$u'_{\text{ref}x} = u_{\text{ref}x} + u_z \tag{10}$$

where u_z is the ZSV. The three-phase average total NP current can be rewritten as follows:

$$\bar{i}'_N = \bar{i}'_{Na} + \bar{i}'_{Nb} + \bar{i}'_{Nc} = -\sum_{x=a,b,c}\left|\frac{2}{3}u'_{\text{ref}x} - 1\right| \cdot i_{ox}. \tag{11}$$

From (10) and (11) it can be seen that the relationship between the total NP current and ZSV is a piecewise-linear function. The inflection points are the ZSVs that make $2u'_{\text{ref}x}/3 - 1$ equal to zero, that is to say, the ones that make one of the three-phase reference voltages equal to 1.5. In order to avoid over-modulation, according to (10), the minimal and maximal ZSVs can be defined as follows:

$$\begin{cases} u_{z\min} = -u_{\text{ref},\min} \\ u_{z\max} = 3 - u_{\text{ref},\max} \end{cases} \tag{12}$$

where $u_{\text{ref},\min}$ and $u_{\text{ref},\max}$ are the minimal and maximal values of the original three-phase reference voltages $u_{\text{ref}a}$, $u_{\text{ref}b}$, and $u_{\text{ref}c}$, respectively.

Although the relationship of the total NP current and ZSV is derived in (11), it is also difficult to compute the expression of the precise ZSV to generate the demanded total NP current directly. A simple solution to this problem is to consider a limited number of ZSVs which are called key ZSVs. Calculating the corresponding average total NP currents of these key ZSVs and comparing them with the demanded average total NP current in (9), respectively, the one who generates the most approximate NP current is chosen as the most appropriate ZSV.

In this paper, the minimal, maximal, and all the ZSVs on the inflection points are selected as the key ZSVs. An example of three-phase reference voltages before and after key ZSV injection under COPWM is shown in Fig. 6. It should be noticed that there are at most three ZSVs on the inflection points.

So the upper and lower dc-link capacitor voltage balancing can be divided into the following steps.

1) First, the minimal, maximal and all the ZSVs on the inflection points are calculated as the key ZSVs and denoted by $u_{zj}(j = 1, 2, 3\ldots)$.
2) Second, calculate the demanded total NP current $i_{N,\text{ref}}$ to balance the voltage deviation according to (9).
3) Third, calculate the corresponding total NP currents i_{Nzj} of these key ZSVs according to (11).
4) Finally, compare the demanded total NP current $i_{N,\text{ref}}$ with i_{Nzj}. The one that generates the most approximate NP current to the demanded total NP current is chosen as the optimal ZSV.

B. Voltage Balancing of the Central DC-Link Capacitor

After the upper and lower dc-link capacitor voltages are balanced by the optimal ZSV injection, the next step is to balance the central dc-link capacitor voltage. According to (4) and (5b), the central dc-link capacitor voltage is affected by the difference of the two NP currents, which can be seen as the average current flowing out of the central dc-link capacitor and can be written as follows:

$$\bar{i}_{d2x} = \bar{i}_{N1x} - \bar{i}_{N2x} = (2d_{x2} - d_{x1} - d_{x3}) \cdot i_{ox}. \tag{13}$$

Substituting (1) and (2) into (13), it is easy to get that $2d_{x2} - d_{x1} - d_{x3}$ always equals to zero, which means the central dc-link capacitor voltage can maintain balanced in a carrier period under ideal and steady conditions. If a voltage deviation appears, according to (13), a way to regulate the central dc-link capacitor voltage is to adjust d_{x1}, d_{x2}, and d_{x3}. In order to not affect the average output voltage, according to (3), the sum of d_{x1}, d_{x2}, and d_{x3} should not be changed.

Taking $u_{d2} < E$ and $i_{ox} > 0$ as an example, according to (5b) and (13), $\bar{i}_{d2x}$ and $2d_{x2} - d_{x1} - d_{x3}$ should be decreased and negative to charge C_{d2}. There are two conditions as follows.

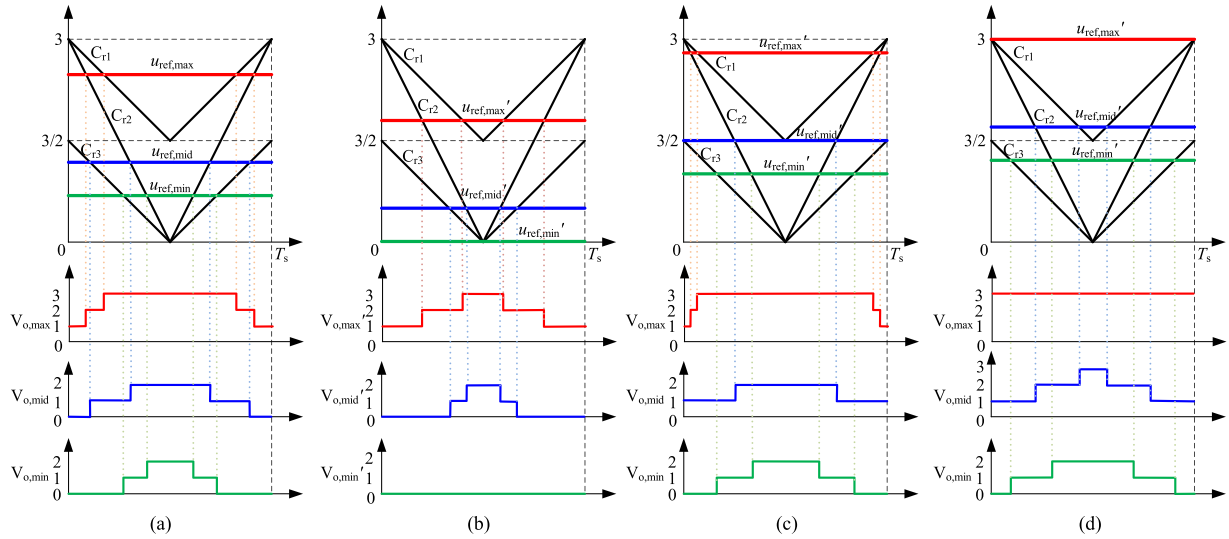


Fig. 6. COPWM with ZSV injection. (a) Original reference voltages without ZSV injection. (b) With minimal ZSV injection. (c) With an inflection ZSV injection. (d) With maximal ZSV injection.

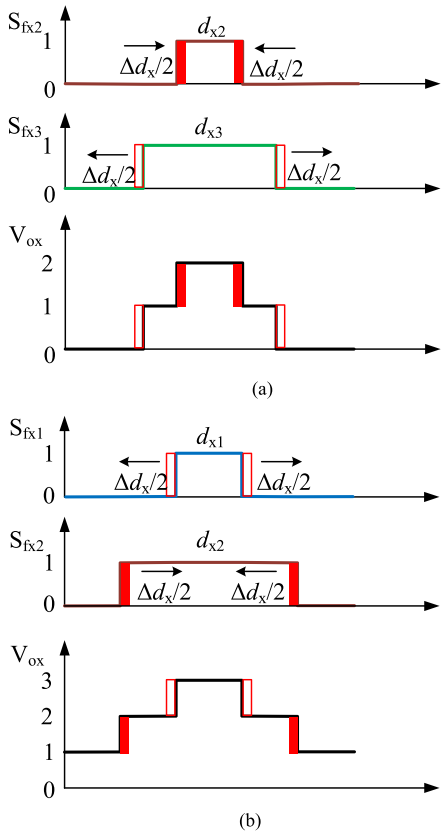


Fig. 7. Central dc-link capacitor voltage balance method. (a) $0 \le u_{refx} < 3/2$. (b) $3/2 \le u_{refx} \le 3$.

1) If $0 \le u_{refx} < 3/2$, d_{x1} is always zero. So d_{x2} can be decreased by Δd_x and d_{x3} can be increased by Δd_x, as shown in Fig. 7(a).
2) If $3/2 \le u_{refx} \le 3$, d_{x3} is always 1. In this condition, d_{x2} can be decreased by Δd_x and d_{x1} can be increased by Δd_x, as shown in Fig. 7(b).

TABLE II
ADJUSTMENTS OF $d_{x1} - d_{x3}$ FOR THE CENTRAL DC-LINK CAPACITOR VOLTAGE BALANCING WHEN $u_{dc2} < E$

u_{refx}	i_{ox}	d_{x1}	d_{x2}	d_{x3}
$0 \le u_{refx} < 3/2$	$i_{ox} > 0$	0	$-\Delta d_x$	Δd_x
	$i_{ox} < 0$	0	Δd_x	$-\Delta d_x$
$3/2 \le u_{refx} \le 3$	$i_{ox} > 0$	Δd_x	$-\Delta d_x$	0
	$i_{ox} < 0$	$-\Delta d_x$	Δd_x	0

By this way, the average output voltage is not affected according to (3) and the average current flowing out of the central dc-link capacitor in a single phase is

$$\bar{i}'_{d2x} = (2d'_{x2} - d'_{x1} - d'_{x3}) \cdot i_{ox} = -3\Delta d_x \cdot i_{ox} \tag{14}$$

which means the central dc-link capacitor can be charged in this condition. Δd_x is very small and can be controlled by a proportional-integral regulator, which must saturate to ensure d_{x1}, d_{x2}, and d_{x3} no larger than 1 and no less than 0. The adjustments of d_{x1}, d_{x2} and d_{x3} when $u_{dc2} < E$ are summarized in Table II. It is similar for $u_{dc2} > E$. With this method, the central dc-link capacitor voltages can be well balanced.

It should be noted that although the average output voltage is not affected, the total NP current is affected a little. According to (4) and Table II, the final total NP current of a single phase after the duty cycle adjustment will be

$$\bar{i}'_{Nx} = \bar{i}'_{N1x} + \bar{i}'_{N2x} = (d'_{x3} - d'_{x1}) \cdot i_{ox} = \bar{i}'_{Nx} \pm \Delta d_x \cdot i_{ox}. \tag{15}$$

That is to say, the variation of the total NP current is $\pm\Delta d_x \cdot i_{ox}$. However, Δd_x is very small and is limited within 10% of the original duty cycles in this paper, so the couple of the two voltage balancing method is very weak.

TABLE III
CIRCUIT PARAMETERS USED FOR SIMULATION

Parameters	Value
dc-link voltage	$U_{dc} = 4800$ V
Line voltage	$U_L = 3.3$ kV
Rated Power	$P = 1$ MVA
Rated Current	$I = 200$ A
Nominal capacitor voltage	$E = 1600$ V
dc-link capacitor	$C_{d1} = C_{d2} = C_{d3} = 1000\ \mu$F
Carrier frequency	$f_c = 1$ kHz
R-L Load	$R = 7.5\ \Omega$, $L = 10$ mH

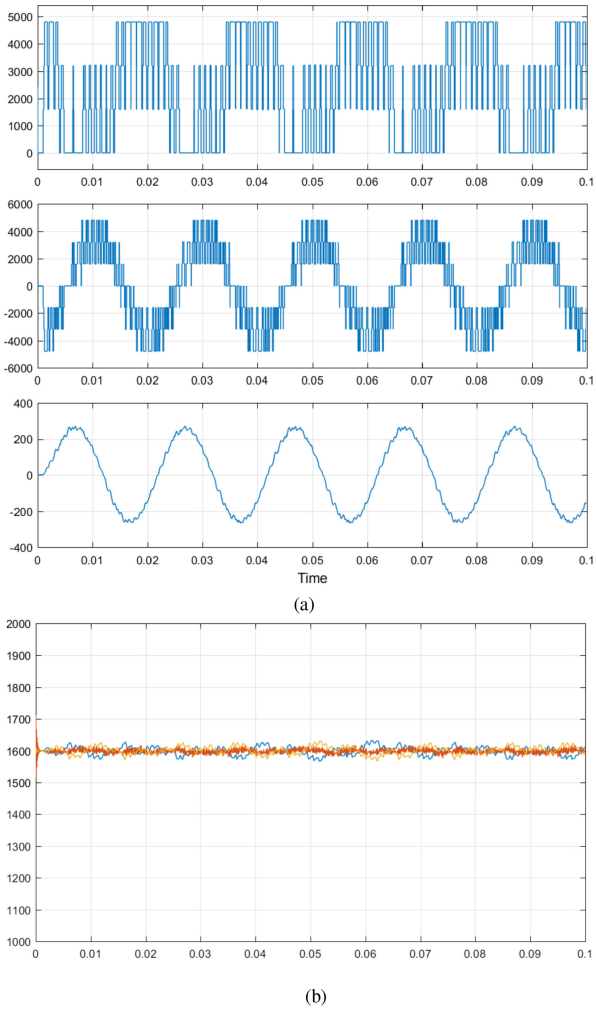


Fig. 8. Simulation results with $m = 0.9$. (a) Phase voltage (top), line voltage (middle), and phase current (bottom). (b) DC-link capacitor voltages.

IV. SIMULATION RESULTS

A 3.3 kV/1 MVA inverter model under MATLAB/Simulink environment has been built to verify the proposed voltage balance method. The circuit parameters used for simulation are given in Table III.

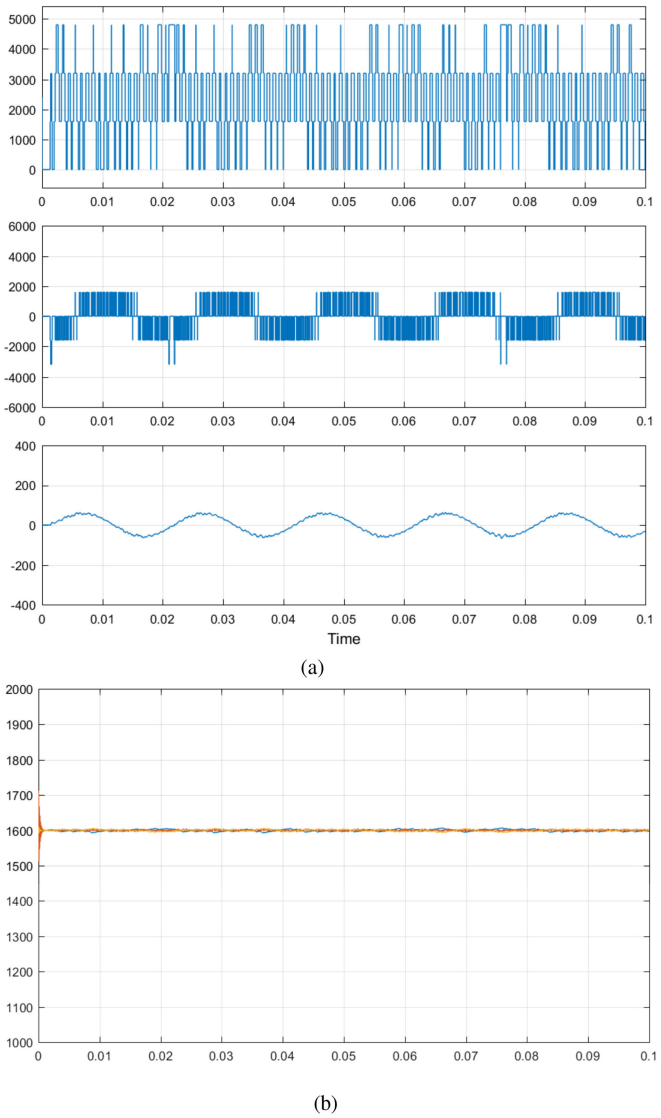


Fig. 9. Simulation results with $m = 0.2$. (a) Phase voltage (top), line voltage (middle), and phase current (bottom). (b) DC-link capacitor voltages.

Figs. 8 and 9 show the waveforms of phase voltage, line voltage, phase current, and three dc-link capacitor voltages with modulation index $m = 0.9$ and $m = 0.2$, respectively. All the capacitor voltages are balanced very well with the proposed voltage balance method. Figs. 10 and 11 are the corresponding harmonic spectrums with $m = 0.9$ and $m = 0.2$. It can be seen that the low-order harmonics caused by ZSV injection in the phase voltage is eliminated in the line voltage and current. Most of the harmonics are around carrier-frequency and multiple carrier-frequency, which are very easy to be filtered.

In order to demonstrate the dynamic performance of the proposed NP potential balance method, Fig. 12 shows the simulation results of dc-link capacitor voltages when their reference values are suddenly changed. In Fig. 12(a), the three dc-link capacitor voltages are controlled at the nominal voltage at first. At $t = 0.2$ s, the upper and lower dc-link capacitor voltages are

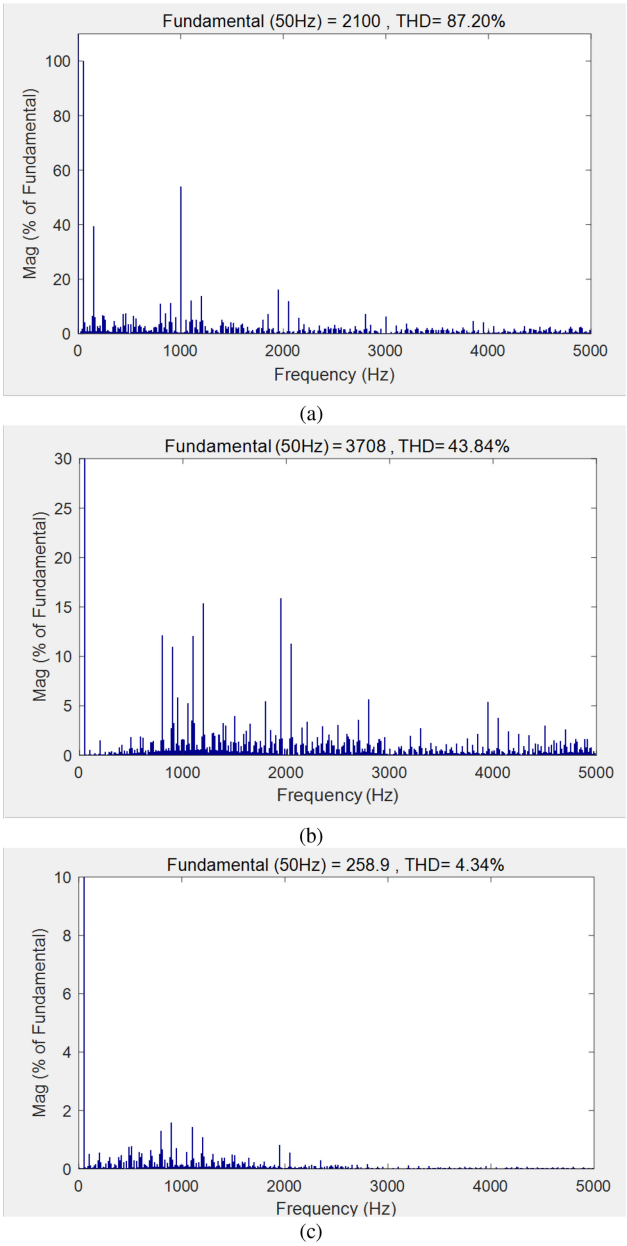


Fig. 10. Simulation harmonic spectrums of (a) phase voltage, (b) line voltage, and (c) phase current with $m = 0.9$.

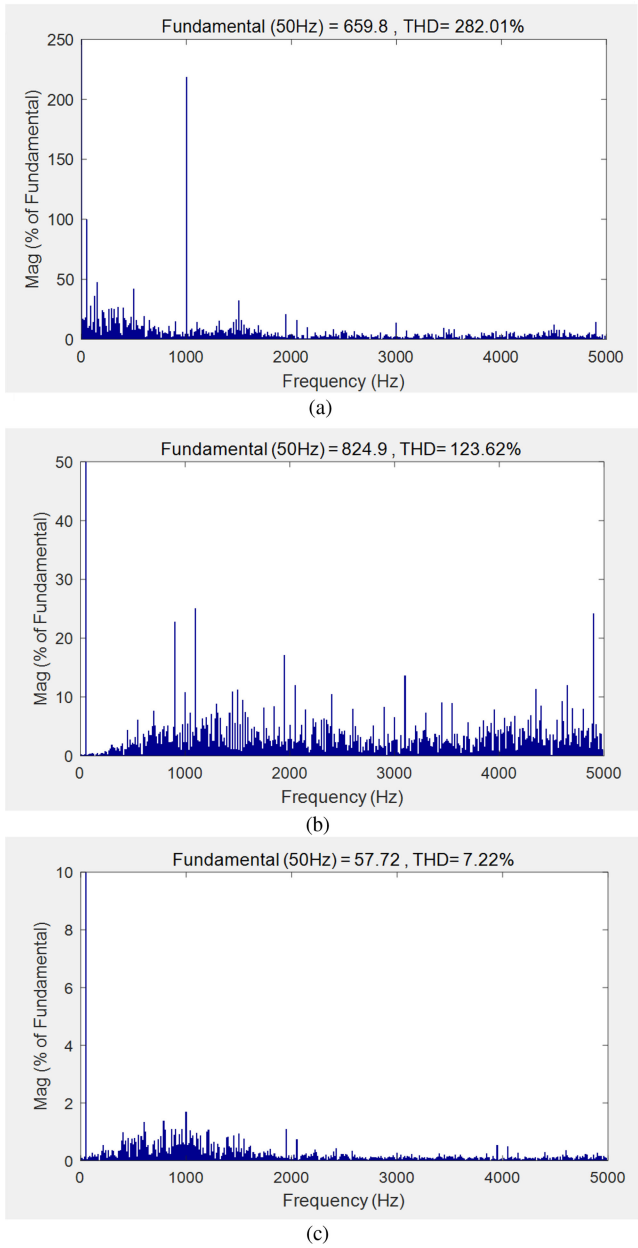


Fig. 11. Simulation harmonic spectrums of (a) phase voltage, (b) line voltage, and (c) phase current with $m = 0.2$.

set to 10% higher than and 10% lower than the nominal value, respectively. Due to the effect of the voltage balance method, the upper and lower dc-link capacitor voltages diverge and gradually stabilize at the new given values while the central dc-link capacitor voltage remains balanced. At $t = 0.3$ s, the upper and lower dc-link capacitor voltages are controlled balanced again.

The situation is similar to the central dc-link capacitor. As shown in Fig. 10(b), the central dc-link capacitor voltage is set to 20% higher than the nominal value at $t = 0.2$ s and then it gradually stabilizes at the new given value. At $t = 0.3$ s, the central dc-link capacitor voltage is controlled back to the nominal value again. It should be noticed that during the whole process the upper and lower capacitor voltages remain balanced, which means the balancing control of the three dc-link capacitors is well decoupled.

V. Experimental Results

To verify the validity of the proposed topology and modulation method, a low power three-phase four-level ANPC inverter prototype was built on the basis of a four-level hybrid-clamped inverter [7], as shown in Fig. 13. The flying capacitors in the original four-level hybrid-clamped inverter were

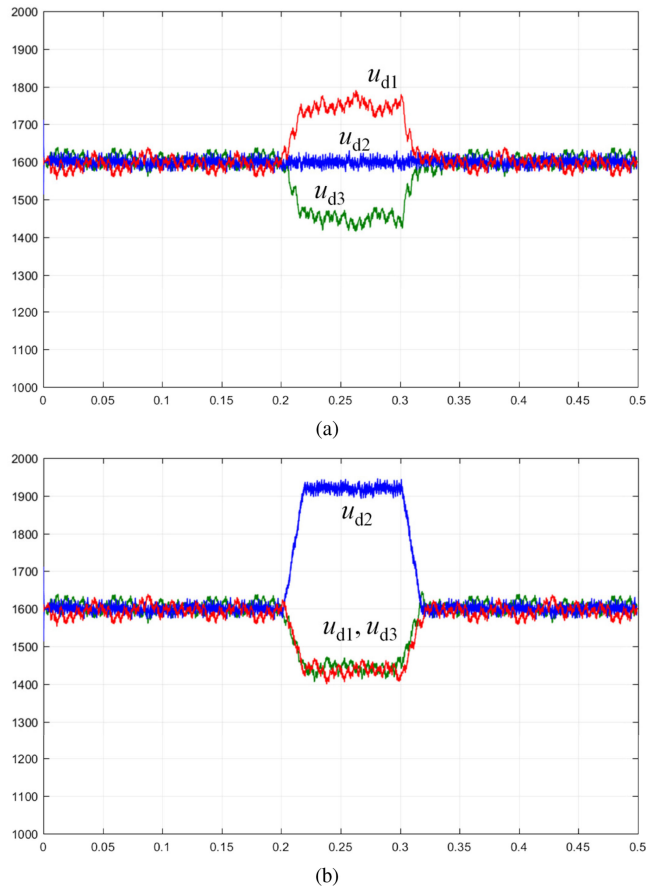


Fig. 12. Dynamic-state simulation result of the dc-link capacitor voltages. (a) Upper and lower dc-link capacitor voltages are controlled unbalanced. (b) Central dc-link capacitor voltage is controlled unbalanced.

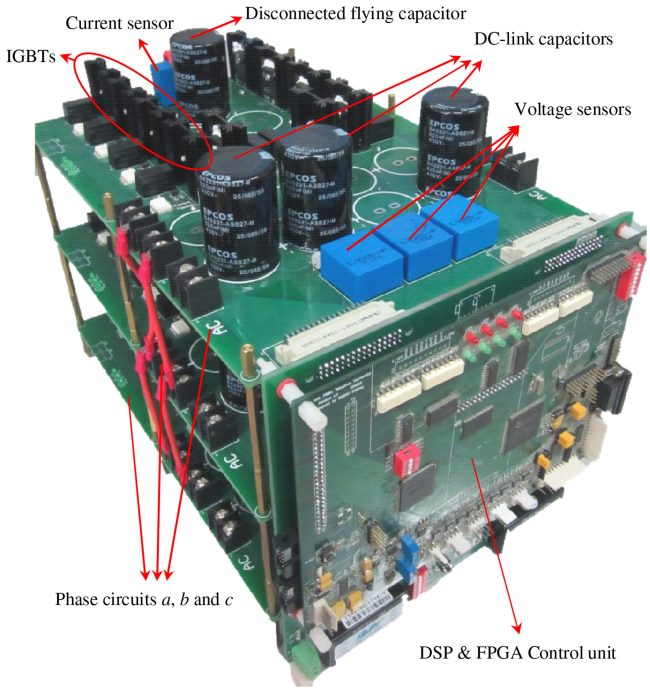


Fig. 13. Three-phase 4L ANPC inverter prototype.

TABLE IV
CIRCUIT PARAMETERS USED FOR EXPERIMENT

Parameters	Value
dc-link voltage	$U_{dc} = 200$ V
Nominal capacitor voltage	$E = 66.7$ V
dc-link capacitor	$C_{d1} = C_{d2} = C_{d3} = 1410\ \mu$F
Carrier frequency	$f_c = 5$ kHz
R-L Load	$R = 22\ \Omega$, $L = 1$ mH

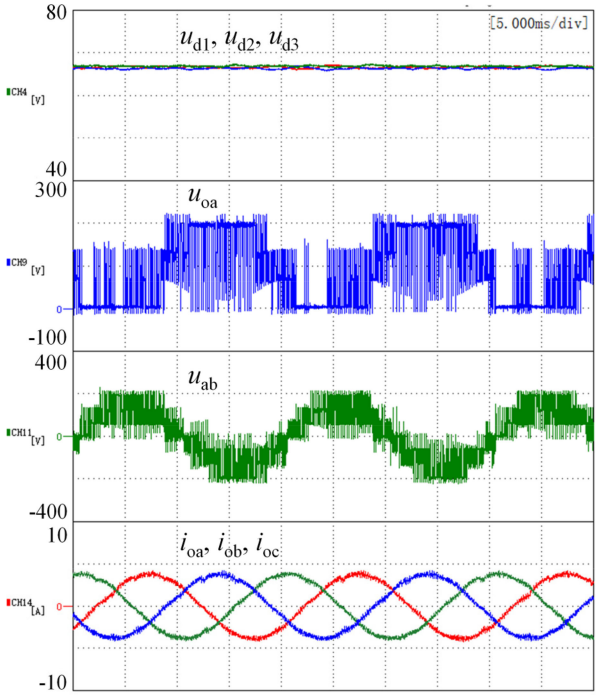


Fig. 14. Experimental results with $m = 0.9$. From top to bottom are dc-link capacitor voltages (10 V/div), phase voltage (100 V/div), line voltage (200 V/div), and three-phase currents (5 A/div).

disconnected. The dc-link capacitors of three phases are parallel connected. The parameters used for the experiment are given in Table IV.

Figs. 14 and 15 show the steady-state experimental results with modulation index $m = 0.9$ and $m = 0.2$, respectively. The waveforms are similar to the simulation. With the proposed NP voltage balance method, the three dc-link capacitor voltages maintain balanced very well. It can be observed that there are some notches in the phase voltage, which looks like over modulation. Indeed it is due to the ZSV injection. When a maximal or minimal ZSV is injected, according to (12), the phase voltage will remain unchanged and stay at the maximal or minimal value. However, the ZSV will be cancelled in the line voltage, and so there is no such notches in the line voltage.

Fig. 16 shows the detailed waveforms of the output phase voltage and the voltage stress across the switch S_{x2}. It can be seen that the phase voltage waveform is the same as that in

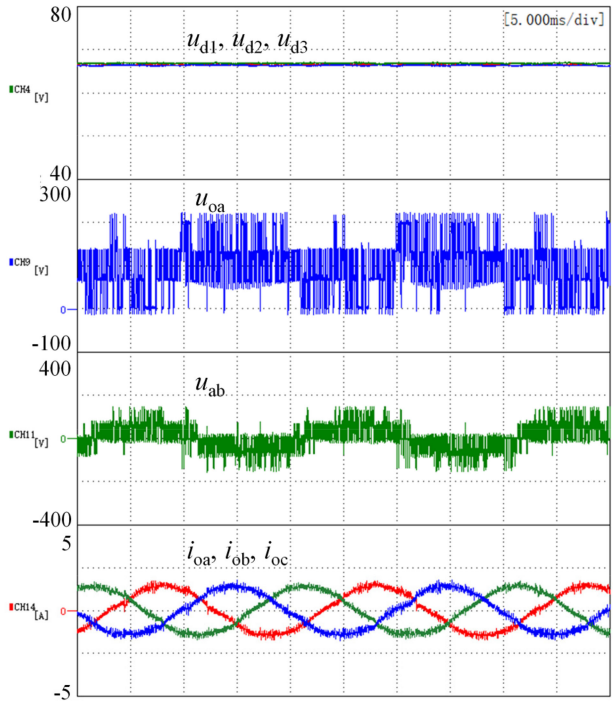


Fig. 15. Experimental results with $m = 0.2$. From top to bottom are dc-link capacitor voltages (10 V/div), phase voltage (100 V/div), line voltage (200 V/div), and three-phase currents (2.5 A/div).

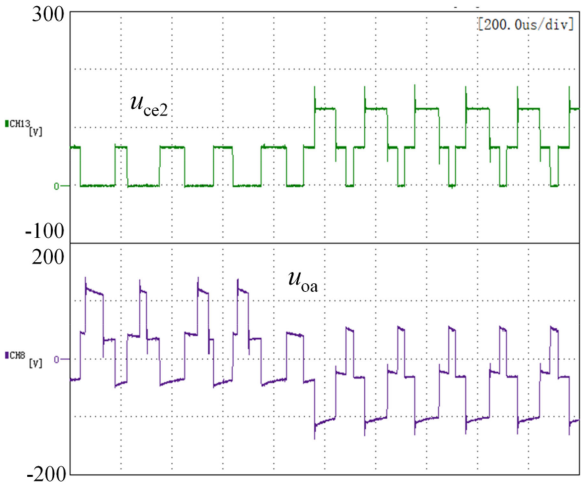


Fig. 16. Detailed waveforms of the switch S_{x2} voltage stress (top) and output phase voltage (bottom).

Fig. 3. The maximal voltage stress of S_{x2} is about 133 V ($2E$). However, the step voltage is only 66.7 V (E), which demonstrate the theoretical analysis about series connected switches.

The harmonic spectrums of phase voltage, line voltage, and current under $m = 0.9$ and $m = 0.2$ are shown in Figs. 17 and 18, respectively. The results are also similar to the simulation. Although a large amount of harmonics exist in the phase voltage due to the ZSV injection, the total harmonic distortion of line voltage is much smaller and most of the harmonics are around carrier frequency and multiple carrier-frequency.

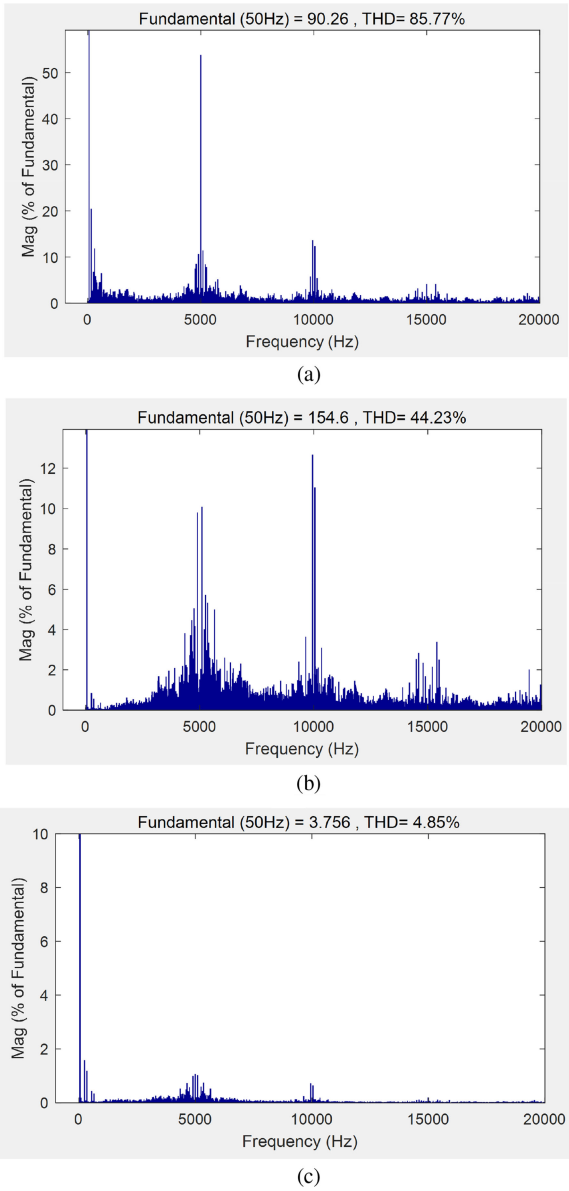
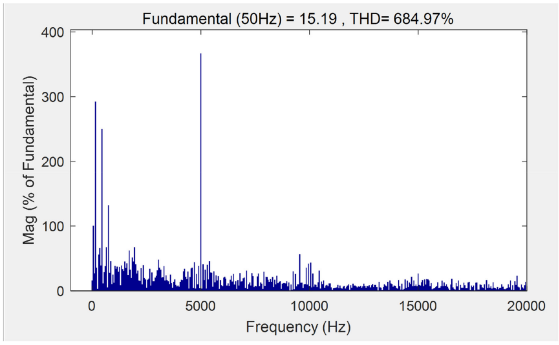


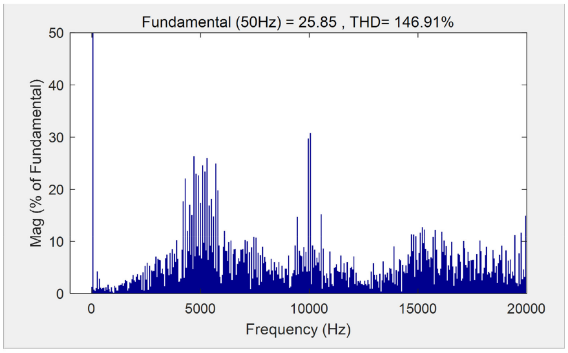
Fig. 17. Experimental harmonic spectrums of (a) phase voltage, (b) line voltage, and (c) phase current with $m = 0.9$.

Fig. 19 shows the performance of NP potential balance method under variable voltage variable frequency (VVVF) condition. The load current increases as the output frequency and modulation index increase. All the capacitor voltages remain balanced very well during the whole process.

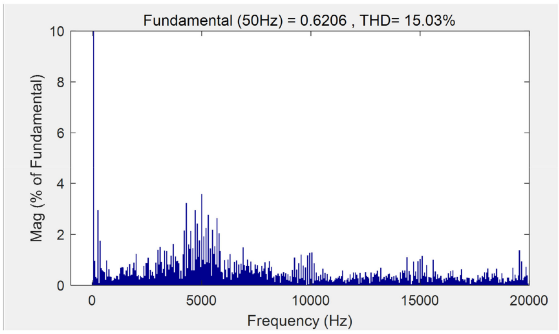
Fig. 20 shows the dynamic-state performance of the voltage balance method. At $t = 6$ s, the reference voltages of the upper, central, and lower dc-link capacitors are set to 10% lower, 25% higher, and 15% lower than the nominal value, respectively. All the capacitor voltages stabilize at the new given values quickly. At about $t = 16$ s, all the capacitor voltages are set back to the nominal value and balanced again. The steady and dynamic state results demonstrate the validity of the voltage balance method.



(a)



(b)



(c)

Fig. 18. Experimental harmonic spectrums of (a) phase voltage, (b) line voltage, and (c) phase current with $m = 0.2$.

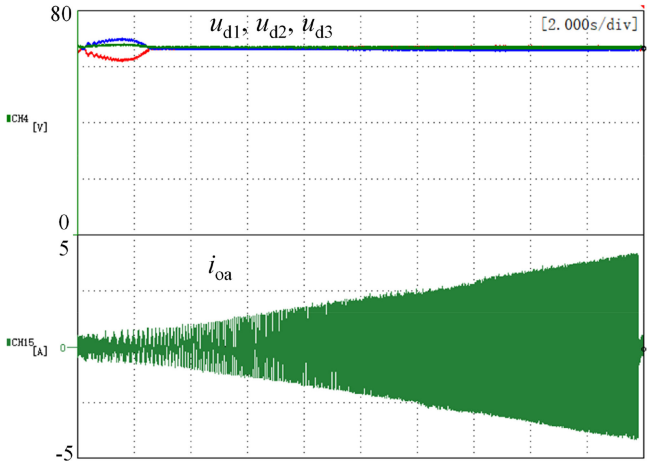


Fig. 19. DC-link capacitor voltage balance performance under VVVF control.

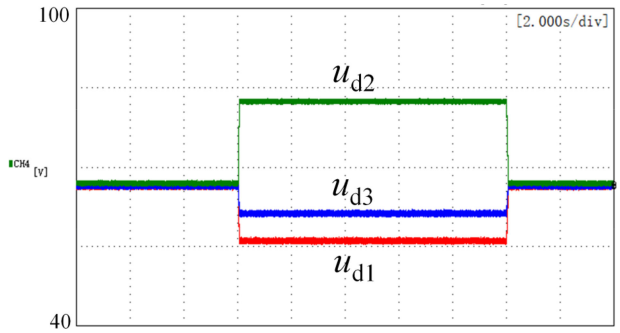


Fig. 20. Dynamic experimental result of the dc-link capacitor voltages while the reference voltages are changed.

VI. Conclusion

In order to improve the power density and reduce the cost of the four-level hybrid-clamped inverter, a four-level ANPC inverter without any flying capacitors is presented and discussed in this paper. The uneven voltage stress and NP voltage imbalance are two main problems of this topology. By applying proper operating rules, the dynamic voltage sharing problem of the series connected switches can be solved. In order to solve the NP voltage balance problem, a decoupled NP voltage balance method based on COPWM is proposed in this paper. The upper and lower dc-link capacitor voltages are balanced by ZSV injection and the central dc-link capacitor voltage is balanced by adjusting the duty cycles of the switching signals. Simulation and experimental results demonstrate the validity of this method.

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