Single-Phase AC–DC–AC Three-Level Three-Leg Converter With Reduced Switch Count

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***Abstract*—This paper presents a new single-phase ac–dc–ac three-level three-leg converter composed of three coupled-inductors and six active switches. The system model, operation principles, and a control strategy are presented and discussed. Additionally, a space-vector pulsewidth modulation technique is developed to double the effective frequency of the grid and load voltages and to reduce the switching losses. The proposed converter is compared to other similar converters in terms of switch count, harmonic distortion, and power losses. The results show that the proposed topology has improved power quality and uses fewer switches and gate drive circuits. These characteristics can potentially reduce the costs and the complexity of the system. In addition, the proposed converter eliminates the requirement for dead time to prevent short circuit of the dc-link. In order to validate the theoretical analysis, simulated and experimental results are presented and discussed.**

***Index Terms*—AC–DC–AC converter, coupled inductors, multilevel inverters, multilevel rectifiers, three-leg (3L) converter.**

I. Introduction

POWER electronics have been increasingly used to improve the quality of electrical power systems by minimizing the impacts of the voltage sags or by eliminating the harmonic distortion. Electric power quality is fundamental to feed sensitive loads such as computers, telecommunication systems, and biomedical instrumentation. Harmonic pollution, voltage instability, and poor power factor are some examples of power quality issues. These problems lead to higher energy usage, lower productivity, higher energy costs, higher maintenance costs, and failure of the equipment [1]. Single-phase and three-phase ac–dc–ac converters have been used in several applications with the goal of mitigating these impacts of poor power quality. They have the capability of power factor correction and voltage regulation to sensitive loads, i.e., an ac–dc–ac converter provides high power quality.

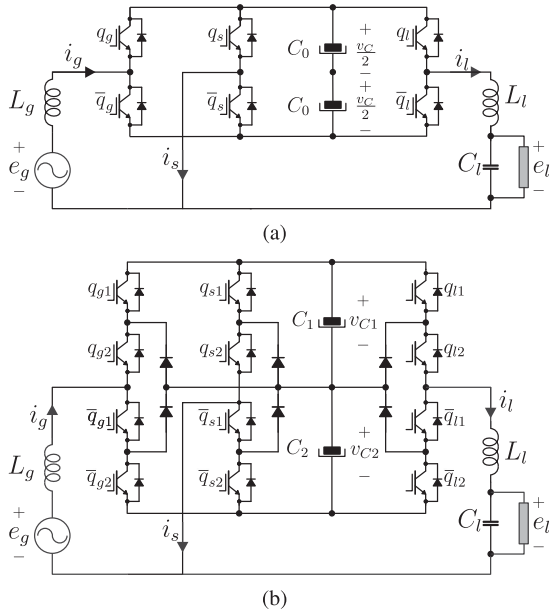

Fig. 1. Conventional configurations. (a) 3L. (b) 3LNPC.

Line conditioners, universal active power filters (APF), and uninterruptible power supplies (UPS) are some examples of single-phase equipment which can be developed by using single-phase ac–dc–ac converters [2]–[4]. A single-phase-to-single-phase ac–dc–ac converter can be obtained by using the conventional three-leg (3L) converter, as shown in Fig. 1(a) [5]. The conventional 3L converter shares a common leg between the input and output stages. This configuration has fewer switches when compared to a four-leg topology and provides the same dc-link voltage capability if both input and output stages operate with the same frequency. This feature allows the 3L converter to decrease the power losses when compared with the four-leg converter [5].

In recent years, 3L ac–dc–ac converters have been obtained by using three-level legs [6]–[8]. In [6], a single-phase three-level 3L converter using silicon carbide (SiC) was proposed. The proposed converter comprises two three-level T-type legs and a common two-level leg. Each T-type leg comprises two SiC MOSFET devices; therefore, switching losses can be reduced or the converter can operate at a higher switching frequency with the same power losses. In [7], the 3L neutral-point-clamped

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(3LNPC) converter was investigated and its unidirectional version was proposed in [8]. The 3LNPC converter can be seen in Fig. 1(b) and it is composed by three bidirectional NPC legs, while the converter in [8] uses one unidirectional NPC leg at the input side. These converters present lower voltage stress across the switches and also allow a reduction in the harmonic distortion when compared to the 3L converter. A specific disadvantage of the 3LNPC converter is the tendency of the dc-link neutral-point potential to deviate from its balanced state. In [7], the space-vector plane generated by the 3LNPC converter and the capacitor current contribution of each vector were presented. However, the balance problem was addressed by a pulsewidth modulation (PWM) scalar technique. Moreover, topologies connected in series or parallel based on the 3L converter have also been recently proposed [9], [10].

Multilevel converters have been intensely researched due to its advantages over a conventional two-level converter, such as lower voltage stress of power semiconductors, lower switching loss and frequency, and lower voltage harmonic distortion [11]. The basic multilevel topologies are cascaded H-bridge (CHB) with isolated dc sources [12], flying capacitors (FC) [13], and NPC [14]. Furthermore, multilevel converters using T-type legs [15] and cascaded transformers [16] have also been researched. The major drawback of these topologies is related to the large number of power semiconductor switches, which are associated with gate driver circuits, making the overall system more expensive, bulky, and complex. Other disadvantages that can be highlighted are the capacitor voltage balancing that increases the control complexity for NPC and T-type converters, the large number of capacitors for the FC converter, and the need of isolated dc sources for the CHB converter [11], [17].

In this context, when the application justifies the use of a three-level converter instead of a two-level converter, one interesting alternative is the use of a coupled-inductor multilevel converter [18], [19]. Basically, the coupled-inductor converter is composed of two unidirectional two-level legs and one coupled inductor [20]. This understanding is important, since it is possible to combine the coupled inductors with the conventional NPC, CHB, or FC multilevel topologies [21]–[24]. This converter has increased its popularity in medium-voltage high-power applications due to benefits such as smaller filters, fewer switches, no need of dead time to avoid short circuit of the dc-link, and its immunity to circulating currents [18], [20], [25]. This topology produces an output voltage with the same number of voltage levels as the NPC converter, but with half the number of controlled switches [25]. Its only weakness is the higher voltage stress when compared to the conventional NPC three-level leg. Due to such benefits, rectifiers and inverters using coupled inductors have been widely discussed in the literature. Several PWM strategies have also been proposed to improve the performance of the coupled inductors. In [26], an interleaved discontinuous space-vector PWM (DSVPWM) strategy for a three-level three-phase voltage source inverter using split-wound coupled inductors was presented. The PWM strategy is able to reduce the inductor losses and improve the performance of the three-phase inverter. However, the use of the coupled-inductor converter in ac–dc–ac conversion has been unexplored.

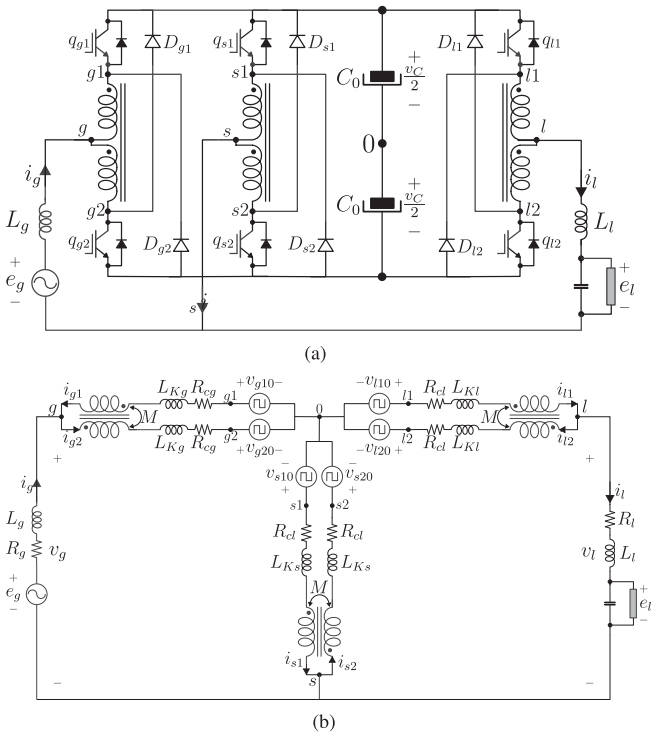


Fig. 2. (a) Proposed single-phase three-level ac–dc–ac converter. (b) Simplified equivalent circuit.

In this paper, a new single-phase-to-single-phase three-level back-to-back converter is proposed. This topology, shown in Fig. 2, uses the concept of split-wound coupled inductors to achieve multilevel features. As a result, it is possible to reduce the harmonic content at the input and output converter sides while using the same number of switches of the conventional 3L topology [27]. Compared to the state of art of ac–dc–ac converters, the use of coupled inductors brought several advantages and the following contributions can be highlighted.

1) The proposed converter has a smaller number of active switches compared with all multilevel solutions presented in literature. There is no other ac–dc–ac multilevel topology in the literature capable of producing five-level voltages at both input and grid sides employing only six switches.
2) It has natural protection against short circuit of the dc-link capacitors, improving the robustness and reliability of the system.
3) There is no need for dead time and, as a consequence, the modulated signals have less harmonic content.
4) The control structure is as simple as the conventional ones. There is no need for an increasing of the sensors or of complexity algorithms, which is a huge disadvantage for the ac–dc–ac multilevel topologies presented in the literature.
5) The ac filter's size and losses can be reduced.

Summarizing, the main contributions of this paper are: 1) a new single-phase-to-single-phase three-level ac–dc–ac converter is presented; 2) a space-vector PWM technique is developed to double the effective frequency of the voltage waveforms and to reduce the switching losses; 3) the operating

principles regarding the synchronization between grid and load converter voltages are presented and discussed; and 4) a comparison between the proposed configuration and similar topologies is discussed. Furthermore, simulation and experimental results are also presented for validation purposes.

II. System Model

The proposed topology is composed of three coupled-inductor three-level legs, [see Fig. 2(a)], inductor and capacitor filters (C_l, R_g, L_g, R_l, and L_l), and one dc-link capacitor bank (C_0). Each phase leg is composed by a coupled inductor, two controlled switches q_{x1} and q_{x2}, and two diodes D_{x1} and D_{x2} (with $x = g, s, l$). An equivalent circuit of the proposed configuration can be seen in Fig. 2(b), where the coupled-inductor model is composed by the coil resistance R_{cx} and an equivalent inductance $L = L_{Kx} + M$.

Applying Kirchhoff's law to the circuit in Fig. 2(b), the following equations can be derived:

$$e_g = R_g i_g + L_g \frac{di_g}{dt} + v_g \tag{1}$$

$$e_l = -R_l i_l - L_l \frac{di_l}{dt} + v_l \tag{2}$$

with

$$v_g = v_{g0} - v_{s0} \tag{3}$$

$$v_l = v_{l0} - v_{s0} \tag{4}$$

where e_g is the grid voltage, i_g is the grid current, v_g is the voltage generated by the rectifier, v_l is the voltage generated by the inverter, e_l is the load voltage, i_l is the load current, v_{g0}, v_{l0}, and v_{s0} are the converter pole voltages, R_g and L_g represent the resistance and inductance of the input filter, respectively, and R_l and L_l represent the resistance and inductance of the output filter, respectively.

According to Kirchhoff's voltage law given by inner loops of the coupled inductors, the following equations can be derived:

$$v_{x10} - v_{x0} = R_{cx} i_{x1} + (L_{Kx} + M)\frac{di_{x1}}{dt} + M\frac{di_{x2}}{dt} \tag{5}$$

$$v_{x0} - v_{x20} = R_{cx} i_{x2} + (L_{Kx} + M)\frac{di_{x2}}{dt} + M\frac{di_{x1}}{dt} \tag{6}$$

combining (5) and (6), it is obtained that

$$v_{\text{Dmx}} = R_{cx} i_{\text{Cmx}} + (L_{Kx} + 2M)\frac{di_{\text{Cmx}}}{dt} \tag{7}$$

$$v_{\text{Cmx}} = v_{x0} + R_{cx} i_{\text{Dmx}} + L_{Kx}\frac{di_{\text{Dmx}}}{dt} \tag{8}$$

with

$$v_{\text{Dmx}} = \frac{v_{x10} - v_{x20}}{2} \tag{9}$$

$$v_{\text{Cmx}} = \frac{v_{x10} + v_{x20}}{2} \tag{10}$$

$$i_{\text{Dmx}} = \frac{i_{x1} - i_{x2}}{2} \tag{11}$$

$$i_{\text{Cmx}} = \frac{i_{x1} + i_{x2}}{2} \tag{12}$$

TABLE I
Switching States and Resulting Leg Conditions

State	q_{x1}	q_{x2}	v_{x0}	Coupled-inductor	I_{Cmx}
00	0	0	0	desmagnetize	decreases
01	0	1	$-v_C/2$	0	constant
02	1	0	$v_C/2$	0	constant
03	1	1	0	magnetize	increases

where v_{Dmx} and v_{Cmx} denote the differential and the common-mode voltages, respectively. L_{Kx}, M, and R_{cx} represent the leakage inductance, mutual inductance, and coil resistance of each bobbin, respectively.

Considering that L_{Kx} and R_{cx} are small quantities, from (8), it can be concluded that the pole voltage v_{x0} depends only on the common-mode voltage v_{Cmx}, which depends on the states of the switches. In this way, it is possible to write v_{x0} as a function of the switching states and the dc-link voltage as follows:

$$v_{x0} = (q_{x1} - q_{x2})\frac{v_C}{2} \text{ with } x \in (g, s, l) \tag{13}$$

where q_{x1} and q_{x2} are the state of the switches of the phase leg x and v_C is the dc-link voltage.

Then, the complete system model is given by

$$e_g = R_g i_g + L_g \frac{di_g}{dt} + \frac{v_{g10} + v_{g20}}{2} - \frac{v_{s10} + v_{s20}}{2} \tag{14}$$

$$e_l = -R_l i_l - L_l \frac{di_l}{dt} + \frac{v_{l10} + v_{l20}}{2} - \frac{v_{s10} + v_{s20}}{2}. \tag{15}$$

The correct operation of each phase leg relies on securing the volt–second balance of the coupled inductors. In this way, several PWM strategies have been presented in the literature for this purpose [19], [26], [28]. These strategies take into account the four possible switching states of one phase leg, as shown in Table I. As can be seen, the switching states result in different winding conditions. When the phase leg is in states (01) and (02), the coupled inductor is shorted and the common-mode current is constant. The switching state (00) increases and state (03) decreases the common-mode current by applying a differential-mode voltage of $+v_C/2$ and $-v_C/2$, respectively, across the coupled-inductor windings. The volt–second balance is secured by equally distributing the time applications of states (00) and (03). The common-mode current is maintained at a positive dc value, and as a consequence, the converter is able to produce optimal multilevel voltage waveforms.

III. Space-Vector PWM

A space-vector technique can be utilized to synthesize the reference voltages v_g^* and v_l^*. Fig. 3 shows the space-vector plane generated by the proposed converter. There are 64 switching states resulting in 18 active vectors ($\mathbf{V}_1 \rightarrow \mathbf{V}_{18}$), a null vector ($\mathbf{V}_0$), and 24 sectors. The voltage vectors are defined by the following equation:

$$\mathbf{v}_{n_g, n_l, n_s} = v_g + j v_l. \tag{16}$$

The voltages v_g and v_l coincide with the real (Re) and the imaginary (Im) axes, respectively, and the vector redundancies are represented as $\mathbf{v}_{n_g, n_l, n_s}$, where n_g, n_l, and n_s are the binary

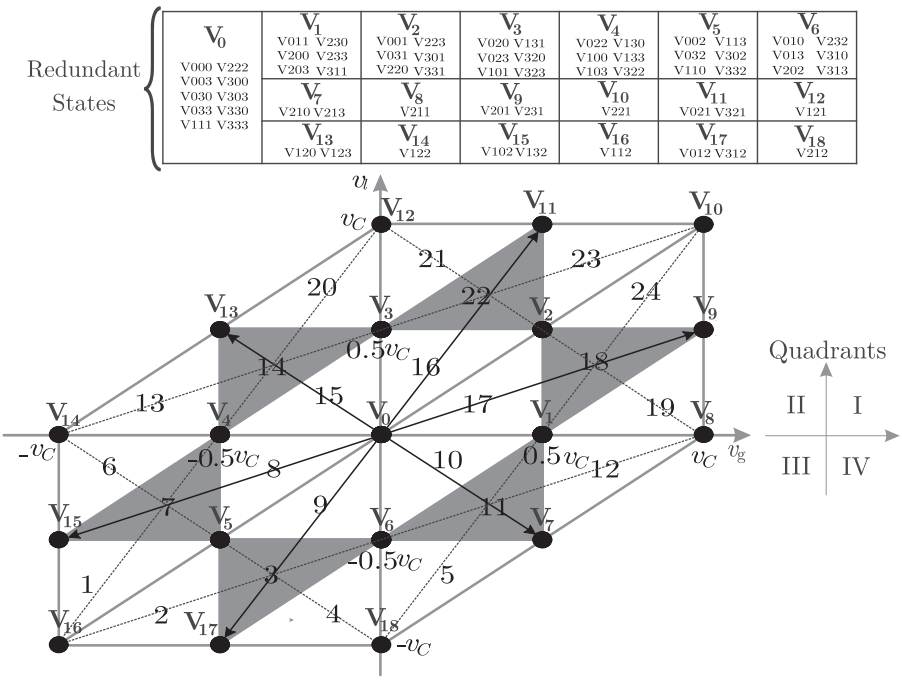


Fig. 3. Space-vector plane generated by the proposed converter.

sequences $q_{g1}q_{g2}$, $q_{l1}q_{l2}$, and $q_{s1}q_{s2}$, respectively, converted to decimal numbers. The reference voltage vector located inside a triangle must be synthesized by

$$\mathbf{v}^* = \mathbf{V}_x \frac{2t_1}{T_s} + \mathbf{V}_y \frac{2t_2}{T_s} + \mathbf{V}_z \frac{2t_3}{T_s} \tag{17}$$

where t_1, t_2, and t_3 are the time weights for vectors $\mathbf{V}_x$, $\mathbf{V}_y$, and $\mathbf{V}_z$, respectively, and half of the switching period is defined by $\frac{T_s}{2} = t_1 + t_2 + t_3$.

The time weights t_1, t_2, and t_3 are calculated as follows:

$$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} \frac{2\text{Re}(\mathbf{V}_x)}{T_s} & \frac{2\text{Re}(\mathbf{V}_y)}{T_s} & \frac{2\text{Re}(\mathbf{V}_z)}{T_s} \\ \frac{2\text{Im}(\mathbf{V}_x)}{T_s} & \frac{2\text{Im}(\mathbf{V}_y)}{T_s} & \frac{2\text{Im}(\mathbf{V}_z)}{T_s} \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} v_g^* \\ v_l^* \\ \frac{T_s}{2} \end{bmatrix}. \tag{18}$$

Since there are redundant switching states for each sector of the plane, there are some possibilities to produce the reference vector $\mathbf{v}^*$. These redundancies and the application sequence of the voltage vectors are selected to minimize the amount of changes in the switching states, reduce the switching losses, and maintain the high-frequency spectrum of the output voltages at twice the switching frequency. Then, two inverter legs are always switching and the third leg is always clamped in $+v_C/2$ or $-v_C/2$. The application sequence of the vectors utilized in this paper follows the concept of [26], that is a combination of two five-segment sequences where the same voltage vector is used at half of the switching period $T_s/2$. Hence, a nine-segment sequence is formed.

To illustrate how the vectors are selected, Fig. 4 shows the application sequence for sectors 16 and 23. In both sectors, the pole voltage v_{s0} is clamped in $-v_C/2$ [only state (01) is applied] while legs g and l are switching. Only one transition occurs in the gating signals from one vector to another, and as a consequence, the switching losses are minimized. Additionally, Fig. 4 shows that the volt–second balance of phase legs g and l is guaranteed by equally distributing the time duration of states (00) and (03) over half of the switching period. For example, in sector 16, vectors $\mathbf{v}_{031}$ and $\mathbf{v}_{301}$ generate the same active vector ($\mathbf{V}_2 = 0.5v_C + j0.5v_C$) but with opposite impact on the differential-mode voltage. Furthermore, since voltages v_g and v_l repeat twice over a switching period, it is possible to double the effective switching frequency of output waveforms v_g and v_l.

When the reference vector is located in sectors 14, 22, 18, 11, 3, and 7, it is not possible to achieve an output switching frequency with twice the switching frequency with the three nearest voltage vectors. Besides that, when $\mathbf{v}^*$ is located in these sectors, the number of switching changes per switching period increases if the three nearest vectors are used. In these cases, $\mathbf{v}^*$ must be synthesized by the two nearest vectors and one more distant. For example, when $\mathbf{v}^*$ is tipped in sector 22, the two nearest vectors from $\mathbf{V}_2$, $\mathbf{V}_3$ and $\mathbf{V}_{11}$ and one vector from $\mathbf{V}_{12}$ or $\mathbf{V}_{10}$ can be used. Fig. 5 shows the application sequence for the case when $\mathbf{V}_{12}$ is used. Sector 22 is divided into two subsectors 22a and 22b. When $\mathbf{v}^*$ is tipped in subsector 22a the application sequence is $\mathbf{V}_2 \rightarrow \mathbf{V}_3 \rightarrow \mathbf{V}_{12} \rightarrow \mathbf{V}_3 \rightarrow \mathbf{V}_2 \rightarrow \mathbf{V}_3 \rightarrow \mathbf{V}_{12} \rightarrow \mathbf{V}_3 \rightarrow \mathbf{V}_2$, while in subsector 22b the sequence is $\mathbf{V}_2 \rightarrow \mathbf{V}_{11} \rightarrow \mathbf{V}_{12} \rightarrow \mathbf{V}_{11} \rightarrow \mathbf{V}_2 \rightarrow \mathbf{V}_{11} \rightarrow \mathbf{V}_{12} \rightarrow \mathbf{V}_{11} \rightarrow \mathbf{V}_2$.

Table II shows the vector sequences for the case that $v_l \geq 0$. Due to the symmetry between the first and fourth quadrant and between the second and the fourth quadrant, it is only necessary to define the application sequences for $v_l \geq 0$ (quadrants I and II). The application sequences for $v_l \leq 0$ (quadrants III and IV) are complementary to the sequences applied when $v_l \geq 0$.

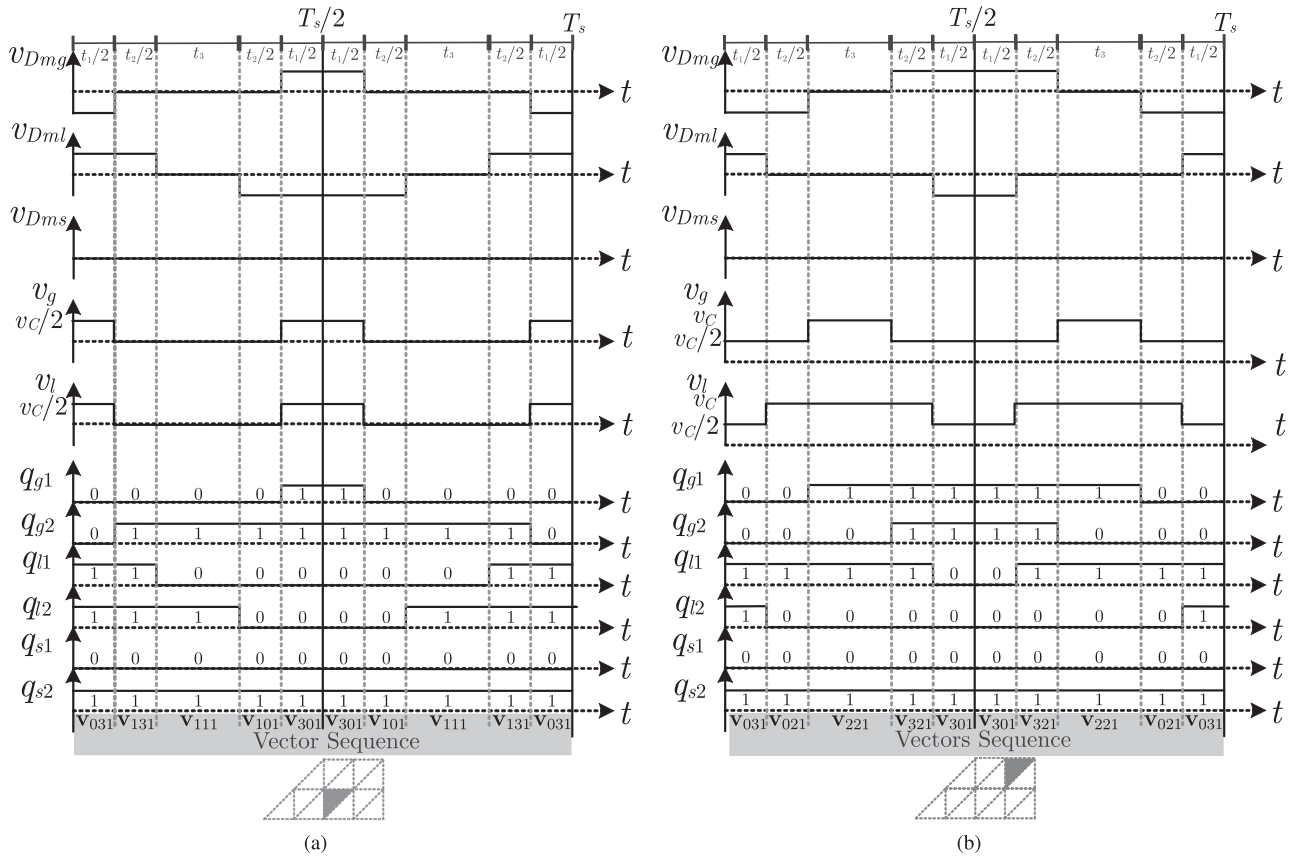


Fig. 4. Application sequences. (a) Sector 16. (b) Sector 23.

For example, if the sequence in sector 16 is $\mathbf{v}_{031} \rightarrow \mathbf{v}_{131} \rightarrow \mathbf{v}_{111} \rightarrow \mathbf{v}_{101} \rightarrow \mathbf{v}_{301} \rightarrow \mathbf{v}_{101} \rightarrow \mathbf{v}_{111} \rightarrow \mathbf{v}_{131} \rightarrow \mathbf{v}_{031}$, the sequence for sector 9 is $\mathbf{v}_{302} \rightarrow \mathbf{v}_{202} \rightarrow \mathbf{v}_{222} \rightarrow \mathbf{v}_{232} \rightarrow \mathbf{v}_{032} \rightarrow \mathbf{v}_{232} \rightarrow \mathbf{v}_{222} \rightarrow \mathbf{v}_{202} \rightarrow \mathbf{v}_{302}$.

IV. Operation Restrictions

Considering V_g^* and V_l^* the amplitude of v_g^* and v_l^*, respectively, and ϵ the phase shift between them, the dc-link voltage value is obtained by the following equations:

$$v_C^* \geq \left|v_g^*\right| \tag{19}$$

$$v_C^* \geq \left|v_l^*\right| \tag{20}$$

$$v_C^* \geq \left|v_g^* - v_l^*\right|. \tag{21}$$

As previously discussed in [27], the 3L converter has the same voltage capability as the four-leg topology when v_g^* and v_l^* have the same frequency. Additionally, in order to satisfy (21), the synchronization angle ϵ needs to be considered. Fig. 6 shows the voltage vector locus and the waveforms of v_g^*, v_l^*, and $v_g^* - v_l^*$ for ϵ equal to 60°. For a higher value of ϵ, the dc-link voltage needs to be increased, otherwise $v_{gl}^* = v_g^* - v_l^*$ becomes higher than v_C and the converter operates in the overmodulation region.

V. Magnetic Element Design

A. Coupled-Inductor Design

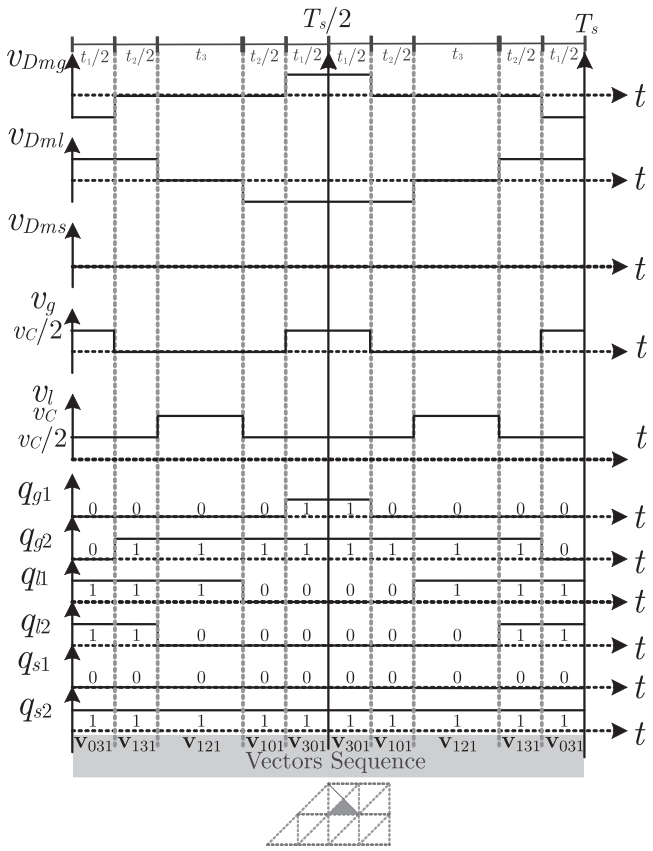
As shown in [18], the coupled inductors should be designed considering the maximum current ripple of the common-mode currents. From Fig. 4(a), notice that the differential-mode voltage v_{Dmg} is positive during the time interval t_1 and, in this interval, the common-mode mode current i_{Cmg} increases. Since the volt–second balance of the coupled inductors needs to be assured, the maximum common-mode current ripple occurs when the voltage $v_C/2$ is applied across the coupled inductors during a time interval of $T_s/2$. Hence, neglecting the resistance R_{cx} in (7), the coupled-inductor self-inductance (L_{sx}) is given by

$$L_{sx} = \frac{v_C}{4 f_s \Delta i_{\text{Cmx}_{\text{max}}}} \tag{22}$$

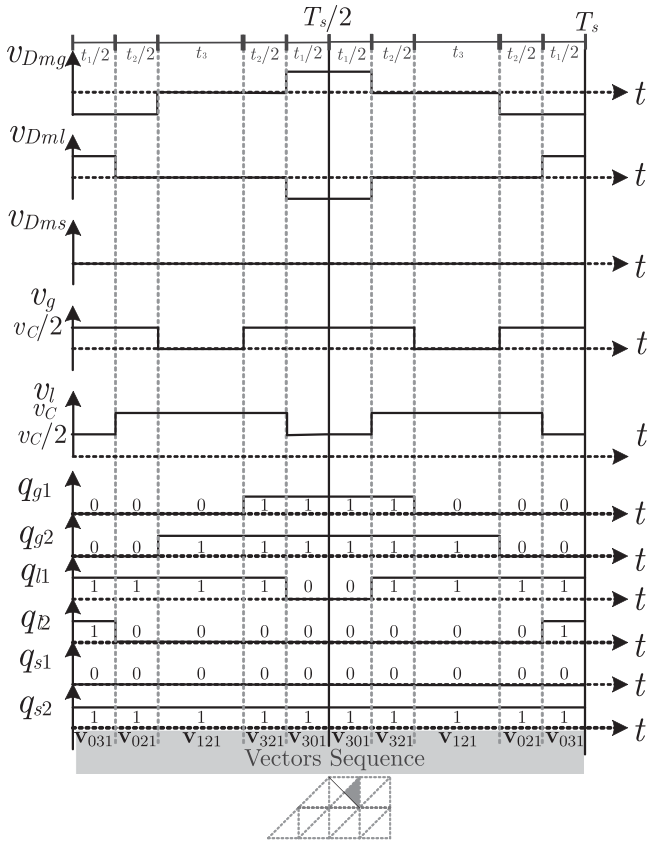
where $L_{sx} = L_{kx} + 2M$ is the self-inductance, $x = g, s, l$, and $\Delta i_{Cmx_{\text{max}}}$ is the maximum current ripple of i_{Cmx}.

B. AC-Filter Design

The ac filters L_g and L_l should be designed considering the maximum input and load current's high-frequency ripple values, respectively [18]. The maximum peak-to-peak current ripple is determined by analysing the voltage across the ac filters. Therefore, the behavior of the current ripple can be divided into two



(a)



(b)

Fig. 5. Sector 22. (a) Subsector 22a. (b) Subsector 22b.

sub-regions—the first region occurs when the modulation index M_x is less than 0.5 and the second region when M_x is higher. Neglecting the leakage inductance L_{kx} and the coupled-inductor winding resistance R_{cx}, the envelop of the normalized input and output currents can be directly extracted from the topological stages and it is determined by

$$\overline{\Delta I_{Lx}} = \frac{\Delta I_{\text{xmax}} 2 f_s L_x}{v_C} \tag{23}$$

where $\overline{\Delta I_{Lx}}$ represent the normalized current through the ac filters and it is defined by the following equation:

$$\overline{\Delta I_{Lx}} = \begin{cases} 3M_x \sin(\omega t) - 2M_x^2 \sin^2(\omega t) - 1, & \text{for } M_x \geq 0.5 \\ M_x \sin(\omega t) - 2M_x^2 \sin^2(\omega t), & \text{for } M_x < 0.5 \end{cases}. \tag{24}$$

Figure 7 shows the normalized peak-to-peak current ripple as a function of ωt for different modulation indexes M_x. As can be seen, the maximum value of the $\overline{\Delta I_{Lg}}$ is equal to 0.125. Thus, from (23), the ac-filter inductance can be determined by

$$L_x = \frac{v_C}{16 f_s \Delta I_x}. \tag{25}$$

The ac-filter equations for topologies 3L and 3LNPC can be obtained in the same manner. For the same current ripple, the proposed converter allows a reduction of 75% and 50% in the size of the ac filters when compared with 3L and 3LNPC, respectively. As a result, the ac-filter losses are lower for the proposed topology than for the conventional ones.

VI. Control Strategy

Figure 8 shows the overall control strategy of the proposed converter. The control system has a cascade structure with an external loop responsible for adjusting the dc-link voltage v_C and an inner loop that adjusts the grid reference current i_g^*. A PI controller adjusts v_C to its reference v_C^* and sets the amplitude of the reference grid current. Then, current i_g is synchronized with the grid voltage via PLL (phase-lock-loop scheme) [29] and it is adjusted to its reference by means of a double sequence controller (R_g) [30] that sets the reference voltage v_g^*.

In order to generate the reference load voltage v_l^*, the synchronization angle ϵ should be taken into account. This angle can be used to reduce the shared-leg current i_s, as discussed in [27], and can vary from 0° to 60°, see Section IV. This limit is always respected if v_l^* is synchronized with the grid voltage e_g. This alternative also minimizes the losses in leg s and improves the overall efficiency of the proposed converter, because i_s is lower than i_g and i_l.

VII. Simulation Results

Computer simulations have been carried out to demonstrate the feasibility of the proposed converter and its advantages. The simulations were carried out in a system rated at 2 kVA and an inductive load with power factor equal to 0.94 lagging. The dc-link voltage reference was set equal to 200 V and the reference load voltage was set to 180 V, resulting in a modulation index equal to 0.9. The load reference voltage v_l^* was

TABLE II
VECTOR APPLICATION SEQUENCES FOR $v_l \geq 0$ (QUADRANTS I AND II)

Sectors		Sequence	Sectors		Sequence
13		$\mathbf{v}_{130} \rightarrow \mathbf{v}_{120} \rightarrow \mathbf{v}_{122} \rightarrow \mathbf{v}_{123} \rightarrow \mathbf{v}_{103} \rightarrow \mathbf{v}_{123} \rightarrow \mathbf{v}_{122} \rightarrow \mathbf{v}_{120} \rightarrow \mathbf{v}_{130}$	19		$\mathbf{v}_{230} \rightarrow \mathbf{v}_{231} \rightarrow \mathbf{v}_{211} \rightarrow \mathbf{v}_{201} \rightarrow \mathbf{v}_{203} \rightarrow \mathbf{v}_{201} \rightarrow \mathbf{v}_{211} \rightarrow \mathbf{v}_{231} \rightarrow \mathbf{v}_{230}$
14	14a	$\mathbf{v}_{130} \rightarrow \mathbf{v}_{120} \rightarrow \mathbf{v}_{121} \rightarrow \mathbf{v}_{123} \rightarrow \mathbf{v}_{103} \rightarrow \mathbf{v}_{123} \rightarrow \mathbf{v}_{121} \rightarrow \mathbf{v}_{120} \rightarrow \mathbf{v}_{130}$	20		$\mathbf{v}_{020} \rightarrow \mathbf{v}_{120} \rightarrow \mathbf{v}_{121} \rightarrow \mathbf{v}_{123} \rightarrow \mathbf{v}_{323} \rightarrow \mathbf{v}_{123} \rightarrow \mathbf{v}_{121} \rightarrow \mathbf{v}_{120} \rightarrow \mathbf{v}_{020}$
	14b	$\mathbf{v}_{130} \rightarrow \mathbf{v}_{131} \rightarrow \mathbf{v}_{121} \rightarrow \mathbf{v}_{101} \rightarrow \mathbf{v}_{103} \rightarrow \mathbf{v}_{101} \rightarrow \mathbf{v}_{121} \rightarrow \mathbf{v}_{131} \rightarrow \mathbf{v}_{130}$	21		$\mathbf{v}_{020} \rightarrow \mathbf{v}_{021} \rightarrow \mathbf{v}_{121} \rightarrow \mathbf{v}_{321} \rightarrow \mathbf{v}_{301} \rightarrow \mathbf{v}_{321} \rightarrow \mathbf{v}_{121} \rightarrow \mathbf{v}_{021} \rightarrow \mathbf{v}_{020}$
15		$\mathbf{v}_{130} \rightarrow \mathbf{v}_{131} \rightarrow \mathbf{v}_{111} \rightarrow \mathbf{v}_{101} \rightarrow \mathbf{v}_{103} \rightarrow \mathbf{v}_{101} \rightarrow \mathbf{v}_{111} \rightarrow \mathbf{v}_{131} \rightarrow \mathbf{v}_{130}$	22	22a	$\mathbf{v}_{031} \rightarrow \mathbf{v}_{131} \rightarrow \mathbf{v}_{121} \rightarrow \mathbf{v}_{101} \rightarrow \mathbf{v}_{301} \rightarrow \mathbf{v}_{101} \rightarrow \mathbf{v}_{121} \rightarrow \mathbf{v}_{131} \rightarrow \mathbf{v}_{031}$
16		$\mathbf{v}_{031} \rightarrow \mathbf{v}_{131} \rightarrow \mathbf{v}_{111} \rightarrow \mathbf{v}_{101} \rightarrow \mathbf{v}_{301}$ $\mathbf{v}_{101} \rightarrow \mathbf{v}_{111} \rightarrow \mathbf{v}_{131} \rightarrow \mathbf{v}_{031}$		22b	$\mathbf{v}_{031} \rightarrow \mathbf{v}_{021} \rightarrow \mathbf{v}_{121} \rightarrow \mathbf{v}_{321} \rightarrow \mathbf{v}_{301} \rightarrow \mathbf{v}_{321} \rightarrow \mathbf{v}_{121} \rightarrow \mathbf{v}_{021} \rightarrow \mathbf{v}_{031}$
17		$\mathbf{v}_{031} \rightarrow \mathbf{v}_{011} \rightarrow \mathbf{v}_{111} \rightarrow \mathbf{v}_{311} \rightarrow \mathbf{v}_{301} \rightarrow \mathbf{v}_{311} \rightarrow \mathbf{v}_{111} \rightarrow \mathbf{v}_{011} \rightarrow \mathbf{v}_{031}$	23		$\mathbf{v}_{031} \rightarrow \mathbf{v}_{021} \rightarrow \mathbf{v}_{221} \rightarrow \mathbf{v}_{321} \rightarrow \mathbf{v}_{301} \rightarrow \mathbf{v}_{321} \rightarrow \mathbf{v}_{221} \rightarrow \mathbf{v}_{021} \rightarrow \mathbf{v}_{031}$
18	18a	$\mathbf{v}_{031} \rightarrow \mathbf{v}_{231} \rightarrow \mathbf{v}_{211} \rightarrow \mathbf{v}_{201} \rightarrow \mathbf{v}_{301} \rightarrow \mathbf{v}_{201} \rightarrow \mathbf{v}_{211} \rightarrow \mathbf{v}_{231} \rightarrow \mathbf{v}_{031}$	24		$\mathbf{v}_{031} \rightarrow \mathbf{v}_{231} \rightarrow \mathbf{v}_{221} \rightarrow \mathbf{v}_{201} \rightarrow \mathbf{v}_{301} \rightarrow \mathbf{v}_{201} \rightarrow \mathbf{v}_{221} \rightarrow \mathbf{v}_{231} \rightarrow \mathbf{v}_{031}$
	18b	$\mathbf{v}_{031} \rightarrow \mathbf{v}_{011} \rightarrow \mathbf{v}_{211} \rightarrow \mathbf{v}_{311} \rightarrow \mathbf{v}_{301} \rightarrow \mathbf{v}_{311} \rightarrow \mathbf{v}_{211} \rightarrow \mathbf{v}_{011} \rightarrow \mathbf{v}_{031}$			

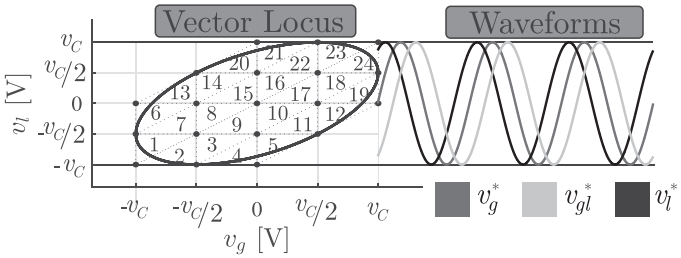


Fig. 6. Vector locus and the sinusoidal waveforms.

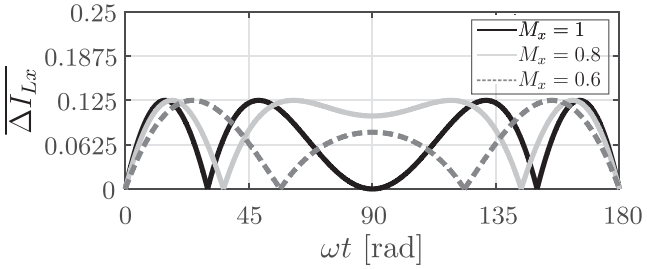


Fig. 7. Normalized peak-to-peak current ripple of the ac filters ΔI_{Lx}.

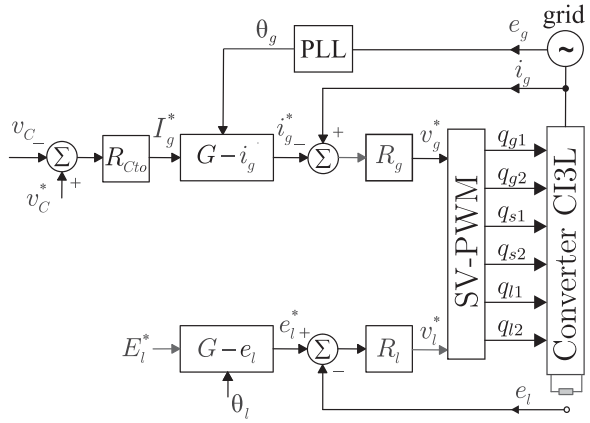


Fig. 8. System control block diagram.

TABLE III
CIRCUIT PARAMETERS

Parameter	Value
Grid Voltage	$e_g = 127$ V(rms)
Reference load voltage	$v_l^* = 127$ V(rms)
Reference DC-link voltage	$v_C^* = 200$ V
DC-link capacitance	$C_0 = 2200$ μF
RL load	$R = 6.45$ Ω, $L = 6$ mH
Switching frequency	$f_s = 10$ kHz
Coupled inductor impedance	$L_z = 1.5$ mH $M_z = 99\%$ of L_z
Filter impedance	$R_g = 0.2\Omega$, $L_g = 4$ mH

synchronized with the grid voltage e_g. The circuit parameters used in the simulations are provided in Table III.

Simulation waveforms shown in Fig. 9 include voltage v_g and its reference (a), voltage v_l and its reference (b), harmonic spectra of v_g (c) and v_l (d), dc-link voltage v_C (e), grid voltage and current (f), and currents i_g, i_l, and i_s (g). The SV-PWM strategy produces five-level output waveforms and, while the actual switching frequency is 10 kHz, v_g and v_l present an effective high-frequency spectrum of 20 kHz (twice the switching frequency). The dc-link voltage v_C, grid-side signals e_g and i_g and currents i_g, i_s, and i_l can be seen in Fig. 9(e)–(g), respectively. As can be seen, all control requirements were established. The grid, load, and shared-leg currents are sinusoidal and properly controlled [see Fig. 9(f) and (g)]. The dc-link voltage is maintained at its reference 200 V [see Fig. 9(e)] and the synchronization technique guarantees a shared-leg current with lower amplitude than i_g and i_l [see Fig. 9(g)].

Figure 10 shows the voltage vector locus and the reference voltages (a), the pole voltages v_{g0} (b), v_{s0} (c), and v_{l0} (d) and the currents through the coupled-inductors winding i_{g1} and i_{g2} (e), i_{s1} and i_{s2} (f), and i_{l1} and i_{l2} (g). It can be noted that when the reference vector v^* is located in quadrants I and III, the phase leg s is clamped in -100 V ($-v_C/2$) and 100 V ($v_C/2$), respectively, while the legs g and l are switching. When v^* is tipped in quadrant II (sector 15) and IV (sector 10), the phase leg

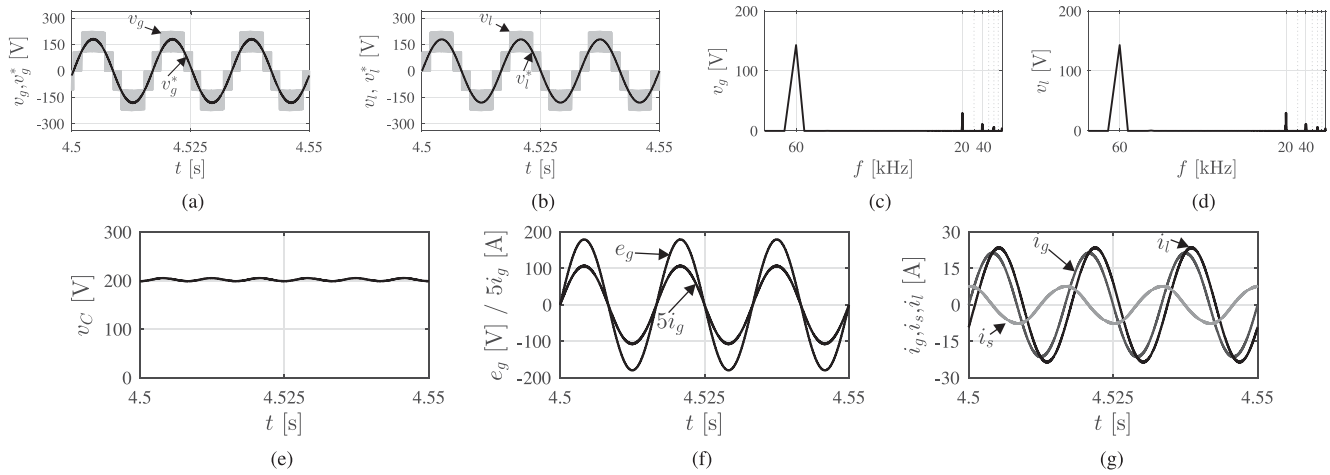


Fig. 9. Simulation results. (a) Voltage v_g and its reference. (b) Voltage v_l and its reference. (c) Harmonic spectra of v_g. (d) Harmonic spectra of v_l. (e) DC-link voltage v_C. (f) Grid voltage e_g and current i_g. (g) Currents i_g, i_l and i_s.

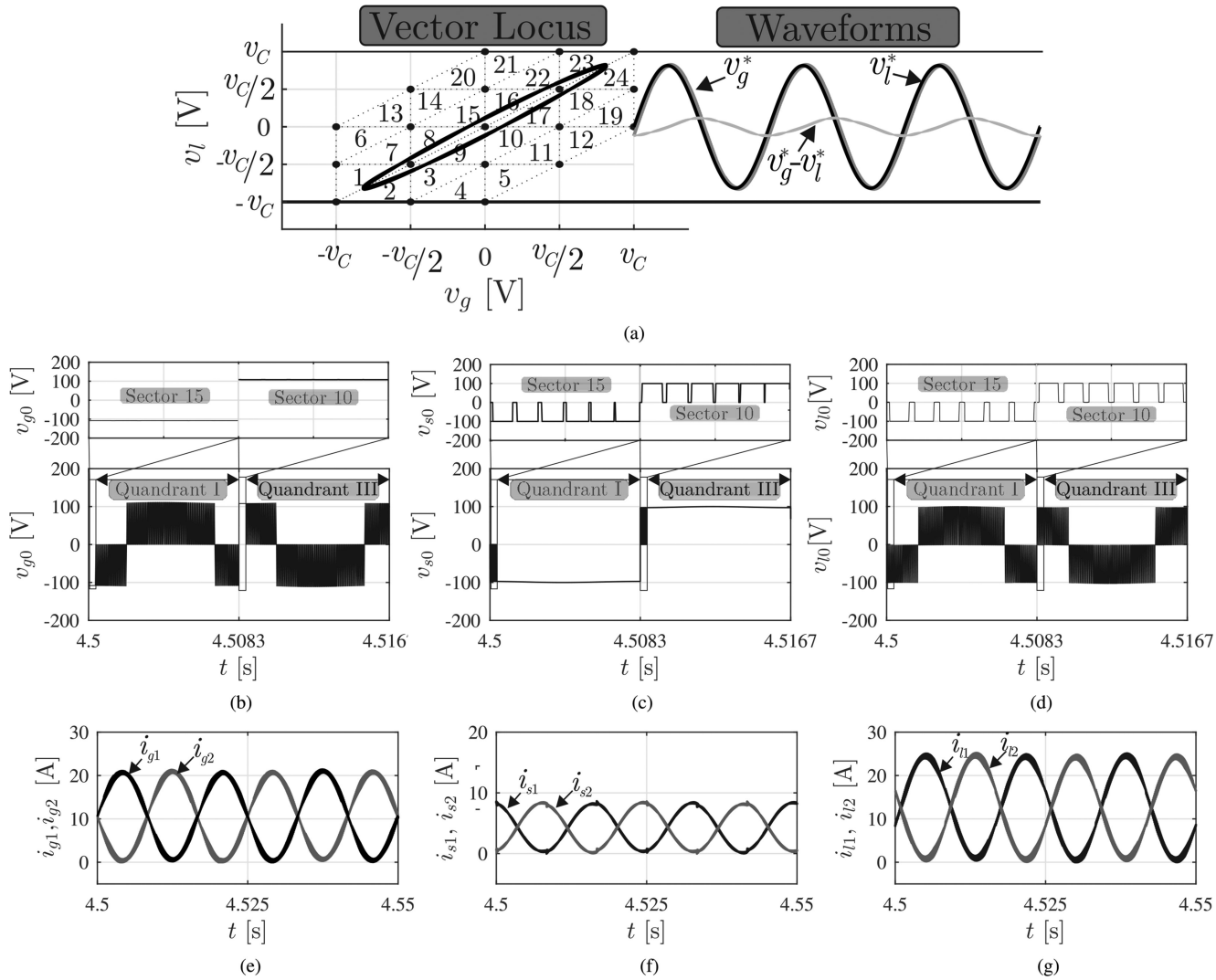


Fig. 10. Simulation results. (a) Voltage vector locus and sinusoidal waveforms. (b) Pole voltage v_{g0}. (c) Pole voltage v_{s0}. (d) Pole voltage v_{l0}. (e) i_{g1} and i_{g2}. (f) i_{s1} and i_{s2}. (g) i_{l1} and i_{l2}.

TABLE IV
COMPARISON BETWEEN THE PROPOSED CONFIGURATION AND TOPOLOGIES 3L AND 3LNPC

Parameter	Conv. 3L	Conv. 3LNPC	Proposed Topology
Number of Switches	6	12	6
Voltage Levels	3	5	5
Number of Diodes	0	6	6
Number of Drivers	6	12	6
Switches voltage rating	v_C	$\frac{1}{2}v_C$	v_C
Legs current ratings	$\begin{cases} i_{gRms} = \frac{I_{gpeak}}{\sqrt{2}} \\ i_{lRms} = \frac{I_{lpeak}}{\sqrt{2}} \\ i_{sRms} = \frac{I_{gpeak} - I_{lpeak}}{\sqrt{2}} \end{cases}$	$\begin{cases} i_{gRms} = \frac{I_{gpeak}}{\sqrt{2}} \\ i_{lRms} = \frac{I_{lpeak}}{\sqrt{2}} \\ i_{sRms} = \frac{I_{gpeak} - I_{lpeak}}{\sqrt{2}} \end{cases}$	$\begin{cases} i_{g1Rms} = i_{g2Rms} = 0.86\frac{I_{gpeak}}{\sqrt{2}} \\ i_{l1Rms} = i_{l2Rms} = 0.86\frac{I_{lpeak}}{\sqrt{2}} \\ i_{s1Rms} = i_{s2Rms} = 0.86\frac{I_{gpeak} - I_{lpeak}}{\sqrt{2}} \end{cases}$
Ac-Filters L_x	$\frac{v_C}{4f_s\Delta I_x}$	$\frac{v_C}{8f_s\Delta I_x}$	$\frac{v_C}{16f_s\Delta I_x}$
Voltage Sensors	3	4	3
Current Sensors	1	1	1

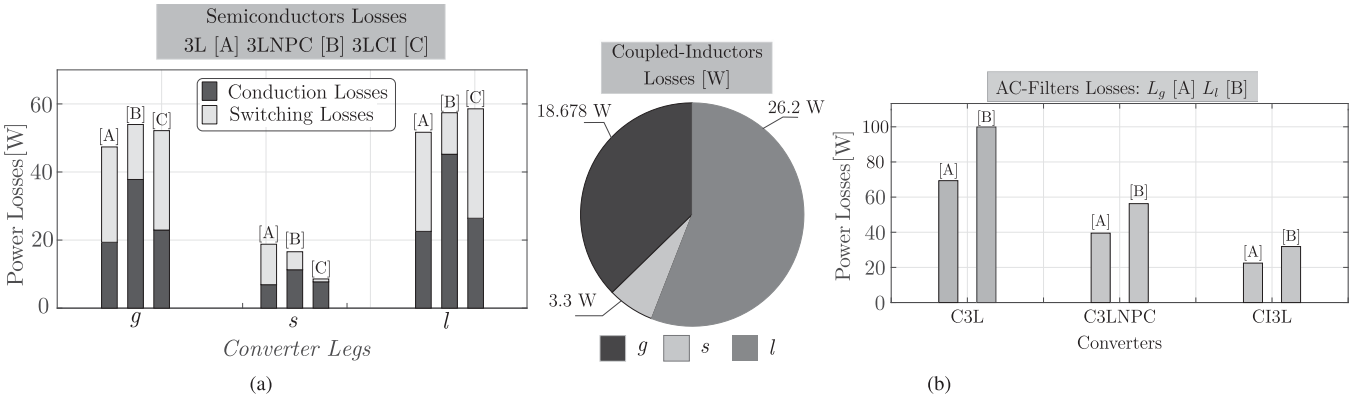


Fig. 11. Power losses. (a) Losses breakdown of the converter legs. (b) Magnetic losses.

g is clamped in -100 and 100 V, respectively, while legs s and l are switching. Furthermore, the currents through the coupled inductors are properly controlled and maintained at a positive dc value [see Fig. 10(e)–(g)].

VIII. COMPARATIVE ANALYSIS

This section compares the proposed converter (3LCI) with the 3L [27] and the 3LNPC [7] converters. Table IV shows the comparison of the aforementioned topologies in relation to the number of components, and the voltage and current ratings of the semiconductors. As can been seen, the proposed converter uses the same number of controlled switches as the 3L topology. In fact, this topology is able to generate the same five-level PWM voltages as the 3LNPC with half the number of switches and gate driver circuit components. This allows a reduction in the cost and complexity of the system, making the 3LCI topology preferable for ac–dc–ac applications. Furthermore, while 3L and 3LNPC topology have to use dead time to prevent short circuit of the dc link, the 3LCI topology requires no dead time and consequently, the generated currents have less harmonic content.

Regarding the switching device specifications, the voltage rating of each semiconductor of 3LCI and 3L topologies are the same and they are twice as those in the 3LNPC topology. As a consequence, 3LNPC has a better performance in terms of switching losses. On the other hand, the current ratings of the devices given by the RMS (root mean square) currents i_g, i_s, and i_l are smaller for 3LCI than for the 3L topology. This happens because the legs of 3LCI operate with grid ($0.86i_{\text{gRms}}$) and load currents ($0.86i_{\text{lRms}}$) 14% smaller than the 3L converter. The inner device current ratings of 3LNPC are the same as that in the 3L topology, as shown in [7], while the upper and lower device current ratings are lower. However, due to a large number of components in the current path, the conduction losses of 3LNPC are higher than those in 3L and 3LCI converters.

In order to investigate the efficiency, the theoretical losses breakdown of each converter leg is presented in Fig. 11(a). The results were obtained by using the parameters presented in Table III. The power losses on the semiconductor are composed of conduction and switching losses and were estimated by using the software PSIM. The power loss breakdown of the proposed converter reveals that leg s has a small contribution with switching losses, in counterpart to the conduction losses. This happens because the shared leg is clamped in $(-v_C/2)$ and $(v_C/2)$ when the reference vector is located in the first and third quadrant, respectively. This allows an improvement in the efficiency of the rectifier, as well as the inverter side of the 3LCI topology.

The total power semiconductor loss is equal to 117.8, 127.8, and 119.3 W for 3L, 3LNPC, and 3LCI topology, respectively. Although 3L topology is more efficient than the 3LNPC and

3LCI converters, these surpass 3L in terms of voltage waveform quality. This means that to generate waveforms with same harmonic content as 3LNPC and 3LCI converters, 3L topology needs a higher switching frequency, which leads to higher power losses.

Regarding the losses introduced by the coupled inductors, it should be noted that the coupled inductors allow a reduction in the current ripple through the ac filters, reducing their size and losses. From Table IV, the 3LCI converter reduces the size of the ac filters by 75% and 50% compared to 3L and 3LNPC converters, respectively. Fig. 11(b) shows the theoretical magnetic losses generated by the aforementioned topologies. The ac filters were designed for the same output current and an inductive load of 2 kVA, and a power factor equal to 0.94 lagging was considered. The power losses on the magnetic elements are composed of conduction and core losses and were estimated by using the winding resistance and the Steinmetz equation [31]. Neglecting the skin and the proximity effects, the copper losses are calculated by the following equations [32]:

$$P_{cu} = \begin{cases} R_{cu} I_{g,l}^2, \text{ for the ac filters} \\ R_{cu}(0.86 I_{g,s,l})^2, \text{ for the coupled inductors} \end{cases}. \quad (26)$$

The copper resistance is calculated as follows:

$$R_{cu} = \rho N \frac{l_w}{A_w} \quad (27)$$

where ρ is the resistivity of the conductor, N is the number of turns of each winding, l_w is the mean length of a turn, and A_w is the cross-sectional area of the copper wire. From Faraday's law, the number of turns N can be calculated as follows [31]:

$$N = \frac{L I_{x_{\text{peak}}}}{B_{\text{peak}} A_e} \quad (28)$$

where B_{peak} is the peak flux density of the magnetic material core and A_e is the cross-sectional area of the core. Then, the copper losses are given by

$$P_{cu} = \begin{cases} \rho \frac{l_w L I_{\text{x,peak}}}{B_{\text{peak}} A_e A_w} I_{g,l}^2, \text{ for the ac filters} \\ \rho \frac{l_w L I_{x,\text{peak}}}{B_{\text{peak}} A_e A_w} (0.86 I_{g,s,l})^2, \text{ for the coupled inductors.} \end{cases} \quad (29)$$

In [18], [33], and [34], a complete investigation of the impact of the coupled inductors in the efficiency and design of these magnetic components was presented. The main conclusion is that the coupled inductor is not a drawback in terms of copper and core losses. It was shown that the common-mode current ripple (ΔI_{Cmx}) is a key parameter for optimizing the copper losses of the coupled inductors. As lower ΔI_{Cmx} is, higher the copper losses of the coupled inductors will be. A ΔI_{Cmx} equal to 43% of I_{Cmx} gives a good performance in terms of both copper and core losses, as shown in [33].

In this paper, the design of the coupled inductors was not optimized in any sense and a ΔI_{Cmx} equal to 15.278% was used. The total copper losses calculated are 15.7, 22.5, and 2.5 W for legs g, l, and s, respectively. Since the converter is supplying a 2-kVA load, this result represents a decrease of 2% in the efficiency of the proposed converter, which is a small contribution. Following the design guidelines of [18], [33], and [34], these losses can be even lower. These results are enough to prove that the resistance of the coupled inductors is not a disadvantage in terms of efficiency.

TABLE V
HARMONIC DISTORTION PRODUCED BY THE COMPARED TOPOLOGIES

Parameter		Conv. 3L	Conv. 3LNPC	Conv. 3LCI
WTHD	v_g	0.16 %	0.14%	0.09%
	v_l	0.22 %	0.16%	0.12%
THD	i_g	0.93%	0.7%	0.57%
	i_l	0.65%	0.5%	0.34%

Regarding a comparison with similar topologies, the proposed topology has as advantages, the reduction of the ac-filter size and losses. The losses of the ac filters of the proposed topology are reduced by 43.28% and 67.85% in relation to 3LNPC and 3L converters, respectively. The total losses generated by the magnetic elements (including the losses of the ac filters) are 102.47 W for the 3LCI, 95.8 W for 3LNPC, and 169 W for the C3L topology. Therefore, one can say that compared with similar topologies, the extra losses introduced by the resistance of the coupled inductors are close to the ones of the larger filters of the standard topologies.

Although it is not trivial to say which option is most cost effective, indeed, topology C3L is the cheapest and topology 3LCI is cheaper than 3LNPC because it provides better power quality with a reduced number of active switches and has fewer isolated gate drivers than the 3LNPC converter, which can drastically reduce the cost of the system. Furthermore, Table IV shows the number of voltage and current sensors of the compared topologies. 3LNPC has one additional voltage sensor than converters 3L and 3LCI, which adds to the cost of the system.

A comparison in terms of harmonic distortion is presented in Table V. The comparison takes into account the weighted total harmonic distortion (WTHD) of the grid and load voltage, v_g and v_l, respectively, and the total harmonic distortion (THD) of i_g and i_l, and the results were obtained by using the parameters given in Table III and the same ac-filter inductances were used. Table V shows that the proposed configuration has a better performance in terms of harmonic distortion than the topologies 3L and 3LNPC. These results are expected, because the voltages v_g and v_l of the 3LCI topology operate with a frequency twice higher than the switching frequency.

IX. EXPERIMENTAL RESULTS

Experimental results are presented in order to validate the operation of the proposed converter, as well as the developed SV-PWM strategy. The experimental setup can be seen in Fig. 12. The switches are IGBTs, from SEMIKRON, with dedicated drivers (SKH123). The gating signals were generated by digital signal processor TMS320F28335, which uses appropriated plug-in boards and sensors to measure the control variables. The experimental parameters used are the same ones used for the simulations and can be seen in Table III.

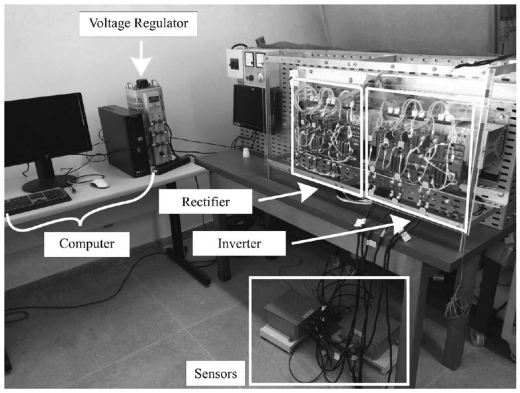


Fig. 12. Photograph of the experimental setup.

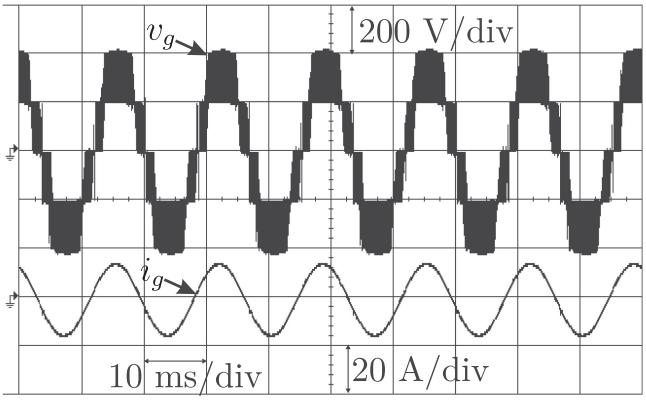


Fig. 13. Experimental waveforms of v_g and the grid current i_g.

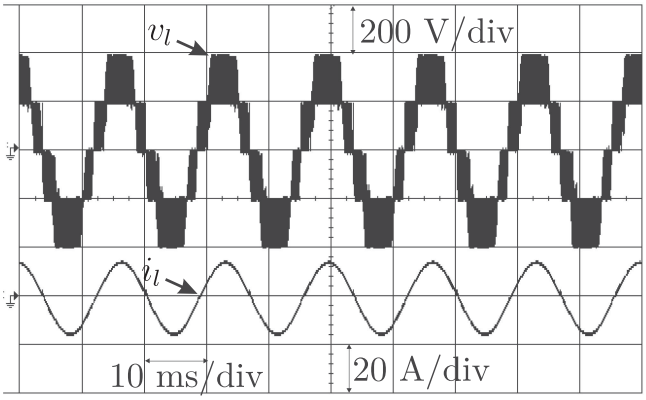


Fig. 14. Experimental waveforms of v_l and the grid current i_l.

Figures 13 and 14 show the voltages v_g and v_l, respectively, of the proposed converter. As expected, voltages v_g and v_l are five-level voltages without any overlap of the voltage levels. Fig. 15 shows the grid voltage e_g and the currents i_g, i_s, and i_l. The grid power factor is close to unity and, as a consequence, only active power is provided by the grid side of the proposed converter. Furthermore, the shared-leg current i_s is lower than i_g and i_l.

The pole and the dc-link voltages can be seen in Fig. 16. As expected, the developed SV-PWM strategy guarantees that

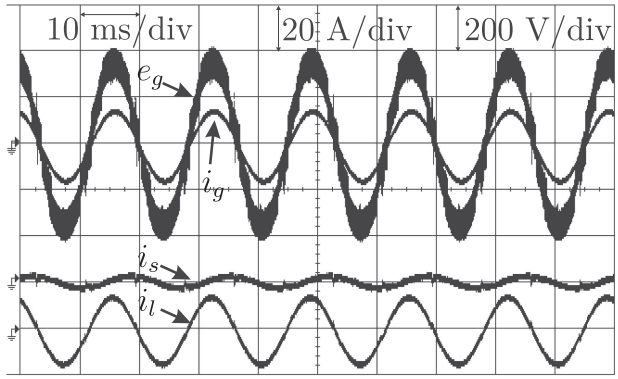


Fig. 15. Experimental waveforms of the grid voltage e_g and the currents i_g, i_s, and i_l.

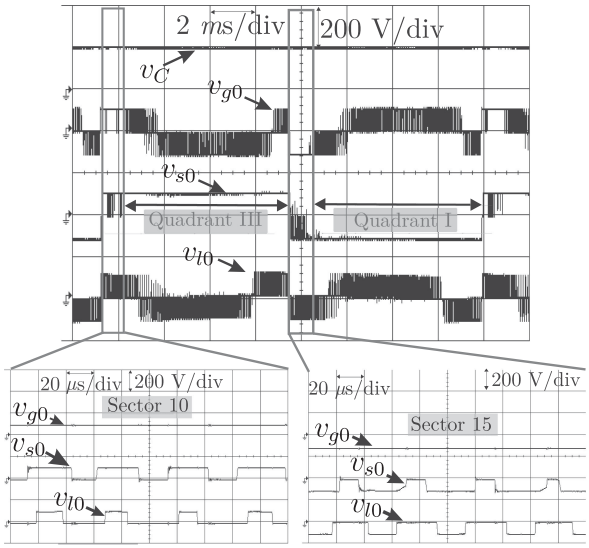


Fig. 16. Experimental waveforms of the pole voltages.

one phase leg is always clamped while the other two legs are switching. In quadrants I and III, phase leg s is clamped in $-v_C/2$ and $v_C/2$, respectively, and in quadrants II and IV, phase leg g is clamped in $v_C/2$ and $-v_C/2$, respectively. Additionally, the dc-link voltage is properly controlled and maintained in 200 V. The experimental waveforms of the pole voltages shown in Fig. 16 are in quite good agreement with the expectations. The results obtained are very similar with simulation results, indicating that the SV-PWM is operating correctly.

The experimental results presented in Figs. 17 and 18 show the behavior of the grid voltage and current, dc-link voltage, load current, and voltages v_g and v_l when the output load changes from ($R = 29.6\ \Omega$, $L = 12$ mH) to ($R = 14.8\ \Omega$, $L = 12$ mH). It can be seen that the dc-link voltage returns to the reference value after a load step and it is properly controlled. The input current is sinusoidal and properly controlled. Even with the load step change, it was possible to obtain output voltages (v_g and v_l) with five levels, validating the SV-PWM strategy.

The input power factor can be seen in Fig. 19. As can be seen, the phase displacement between e_g and i_g equals 3.4°. Hence, the grid current presents a sinusoidal shape with an input factor

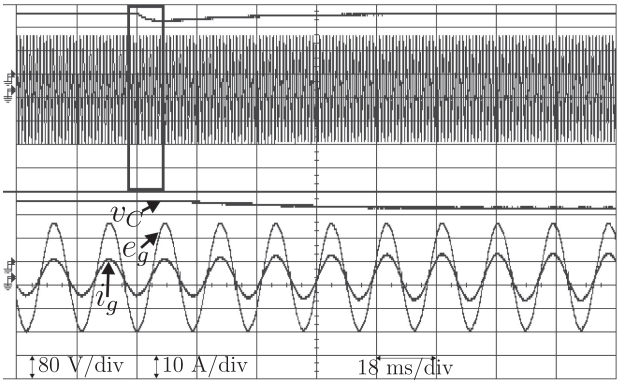


Fig. 17. Transient load response e_g, i_g, and v_c.

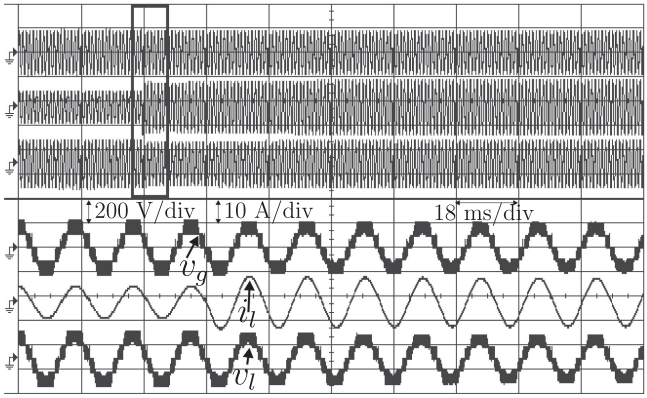


Fig. 18. Transient load response v_g, i_l, and v_l.

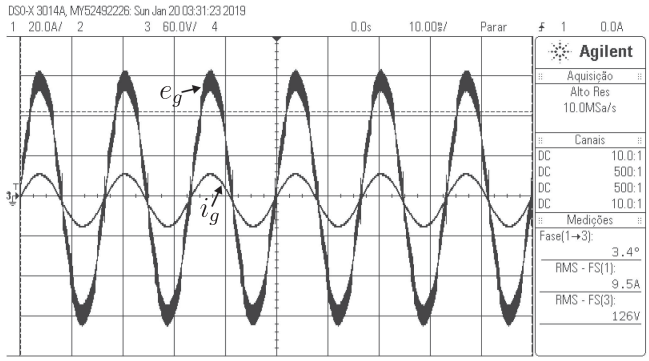


Fig. 19. Input power factor.

close to unity, indicating the correct operation of the control strategy.

In conclusion, all of the waveforms obtained in the laboratory are in good agreement with the simulations, which validates the theoretical analysis of the proposed converter.

X. Conclusion

A single-phase-to-single-phase ac–dc–ac three-level 3L converter was proposed in this paper. The topology is composed of three coupled inductors and uses only six active switches. In order to improve the performance of the configuration, a space-vector PWM technique was developed. The technique ensured five-level voltage waveforms at the input and output converter sides with an effective switching frequency equal to twice the sampling frequency. Additionally, the SV-PWM strategy guaranteed that one phase leg is always clamped while the other two legs are switching. By doing this, the switching losses were reduced and the overall efficiency of the proposed converter was increased.

In order to prove the concept, the proposed topology was experimentally tested. All the results obtained were in good agreement with the theoretical analysis, validating the SV-PWM technique and the control strategy. With the developed control strategy, it was possible to obtain a sinusoidal input current and to regulate the dc-link voltage without the need of complex algorithms, which is a major drawback of the 3LNPC converter.

A comparison of the proposed topology with the 3L and 3LNPC converters was performed. Compared to these solutions, the proposed topology has natural protection against dc-link short circuit, which improves the robustness and the reliability of the system, and eliminates the need for dead time, improving the quality of the modulated signals. The proposed converter can produce five-level output voltage and uses only six active switches. The reduced number of switches also brought the advantage of fewer isolated gate drivers, which decreased the cost and complexity of the system. Regarding the increase in the number of magnetic elements, it has been proved that the coupled inductors reduce the size of the ac filters by 75% and 50% when compared to 3L and 3LNPC converters, respectively. Therefore, the extra losses introduced by the coupled inductors can be traded for the losses associated with the large ac filters of 3LNPC and 3L topologies. In summary, 3LNPC and 3L converters have interesting features for ac–dc–ac applications, but, at the same time, do not have multilevel features, robustness, fewer active switches, and a simplified control scheme. In this scenario, the coupled-inductor 3L topology has proved to be an attractive alternative for applications such as universal power filters and UPS.

References

[1] B.-R. Lin, T.-C. Wei, and H.-K. Chiang, "Novel ac line conditioner for power factor correction," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 40, no. 1, pp. 168–179, Jan. 2004.

[2] Y. Lu, G. Xiao, X. Wang, F. Blaabjerg, and D. Lu, "Control strategy for single-phase transformerless three-leg unified power quality conditioner based on space vector modulation," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2840–2849, Apr. 2016.

[3] W. R. N. Santos, E. de Moura Fernandes, E. R. C. da Silva, C. B. Jacobina, A. C. Oliveira, and P. M. Santos, "Transformerless single-phase universal active filter with UPS features and reduced number of electronic power switches," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4111–4120, Jun. 2016.

[4] J.-H. Choi, J.-M. Kwon, J.-H. Jung, and B.-H. Kwon, "High-performance online UPS using three-leg-type converter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 889–897, Jun. 2005.

[5] J. Kwon, K. Kim, and B. Kwon, "Instant voltage compensator based on a three-leg converter," *IET Power Electron.*, vol. 6, no. 8, pp. 1618–1625, Sep. 2013.

[6] O. Kwon, J. Kwon, and B. Kwon, "Highly efficient single-phase three-level three-leg converter using SiC mosfets for ac– ac applications," *IEEE Trans. Ind. Electron.*, vol. 65, no. 9, pp. 7015–7024, Sep. 2018.

[7] I. S. de Freitas, C. B. Jacobina, E. R. C. da Silva, and T. M. Oliveira, "Single-phase ac–dc–ac three-level three-leg converter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4075–4084, Dec. 2010.

[8] N. S. M. L. Marinus, C. B. Jacobina, N. Rocha, and R. P. R. de Sousa, "An unidirectional single-phase ac–dc–ac three-level three-leg converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2017, pp. 1534–1541.
[9] N. Rocha, A. E. L. da Costa, and C. B. Jacobina, "Parallel of two unidirectional ac–dc–ac three-leg converters to improve power quality," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7782–7794, Sep. 2018.
[10] N. B. de Freitas, C. B. Jacobina, A. C. N. Maia, and A. C. Oliveira, "Six-leg single-phase to three-phase converter," *IEEE Trans. Ind. Appl.*, vol. 53, no. 6, pp. 5527–5538, Nov./Dec. 2017.
[11] M. R. Banaei, H. Khounjahan, and E. Salary, "Single-source cascaded transformers multilevel inverter with reduced number of switches," *IET Power Electron.*, vol. 5, no. 9, pp. 1748–1753, Nov. 2012.
[12] E. Babaei, S. Laali, and S. Alilu, "Cascaded multilevel inverter with series connection of novel H-bridge basic units," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6664–6671, Dec. 2014.
[13] P. R. Kumar, R. S. Kaarthik, K. Gopakumar, J. I. Leon, and L. G. Franquelo, "Seventeen-level inverter formed by cascading flying capacitor and floating capacitor H-bridges," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3471–3478, Jul. 2015.
[14] L. Zhang, K. Sun, L. Feng, H. Wu, and Y. Xing, "A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 730–739, Feb. 2013.
[15] E. C. dos Santos, J. H. G. Muniz, E. R. C. da Silva, and C. B. Jacobina, "Nested multilevel topologies," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4058–4068, Aug. 2015.
[16] H. K. Jahan, K. Zare, and M. Abapour, "Verification of a low component nine-level cascaded-transformer multilevel inverter in grid-tied mode," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 1, pp. 429–440, Mar. 2018.
[17] S. Kouro *et al.*, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
[18] C. Chapelsky, J. Salmon, and A. M. Knight, "High-quality single-phase power conversion by reconsidering the magnetic components in the output stage—Building a better half-bridge," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2048–2055, Nov./Dec. 2009.
[19] J. Ewanchuk, J. Salmon, and A. M. Knight, "Performance of a high-speed motor drive system using a novel multilevel inverter topology," *IEEE Trans. Ind. Appl.*, vol. 45, no. 5, pp. 1706–1714, Sep./Oct. 2009.
[20] C. A. Teixeira, B. P. McGrath, and D. G. Holmes, "Topologically reduced multilevel converters using complementary unidirectional phase-legs," in *Proc. IEEE Int. Symp. Ind. Electron.*, May 2012, pp. 2007–2012.
[21] B. Vafakhah, J. Ewanchuk, and J. Salmon, "Multicarrier interleaved PWM strategies for a five-level NPC inverter using a three-phase coupled inductor," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2549–2558, Nov./Dec. 2011.
[22] D. Floricau, E. Floricau, and G. Gateau, "New multilevel converters with coupled inductors: Properties and control," *IEEE Trans. Ind. Electron.*, vol. 58, no. 12, pp. 5344–5351, Dec. 2011.
[23] X. Li, B. Zhang, D. Qiu, L. Qu, G. Zhang, and F. Xie, "Modular multilevel converters using split wound coupled inductors," in *Proc. IECON - 41st Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2015, pp. 2713–2716.
[24] S. Salehahari, R. Pashaei, E. Babaei, and C. Cecati, "Coupled-inductor based multilevel inverter," in *Proc. 14th Int. Conf. Elect. Eng./Electron., Comput., Telecommun. Inf. Technol.*, Jun. 2017, pp. 907–910.
[25] B. Vafakhah, A. M. Knight, and J. Salmon, "Improved interleaved discontinuous carrier-based PWM strategy for 3-level coupled inductor inverters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2011, pp. 2095–2101.
[26] B. Vafakhah, J. Salmon, and A. Knight, "Interleaved discontinuous space-vector PWM for a multilevel PWM VSI using a three-phase split-wound coupled inductor," *IEEE Trans. Ind. Appl.*, vol. 46, no. 5, pp. 2015–2024, Sep./Oct. 2010.
[27] C. B. Jacobina, T. M. Oliveira, and E. R. C. da Silva, "Control of the single-phase three-leg ac/ac converter," *IEEE Trans. Ind. Electron.*, vol. 53, no. 2, pp. 467–476, Apr. 2006.
[28] B. Vafakhah, J. Salmon, and A. M. Knight, "A new space-vector PWM with optimal switching selection for multilevel coupled inductor inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2354–2364, Jul. 2010.
[29] R. M. S. Filho, P. F. Seixas, P. C. Cortizo, L. A. B. Torres, and A. F. Souza, "Comparison of three single-phase PLL algorithms for UPS applications," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2923–2932, Aug. 2008.
[30] C. B. Jacobina, M. B. de R. Correa, T. M. Oliveiro, A. M. N. Lima, and E. R. C. da Silva, "Current control of unbalanced electrical systems," *IEEE Trans. Ind. Electron.*, vol. 48, no. 3, pp. 517–525, Jun. 2001.
[31] C. McLyman, *Transformer and Inductor Design Handbook*. Boca Raton, FL, USA: CRC Press, 2011.
[32] A. Knight, J. Salmon, H. Syed, B. Vafakhah, and J. Ewanchuk, "A compact variable speed drive for mobile flywheel energy storage systems," in *Proc. 19th Int. Conf. Elect. Mach.*, 2010, pp. 1–6.
[33] C. Chapelsky, J. Salmon, and A. M. Knight, "Design of the magnetic components for high-performance multilevel half-bridge inverter legs," *IEEE Trans. Magn.*, vol. 45, no. 10, pp. 4785–4788, Oct. 2009.
[34] J. Salmon, J. Ewanchuk, and A. M. Knight, "PWM inverters using split-wound coupled inductors," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2001–2009, Nov./Dec. 2009.

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