# Modeling and Experimental Assessment of the EMI Characteristics of Switching Converters With Power Semiconductor Filters

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***Abstract*—An input filtering technology named "power semiconductor filter (PSF)" has been proposed recently. Its operating principle is based on using a series pass device (SPD) to profile the wave shape and magnitude of the input current of converters. The voltage across the SPD is regulated around the "knee point" of the current–voltage characteristic of the SPD to minimize the power dissipation of the SPD. This paper reports the conducted electromagnetic interference (EMI) performance of the converters with the PSF. To suppress differential-mode (DM) EMI, a fast current regulation circuit is proposed to tightly regulate the current through the SPD. To suppress common-mode (CM) EMI, a single CM noise bypass capacitor is proposed. Detailed mathematical models for describing the frequency response of the SPD and main components in the driving network are formulated. A set of selection guidelines for the components will be given. The derived models will be validated by comparing the theoretical prediction with the measurement results of a 100 W, 90–264 Vac LED driver using a buck–boost converter. Results reveal that the PSF reduces the DM noise level by 47.47 dB$\mu$V. The CM noise level is reduced by 21.4 dB$\mu$V with the bypass capacitor. An integrated circuit for the controller is illustrated to demonstrate the feasibility of reducing the form factor of the filtering section.**

***Index Terms*—Active filter, electromagnetic interference (EMI), power factor correction, power semiconductor filter.**

## I. Introduction

HIGH-FREQUENCY switching networks are main components for performing energy conversion in switching mode power converters. However, they are also sources of input current harmonics and electromagnetic interference (EMI) that would affect normal operation of other equipment sharing with the same supply mains [1], [2]. Although low-frequency input current harmonics can be mitigated by applying sophisticated control to modulate the switching sequence or pattern of the switches [3], [4], input filters are still needed to attenuate unwanted high-frequency noise from getting into the supply. Typical input filters are made up of passive components [5]. Apart from bulky volume, acoustic noise, thermal management, filter resonance, confined operating frequency range, and electromagnetic coupling among components within the confined space also impose challenges to system designers to design passive input filter [6]–[8]. Furthermore, parasitic elements in the practical filter components will affect high-frequency filtering performance [8].

As discussed in [9] and [10], the volume of passive EMI filter is one of the key limiting factors for boosting power density as miniaturization of passive components fall behind the switching network. Therefore, active EMI filtering methods are developed to reduce the reliance of bulky passive component [11]–[19]. Prior art utilizes operational amplifier (Op-amp) and/or push–pull transistor amplifier to construct either differential-mode (DM) or common-mode (CM) active EMI filters [13]–[17], [19]. Since those active circuits are designed to deal with either DM or CM noise, some proposals have combined those circuits with passive filters to form various hybrid EMI filters for volume reduction [16]–[19]. The approaches for performing active noise filtering can be categorized into noise voltage cancelation and noise current cancelation techniques [11], [17], [19]. Their idea is based on injecting a compensation voltage/current into the power line to counteract the noise voltage/current produced by the apparatus. In the circuit implementation, electrical isolation is needed. Thus, high-voltage capacitors and current transformers are commonly used to do sensing and voltage/current injection into the line [12]–[15], [16]–[19]. Nevertheless, their characteristics are frequency-dependent, and thus, affect the range of the operating frequency [18]. Moreover, bulky sensing transformer is required if the filter is designed for low-frequency operation [20], [21]. In addition, unwanted phase shift, due to the sensing and injection devices, will limit the effectiveness of

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the filter. Although some designs using active circuits exhibit high insertion loss in the 50 Ω/50 Ω test circuit in the laboratory, they only give an attenuation of 5–20 dB$\mu$V practically in the designed frequency range [13]–[15], [17], [18], [20], [21]. It is because the filter could be operated under mismatched condition, where the impedance of the noise source (i.e., switching converter) is unknown and could be much different from 50 Ω [22], [23].

Some methods apply various modulation techniques, such as chaotic and randomized switching [24]–[26], to suppress EMI. However, they might face the challenge of introducing undesired low-frequency harmonics [26].

An active DM filtering technology named "power semiconductor filter (PSF)" for filtering input current harmonic of switching converter is proposed in [27] and [28]. It offers better system dynamic via reducing the use of passive components in the input filter. Instead of using active noise voltage or current cancellation techniques, the PSF converts the input characteristic of the converter into a current source by inserting a series-pass device (SPD) and operating it as a controllable current source [29]. The DM impedance is the output impedance of the current source that can reduce unwanted current harmonics from getting into the source. The power dissipation of the SPD is limited by a SPD voltage control loop, so that the power loss of the PSF is less than 1% of the total efficiency [27]. Moreover, resistive current sensing is used. Its size and cost are lower than that of high-voltage capacitors and current transformers used in counterparts, particularly, filters for low-frequency attenuation. More importantly, the PSF can achieve a wide filtering bandwidth, covering from low-frequency current harmonics, i.e., grid frequency, to high-frequency conducted EMI noise. The PSF can also act as an input current limiter that limits inrush current and isolates the power conversion stage from the supply upon fault conditions. Thus, no dissipative resistors (typically in the range of few ohms) or NTC thermistors for limiting inrush current [30]–[33] are needed. It can also get rid of bypass relays and their associated driving circuits that would introduce power dissipation of 0.5–1 W [30].

This paper extends the work presented in [27] and [28] by studying the conducted EMI performance of converters with the PSF. Detailed mathematical models for describing the frequency response of individual components, including the SPD, operational amplifiers in the driving network, will be formulated and verified experimentally. They will then be incorporated into the system model to study the EMI performances. A 100 W, 90–264 Vac buck–boost converter for driving a string of LEDs has been built to evaluate both the DM and CM characteristics. The theoretical prediction of the derived EMI model will be favorably compared with the experimental results.

## II. Brief Overview on the Operation of the PSF

The operation of the PSF is briefly described. It is illustrated in Fig. 1(a) by applying it to a 100 W buck–boost LED driver. The driver allows a universal input of 90–264 Vac, 47–63 Hz. The output LED string current is adjustable from 0 to 500 mA. The maximum LED voltage is 200 Vdc. Fig. 1(b) shows the photo

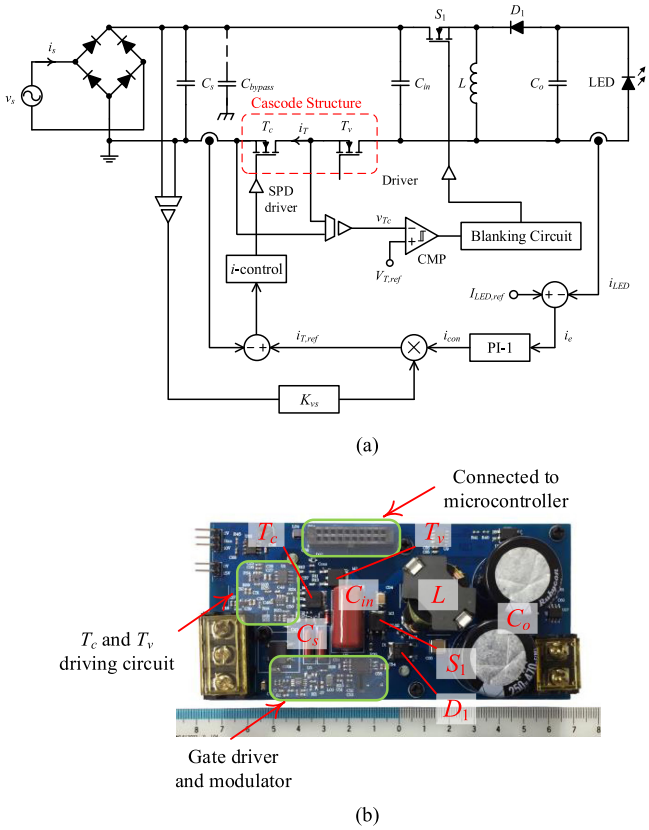


Fig. 1. Structure of buck–boost LED driver prototype. (a) Circuit schematic of the buck–boost LED driver with the PSF. (b) Photo of the prototype.

TABLE I
List of Components Used in the Prototype

| Parameter / Component | Value | Parameter / Component | Value |
|---|---|---|---|
| $C_s$ | 0.2 µF | $C_{in}$ | 1.1 µF |
| $L$ | 200 µH | $C_o$ | 942 µF |
| $T_c$ | STD19N3LLH 6AG | $T_v$ | IPD60R180P7 |
| CMP | LM1713 | LED | CREE CXA2530 |
| $S_1$ | STD8N80K5 | $D_1$ | STPSC2H12 |
| SPD driver | AD8532 | Microcontroller | dsPIC33EP16GS506 |

of the prototype. The value and part number of the components are tabulated in Table I.

The system consists of a diode bridge, a series-pass module (SPM), and a standard buck–boost converter. A string of LEDs is connected to the output of the converter. The SPM, which is constructed by two MOSFETs, $T_c$ and $T_v$, connected in a cascode structure [34], is connected in series with the buck–boost converter to profile the input current. MOSFET $T_c$ is a low-voltage device having high output impedance. It is the main device to profile the waveform of the input current. MOSFET $T_v$ is a high-voltage device. It is used to share the major voltage stress on the

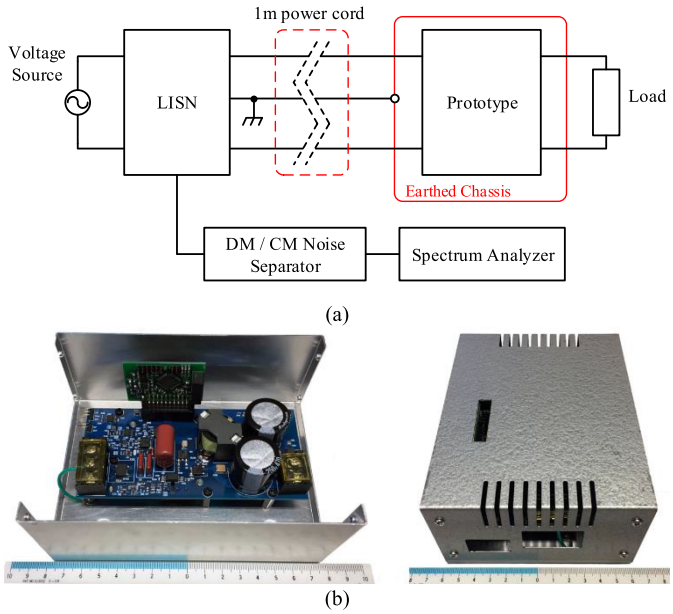


Fig. 2. Setup for testing EMI performance. (a) Equipment and connections. (b) Metal enclosure for the prototype.

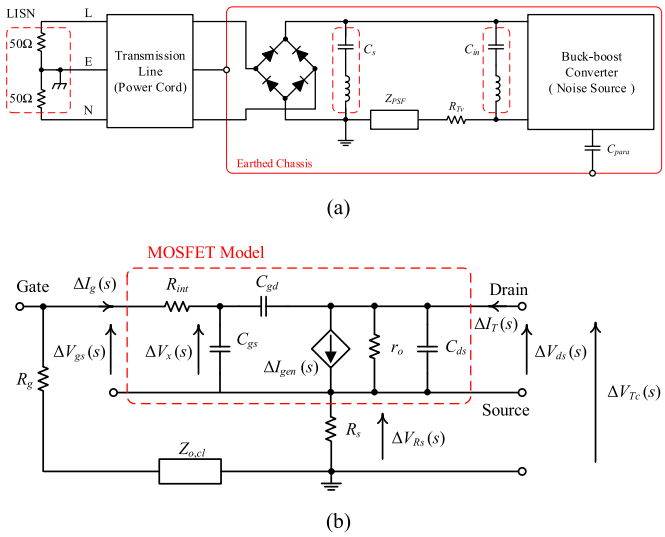


Fig. 3. Simplified circuit model for studying EMI performance. (a) AC model of the buck–boost PFC with the PSF. (b) AC equivalent-circuit model for $T_c$.

SPM at start up and around zero crossings of the supply voltage. It is dominantly turned ON with a very low ON-state resistance.

The output LED current $i_{\rm LED}$ is regulated by first comparing it with the current reference $I_{\rm LED,ref}$ and then processing the error $i_e$ with the error amplifier PI-1, which is a proportional-plus-integral controller, to generate the control signal $i_{\rm con}$. $i_{\rm con}$ is then multiplied by the down-scaled, rectified supply voltage $K_1|v_s|$ to generate the input current reference $i_{T,\rm ref}$. The current through $T_c$ is regulated at $i_{T,\rm ref}$ by comparing its value with $i_{T,\rm ref}$ and generating a control signal to $T_c$ through the current controller "*i*-control."

To minimize the power loss of the SPM, the voltage across $T_c$ is regulated at a low value by a bang-bang controller. It is first sensed and then compared with a reference voltage $V_{T,\rm ref}$ by a comparator CMP to generate the gate signal for the main switch $S_1$. The value of $V_{T,\rm ref}$ is small, typically less than 2 V. Ideally, the SPM is operated as a current source with infinite output impedance. The ripple current generated by the buck–boost converter will be circulated through the input capacitor $C_{\rm in}$. The microcontroller is used to perform the function of generating an LED current reference and housekeeping function in the system.

## III. Modeling and Analysis of EMI Characteristics

Fig. 2 shows the setup for testing the prototype. The DM/CM noise separator is used to separate the noise obtained from the line impedance stabilization network (LISN) for studying the DM and CM noise spectra. Moreover, the LED driver prototype is put into an earthed chassis to emulate actual operating condition. Fig. 2(b) shows the photo of the earthed metal enclosure that introduces paths for the CM noise.

Fig. 3 shows the circuit model for analyzing the EMI characteristics of the converter. The buck–boost converter is the noise source. For the sake of simplicity in illustrating the impact of the PSF on reducing DM and CM noise levels, nonlinear behaviors of the components and parasitic elements in the buck–boost converter are neglected in the model. However, without loss of generality, sophisticated circuit models, as discussed in [35]–[39], can be integrated into the circuit model. The validity of the proposed model is confirmed by the measurement results being in close agreement with theoretical predictions. In fact, it would be more appropriate to use sophisticated simulation software, such as SPICE and ADS, to study EMI characteristics with all nonlinear and parasitic elements included.

The parasitic capacitor $C_{\rm para}$ represents the CM noise path to the LISN due to the coupling between the power stage and the earthed chassis [35], [37], [40]. The LISN is modeled by two 50 Ω resistors [41], [42] and $T_v$ is fully turned ON during the normal operation with the ON-state resistance $R_{Tv}$ [34]. As stated in the EMI measurement standard, the power cord connecting between the LISN and the prototype is 1 m long. The impedance, $Z_{\rm PSF}$, represents the output impedance of the PSF. Its equivalent circuit is shown in Fig. 3(b). It is composed of three major components, including the closed-loop output impedance of the driver (AD8532) $Z_{o,cl}$ [43], 0.1 Ω current sensing resistor $R_s$, and small-signal model of the SPD (i.e., $T_c$) [29]. The output impedance of AD8532 and the parameters of STD19N3LLH6AG is obtained from either datasheets or SPICE models provided by the manufacturers [43], [44].

## IV. DM Noise Characteristics

Based on Fig. 3(a), the DM noise current propagation model is shown in Fig. 4. The current source, $i_{\rm DM}$, represents the pulsating input current of the buck–boost converter. The impedance, $Z_{\rm cable,DM}$, is the DM impedance of the power cord. Finally, $Z_{Cs}$ and $Z_{C\rm in}$ are the impedances of the capacitors $C_s$ and $C_{\rm in}$, respectively. $Z_{\rm PSF}$ provides a high impedance path that makes the noise current circulate through $Z_{C\rm in}$ (i.e., $C_{\rm in}$). The DM noise current through the LISN is thus reduced.

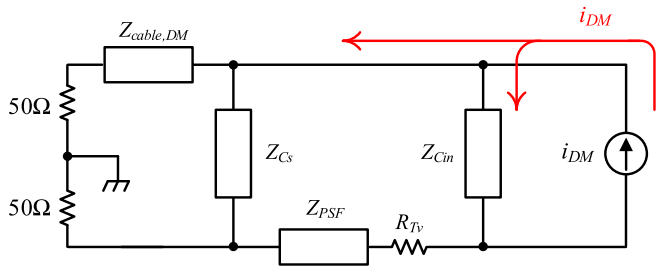


Fig. 4. Simplified DM noise current propagation path.

### A. Effects of Nonideal Characteristics of SPD

The SPD, that is, MOSFET $T_c$ is ideally operated as a current source with infinite output impedance. However, practical SPD has several nonideal characteristics that limit the filtering performance. They are described as follows.

*1) Channel-Length Modulation:* As discussed in [45], the MOSFET channel-length modulation will cause finite output impedance, $r_o$, which can be expressed as follows:

$$r_o \simeq \frac{1}{\lambda\, I_T} \tag{1}$$

where λ is the channel-length modulation parameter of the selected MOSFET device and $I_T$ is the dc value of the drain current.

$r_o$ introduces a leakage path and will lower the low-frequency noise filtering ability of the system. More importantly, the value of $r_o$ reduces as $i_T$ increases.

*2) Leakage Paths Formed by Intrinsic Capacitances:* The voltage-dependent intrinsic capacitances, including gate–source capacitance, $C_{gs}$, gate–drain capacitance, $C_{gd}$, and drain–source capacitance, $C_{ds}$, of the MOSFET, form leakage paths for high-frequency noise. Fig. 5(a) shows the measured values of $C_{gs}$, $C_{gd}$, and $C_{ds}$ of STD19N3LLH6AG under different drain–source voltages, $v_{ds}$, with the method described in [46]. Fig. 5(b) shows the values of $C_{gs}$, $C_{gd}$, and $C_{ds}$, calculated by the input capacitance $C_{iss}$, output capacitance $C_{oss}$, and reverse transfer capacitance $C_{rss}$ of IRF540N given on the datasheet [47] with the equations of

$$C_{gs} = C_{iss} - C_{rss} \tag{2}$$

$$C_{gd} = C_{rss} \tag{3}$$

$$C_{ds} = C_{oss} - C_{rss}. \tag{4}$$

The values of $C_{gs}$, $C_{gd}$, and $C_{ds}$ typically range from hundred pF to nF in high-power MOSFET, such as IRF540N, when the drain–source voltage is less than 2 V—preferred biasing condition of the SPD. Thus, they will give challenges on controlling the drain current, thus affecting the filtering ability of the PSF.

*3) Noise Coupling From Drain to Gate of SPD:* When disturbances appear on $v_{Tc}$, $C_{gs}$ and $C_{gd}$ cause capacitive coupling effects, and a voltage $v_x$ is built on $C_{gs}$. As a result, unwanted noise current $i_{\text{gen}}$, due to the trans-conductance of the MOSFET, will appear. The coupling effect can be reduced by using a driver with low output impedance and MOSFET with small intrinsic gate resistance $R_{\text{int}}$. Based on Fig. 3(b), $i_{\text{gen}}$ can

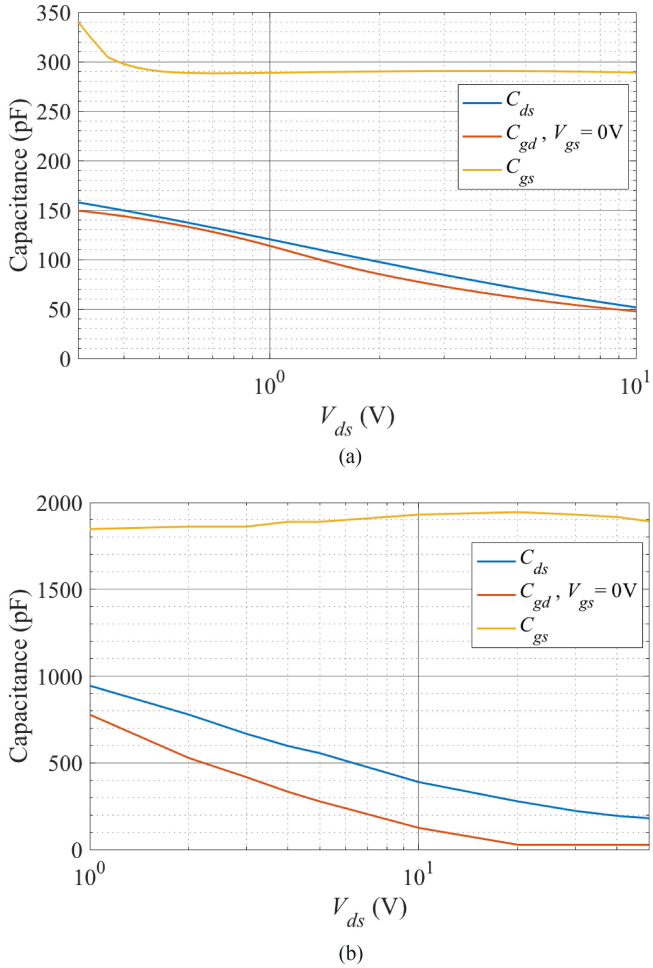


Fig. 5. Measured and calculated capacitances versus drain-source voltage, $v_{ds}$. (a) Measured capacitances versus $v_{ds}$ of STD19N3LLH6AG ($f = 1$ MHz). (b) Capacitances versus $v_{ds}$ of IRF540N ($f = 1$ MHz).

be expressed as follows:

$$\Delta I_{\text{gen}}(s) = g_m\, \Delta V_x(s) = g_m \frac{k_1}{k_2}\, \Delta V_{Tc}(s) \tag{5}$$

$$k_1(s) = Z_{cgd}\left(R_g r_o Z_{cds} + R_{\text{int}} r_o Z_{cds} - R_s\left(r_o + Z_{cds}\right) \times Z_{cgd} + r_o Z_{cds} Z_{o,cl}\right) \tag{6}$$

$$k_2(s) = r_o R_s Z_{cds} + \begin{pmatrix} r_o R_s + \left(r_o + R_s + g_m r_o R_s\right) Z_{cds} Z_{cgd} Z_{cgs} \\ + k_3 r_o R_s\left(R_g + R_{\text{int}} + Z_{o,cl}\right) + k_4\left(r_o + R_s\right) \\ \times \left(R_g + R_{\text{int}} + Z_{o,cl}\right) \end{pmatrix} \tag{7}$$

$$k_3(s) = Z_{cds} + Z_{cgd} + Z_{cgs} + g_m Z_{cds} Z_{cgs} \tag{8}$$

$$k_4(s) = Z_{cds}\left(Z_{cgd} + Z_{cgs}\right) \tag{9}$$

where $Z_{cds} = \frac{1}{s\, C_{ds}}$, $Z_{cgd} = \frac{1}{sC_{gd}}$, and $Z_{cgs} = \frac{1}{sC_{gs}}$.

### B. Output Impedance of the PSF

The equivalent output impedance of the PSF, $Z_{\text{PSF}}$, is determined by modeling the MOSFET model in Fig. 3(b) with the

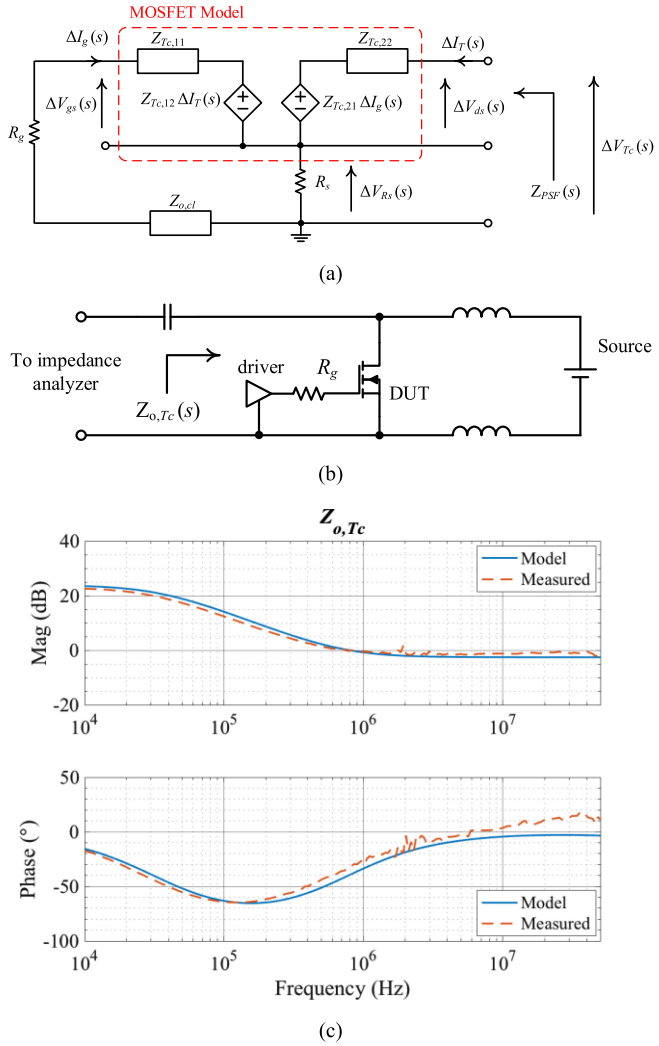


Fig. 6. Modeling of $Z_{\rm PSF}$. (a) Equivalent-circuit model of PSF with Z-parameter model. (b) Setup for measuring $Z_{o,Tc}$. (c) Measured impedance of $T_c$ under a biased condition with $R_g = 520\ \Omega$.

Z-parameter circuit model [48] and current control circuit included. It is shown in Fig. 6(a). The effect of the PFC feedback controller is neglected as the bandwidth of the controller is far below the switching frequency. The four Z-parameters including $Z_{Tc,11}$, $Z_{Tc,12}$, $Z_{Tc,21}$, and $Z_{Tc,22}$ are expressed as follows:

$$Z_{Tc,11}(s) = R_{\rm int} + \frac{Z_{cgs}\left(Z_{cgd}Z_{cds} + r_o(Z_{cgd} + Z_{cds})\right)}{m_1(s)} \tag{10}$$

$$Z_{Tc,12}(s) = \frac{r_o Z_{cds} Z_{cgs}}{m_1(s)} \tag{11}$$

$$Z_{Tc,21}(s) = \frac{r_o Z_{cds} Z_{cgs}(1 - g_m Z_{cgd})}{m_1(s)} \tag{12}$$

$$Z_{Tc,22}(s) = \frac{r_o Z_{cds}(Z_{cgd} + Z_{cgs})}{m_1(s)} \tag{13}$$

$$m_1(s) = Z_{cds}(Z_{cgd} + Z_{cgs}) + r_o(Z_{cgd} + Z_{cds} + Z_{cgs} + g_m Z_{cds} Z_{cgs}). \tag{14}$$

TABLE II
PARAMETERS AND CONDITIONS FOR SMALL-SIGNAL ANALYSIS OF STD19N3LLH6AG

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $R_{int}$ | 1.85Ω | $C_{gs}$ | 289.7pF |
| $C_{gd}$ | 131pF | $C_{ds}$ | 108.8pF |
| $g_m$ | 3.97 | $r_o$ | 15.56Ω |
| $v_{ds}$ | 1.413V | $i_T$ | 0.87A |

Based on Fig. 6(a)

$$Z_{\rm PSF}(s) = \frac{Z_{Tc,22}(Z_{Tc,11} + R_g + Z_{o,cl}) - Z_{Tc,12}Z_{Tc,21}}{Z_{Tc,11} + R_s + R_g + Z_{o,cl}} + \frac{R_s(Z_{Tc,11} - Z_{Tc,12} - Z_{Tc,21} + Z_{Tc,22} + R_g + Z_{o,cl})}{Z_{Tc,11} + R_s + R_g + Z_{o,cl}}. \tag{15}$$

Fig. 6(b) shows the setup for measuring the output impedance of the SPD and Fig. 6(c) shows the comparison of the measured output impedance $Z_{o,Tc}$ of STD19N3LLH6AG and calculated results of the $Z_{o,Tc}$ under the biasing condition of $v_{ds} = 1.413$ V and $i_T = 0.87$ A. In the measurement, $R_g$ is set at 520 Ω so that the effects of the circuit for biasing the device at the operating point and the output impedance of gate driving circuit on parameter extraction can be ignored. The parameters used in calculating $Z_{Tc}$ are shown in Table II. The values are obtained from datasheets and models, provided by manufacturers, and measurements, such as curve tracer or methods suggested in [46]. The derived model is in close agreement with the measurement results.

After determining the small-signal model of the MOSFET, the remaining parameter is the output impedance $Z_{o,cl}$ of the Op-amp driver AD8532 configured as a voltage follower. The output impedance of feedback Op-amp can be obtained from the datasheet [43] or measurement. $Z_{o,cl}$ is modeled by the method described in [49]. The model is shown in Fig. 7(a), while Fig. 7(b) shows the comparison of the derived model and the measured output impedance. Fig. 8 shows $Z_{\rm PSF}$ under different values of $R_g$. The datasheet of AD8532 has mentioned that minimum value of 20 Ω for $R_g$ is used in the prototype for op-amp output current limiting. It is shown in Fig. 8 that the smaller value of $R_g$ can achieve better filtering ability because less noise current will be generated by the controllable current source hence the voltage of $v_x$ will be reduced. However, the capacitive load ($C_{gs}$) driving capabilities of the Op-amp should be taken into account, which can cause instability issue.

### C. Fast Current Regulation Circuit for SPD

The DM reduction ability of the original driving method of PSF structure is dependent on the intrinsic parameters of the chosen device, and magnitude of $I_T$ defined in (1). To mitigate the effects of nonideal characteristics of the SPD, a fast current regulation circuit is proposed and shown in Fig. 9.

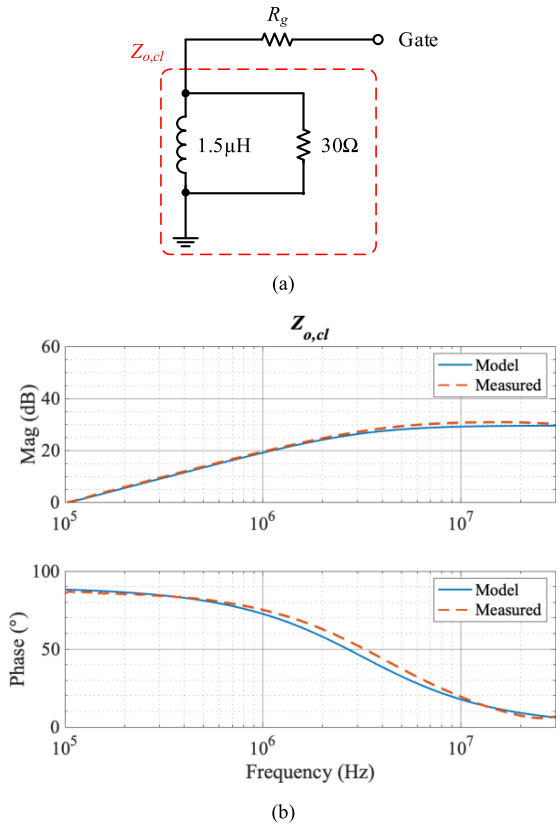


Fig. 7. Output impedance of AD8532 in voltage follower configuration. (a) Model used to determine $Z_{o,cl}$. (b) Comparison of the theoretical $Z_{o,cl}$ of AD8532 and measurement results.

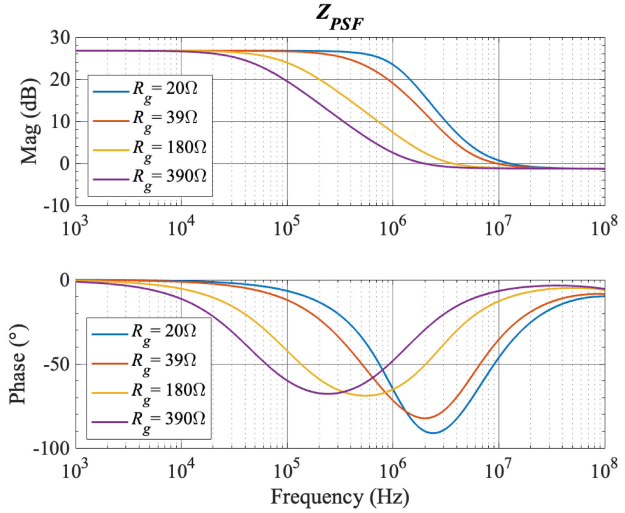


Fig. 8. $Z_{\mathrm{PSF}}$ with different values of $R_g$.

The current regulation circuit has a wide bandwidth, covering the conducted EMI frequency range without system instability. The preamplifier OA1 amplifies the voltage across the current sensing resistor $R_s$, $v_{Rs}$, so that the signal-to-noise ratio of the regulation loop can be improved. Hence, the sensitivity to the change of voltage reference $v_{iTc,\mathrm{ref}}$ can be reduced. The low-pass filter formed by the resistor $R_a$ and capacitor $C_a$ is for

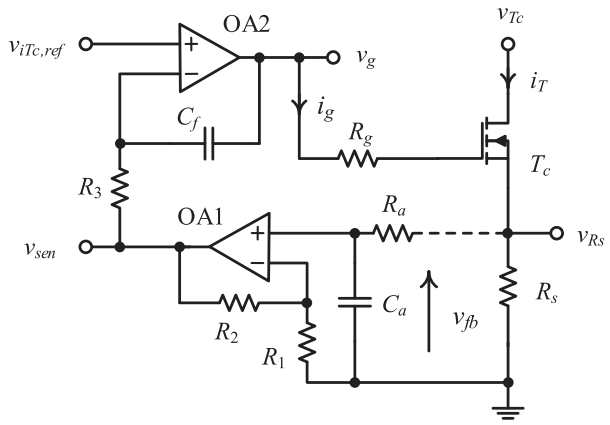


Fig. 9. Fast current regulation circuit.

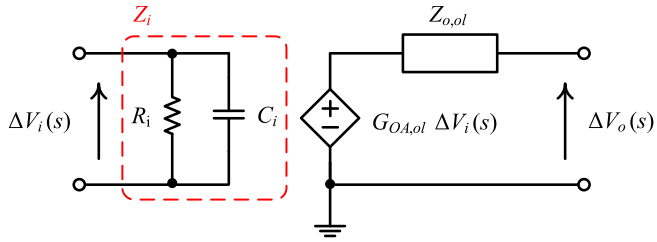


Fig. 10. Model of the operational amplifier.

signal conditioning. Then, the feedback amplifier OA2 regulates the current passing through $T_c$, so that the output of the preamplifier circuit $v_{\mathrm{sen}}$ equals $v_{iTc,\mathrm{ref}}$. Thus, $i_T$ is regulated at the level of

$$i_T = \frac{1}{\left(1+\frac{R_2}{R_1}\right)R_s} v_{iTc,\mathrm{ref}}. \tag{16}$$

The resistor $R_3$ and capacitor $C_f$ in OA2 are used to compensate the current loop to ensure its operational stability.

*1) Modeling and Stability Analysis of the Current Regulation Circuit:* The bandwidth of the fast current regulation circuit is determined by the characteristics of preamplifier OA1 and the feedback amplifier OA2. A high-speed voltage feedback amplifier, Linear Technology LTC6268-10, is used for OA1 and OA2 [47]. The operational amplifier is modeled by using the technique described in [14] and [50].

Fig. 10 shows the operational amplifier model used in the analysis. Based on the datasheet in [51], the input impedance $Z_i$ of the input port of LTC6268-10 is 1000 GΩ in parallel with a 0.1 pF differential input capacitance. The output stage of the amplifier is modeled by a controllable voltage source having an open-loop gain of the amplifier $G_{OA,ol}$ in-series with the open-loop output impedance $Z_{o,ol}$.

Fig. 11 shows the Bode plot of the open-loop gain $G_{OA,ol}$ of LTC6268-10. Based on the measurement results, the amplifier is modeled by a transfer function with two poles

$$G_{OA,ol}(s) = \frac{A_o}{\left(1+\frac{s}{2\pi f_1}\right)\left(1+\frac{s}{2\pi f_2}\right)}. \tag{17}$$

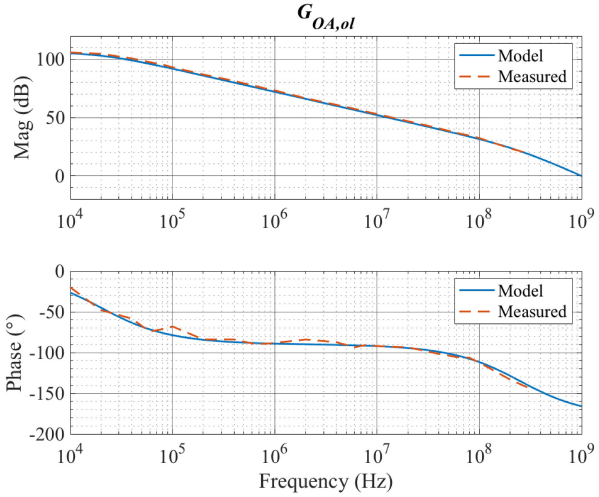


Fig. 11. Open-loop gain of LTC6268-10.

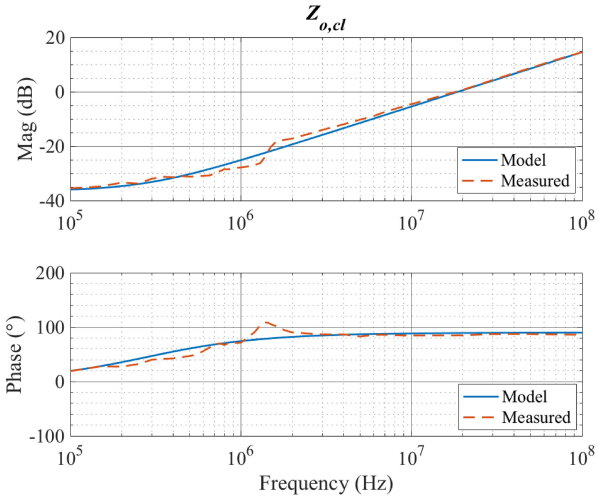


Fig. 12. Closed-loop output impedance of LTC6268-10 with $A_v = 11$.

The values of $A_o$, $f_1$, and $f_2$ are found to be 200 k, 20 kHz, and 250 MHz, respectively. The response estimated by the model is in close agreement with the measurement results.

Fig. 12 shows the measured closed-loop impedance, $Z_{o,cl}$, of LTC6268-10 with the feedback gain $A_v = 11$, where $R_1 = 50\ \Omega$ and $R_2 = 500\ \Omega$. Results show that $Z_{o,cl}$ in this condition can be modeled by an *RL* circuit with resistance and inductance equal to 15 m$\Omega$ and 8.5 nH, respectively. Then, the open-loop output impedance $Z_{o,ol}$ of the amplifier shown in Fig. 11 can be calculated by the equation of [14]

$$Z_{o,ol}(s) = Z_{o,cl}\left(1 + \frac{1}{A_v}G_{OA,ol}\right). \tag{18}$$

The calculated $Z_{o,ol}$ with the model given in Fig. 12 is shown in Fig. 13. It is found that $Z_{o,ol}$ can be modeled by a 280 $\Omega$ resistor in parallel with an *RC* circuit with the values of resistor and capacitor equal to 20 $\Omega$ and 26 nF, respectively. With the characteristics of $G_{OA,ol}$ and $Z_{o,ol}$ determined in (17) and (18), respectively, the model of the operational amplifier in Fig. 10 can be obtained.

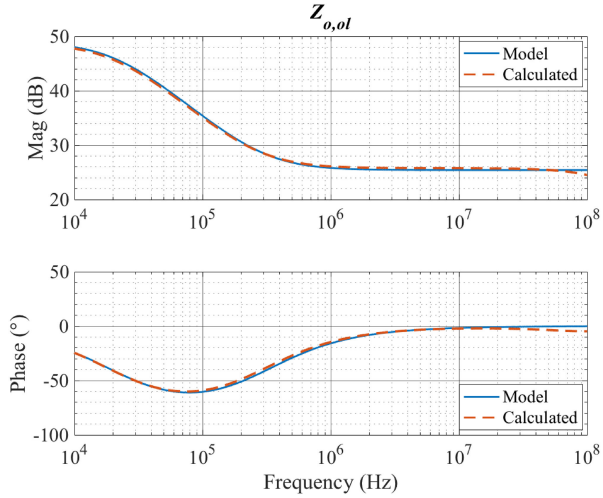


Fig. 13. Calculated open-loop output impedance of LTC6268-10.

Fig. 14(a) shows the ac model of the current regulation circuit, where voltage $v_{i1}$ and $v_{i2}$ are the differential input voltage of OA1 and OA2, respectively. In order to find the loop gain and output impedance of the system, the ac components of the current reference, $v_{iTc,\mathrm{ref}}$, is set to zero. A *Z*-parameter circuit model is applied for the OA1 and OA2 in Fig. 14(a). The *Z*-parameters for the pre-amplifier circuit, $Z_{\mathrm{PA},11}$, $Z_{\mathrm{PA},12}$, $Z_{\mathrm{PA},21}$, and $Z_{\mathrm{PA},22}$, and that for the feedback amplifier circuit, $Z_{\mathrm{FBA},11}$, $Z_{\mathrm{FBA},12}$, $Z_{\mathrm{FBA},21}$, and $Z_{\mathrm{FBA},22}$, are

$$Z_{\mathrm{PA},11}(s) = R_a + \frac{Z_a\left(Z_i\left(R_2 + Z_{o,ol}\right) + R_1\left(R_2 + Z_i\left(1 + G_{OA,ol}\right) + Z_{o,ol}\right)\right)}{m_2(s)} \tag{19}$$

$$Z_{\mathrm{PA},12}(s) = -\frac{R_1 Z_a Z_{o,ol}}{m_2(s)} \tag{20}$$

$$Z_{\mathrm{PA},21}(s) = \frac{Z_a\left(Z_i G_{OA,ol}\left(R_1 + R_2\right) + R_1 Z_{o,ol}\right)}{m_2(s)} \tag{21}$$

$$Z_{\mathrm{PA},22}(s) = -\frac{Z_{o,ol}\left(R_1\left(R_2 + Z_a + Z_i\right) + R_2\left(Z_a + Z_i\right)\right)}{m_2(s)} \tag{22}$$

$$m_2(s) = \left(Z_a + Z_i\right)\left(R_2 + Z_{o,ol}\right) + R_1\left(R_2 + Z_a + Z_i\left(1 + G_{OA,ol}\right) + Z_{o,ol}\right) \tag{23}$$

$$Z_{\mathrm{FBA},11}(s) = R_3 + \frac{Z_i(Z_{o,ol} + Z_{cf})}{m_3(s)} \tag{24}$$

$$Z_{\mathrm{FBA},12}(s) = -\frac{Z_i Z_{o,ol}}{m_3(s)} \tag{25}$$

$$Z_{\mathrm{FBA},21}(s) = \frac{Z_i(Z_{o,ol} - Z_{cf}G_{OA,ol})}{m_3(s)} \tag{26}$$

$$Z_{\mathrm{FBA},22}(s) = -\frac{Z_{o,ol}(Z_i + Z_{cf})}{m_3(s)} \tag{27}$$

$$m_3(s) = Z_i(1 + G_{OA,ol}) + Z_{o,ol} + Z_{cf} \tag{28}$$

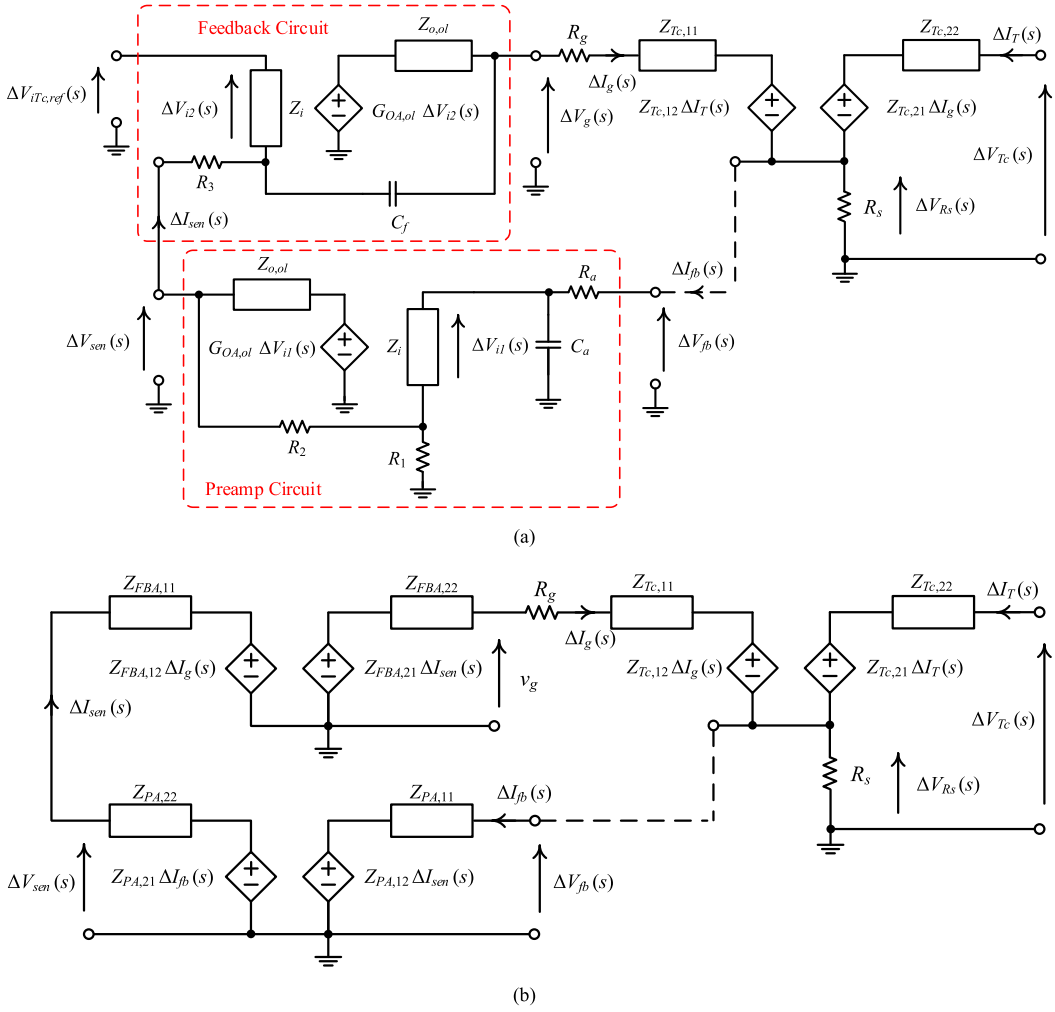


Fig. 14. AC model of the fast current regulation circuit. (a) AC model of the current regulation circuit with the derived Op-amp model. (b) Simplified ac model of the current regulation circuit with Z-parameter.

The open-loop gain $G_{\rm OL}$ of the feedback system is calculated by using the Z-parameter circuit model shown in Fig. 14(b). By setting the ac component of $v_{Tc}$, $\Delta V_{Tc}$ to zero and using (19)–(28), the following variables can be derived:

$$I_{\rm in}(s) = \frac{V_{fb}(s) - Z_{\rm PA,12} I_{\rm sen}(s)}{Z_{\rm PA,11}} \tag{29}$$

$$I_{\rm sen}(s) = \frac{Z_{\rm PA,21} I_{\rm in}(s) - V_{\rm sen}(s)}{Z_{\rm PA,22}} \tag{30}$$

$$I_{\rm sen}(s) = \frac{V_{\rm sen}(s) - Z_{\rm FBA,12} I_g(s)}{Z_{\rm FBA,11}} \tag{31}$$

$$I_g(s) = \frac{Z_{\rm FBA,21} I_{\rm sen}(s) - V_g(s)}{Z_{\rm FBA,22}} \tag{32}$$

$$I_g(s) = \frac{V_g(s) - Z_{Tc,12} I_T(s) - V_{Rs}(s)}{R_g + Z_{Tc,11}} \tag{33}$$

$$I_T(s) = \frac{0 - Z_{Tc,21} I_g(s) - V_{Rs}(s)}{Z_{Tc,22}} \tag{34}$$

$$I_T(s) + I_g(s) = \frac{V_{Rs}(s)}{R_s}. \tag{35}$$

Based on (29)–(35), $G_{\rm OL}$ can be expressed as Eq. (36), which is shown at the bottom of this page, where

$$m_4(s) = Z_{\rm FBA,11} Z_{\rm PA,11} + Z_{\rm PA,12} Z_{\rm PA,21} + Z_{\rm PA,11} Z_{\rm PA,22} \tag{37}$$

$$m_5(s) = Z_{\rm FBA,12} Z_{\rm FBA,21} Z_{\rm PA,11} + m_4 \left( R_g + Z_{\rm FBA,22} + Z_{Tc,11} \right). \tag{38}$$

Fig. 15 shows the Bode plot of the $G_{\rm OL}$ with and without the compensation capacitor $C_f$. It is shown that both gain margin (–4.496 dB at 193.8 MHz) and phase margin (–47.32° at 265.1 MHz) are negative if there is no compensation capacitor.

$$G_{\rm OL}(s) = \frac{V_{Rs}(s)}{V_{fb}(s)} = \frac{R_s Z_{\rm FBA,21} Z_{PA,21} \left( Z_{Tc,21} - Z_{Tc,22} \right)}{m_4 \left( Z_{Tc,12} Z_{Tc,21} + R_s \left( Z_{Tc,12} + Z_{Tc,21} + Z_{Tc,22} \right) \right) - m_5 \left( R_s + Z_{Tc,22} \right)} \tag{36}$$

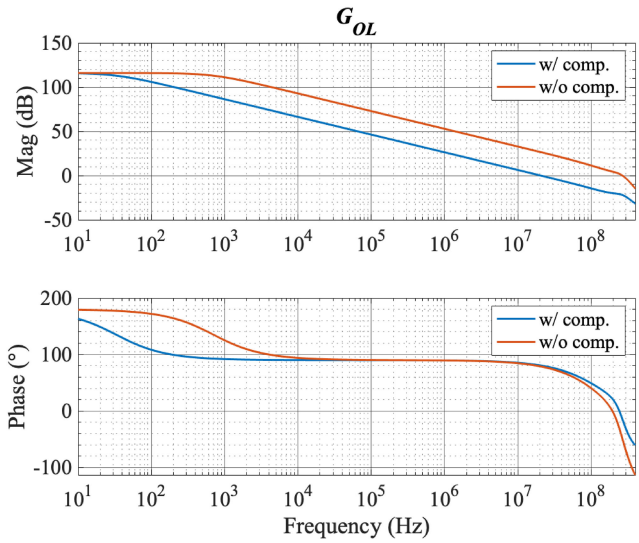


Fig. 15. Open-loop gain of the entire current regulation system.

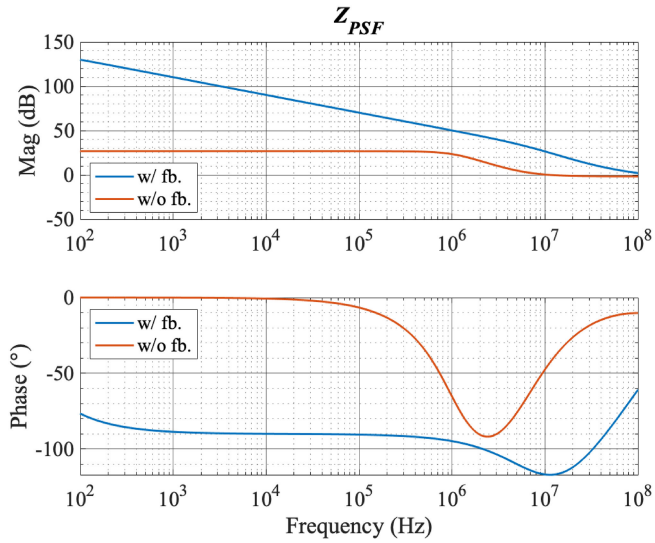


Fig. 16. Comparison of $Z_{\rm PSF}$ with and without the current regulation circuit.

TABLE III
COMPONENT VALUES USED IN THE CURRENT REGULATION CIRCUIT

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $R_a$ | 1 mΩ | $C_a$ | 0.45 pF |
| $R_1$ | 90.9 Ω | $R_2$ | 909 Ω |
| $R_3$ | 109 Ω | $C_f$ | 220 pF |
| $R_g$ | 1 Ω | $R_s$ | 0.1 Ω |

After adding a 220 pF compensation capacitor, sufficient gain margin (20.92 dB at 241.8 MHz) and phase margin (80.62° at 20.43 MHz) is achieved. The component values are given in Table III.

*2) Model of Output Impedance for PSF With Fast Current Controller:* Based on Fig. 14(b), the output impedance of PSF with the fast current feedback loop, $Z_{{\rm PSF},fb}$, is obtained by setting $v_{fb} = v_{Rs}$. Then

$$I_{\rm in}(s) = \frac{V_{Rs}(s) - Z_{\rm PA,12} I_{\rm sen}(s)}{Z_{\rm PA,11}} \tag{39}$$

$$I_T(s) = \frac{V_T(s) - Z_{Tc,21} I_g(s) - V_{Rs}(s)}{Z_{Tc,22}}. \tag{40}$$

Based on (30)–(33), (35), and (39)–(40), $Z_{{\rm PSF},fb}$ can be expressed as follows:

$$Z_{{\rm PSF},fb}(s) = \frac{V_{Tc}(s)}{I_T(s)} = Z_{Tc,22} + \frac{R_s\left(m_5 - m_4\left(Z_{Tc,12} + Z_{Tc,21}\right) + Z_{Tc,21} Z_{\rm PA,21} Z_{\rm FBA,21}\right)}{m_5 + R_s\left(m_4 - Z_{\rm PA,21} Z_{\rm FBA,21}\right)} - \frac{m_4 Z_{Tc,12} Z_{Tc,21}}{m_5 + R_s\left(m_4 - Z_{\rm PA,21} Z_{\rm FBA,21}\right)}. \tag{41}$$

Fig. 16 shows the comparison of $Z_{\rm PSF}$ with the current regulation circuit and the one obtained in Section III-B. The current regulation circuit can greatly increase the output impedance, especially in the low-frequency range. The impedance varies between 90.15 and 70.13 dBΩ between 10 and 100 kHz. Apart from dealing with the nonideal characteristics of the SPD, as discussed in Section III-A, high input impedance can also avoid possible resonance between the high-order input filter and the grid impedance [6], [52].

Apart from this, it can also be observed that the PSF has high output impedance in the low-frequency range. For example, the output impedance of the PSF is 16.25 kΩ at 20 kHz, indicating that PSF is more suitable for applications with low switching frequency. If the impedance is realized with a single inductor, the required value will be 129.3 mH, which is physically large and thus limits the power density. Furthermore, the output impedance of the PSF is increased by 68.8 times (from 21.5 Ω to 1.479 kΩ) at 220 kHz, showing the importance of adding a fast current regulation circuit.

Fig. 17(a) shows the comparison of the measured peak DM noise level of the prototype without PSF and for prototype with the proposed current regulation circuit and PSF. Fig. 17(b) shows the measured noise for prototype with and without the current regulation circuit. Results confirm that the current regulation circuit could greatly enhance the filtering ability of PSF for handling DM noise. The noise level at switching frequency is reduced from 108.2 to 60.73 dB$\mu$V, that is, a reduction of 47.47 dB$\mu$V.

*3) Selection Guidelines for SPD and Op-Amp in PSF for EMI Filtering:* Based on the previous discussions, the selection guidelines for the SPD and the Op-amp driver are listed as follows:

1) The SPD has small internal gate resistance $R_{\rm int}$ for limiting minimum $i_{\rm gen}$ and exhibits high-frequency controllability when the fast current regulation circuit is applied.
2) The SPD has small parasitic capacitances $C_{gs}$, $C_{gd}$, and $C_{ds}$ to increase the impedance of high-frequency leakage paths and mitigate the driving requirement of the amplifier.

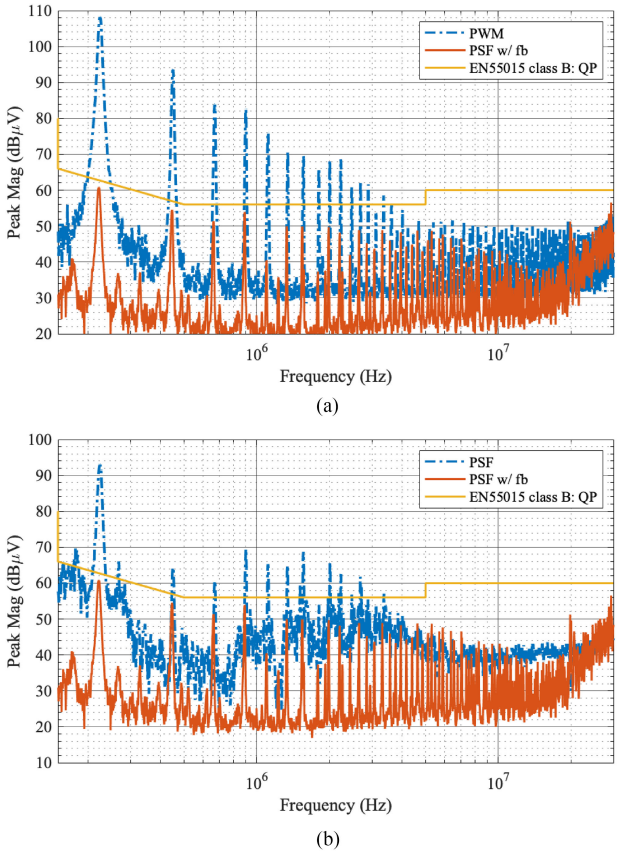


Fig. 17. Measured peak DM noise level of the prototype. (a) Prototype without PSF and with PSF and current regulation circuit. (b) Prototype with and without current regulation circuit.

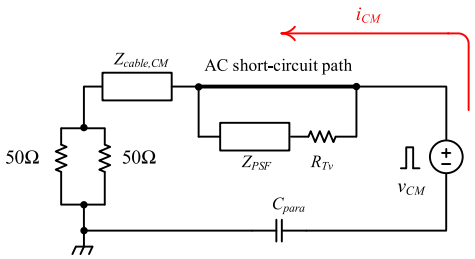


Fig. 18. Simplified CM noise current propagation path.

3) The SPD has small channel-length modulation index λ to reduce the leakage current.
4) The Op-amp should have small $Z_{o,cl}$ within the frequency of interest.

## V. CM Noise Characteristics

Fig. 18 shows the simplified CM noise current propagation model derived from Fig. 3(a). The voltage source, $v_{\rm CM}$, represents the pulsating voltage in the high voltage switching node. The impedance, $Z_{\rm cable,CM}$, is the CM impedance of the 1 m power cord. The CM current $i_{\rm CM}$ will flow through the LISN via a low impedance circuit path formed by the positive output of the diode bridge. Thus, applying PSF alone should not effective on filtering the CM noise.

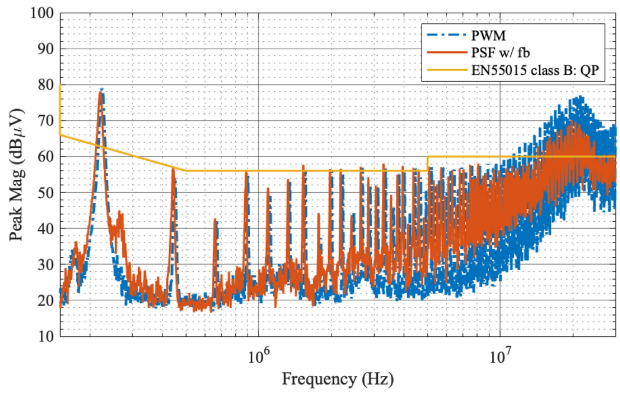


Fig. 19. Measured peak CM noise level of the prototype with and without the PSF.

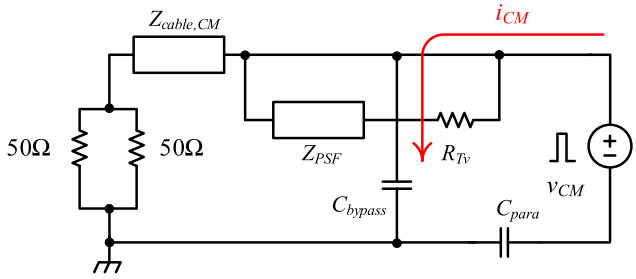


Fig. 20. CM noise current propagation path with CM current bypass capacitor.

Fig. 19 shows the measured peak CM noise level of the prototype with and without PSF. It shows that the PSF is not effective in reducing CM noise even if the fast current regulation circuit is applied to boost the value of $Z_{\rm PSF}$. The CM noise level at switching frequency is around 78 dBμV in both cases. The CM noise profile in both cases is similar and confirmed the prediction of the model in Fig. 18.

Since $Z_{\rm PSF}$ is high, the CM noise current through it is very small. As shown in Fig. 18, the CM noise is reduced by shunting the CM current on a low-impedance circuit path to the earth with a bypass capacitor $C_{\rm bypass}$. Fig. 20 illustrates the method. Fig. 1 shows the physical connection. Instead of using a bulky CM choke, a single bypass capacitor is used.

Fig. 21 shows the measured CM results of the prototype with and without PSF after adding 2.2 nF bypass capacitor in the mentioned circuit node. The CM noise level of the prototype at the switching frequency is reduced from 78.01 to 56.61 dBμV with the bypass capacitor. The bypass capacitor is effective in shunting the CM noise current at frequency below 10 MHz. Thus, the model shown in Fig. 20 is confirmed that PSF helps to block the CM noise current in one of the conduction paths. However, the CM noise between 10 and 30 MHz cannot be reduced. This issue will be discussed later.

## VI. Experimental Verifications of Prototype Under AC Operation

The EMI performance of the prototype under ac operation is measured. Fig. 22 shows the steady-state waveforms of $v_s$,

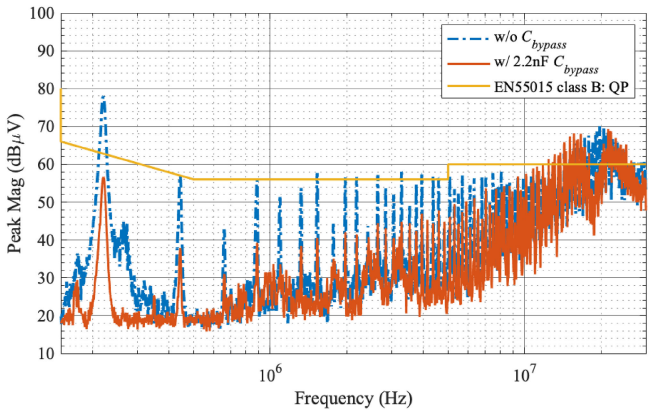


Fig. 21. Measured peak CM noise level of the prototype with CM current bypass capacitor.

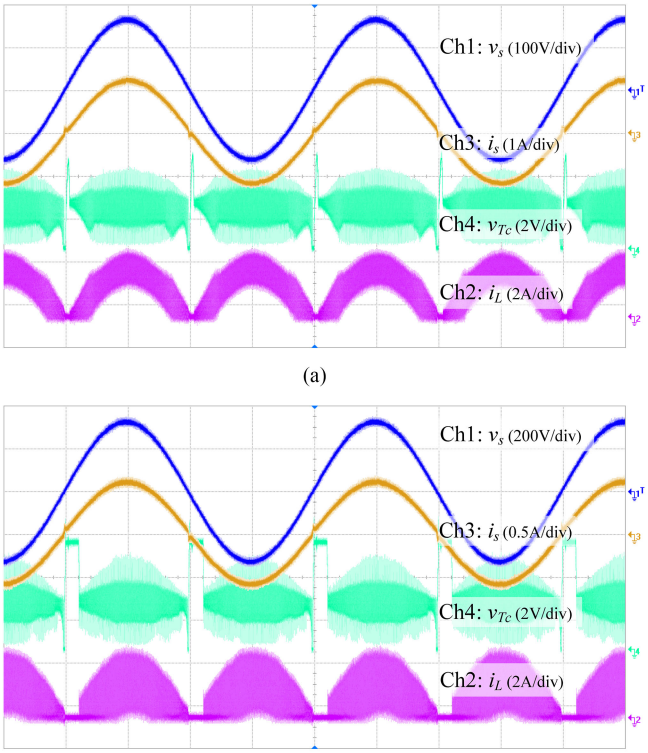


Fig. 22. Key voltage and current waveforms under low- and high-line conditions. (a) Low-line condition ($v_s = 115$ V). (b) High-line condition ($v_s = 230$ V).

$i_s$,$v_{Tc}$, and the inductor current $i_L$ under the low- and high-line conditions, respectively, and at the rated output power. The waveform of $i_s$ is near sinusoidal.

Fig. 23 shows the measured DM and CM EMI of the prototype with and without the current regulation circuit (both with PSF) under the low- and high-line conditions. The results reveal that the fast current regulator can effectively enhance the filtering performance of PSF on suppressing DM noises.

Fig. 24 shows the measured efficiency, power factor, and input current total harmonic distortion ($\text{THD}_i$) of the final prototype. The efficiency of the driver under rated load conditions

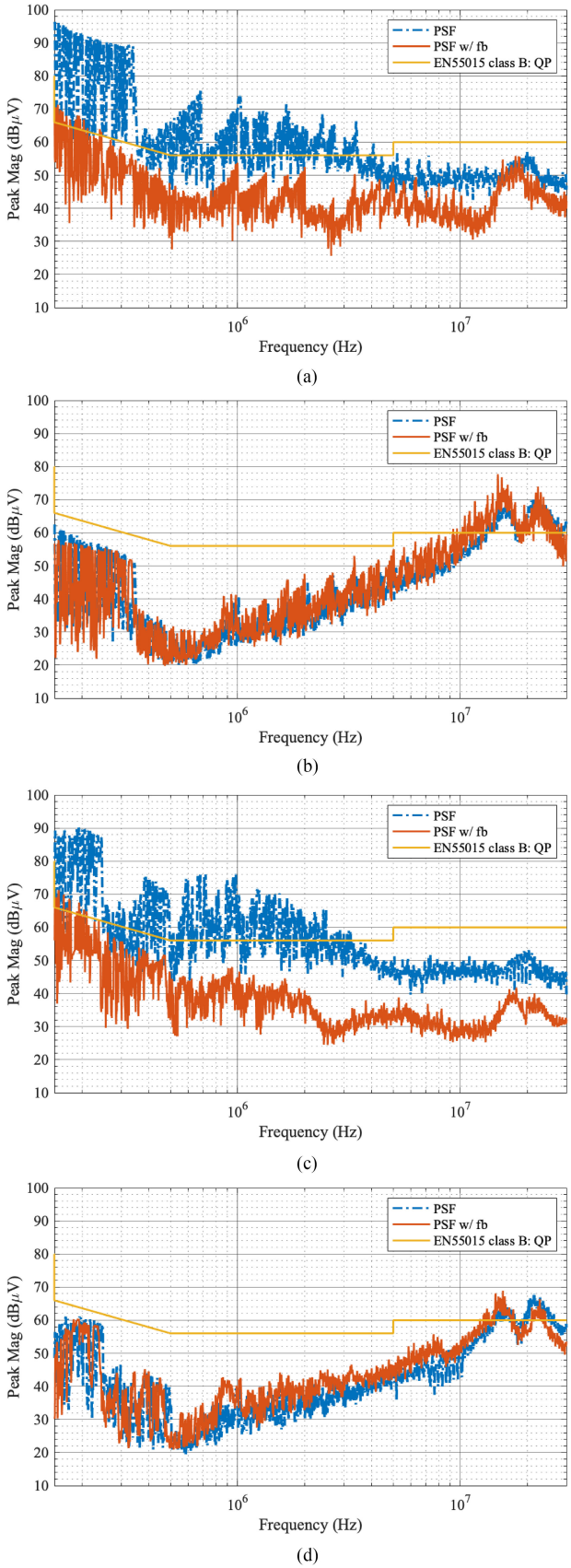


Fig. 23. Comparisons of the measured DM and CM noise of the prototype. (a) DM ($v_s = 115$ V). (b CM ($v_s = 115$ V). (c) DM ($v_s = 230$ V). (d) CM ($v_s = 230$ V).

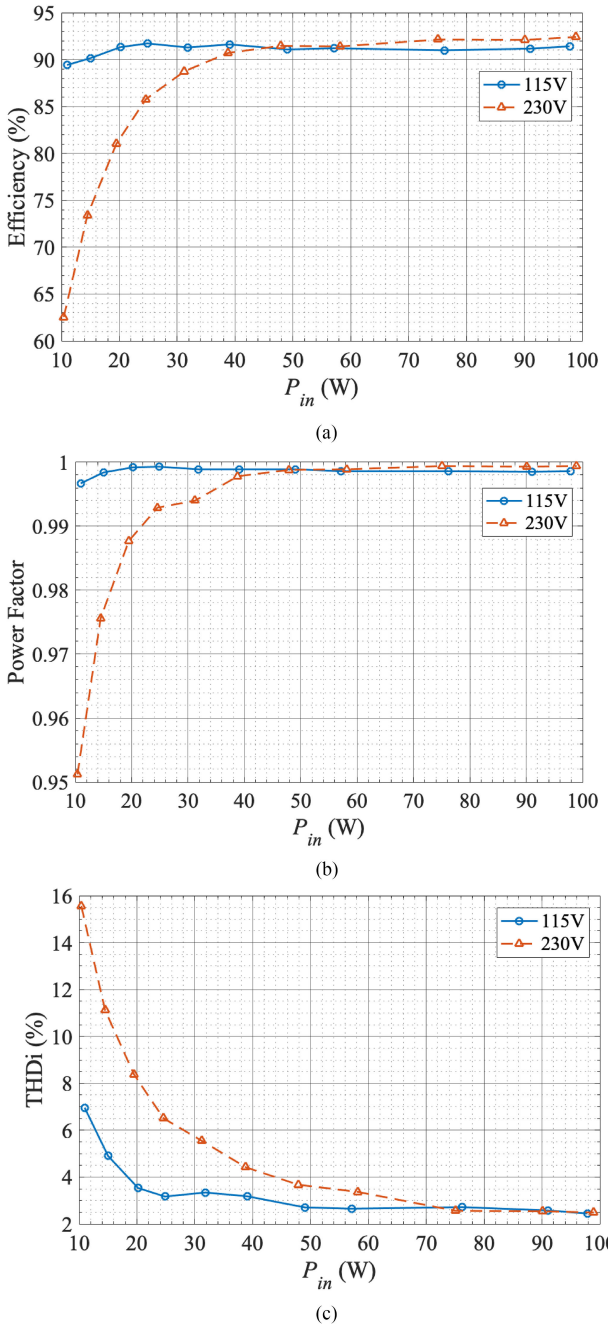


Fig. 24. Measurement results of the prototype under different loading conditions. (a) Efficiency. (b) Power factor. (c) THDi.

are 91.41% and 92.41%, respectively, under low- and high-line conditions. The power factor is higher than 0.95 over the operating range. Furthermore, the THDi curve in Fig. 24(c) reveals that the prototype with PSF can achieve very low THDi over a wide operating range. The THDi is increased, at the light load condition, because the zero-crossing distortion introduced by the diode-bridge circuit and the leakage current introduced by $C_s$ start to dominant the results.

Fig. 25(a) and (b) show the comparison of the measured power factor and THDi between the PSF prototype and the state-of-the-art commercial LED drivers, respectively [31], [53], [54].

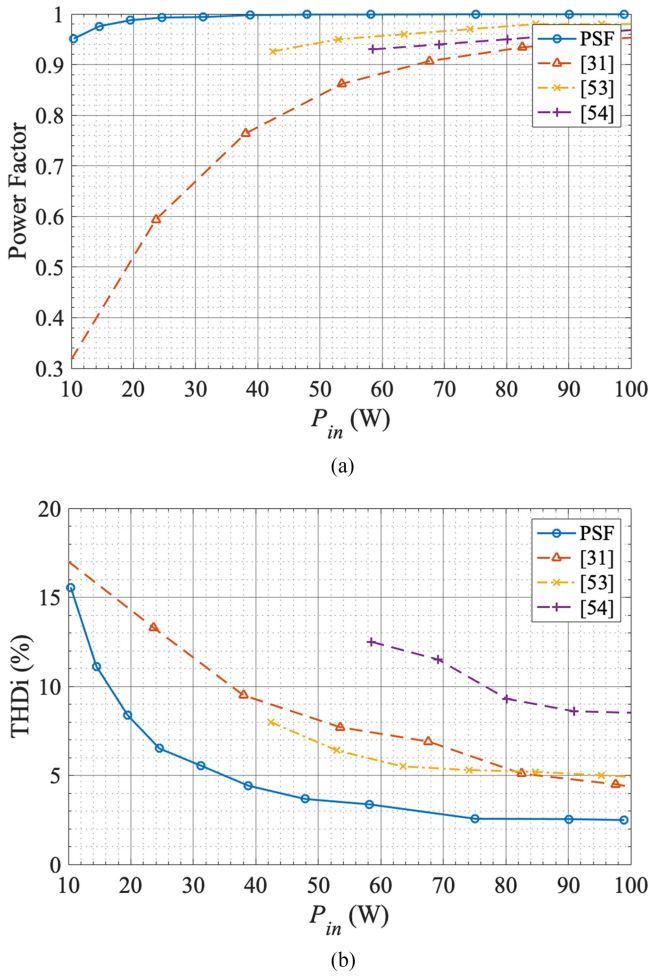


Fig. 25. Comparison of PF and THDi with commercial state-of-the-art LED drivers under high-line condition. (a) Power factor. (b) THDi.

The results show that the proposed PSF solution achieves better performance in both power factor and THDi compared with other LED drivers with active PFC technology.

## VII. Discussion and Further Development

The CM results in Fig. 23 shows a noise peak in the frequency range from 10 to 30 MHz. It is due to the cable impedance of the power cord [55]. Fig. 26 shows the measured CM impedance of the cable with the load open-circuited, which is similar to the current situation. The CM impedance of the cable is less than 10 Ω at the resonant frequency. Thus, the use of low impedance current shunting element (i.e., the bypass capacitor) is not effective at this frequency range. An alternative is to use a small earth choke or high-frequency CM choke of less than 100 $\mu$H to damp the noise.

The study in the previous sections is based on discrete implementation which limits the size reduction and filtering performance of the proposed PSF. Fig. 27 shows an integrated circuit prototype which has the feedback controller, modulator, main switch gate driver, cascode MOSFET driver, and high-speed SPD

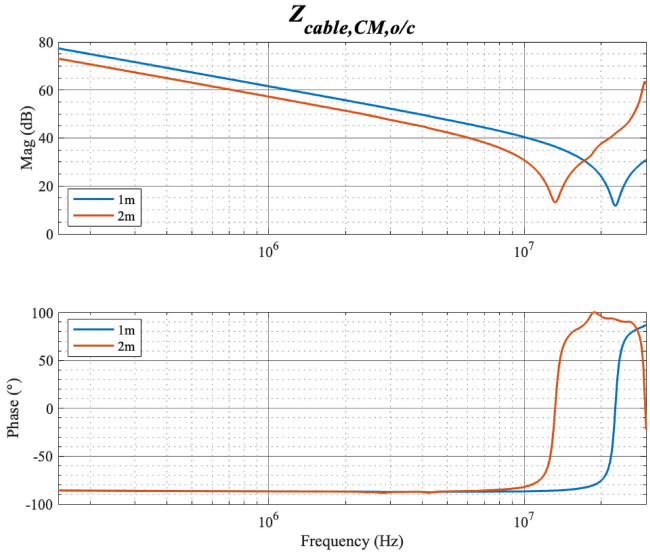


Fig. 26. Measured CM impedance of the power cord.

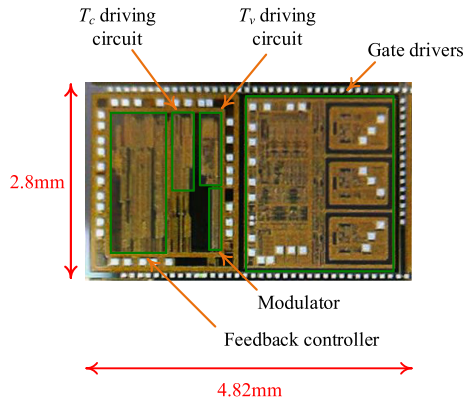


Fig. 27. Monolithic integration of the controller for PSF.

driver integrated (see Figs. 1 and 9). Significant circuit size reduction is achieved if all discrete components are implemented with a single monolithic integrated circuit. Further research is dedicated to investigating the overall volume reduction with the monolithic integration.

## VIII. Conclusion

This paper has presented the technique to model the EMI characteristics of switching converters with the power semiconductor filter. Detailed *Z*-parameter models for the SPD and driving circuit have been formulated. A fast current regulation circuit, which is used to compensate the non-ideal characteristics of the series pass device for profiling the waveform of the input current of the converter, has been proposed. A comprehensive experimental assessment on the EMI performance of a 100 W, 90-264 V buck–boost converter prototype has been conducted to investigate the effectiveness of the fast current regulation circuit and the use of CM current bypass capacitor. The experimental results are in close agreement with the theoretical predictions.

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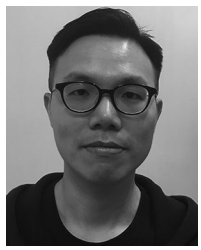

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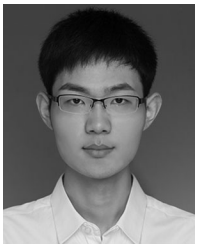

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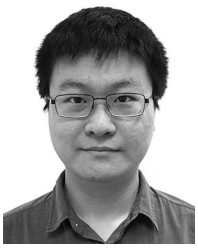

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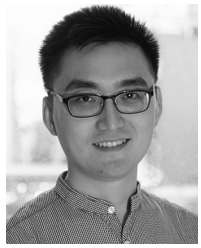

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