Letters

Measurement of Large-Signal C_{OSS} and C_{OSS} Losses of Transistors Based on Nonlinear Resonance

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***Abstract*—In this letter, we present a new measurement technique to evaluate the large-signal output capacitance (C_{OSS}) of transistors as well as the C_{OSS} energy dissipation (E_{DISS}), based on the nonlinear resonance between a known inductor and the output capacitance of the device under test. The method is simple and robust, and only requires a single voltage measurement to extract the large-signal C_{OSS} both in charging and discharging transients. By changing the circuit parameters, it is possible to tune the resonance frequency (even above 40 MHz) and the voltage swing (even above 1 kV) with dv/dt exceeding 100 V/ns, even though the method relies only on a low-voltage dc source, without the need for high-voltage RF amplifiers. The single-pulse operation of the method enables measuring C_{OSS} and E_{DISS} at very high frequency and dv/dt values without any thermal runaway. Using the proposed method, we extracted large-signal C_{OSS} and E_{DISS} of power transistors based on different semiconductor technologies. The obtained results were verified by Sawyer–Tower method and data reported in the literature. In particular, dv/dt-independent C_{OSS} losses were measured in cascode GaN transistors. The precise characterization of large-signal C_{OSS} of transistors presented in this letter is essential for the design of power converters, especially those operating at high switching frequencies.**

***Index Terms*—C_{OSS} losses, energy dissipation (E_{DISS}), GaN, HEMT, hysteresis, large-signal, nonlinear resonance, output capacitance, Sawyer–Tower, Si, SiC, superjunction.**

I. Introduction

LARGE-SIGNAL analysis of the output capacitance (C_{OSS}) of transistors has great importance in the design of power converters, as the small-signal C_{OSS} values are not always valid in the switching transients, especially when hysteresis exists [1]–[4]. The C_{OSS} hysteresis can lead to a considerable power loss, which is not recoverable with soft switching topologies [5]–[8]. The significant energy dissipation (E_{DISS}) observed in the charging and discharging process of the output capacitance of some Si superjunction (SJ) MOSFETs initiated studies on their large-signal C_{OSS} [8], [9]. The lower-than-expected efficiency in soft-switched GaN-based power converters, again highlights the need for precise measurements of C_{OSS} losses [1], [2].

Sawyer–Tower (ST) is a typical electrical measurement method used to evaluate large-signal output capacitance of transistors and diodes [10], [11]. In this method, the gate and source of the transistor are shorted to turn OFF the device, and a high-amplitude sinusoidal waveform is applied to the series connection of the device under test (DUT) and a reference linear capacitor (C_{REF}). The stored charge in the C_{OSS} of the transistor is assumed to be equal to the charge stored in the reference capacitor. This assumption is valid when the leakage current in DUT is much smaller than the displacement current, otherwise it may lead to the observation of spurious hysteresis [12]. The choice of C_{REF} is crucial in the ST method, since it depends on the range of interest for C_{OSS}, which however has a significant nonlinearity leading to a variation by a few orders of magnitude when changing drain-to-source bias. As a result, a fixed value of C_{REF} is not always suitable to capture such large nonlinearity. Another major limitation of the ST method is that the measurements are performed in steady-state regime. In case of devices with C_{OSS} hysteresis, the junction can significantly heat up due to hysteresis losses, which could potentially affect the measurement accuracy. For instance, the leakage current is much larger at higher temperatures, and can become comparable to the displacement currents in C_{OSS} and C_{REF}, resulting in an incorrect C_{OSS} measurement [12]. Another restriction caused by any steady-state measurement is the limitation of voltage swing/frequency applied to the DUT before thermal runaway [1]. In addition, the need for high-amplitude sinusoidal voltage source in the ST method constrains the maximum voltage and frequency that can be applied to characterize large-signal C_{OSS}, and the typical values of dv/dt in switching transients, especially for GaN transistors, can only be achieved at very high frequencies, in the range of tens of megahertz [2].

In this letter, we present a simple and robust measurement method to capture large-signal C_{OSS} as well as C_{OSS} energy dissipation during a single charging/discharging process (E_{DISS}) during a single charging/discharging process. The method works

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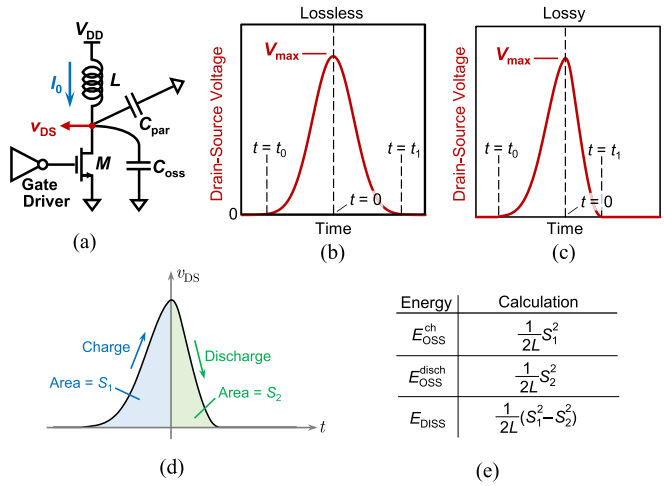

Fig. 1. Proposed method for large-signal $C_{\rm OSS}$ and $E_{\rm DISS}$ measurement. (a) Circuit and samples of $v_{\rm DS}$ voltage waveforms for devices with (b) lossless and (c) lossy $C_{\rm OSS}$ charging/discharging processes. (d) Areas below $v_{\rm DS}$ waveform for charging (S_1) and discharging (S_2) processes translate to (e) $C_{\rm OSS}$ charging/discharging energies as well as the dissipated energy $E_{\rm DISS}$.

based on the nonlinear resonance between a precalibrated inductor and the output capacitance of the DUT. By changing the circuit parameters, it is possible to tune the dv/dt (above 100 V/ns), frequency (above 40 MHz), and the voltage swing (above 1 kV), even though the method relies only on a low-voltage dc source, without the need for RF power amplifiers. In addition, large-signal $C_{\rm OSS}$ and $E_{\rm DISS}$ can be measured in steady-state regime as well as under a single pulse condition, which eliminates the effect of self-heating from the measurement, and does not thermally limit the maximum voltage swing, frequency, and dv/dt applied to the DUT.

II. Methodology

Fig. 1(a) illustrates the proposed circuit for large-signal $C_{\rm OSS}$ and $E_{\rm DISS}$ measurement. The transistor M is ON for $t < t_0$, charging the inductor L with the current I_0. By turning OFF the transistor at $t = t_0$, the inductor resonates with $C_{\rm OSS}$ and the parasitic capacitances $C_{\rm par}$. This results in the generation of a pulse with an amplitude $V_{\rm max}$ at the output node. By measuring the drain–source voltage waveform ($v_{\rm DS}$), and knowing the values of L and $C_{\rm par}$, one can simply extract large-signal $C_{\rm OSS}$ as well as $E_{\rm DISS}$. The circuit has a high step-up, which enables to probe $C_{\rm OSS}$ and $E_{\rm DISS}$ at very large voltages [13]. It is important to note that the resonant nature of the circuit guarantees a soft switching at $t = t_0$ with negligible losses. The losses related to the internal gate resistance of transistor and the sink resistance of the gate driver are also negligible. The governing equation of the circuit shown in Fig. 1(a) is

$$LC(v_{\rm DS})\frac{dv_{\rm DS}}{dt} = LI_0 - \int_{t_0}^{t} v_{\rm DS}(t)\,dt \tag{1}$$

where $C = C_{\rm OSS} + C_{\rm par}$ is the total nonlinear voltage-dependent capacitance at the output node. When $v_{\rm DS}$ peaks at $t = 0$, the inductor has zero current, so the inductor flux ($\varphi = LI_0$) can be calculated by integration of its voltage. Since $v_{DD} \ll v_{\rm DS}$

$$LI_0 = \int_{t_0}^{0} v_{\rm DS}(t)\,dt. \tag{2}$$

Replacing (2) in (1) yields

$$C(v_{\rm DS}) = \frac{\int_{t_0}^{0} v_{\rm DS}(t)dt - \int_{t_0}^{t} v_{\rm DS}(t)\,dt}{L\frac{dv_{\rm DS}}{dt}}. \tag{3}$$

Equation (3) presents the expression of the capacitance C exclusively as a function of $v_{\rm DS}$. The inductance value of L in the denominator of (3) should be properly measured to accurately extract the large-signal $C_{\rm OSS}$. It should be noted that $v_{\rm DS}$ starts from 0 at $t = t_0$, increases to the maximum value of $V_{\rm max}$ at $t = 0$, and then again, decreases to 0. This results in a double-sweep large-signal measurement of output capacitance for each pulse. In the case of devices without $C_{\rm OSS}$ losses, the measured $v_{\rm DS}$ has a symmetric waveform [see Fig. 1(b)], while devices with $C_{\rm OSS}$ losses present a nonsymmetric waveform [see Fig. 1(c)].

Equation (3) can be used to calculate the energy transferred to (or recovered from) $C_{\rm OSS}$ during a time interval T

$$E_T = \int_T v_{\rm DS}C(v_{\rm DS})\,dv_{\rm DS}. \tag{4}$$

After replacing (3) in (4), the $C_{\rm OSS}$ charging ($T = [t_0, 0]$) and discharging ($T = [0, t_1]$) energies can be extracted as

$$E_{\rm OSS}^{\rm ch} = \frac{1}{2L}\left(\int_{t_0}^{0} v_{\rm DS}(t)\,dt\right)^2 \tag{5}$$

and

$$E_{\rm OSS}^{\rm disch} = \frac{1}{2L}\left(\int_{0}^{t_1} v_{\rm DS}(t)\,dt\right)^2 \tag{6}$$

respectively. The difference between (5) and (6) gives the energy dissipated in $C_{\rm OSS}$

$$E_{\rm DISS} = \frac{1}{2L}\left(\left(\int_{t_0}^{0} v_{\rm DS}(t)dt\right)^2 - \left(\int_{0}^{t_1} v_{\rm DS}(t)dt\right)^2\right). \tag{7}$$

Fig. 1(d) and (e) depict the correspondence of the $C_{\rm OSS}$ charging/discharging/dissipated energies to the areas below the $v_{\rm DS}$ curve. This makes the method numerically convenient since it just relies on the integration of a single voltage waveform, which can be accurately measured even at ultra-fast charging/discharging cycles, even below 10 ns. It should be noted that the use of a high-Q inductor L leads to negligible deformation of $v_{\rm DS}$ waveform, even below the measurement accuracy of typical oscilloscopes.

III. Experiments

We demonstrate the applicability of the proposed method for large-signal $C_{\rm OSS}$ measurement as well as to extract $E_{\rm DISS}$ for different transistors (listed on Table I). Fig. 2(a) shows the experimental set-up with different test boards compatible with different transistor packages. The captured $v_{\rm DS}$ and $v_{\rm GS}$

TABLE I
SPECIFICATIONS OF THE EVALUATED TRANSISTORS

No.	Technology	Voltage/Current Ratings		Reported E_{OSS} at 400 V (μJ)
		Voltage (V)	Current (A)	
M1	SiC	650	93	22.0
M2	Si SJ	650	60	17.5
M3	SiC	900	36	8.5
M4	GaN*	650	65	15.5
M5	GaN*	650	65	7.0
M6	GaN*	600	30	3.0

* GaN transistor M4 is cascode, while transistors M5 and M6 are enhancement-mode.

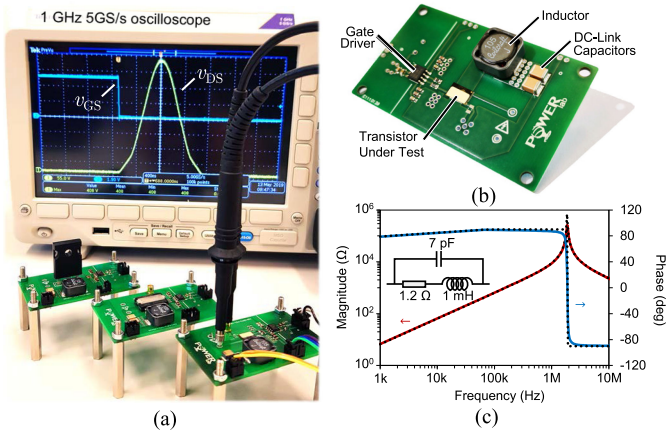

Fig. 2. Photographs of (a) experimental set-up and (b) test board. (c) Measured (solid lines) and modeled (dotted lines) impedance of a 1-mH inductor. The inset shows the equivalent circuit model of the inductor.

waveforms verify the soft switching in the circuit since the transistor turns OFF ($v_{GS} = 0$) before building-up the v_{DS} voltage. A test board with 1-mH inductor is shown in Fig. 2(b). The impedance of the employed inductor was measured using a Keysight E4990A impedance analyzer, as shown in Fig. 2(c). Based on this measurement, we extracted and de-embedded the parasitic capacitance of the inductor [inset of Fig. 2(c)]. The results for M1 (SiC) and M2 (Si SJ) using 1-mH inductor, shown in Fig. 3(a) and (c), respectively, illustrate the shape of the v_{DS} pulse for these two transistors, which translates into large-signal C_{OSS} [shown in Fig. 3(b) and (d), respectively]. The obtained large-signal C_{OSS} were verified with ST method performed at 300 kHz [dashed lines in Fig. 3(b) and (d)]. It should be noted that although the measurements were done at $V_{max} = 100$ V, the supply voltage v_{DD} was very small, e.g., $v_{DD} = 100$ mV in Fig. 3(a).

The large values of inductor L result in relatively small resonance frequencies, e.g., 300 kHz for M1 (SiC) in Fig. 3(a), however, much higher frequencies and dv/dt values can be obtained with smaller inductors [see Fig. 4(a)]. Fig. 4(b) shows measurement results for M2 (Si SJ) with a 500-nH air-core inductor. By changing the small voltage v_{DD}, the peak voltage V_{max} was tuned at 250, 450, and 650 V. Fig. 4(c) shows the extracted large-signal C_{OSS}, presenting considerable hysteresis loops. The reported small-signal C_{OSS} from the device datasheet

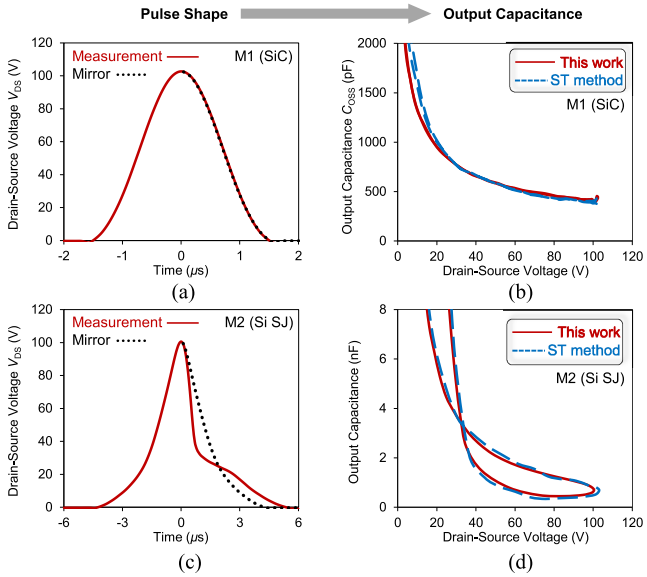

Fig. 3. (a) Measured v_{DS} (solid line) and mirrored waveform (dotted line) for M1. (b) Extracted C_{OSS} for M1 using the proposed method (solid line) and by ST method (dashed line). (c) Measured v_{DS} (solid line) and mirrored waveform (dotted line) for M2 shows a nonsymmetrical charging/discharging process. (d) Extracted C_{OSS} for M2 using the proposed method (solid line) and by ST method (dashed line).

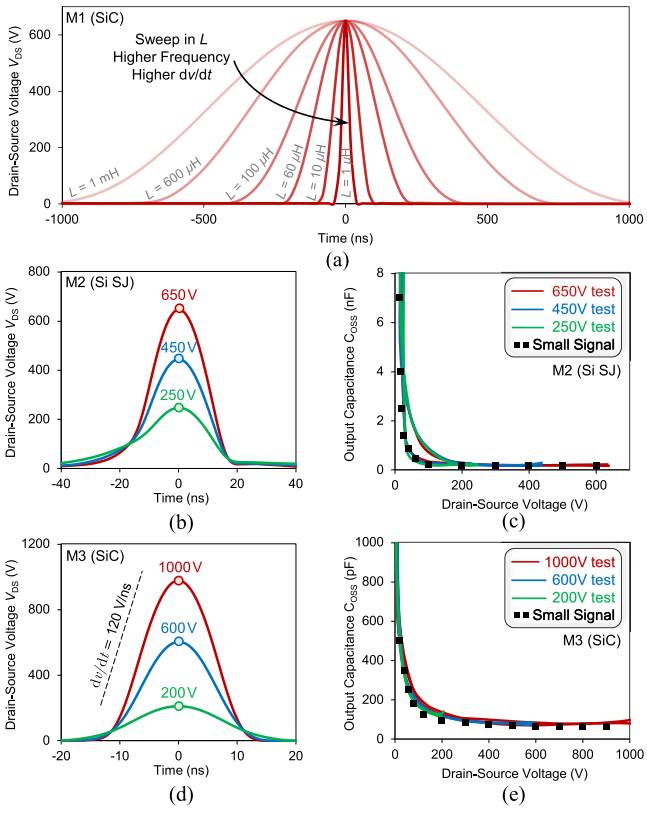

Fig. 4. (a) Measured v_{DS} for M1 (SiC) using different values of L showing the possibility of capturing large-signal C_{OSS} and E_{DISS} at very frequencies. (b) Measured v_{DS} for M2 (Si SJ) at $V_{max} = 250$, 450, and 650 V, and (c) the corresponding large-signal C_{OSS}. (d) Measured v_{DS} for M3 (SiC) at $V_{max} = 200$, 600, and 1000 V, and (e) the corresponding large-signal C_{OSS}. Discrete points show small signal C_{OSS} reported in datasheets.

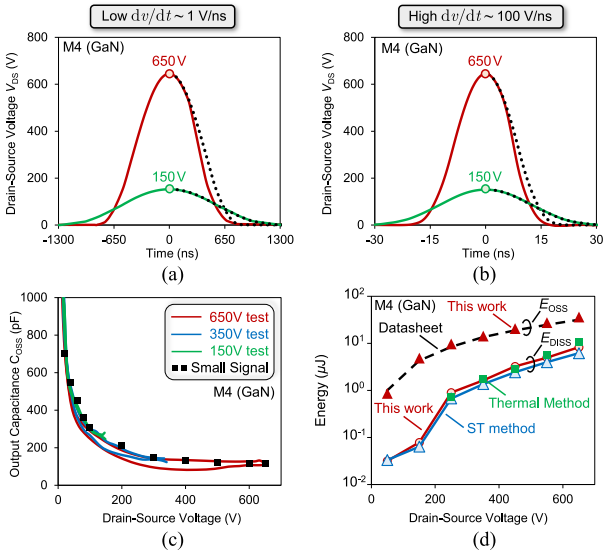

Fig. 5. Capturing large-signal C_{OSS} and E_{DISS} at low and high dv/dt values for M4 (cascode GaN). (a) Low and (b) high dv/dt measurements with $L =$ 1 mH and $L = 500$ nH inductors, respectively. The mirrors (dotted lines) show symmetry at low voltage tests (150 V) and nonsymmetry at high voltage tests (650 V). Large signal C_{OSS} and E_{DISS} are not functions of dv/dt in this cascode GaN transistor. (c) Extracted large signal C_{OSS} for $V_{max} = 150$, 350, and 650 V. (d) Extracted losses from the proposed technique, validated with ST and thermal method.

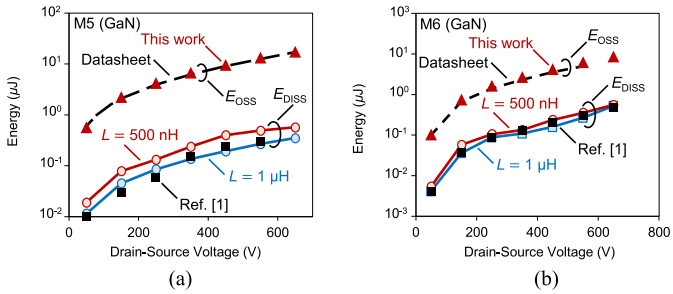

Fig. 6. Extracting E_{OSS} and C_{OSS} losses for enhancement-mode GaN transistors (a) M5 and (b) M6, for $L = 500$ nH and $L = 1$ μH. The extracted E_{OSS} values (Δ) (equal for both cases $L = 500$ nH and 1 μH) are in agreement with reported data in datasheets (dashed lines) and the obtained E_{DISS} for $L = 1$ μH ($f \sim 10$ MHz) shows a good agreement with reported data in [1] ($\square$).

[discrete points in Fig. 4(c)] closely match the extracted large-signal C_{OSS} in the discharge cycle.

The method is capable of being performed at high voltage levels. Fig. 4(d) shows the measured v_{DS} waveforms with $L = 500$ nH at three different voltages 200, 600, and 1000 V, and the corresponding large-signal capacitances are shown in Fig. 4(e). For the 1000 V measurement, a resonance frequency of 40 MHz and dv/dt of 120 V/ns show the potential of the method in operating at very high frequencies and amplitudes, at the same time, without the risk of thermal runaway. To put these numbers in perspective, with the same measurement specifications for a device with an output capacitance of ~100 pF, the amplifier in the ST method would require to provide ~3 kVA of reactive power at 40 MHz.

The use of GaN-on-Si HEMTs in high-frequency converters is rapidly growing, due to their outstanding features such as low R_{ON} and small gate charge. Unexpected losses in soft-switched GaN-based power converters initiated studies on C_{OSS} losses in these devices [1], [2]. Fig. 5(a) and (b) show the measured voltage waveforms over a cascode GaN transistor (M4), at low and high dv/dt values, respectively. At 150-V tests, the generated v_{DS} waveforms are almost symmetrical for both low and high dv/dt tests. At a higher voltage $V_{max} = 650$ V, however, there is a significant asymmetry in both waveforms. Fig. 5(c) presents the extracted large-signal C_{OSS} for $V_{max} = 150$, 350, and 650 V, showing that the hysteresis loop becomes drastically larger at higher voltages. This indicates a fundamentally different loss mechanism than that in enhancement-mode GaN devices, since the device becomes significantly lossy at high voltages. The extracted E_{OSS} and C_{OSS} losses at different voltage levels are shown in Fig. 5(d). The significant increase in C_{OSS} losses appearing for $v_{DS} > 250$ V, is in agreement with the previously measured C_{OSS} losses for cascode GaN devices [1]. The extracted E_{DISS} based on the proposed method, were verified with thermal method and ST measurements performed at a wide range of different frequencies from 10 to 300 kHz. The agreement between E_{OSS} reported in datasheet [dashed line in Fig. 5(d)] and the extracted E_{OSS} from (5) [Δ in Fig. 5(d)] is another indication of the accuracy of the proposed method. At the highest test voltage of 650 V, 26% of E_{OSS} is dissipated during charging and discharging processes. Although dv/dt-dependent losses have been observed in some of the advanced GaN HEMTs [1], [2], as it can be seen in Fig. 5(a) and (b), the proposed method did not show any significant difference for GaN device M4, which opens opportunities for further investigation of these effects on different devices.

Fig. 6(a) and (b) show E_{OSS} and single-cycle charging/discharging losses of enhancement-mode GaN transistors M5 and M6, respectively. The extracted E_{OSS} (Δ) for both devices matches well with data reported in their datasheets (dashed lines). For E_{DISS}, larger losses were extracted for smaller inductor $L = 500$ nH, corresponding to higher dv/dt. The obtained losses for M5 and M6 are considerably lower than losses detected for M4, e.g., 3.5% of nominal E_{OSS} at 650 V for M5. The obtained results for $L = 1$ μH (leading to a resonance frequency of ~10 MHz) are in agreement with previously reported C_{OSS} losses for M5 and M6 at the same frequency [1].

IV. Conclusion

In this letter, we demonstrated a new measurement technique to evaluate the large-signal C_{OSS} and C_{OSS} losses of transistors. The method has several advantages, which are as follows:

1) Using a low-voltage dc source, high voltage swings (>1000 V), high frequencies (> 40 MHz), and high values of dv/dt (> 120 V/ns) can be obtained.
2) The method can be performed in single-pulse mode, which eliminates thermal issues like thermal runaway or increasing leakage at high temperatures, even at very high voltage swings and high values of dv/dt.

3) Unlike ST, where the circuit is not representative of the operating conditions of a device in a switching circuit [2], the nature of the proposed circuit has similarities to the concept of resonant converters.
4) The simplicity of the circuit, relying on just two main elements (inductor and DUT), minimizes the parasitic effects in waveforms. For instance, any kind of voltage ringing over DUT in more complicated circuits leads to partial C_{OSS} charging/discharging that causes additional losses. These ringings are more dominant in high dv/dt values and can potentially affect the accuracy of measurement. For the proposed method, however, there is always one smooth charging and discharging curve, without any ringing.

Evaluation of a cascode GaN transistor with the proposed method, showed dv/dt-independent C_{OSS} loss that was drastically increased after 250 V, reaching 26% of E_{OSS} at the maximum rating voltage of 650 V (M4). Considerably smaller C_{OSS} losses were measured for two enhancement-mode GaN transistors (M5 and M6). The simplicity and consistency of the proposed method enables the study of large-signal C_{OSS} and C_{OSS} losses of transistors, which can significantly influence the performance of power converters, especially those operating at high switching frequencies.

REFERENCES

[1] G. Zulauf, S. Park, W. Liang, K. Surakitbovorn, and J. Rivas-Davila, "C_{OSS} losses in 600 V GaN power semiconductors in soft-switched, high- and very-high-frequency power converters," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10748–10763, Dec. 2018.

[2] M. Guacci *et al.*, "On the origin of the C_{OSS}-losses in softswitching GaN-on-Si power HEMTs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 679–694, Jun. 2019.

[3] J. Roig and F. Bauwens, "Origin of anomalous C_{OSS} hysteresis in resonant converters with superjunction FETs," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 3092–3094, Sep. 2015.

[4] G. D. Zulauf, J. Roig-Guitart, J. D. Plummer, and J. M. Rivas-Davila, "C_{OSS} measurements for superjunction MOSFETs: Limitations and opportunities," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 578–584, Jan. 2019.

[5] G. Zulauf, Z. Tong, J. D. Plummer, and J. M. Rivas-Davila, "Active power device selection in high- and very-high-frequency power converters," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6818–6833, Jul. 2019.

[6] D. Rothmund, D. Bortis, and J. W. Kolar, "Accurate transient calorimetric measurement of soft-switching losses of 10 kV SiC MOSFETs and diodes," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5240–5250, Jun. 2018.

[7] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016.

[8] J. Fedison and M. Harrison, "C_{OSS} hysteresis in advanced superjunction MOSFETs," in *Proc. Appl. Power Electron. Conf. Expo.*, 2016, pp. 247–252.

[9] J. Fedison, M. Fornage, M. Harrison, and D. Zimmanck, "C_{OSS} related energy loss in power MOSFETs used in zero-voltage-switched applications," in *Proc. 29th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 150–156.

[10] Z. Tong, G. Zulauf, J. Xu, J. D. Plummer, and J. Rivas-Davila, "Output capacitance loss characterization of silicon carbide Schottky diodes," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 856–878, Jun. 2019.

[11] S. Ben-Yaakov, "Some observations on loss and hysteresis of ferroelectric based ceramic capacitors," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9127–9129, Nov. 2018.

[12] J. F. Scott, "Ferroelectrics go bananas," *J. Phys. Condens. Matter*, vol. 20, no. 2, Dec. 2007, Art. no. 021001.

[13] M. S. Nikoo, A. Jafari, and E. Matioli, "GaN transistors for miniaturized pulsed-power sources," *IEEE Trans. Plasma Sci.*, vol. 47, no. 7, pp. 3241–3245, Jul. 2019.