High Off-State Impedance Gate Driver of SiC MOSFETs for Crosstalk Voltage Elimination Considering Common-Source Inductance

Chengmin Li, *Student Member, IEEE*, Zhebie Lu, *Student Member, IEEE*, Ying Chen, Chushan Li, *Member, IEEE*, Haoze Luo, *Member, IEEE*, Wuhua Li, *Member, IEEE*, and Xiangning He, *Fellow, IEEE*

***Abstract*—The crosstalk voltage on the gate-source terminal of SiC power MOSFETs in a phase-leg circuit is composed of the gate–drain capacitor introduced voltage and the common-source inductor introduced voltage. The mathematical model of the crosstalk voltage indicates that to suppress two types of crosstalk voltage, there exists a contradictory requirement on the OFF-state gate loop impedance. This challenge reduces the effectiveness of conventional crosstalk elimination methods. As an improvement, a crosstalk voltage suppression circuit that synchronously eliminates the crosstalk voltage of gate–drain capacitance and the common-source inductance is proposed. In this article, instead of creating low-impedance gate loop in the OFF-state, a high-impedance gate loop is formatted to eliminate the voltage drop on the common-source inductance. Meanwhile, the potential false turn-ON or the negative voltage spikes caused by gate–drain capacitance is eliminated by the precharge voltage in the gate-source capacitor. The required prestored charge is analyzed considering the nonlinear behavior of the junction capacitance of the SiC MOSFETs. The proposed gate driver is experimentally verified in different switching conditions.**

***Index Terms*—Active miller clamping circuit, crosstalk voltage, gate drive of SiC devices, SiC power MOSFETs.**

I. Introduction

SiC power MOSFETs demonstrate outstanding performances in high-speed switching and enable more efficient power conversion systems. However, only improvements of the device are not enough. Some package and design constraints such as the negative influence of the parasitic parameters are being more and more significant in the high-speed switching operation [1], [2]. Among them, the crosstalk phenomenon in a phase-leg circuit, which means the interfere voltage introduced to the gate electrode in the OFF-state during the fast switching transition of another device, is one of the most concerned challenges for MOS-gated devices [3], [4].

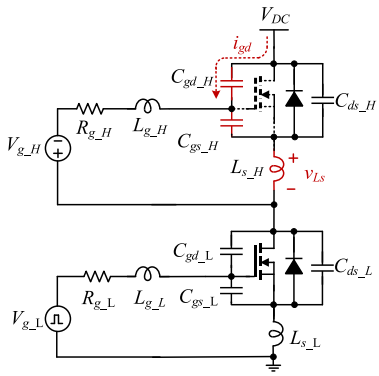


Fig. 1. Crosstalk phenomenon in power MOSFET.

Fig. 1 demonstrates the crosstalk phenomenon in a phase-leg configuration. R_g and L_g refer to the total equivalent gate loop resistance and inductance, respectively. L_s is the common-source inductance. C_{gd}, C_{gs}, and C_{ds} are gate–drain capacitor, gate-source capacitor, and drain-source capacitor, respectively. With respect to the upper device in the phase-leg circuit, when the lower MOSFET is turned ON or turned OFF, a voltage step occurs at the gate–drain of the device and a current step flow through the common-source inductor L_{s_H}. It will introduce a displacement current through the gate–drain capacitor and an induced voltage on the common-source inductor. The positive spike voltage may cause a false turn-ON of the device, which increase the switching loss or even cause the shoot through of the dc link [5]. The negative spike voltage may be lower than the minimum allowable voltage of the gate-source and damage the gate electrode. For SiC devices, the crosstalk is more harmful due to the very fast switching speed capability, which is more than six times faster than the Si IGBT [6]. Moreover, the gap between the threshold voltage and the minimum allowable negative gate-source voltage of SiC MOSFETs is lower than Si devices [7]. Thus, to fully realize the fast switching speed of the SiC devices, the crosstalk voltage should be limited within the safe operation area.

Manuscript received March 26, 2019; revised June 8, 2019; accepted July 17, 2019. Date of publication July 30, 2019; date of current version December 13, 2019. This work was supported in part by the National Key Research and Development Program of China under Grant 2017YFE0112400, in part by the National Nature Science Foundations of China under Grants 51677166 and 51877192, and in part by Zhejiang Provincial Natural Science Foundation under Grant LR16E070001. Recommended for publication by Associate Editor J. Popovic-Gerber. *(Corresponding author: Wuhua Li.)*

C. Li, Z. Lu, Y. Chen, H. Luo, W. Li, and X. He are with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China (e-mail: lichengmin@zju.edu.cn; jebeloo@zju.edu.cn; chenyingqzh@163.com; luohaoze@163.com; woohualee@zju.edu.cn; hxn@zju.edu.cn).

C. Li is with the Zhejiang University–University of Illinois at Urbana-Champaign Institute, Zhejiang University, Hangzhou 310058, China (e-mail: chushan@intl.zju.edu.cn).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2019.2932263

Many methods have been reported to reduce the crosstalk voltage. Since the crosstalk voltage is caused by high-speed switching, reducing the switching speed is the straight forward way. Increasing the gate drive resistance and some active closed-loop *dv/dt* methods are effective [8]–[9], [10]. In some applications, an extra parallel capacitor is added to the gate-source to reduce the crosstalk voltage [11], [12]. But the switching speed is reduced and higher switching loss is introduced. Another method is adding a negative gate-source voltage to prevent false turn-ON of the device during switching transients of another device [13]. In [14] and [15], a simple level shifter is proposed to generate a negative voltage to the gate source. In [16], a gate driver with multilevel negative voltage is adopted to adapt to the polarity of the voltage spike induced. However, due to the high-speed switching and the lower tolerance of the negative gate-source voltage of the SiC MOSFETs, the required negative voltage may exceed the recommended negative voltage from the datasheet, bringing underlying reliability issues. What is more, the oscillations in the loop and the influence of the parasitic parameters make it difficult to design the value of the negative voltage [17].

As an improvement, a series of methods that create a low-impedance path of the displacement current produced by high *dv/dt* are proposed. As demonstrated in Fig. 1, the crosstalk voltage contains the voltage drop on the gate loop impedance induced by the gate–drain displacement current. In [18], Miller clamp circuit is proposed, which utilizes an auxiliary transistor to bypass the relatively large external gate resistor. Thus, the impedance of the gate loop is reduced. Many similar methods are proposed to provide a low-impedance path of the displacement current [19], [20].

However, there are several limitations in the aforementioned methods. First, the influence of the common-source inductance on the crosstalk voltage is neglected. It has been acknowledged that the common-source inductance has a significant influence on the switching transition of the device, whereas the influence on the crosstalk voltage has not been modeled explicitly [21]. Generally, the voltage drop on the common-source inductor is added to the gate-source loop, as well as the gate–drain displacement current. Reducing the gate loop impedance decreases the crosstalk voltage from the gate–drain displacement current. Meanwhile, the crosstalk voltage from the voltage drop on the common-source inductor is increased. The increased crosstalk voltage is contrary to the expectation that reducing the loop impedance helps reducing the crosstalk voltage. Second, due to the relatively large internal gate resistance, the effects of the low-impedance clamping methods are limited by the relatively large voltage drop on the internal resistance [13].

To give an accurate design guideline on crosstalk voltage suppression methods, an analytical model of the crosstalk voltage considering the Miller capacitor and the common-source inductor is given in this article. In the light of the analytical model, a high OFF-state impedance gate driver is proposed to eliminate the *dv/dt* and *di/dt* induced crosstalk voltage simultaneously. The operation principle and parameter design are discussed in detail. Based on the analysis, a parameter design guideline of the proposed scheme is given. Then the validation of the proposed method is verified by a series of experiments in the double pulse test under different operation conditions.

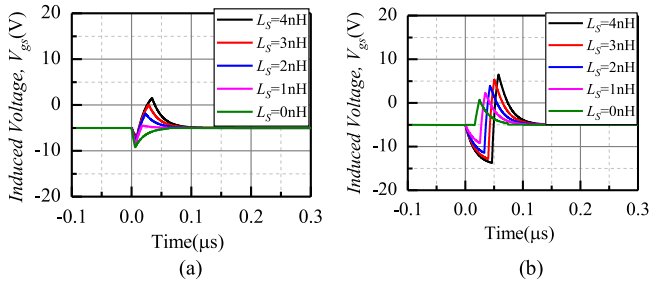


Fig. 2. Crosstalk voltage based on the proposed analytical model. (a) Crosstalk voltage when the lower device is turned OFF. (b) Crosstalk voltage when the lower device is turned ON.

The sections of this article are organized as follows. Section II gives an analytical model of the crosstalk voltage considering the common-source inductor. Section III proposes a gate driver circuit to suppress the crosstalk voltage from the common-source inductor and the gate–drain capacitor synchronously. Section IV gives the assessment of the OFF-state negative voltage design of the proposed gate driver. Section V validates the proposed gate drive in different switching conditions in experiments. Section VI concludes this article.

II. Influence of the Common-Source Inductor on Crosstalk Voltage

There exist a series of parasitic parameters in the SiC MOSFET inside the package. These coexisting nonidealities introduce crosstalk voltage to the gate loop and their influences should be comprehensively investigated. Both the voltage change rate and current change rate in the power loop generate crosstalk voltage and the value is deeply related to the switching behavior of the other device. In these parasitic parameters, the influence of the common-source inductor on the crosstalk voltage needs to be quantized.

Considering a phase-leg circuit where the high-side device is in the OFF-state and the low-side device is turned ON or turned OFF, as shown in Fig. 1, the crosstalk voltage of the upper device is controlled by the behavior of the switching device in the lower leg. An analytical model from [24] is leveraged here to describe the switching device. Further, an analytical model of the crosstalk voltage is proposed taking the nonlinear gate–drain capacitor, the common-source inductor and the reverse recovery of the body diode into account. Besides, the detailed deduction process is given in the appendix section. To simplify the analysis, the parasitic oscillations in the power loop are ignored.

Fig. 2 gives the calculation results of the crosstalk voltage during the turn-ON and turn-OFF process based on the proposed crosstalk voltage model. In the calculation, the gate resistance keeps the same and the common-source inductance is adjusted to explore the influence on crosstalk voltage. In the analytical model, the device parameters are extracted from the datasheet of CREE C2M0025120D or can be measured from the experiments. The values of the parameters are listed in Table I.

TABLE I
PARAMETERS IN CROSSTALK CALCULATION

Parameter	Symbol	Value
Load current	I_L	75 A
Bus voltage	V_{dc}	600 V
Gate driving voltage	V_{g_on}/V_{g_off}	+20 V/-5 V
Gate resistance	R_g	5 Ω
Common source inductance	L_s	4 nH
Gate source capacitance	C_{gs}	2.76 nF
Stored charge in C_{ds}	Q_{oss}	420 nC
Transfer curve fitting parameters	X, k_1, k_2, V_{th}	1.723, 4.02, 3.28 A, 4.02 V
Reverse recovery charge	Q_{rr}	406 nC
Carrier lifetime in the bodydiode	τ_C	36.3 ns
Drift region transit time of bodydiode	T_m	45.14 ns
Leakage inductance in power loop	L_d	20 nH

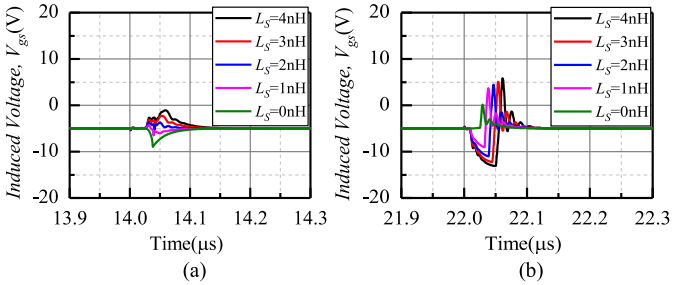


Fig. 3. Simulation results of induced crosstalk voltage. (a) Crosstalk voltage when the lower device is turned OFF. (b) Crosstalk voltage when the lower device is turned ON.

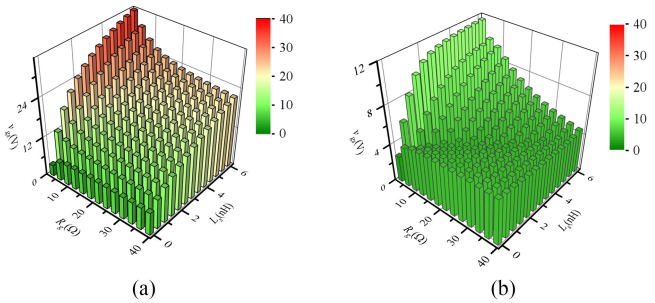


Fig. 4. Relationship between the crosstalk voltage, OFF-state impedance, and common-source inductor of the upper device. (a) Peak to peak crosstalk voltage at turn-ON. (b) Peak to peak crosstalk voltage at turn-OFF.

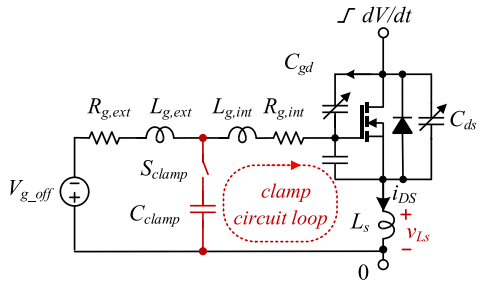


Fig. 5. Equivalent circuit of Miller clamping circuit.

Meanwhile, SPICE simulations are conducted with the numerical model from CREE, as demonstrated in Fig. 3. The calculated crosstalk voltage matches well with the simulation results in time and amplitude. The deviation is mainly from the parasitic oscillations in the power loop, which are simplified in the proposed analysis. Both analytical model and SPICE simulation indicate that at a given switching speed, when the common-source inductance increases, the crosstalk voltage increases.

Based on the proposed model, the parameter scan calculations are conducted to demonstrate the influence of the common-source inductor and the OFF-state external resistor. The switching speed of the lower device stays the same in the calculation. The result of the peak to peak crosstalk voltage in turn-ON/OFF process is given in Fig. 4. When there is no common-source inductance, the crosstalk voltage is merely from the gate–drain capacitor, thus, a smaller OFF-state gate resistor is preferred to reduce the crosstalk voltage. In this case, the widely adopted Miller clamping method, which reduces the resistance at the terminal of the devices, as pictured in Fig. 5, is effective to decrease the crosstalk voltage caused by gate–drain capacitance. However, if there is a common-source inductor, the crosstalk voltage increases dramatically when the OFF-state gate resistance decreases and threatens the reliable operation of the device. Considering the Miller clamping circuit with common-source inductance, the low-impedance clamp circuit is formed and the crosstalk voltage caused by common-source inductance is increased as a consequence. As a result, in high common-source inductance conditions, the Miller clamping circuit is not suitable.

Regarding the gate–drain capacitor introduced crosstalk voltage, the external gate loop impedance, and the gate-source capacitor are connected in parallel, a small OFF-state gate loop impedance is beneficial for reducing the voltage drop of the displacement current. For the common-source inductor introduced crosstalk voltage, the external gate loop impedance and the gate-source capacitor are connected in series; a higher external gate loop impedance is preferred to mitigate the voltage drop on gate-source capacitor. It is concluded that there exists a contradictory on the gate loop impedance for the two types of the crosstalk voltage. To fully utilize the fast switching capability of the SiC power MOSFETs, efforts should be paid to reduce the crosstalk voltage from the gate–drain capacitor and the common-source inductor at the same time.

III. PROPOSED CROSSTALK VOLTAGE SUPPRESSION CIRCUIT

In this section, a crosstalk voltage suppression circuit with multilevel gate voltage and shaped gate loop impedance is proposed to reduce the crosstalk voltage. The L_s and C_{gd} induced crosstalk voltage are eliminated separately. Specially, the L_s induced crosstalk voltage is eliminated through a high-impedance gate loop instead of creating low-impedance gate loop in conventional methods.

The circuit of the proposed scheme is shown in Fig. 6. The switch S_1 and S_2 are used to turn ON or turn OFF the device during switching transients, which is the same as the conventional gate driver. Another auxiliary clamping circuit composed of a bidirectional switch S_3 and a resistor R_{clamp} is added to tune the voltage level in the OFF-state to ensure the

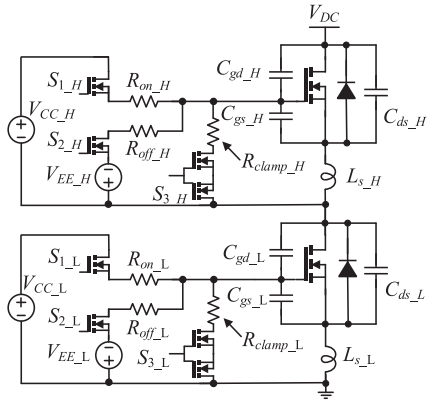


Fig. 6. Proposed high OFF-state impedance gate driver.

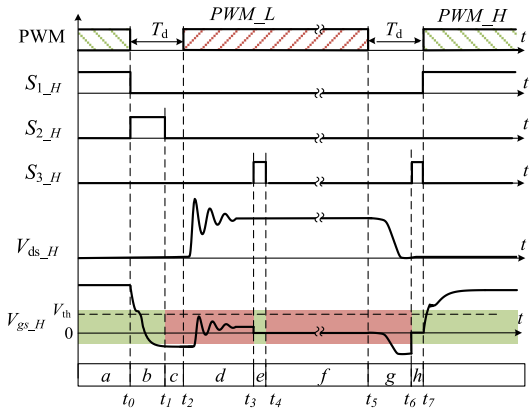


Fig. 7. Operation scheme of the proposed driver.

reliable operation. During the switching transients of the other device in the phase leg, S_1, S_2, and S_3 of the OFF-state device is turned OFF and the high-impedance gate loop is formed. As a result, the voltage drop on the common-source inductor is isolated from the gate source of SiC MOSFETs. As a result, the crosstalk voltage is only generated by displacement current from C_{gd}, which is eliminated by charging or discharging the gate-source capacitor before the drain-source voltage step of the device. Moreover, a large resistor parallel connected to the gate-source capacitor, which is omitted in Fig. 6, is required to prevent the potential electro-static discharge (ESD) on the gate-source terminal. Due to the large value, this resistor has little influence on the normal operation of the gate driver.

The operation principle of the driving circuit can be divided into five stages, as demonstrated in Fig. 7. In the figure, pulsewidth modulation (PWM) is the logical output of the phase leg, S_{1_H}, S_{2_H}, and S_{3_H} are driving signals of the upper gate driver, V_{ds_H} and V_{gs_H} are the drain-source and gate-source voltage waveforms. The equivalent circuit in each stage is demonstrated in Fig. 8. In the following analysis, the time sequence of the upper device is given when the lower device is turned ON or turned OFF. Since the turn-ON or turn-OFF of the auxiliary transistors in the gate driver loop is much faster than the devices in the main power loop, the switching transitions are viewed as ideal in the analysis.

Stage t_0–t_1: The equivalent circuit is demonstrated in Fig. 8(b). Before t_0, the upper device is on the ON-state, the gate-source voltage is at a high level. At t_0 the upper switch is turned OFF, and S_1, S_3 keeps in the OFF-state, then S_2 is turned ON to discharge the gate-source capacitor. R_{g_off} is the turn-OFF gate resistor. The turn-OFF process ends at t_1 when the oscillation of the drain-source voltage disappears. The gate-source capacitor is charged to the negative voltage and wait for the turn-ON of the lower device. The turn-OFF time t_{off} of the device can be calculated from the appendix equations in (A3) and (A8). The duration of this period should be larger than the turn-OFF time of the upper devices and lower than the deadtime, namely

$$t_{\mathrm{off}} < t_1 - t_0 < T_d \tag{1}$$

where T_d is the deadtime, which is the turn-ON delay time of the device to ensure the safe operation of the device. In this period, the gate-source voltage is the negative driving voltage and the gate loop impedance keeps in the low state.

Stage t_1–t_2: The equivalent circuit is demonstrated in Fig. 8(c). At t_1, S_2 turns OFF, S_3, S_1 remains in the OFF-state. During this period, the impedance of the gate loop is switched to the high-impedance state. The turn-ON of the lower device occurs when the deadtime ends. This stage ends when the lower device turns ON, satisfies

$$t_2 - t_1 = T_d - (t_1 - t_0)\,. \tag{2}$$

Stage t_2–t_3: The equivalent circuit is demonstrated in Fig. 8(d). At t_2, the lower device turns ON. The voltage of the lower device decreases from bus voltage to zero. Meanwhile, the gate–drain voltage of the upper device increases from zero to the bus voltage, accompanied by the voltage ring. In this stage, the gate–drain capacitor is charged, thus, the displacement current will cause a positive step on the gate source of the upper device. Since there is a preset negative voltage in the gate-source capacitor, the device will not turn ON if the voltage is properly assigned. The selection of the negative voltage will be discussed in Section IV. This stage ends when the clamping switch turns ON. The duration of this period satisfies

$$t_{\mathrm{on}} < t_3 - t_2 < T_{\mathrm{PWM\_}L} \tag{3}$$

where t_{on} is the turn-ON time of the lower device and can be calculated from (A13) to (A18). $T_{\mathrm{PWM\_}L}$ is the pulsewidth of the lower device. The upper limit duration of this stage is to ensure the clamping circuit is turned ON during the ON-state of the lower device. Since turn-ON time t_{on} of the SiC power devices is relatively short, the value of t_3–t_2 is very small. Equation (3) can be satisfied in most cases. However, under extreme conditions, when $T_{\mathrm{PWM\_}L} < t_{\mathrm{on}}$, the clamping pulse of S_3 is ignored to avoid the low-impedance gate loop of the lower device.

Stage t_3–t_4: The equivalent circuit is demonstrated in Fig. 8(e). At t_3, S_3 turns ON to clamp the gate-source voltage to zero before the turn-OFF of the lower device. Then at t_3, S_3 turns OFF. The impedance of the gate loop remains large to isolate the influence of the common-source inductor. The duration of this period depends on the response time of the clamping circuit,

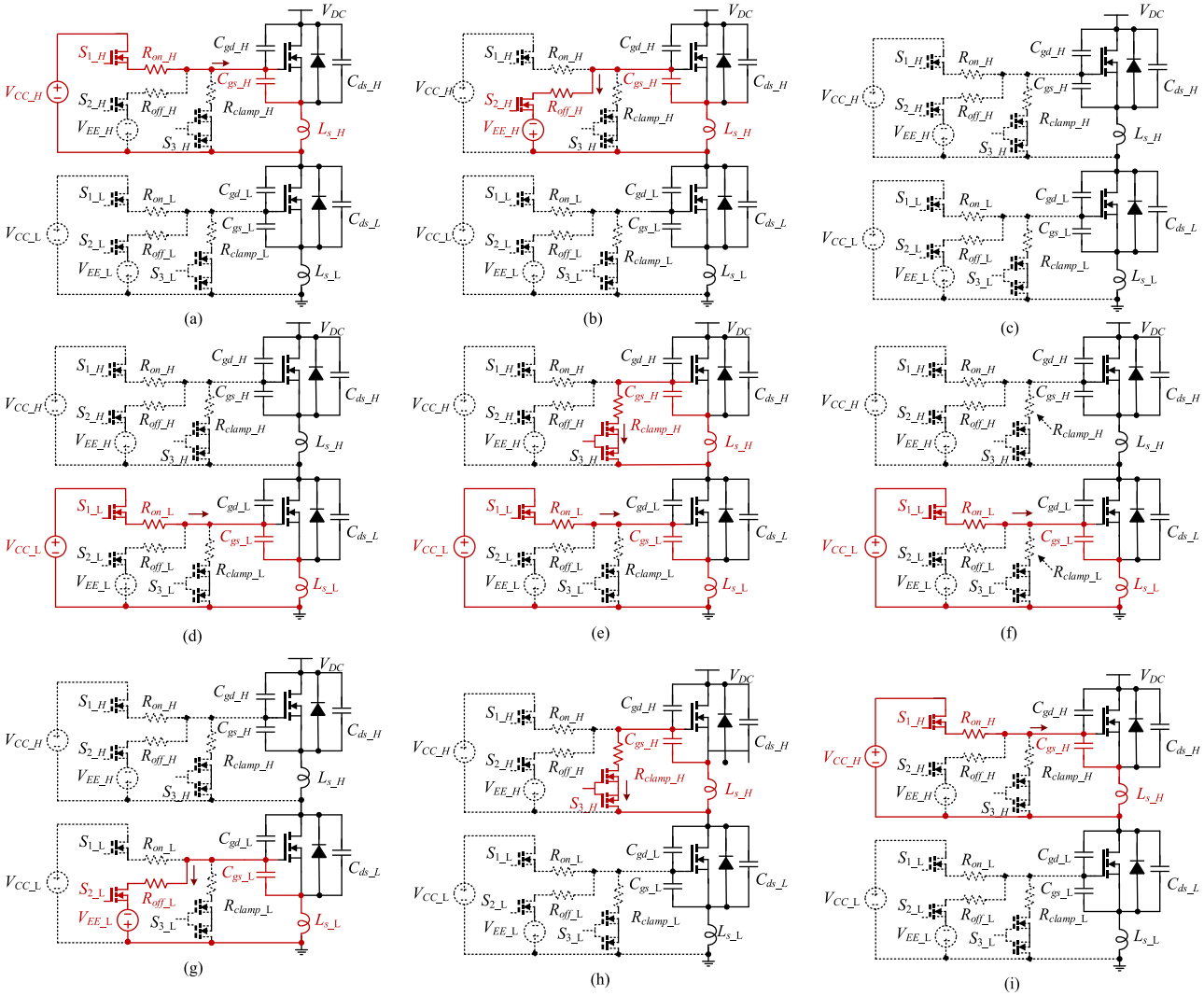


Fig. 8. Equivalent circuit in each stage.

namely

$$(R_{\text{clamp}} + R_{g,\text{int}} + R_s)C_{gs} < t_4 - t_3 \tag{4}$$

where R_s is the ON-state resistance of the clamping switch. $R_{g,\text{int}}$ is the internal gate resistance of the SiC MOSFET, R_{clamp} is the resistance of the clamping resistor. Basically, this period should be as small as possible to ensure the device can operate in the low-pulse conditions.

Stage t_4–t_5: The equivalent circuit is demonstrated in Fig. 8(f). In this stage, the upper device remains in high gate loop impedance, and the lower device is in the ON-state.

Stage t_5–t_6: The equivalent circuit is demonstrated in Fig. 8(g). At t_5, the lower device is turned OFF by turning ON S_{2_L}. The voltage of the upper devices will decrease as a result. The displacement current induces a negative voltage spike on the gate source of the upper device. In this stage, the gate loop of the upper device is in the high-impedance stage. The influence of the common-source inductance can be ignored. The duration of this stage should larger than the turn-OFF time of the lower device and smaller than the deadtime, namely

$$t_{\text{off}} < t_6 - t_5 < T_d. \tag{5}$$

The voltage fall time can be calculated using equations in the appendix section.

Stage t_6–t_7: The equivalent circuit is demonstrated in Fig. 8(h). At t_6, the clamping switch of the upper device will be turned on to drive the gate-source voltage to the zero. When the gate-source voltage is increased to zero, the upper device is turned ON. The OFF-state of the upper device is ended. The duration of the stage should be enough to discharge the gate-source capacitor, namely

$$t_7 - t_6 = T_d - (t_6 - t_5) > (R_{\text{clamp}} + R_{g,\text{int}} + R_s)C_{gs}. \tag{6}$$

At t_7, the upper device is turned ON. Since the control strategy of the lower device in the OFF-state is same as the upper device, the detailed description is omitted.

In the proposed scheme, the value selection of R_{clamp} is quite important. Basically, R_{clamp} should be as small as possible to ensure the fast clamping of the gate-source voltage.

The clamping circuit conducts in two stages, namely t_3–t_4 and t_6–t_7 in Fig. 7. In both stages, the voltage of gate-source capacitor is discharged to zero through the loop resistors. The upper limit of the response time of the clamping circuit loop is reflected in stage t_6–t_7, in which the gate-source voltage must be clamped to zero before the upper device is turned ON. The lower limit of the response time is to ensure enough damping resistance in the loop to avoid possible oscillations. As a result, the range of the R_{clamp} satisfies

$$2\sqrt{\frac{L_{\text{loop}}}{C_{gs}}} < R_{\text{clamp}} + R_{g,\text{int}} + R_s < \frac{T_d - t_{\text{off}}}{C_{gs}} \tag{7}$$

where T_d is the deadtime, t_{off} is the turn-OFF time of the lower device, and L_{loop} is the parasitic inductance in the clamping loop.

With the proposed circuit and control scheme, the influence of the common-source inductance on the crosstalk voltage is eliminated by the proposed high-impedance gate loop. The influence of C_{gd} induced crosstalk voltage is canceled by the prestored charge in the gate-source capacitance.

IV. Assessment of Off-State Gate Voltage Requirements of SiC Power MOSFET

In the proposed gate driver, the voltage level in the OFF-state should be considered comprehensively to ensure the reliable crosstalk elimination under various operation conditions. Since the influence of the common-source inductance is ignored, the analysis mainly focuses on the required charge of the gate-source capacitance. In this section, the design of the negative value of the OFF-state voltage is discussed considering the nonlinear characteristics of the devices. When there is a large gate loop impedance, the charge stored in the gate–drain capacitor is totally transferred to the gate-source capacitor. The gate–drain capacitance is voltage dependent and must be considered when selecting the proper OFF-state negative voltage.

The gate–drain capacitance can be approximated as [22]

$$C_{gd} = \frac{C_{gd0}}{\sqrt{1 + \frac{v_{gd}}{v_{td}}}} \tag{8}$$

where C_{gd0} is the junction capacitance at $v_{gd} = 0$, and V_{td} is the gate–drain overlap depletion threshold.

The coefficients in (8) can be acquired from the capacitance curve in the datasheet, as demonstrated in Fig. 9. In the OFF-state of the device in a phase leg, the voltage rising phase and falling phase occur due to the switching of the other device. When the voltage across the device rises, the gate-source capacitor is charged by the displace current from the drain-source capacitance, the total charge during this phase is

$$q_{gd} = \int_0^{V_{gd}} C_{gd}(v)dv \tag{9}$$

where q_{gd} is the stored charged in the gate–drain capacitor. When the voltage rises to the bus voltage, the Bode diode is fully turned OFF. The gate–drain voltage starts to oscillate to the power loop parasitic parameters. After the voltage of the body diode increases to the bus voltage, the voltage across the drain-source capacitance is relatively large, as a result, the drain-source capacitance C_{oss} can be viewed as constant to simplify the analysis, the expression of the drain-source voltage is [4]

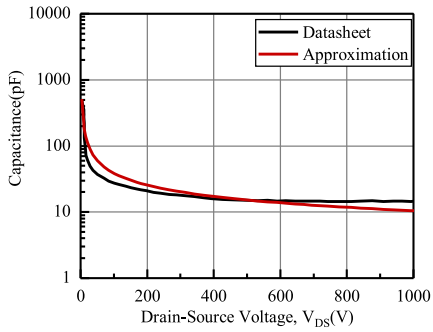


Fig. 9. Drain-source capacitance of SiC power MOSFETs: CREE c2m0025120d.

$$V_{gd} = \begin{cases} V_{\text{DC}}\left(1 - \cos\left(\frac{\pi t}{2t_{ri}}\right)\right), 0 \le t \le t_{\text{ri}} \\ V_{\text{DC}} + (V_{\text{rated}} - V_{\text{DC}})\, e^{-\alpha(t-t_{\text{ri}})} \cos\ (\omega t), t > t_{\text{ri}} \end{cases} \tag{10}$$

where $\alpha = R_{\text{stray}}/2(L_s + L_d)$ and $\omega = \sqrt{1/(C_{OSS}(L_s+L_d)) - \alpha^2}$, R_{stray} is the resistance in the power loop, C_{oss} is the output capacitance at the bus voltage, V_{rated} is the rated voltage of the devices, V_{DC} is the bus voltage, t_{ri} is the drain-source voltage rising time. In the expression of the gate–drain voltage, the peak voltage is selected as the rated voltage of the device, which is the largest allowable voltage of the devices in the design consideration.

When the voltage across the device falls, there exists a discharge current flowing through gate-source capacitor, the total charge in this phase is

$$q_{gd} = \int_{V_{gd}}^{0} C_{gd}(v)dv \tag{11}$$

where

$$V_{gd} = \begin{cases} V_{\text{DC}}\left(1 - \sin\left(\frac{\pi t}{2t_{fi}}\right)\right), 0 \le t \le t_{fi} \\ 0, t > t_{fi} \end{cases} \tag{12}$$

where t_{fi} is the drain-source voltage falling time. The difference between the voltage rising phase and voltage falling phase is that there are no oscillations occurred in the OFF-state device. The total stored charge will be passed to the gate-source capacitor during this period. The gate-source capacitance is a voltage-dependent parameter. Typically, C_{gs} from datasheet is given at $V_{gs} = 0$ V. When the gate-source voltage is applied, C_{gs} is larger than the value given in the datasheet [25]. Accurate C_{gs} can be acquired from the curve tracer or by the experiments. For simplicity, in the following analysis, the gate-source capacitance is viewed as constant. It is a conservative estimation of the required charge. To eliminate the induced charge of the turn-ON of the lower device, the required negative voltage to prevent the

TABLE II
CALCULATED NEGATIVE GATE-SOURCE VOLTAGE TO PREVENT FALSE TURN-ON OF DEVICES

Company	Devices	$V_{neg\_turn\ on}$(V)	$V_{neg\_turnoff}$ (V)	V_{neg_max}(V)
CREE 900V/36A	c3m0065090d	-9.4	-8.7	-10
CREE 1200V/30A	c3m0075120d	-0.9	-2.4	-10
CREE 1200V/90A	c2m0025120d	-8.0	-7.9	-10
CREE 1700V/72A	c2m0045170d	-5.6	-6.0	-10
Infineon 1200V/25A	FF45MR12W1M1	-6.9	-6.5	-10
Infineon 1200V/52A	IMZ120R045M1	-7.0	-8.0	-10
Infineon 1200V/100A	FF11MR12W1M1	-6.9	-6.2	-10
Rohm 1200V/100A	bsm080d12p2c008	-8.0	-7.3	-5

false turn-ON is given by

$$V_{\text{neg\_turnon}} = -k\left(\frac{q_{gd}}{C_{gs}} - V_{\text{th}}\right) \tag{13}$$

where $V_{\text{neg\_turnon}}$ is the negative voltage required to ensure safe switching of the upper device during the turn-ON of the lower device, k is the margin in design to prevent the disturbance from the variation of the parameters and other factors. At t = 0, $V_{\text{neg\_turnon}}$ reaches its maximum value, namely

$$V_{\text{neg\_turnon}} = -k\left(\frac{C_{gd0}V_{Td}}{C_{gs}}\left(\sqrt{1+\frac{V_{\text{rated}}}{V_{Td}}}-1\right) - V_{\text{th,min}}\right). \tag{14}$$

Let $k = 1.1$, $V_{\text{th,min}}$ is the gate threshold voltage at the maximum junction temperature, since the threshold voltage of the gate-source decreases significantly due to the junction temperature rising [25]. Another consideration is the negative gate-source voltage generated in stage t_6–t_7 in Fig. 7. When the lower device is turned OFF, the drain-source voltage of the upper device decreases from the bus voltage to the zero. A negative gate-source voltage is generated during this process, the value is

$$V_{\text{neg\_turnoff}} = -\frac{q_{gd}(V_{\text{DC}})}{C_{gs}} \tag{15}$$

where $V_{\text{neg\_turnoff}}$ is the gate-source voltage after turn-OFF of the lower device in stage t_6–t_7, V_{DC} is the bus voltage. Table II gives a series of the calculated negative voltages by (14) and (15) from the products in the market. In the calculation, the bus voltage is empirically selected as $V_{\text{DC}} = 0.75\ V_{\text{rated}}$.

On one side, the negative voltage should be enough to prevent false turn-ON of the devices, on the other side, the negative voltage should not exceed the negative voltage tolerance of the device. From the calculated results, most devices satisfy this requirement. It should be pointed out that the required negative voltage may be lower than the recommended negative voltage of the device. Fortunately, the negative voltage endurance of the gate source is related to the length of the stress time. As demonstrated in Fig. 10, regarding the Rohm products, the acceptable surge negative voltage is –10 V in 300 ns. Thus, if the negative voltage endurance time is controlled in only a short period of time, the value of the negative voltage can be increased, which allows larger precharge voltage selection of the gate-source capacitance. And thanks to the proposed driving scheme, the negative voltage is only added to the gate source in a short period of time, as pictured in Fig. 7.

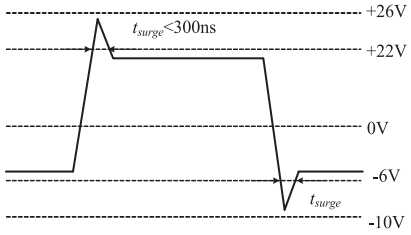


Fig. 10. Acceptable driving voltage waveform of SiC power MOSFETs of Rohm SCT2080KEHR.

Moreover, as demonstrated in (14), the precharge voltage is only related to the charge stored in the gate–drain capacitor, which is unaffected by the switching speed of the device and the switching current of the device. It is different from the traditional methods, where the voltage induced across the common-source inductance is related to the current variation speed. Only the voltage at the start and end of the transition needs to be considered in designing the negative OFF-state voltage.

Above all, with the proposed method, the analysis of the crosstalk voltage is simplified. The OFF-state negative voltage can be selected in consideration of the junction temperature and the nonlinear factors of the gate–drain capacitance. These parameters can be easily extracted from the datasheet or from the experiments.

V. EXPERIMENTAL VERIFICATION

In this section, the proposed gate driver is verified through a set of experiments. The experiments are conducted with the CREE 1200V/90 A SiC power MOSFET with TO247-3 package. In the experiment, the upper device acts as the device under disturbance, and the lower device is switching. The voltage is measured by the passive voltage probe with 500-MHz bandwidth and the current is measured by the shunt resistor with 200-MHz bandwidth. The oscilloscope is Lecory HDO6054A with 500-MHz bandwidth. To ensure safety, the oscilloscope is powered by an isolated transformer and controlled remotely. Apparently, driving the upper switch and measuring the lower switch is commonly suggested in practice, which is also effective in verifying the proposed gate driver.

A. Verification of the Proposed Gate Driver

In the test, the deadtime is selected as $T_d = 1\ \mu$s. The turn-OFF time of the device is within 50 ns, and $R_{g,\text{int}} = 1.1\ \Omega$, $R_s = 0.7\ \Omega$, $C_{gs} = 2.7$ nF. The loop inductance is approximately 15 nH. Based on the design criteria in (7), the range of R_{clamp} is

$$2.9\ \Omega < R_{\text{clamp}} < 350.0\ \Omega. \tag{16}$$

Thus, $R_{\text{clamp}} = 3\ \Omega$ is selected. According to the analysis in Section III, the time duration in each stage is listed in Table III. Fig. 11 demonstrates the waveform of the gate driver with the control sequence of each stage. The S_{1_H}, S_{2_H}, and S_{3_H} are the driving signals of the auxiliary transistors of the gate driver

TABLE III
SELECTED TIME IN EACH STAGE

stage	time
b	t_0-t_1=0.8μs
c	t_2-t_1=0.2μs
d	t_3-t_2=0.8μs
e	t_4-t_3=0.4μs
g	t_6-t_5=0.8μs
h	t_7-t_6=0.2μs

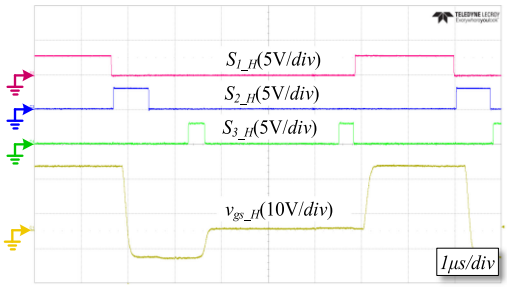


Fig. 11. Gate driver time sequence of the proposed driver.

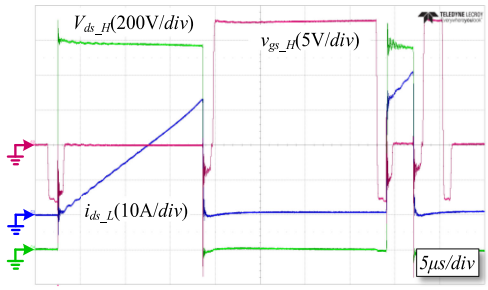


Fig. 12. Double pulse test of the proposed gate driver at 600 V/60 A with $R_{g\_L} = 5\ \Omega$.

of the upper device. Experimental results demonstrate that the proposed driving scheme is realized by the designed prototype. Since the maximum operation bus voltage of the experimental platform is 600 V, the negative voltage is set to –7.5 V, which is enough to prevent false turn-ON of the device.

B. Crosstalk Voltage Extraction and Experimental Verification of the Proposed Driver

In the designed driver, the double pulse test at 600 V/60 A is conducted. The result is demonstrated in Fig. 12. In reality, the voltage probe can only measure the voltage at the terminals of the package, which is the sum of the gate-source voltage and the voltage drop on the common-source inductor in the high-impedance state. To acquire the real crosstalk voltage of the gate-source capacitor, the voltage drop on the common-source inductor should be excluded.

The measurement method of the common-source inductance is demonstrated in Fig. 13. In the turn-OFF process of the lower device, the current of the upper device increases to the load current. But the drain-source voltage will remain constant due to the forward conduction of the body diode. In this phase, the

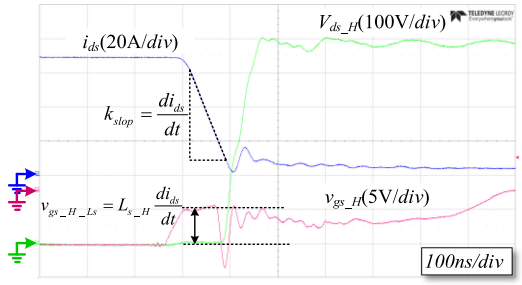


Fig. 13. Measurement of common-source inductance.

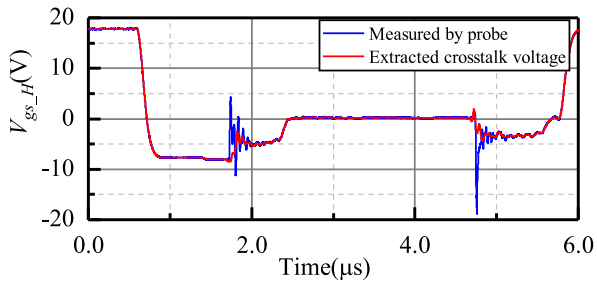


Fig. 14. Crosstalk voltage before and after removing voltage drop on common-source inductance V_{Ls}.

measured gate-source voltage $v_{gs\_H\_Ls}$ is the voltage drop on the common-source inductor. In conjunction with the current change rate $k_{\rm slop}$, the common-source inductance is estimated by

$$L_{s\_H} = \frac{v_{gs\_H\_Ls}}{k_{\rm slop}}. \tag{17}$$

In the proposed setup, the extracted common-source inductance is

$$L_{s\_H} = 4.86\ \text{nH}. \tag{18}$$

Thus, the extracted voltage on the gate-source terminal is

$$v_{gs\_H} = v_{\rm probe} - L_{s\_H}\frac{di_{ds}}{dt} \tag{19}$$

where $v_{\rm probe}$ is the voltage measured voltage at the gate-source terminal of the package, i_{ds} is the measured drain-source current. With this method, the crosstalk voltage is calculated with gate-source terminal voltage and current. Fig. 14 demonstrates the calculated crosstalk voltage from the waveform in Fig. 12. At time 1.8 μs, the lower device turns ON and a positive voltage step occurs at the drain source of SiC MOSFETs, as a result, the gate-source voltage increases about 3 V. At time 4.8 μs, the lower device turns OFF, there is a negative voltage step on the drain source of the upper device, the gate-source voltage decreases about 3.0 V consequently. There is a significant deviation in the measured crosstalk voltage and the extracted crosstalk voltage on the gate-source capacitance. The voltage stress of the gate-source terminal is smaller than the measured voltage from the probe. In the following waveforms, the crosstalk voltage refers to the voltage on the gate-source capacitance with the voltage drop on the common-source inductor removed.

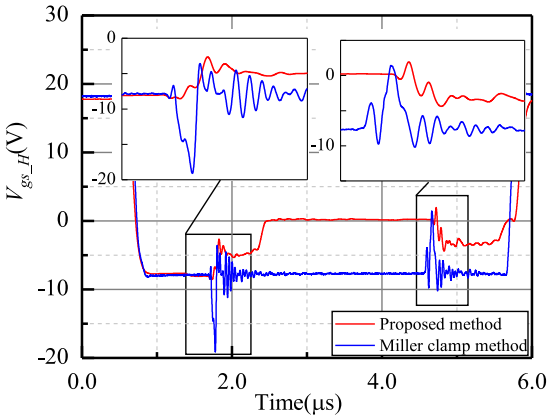


Fig. 15. Crosstalk voltage of the proposed method and Miller clamping method at 600 V/60 A.

C. Performance Comparison Between the Miller Clamping Method and Proposed Gate Driver

A performance comparison between the Miller clamping circuit [18] and proposed gate driver is provided. As demonstrated in Fig. 5, since the voltage probe measures the voltage at the terminals, the crosstalk voltage is extracted as with the method in part *B*. Ignoring the ripple voltage on the clamp capacitor, the extracted crosstalk voltage is calculated by

$$V_{gs\_H} = V_{\text{probe}} - \frac{R_{g,\text{int}}\left(R_s + R_{g,\text{ext}}\right)\left(V_{g\_\text{off}} - V_{\text{probe}}\right)}{R_s R_{g,\text{ext}}} - L_{s\_H}\frac{di_{ds}}{dt} \tag{20}$$

where $R_{g,\text{int}}$ is the internal gate resistor, $R_{g,\text{ext}}$ is the external gate resistor, $R_s = 0.35\ \Omega$ is the resistance of the clamping switch. In the test, $R_{g\_L} = 5\ \Omega$ is adopted. The extracted crosstalk voltage of the proposed method and Miller clamp method is given in Fig. 15. It is demonstrated that Miller clamp method is insufficient in eliminating crosstalk voltage. The induced peak negative voltage exceeds –10 V, which is the suggested maximum negative voltage in the datasheet. If there is an increase in the negative voltage to make the peak negative voltage in the permitted range, the peak positive voltage may be larger than the threshold voltage of the device. As a contrast, the proposed method guarantees the crosstalk voltage in the safe range, which validates the effectiveness of the proposed method.

D. Influence of the Operation Point on the Crosstalk Voltage

From the above analysis, the value of the crosstalk voltage of the proposed driving scheme is only related to the drain-source voltage of the device. Figs. 16 and 17 demonstrate the measured crosstalk voltage at different voltage/current conditions. When the drain-source voltage increases from 200 to 600 V, the crosstalk voltage increases accordingly. At 30 and 60 A switching conditions, the crosstalk voltage is nearly the same, which owes to the elimination of the influence of the common-source inductance. The switching current hardly affects the crosstalk voltage.

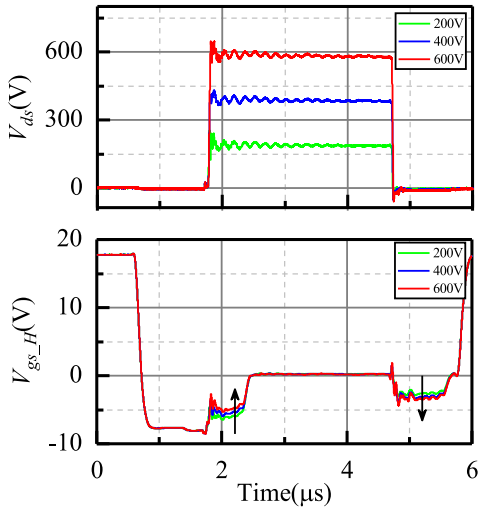


Fig. 16. Crosstalk voltage at different bus voltage at 60 A.

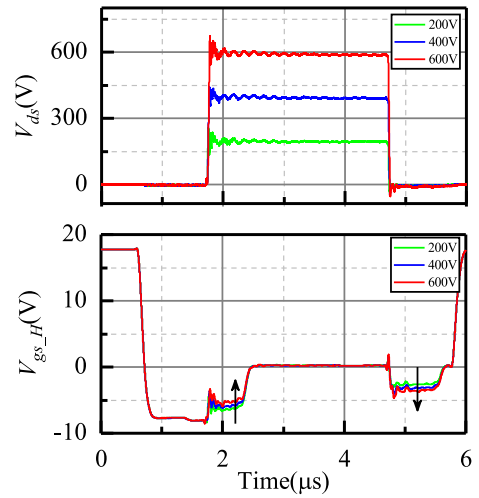


Fig. 17. Crosstalk voltage at different bus voltage at 30 A.

E. Influence of the Switching Speed on the Crosstalk Voltage

In conventional methods, the crosstalk voltage is influenced by the switching speed due to the gate–drain capacitor and the common-source inductor. In the proposed gate driver, the value of the crosstalk voltage is only related to the start point and end point of the gate–drain voltage. The switching speed on the crosstalk voltage is negligible. Fig. 18 demonstrates the crosstalk voltage measurements at different driving resistance at 600 V/60 A. Experimental results demonstrate that the crosstalk voltage keeps nearly the same at different gate driver resistors.

F. Influence of the Junction Temperature on the Crosstalk Voltage Elimination

In the continuous switching of the device, the junction temperature of the device will increase. And the threshold voltage will decrease as the increase of junction temperature. To verify the

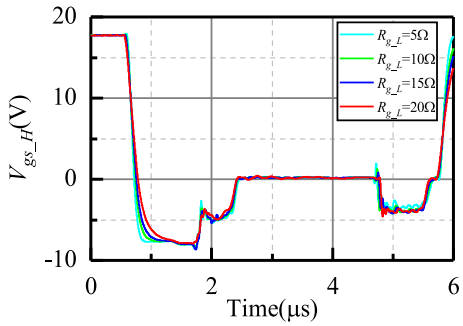


Fig. 18. Crosstalk voltage at different switching speeds of the lower device.

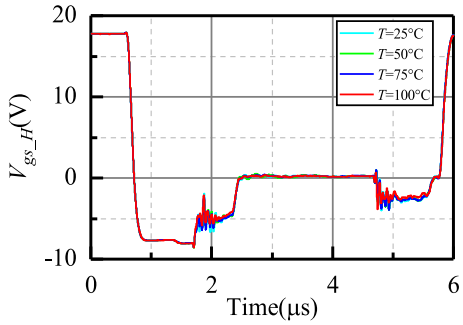


Fig. 19. Influence of junction temperature on crosstalk voltage at 600 V/60 A and $R_{g\_L} = 5\ \Omega$.

validity of the proposed gate driver under high junction temperature conditions, the proposed method is verified in high junction temperature conditions at 600 V/60 A. The measured crosstalk voltage is demonstrated in Fig. 19. As junction temperature increases, the crosstalk voltage remains constant. Compared with traditional results that the crosstalk voltage is influenced by the junction temperature significantly [27], the proposed scheme demonstrates less temperature dependence.

In conclusion, the proposed gate driver is verified in different operation points, different switching speeds, and different junction temperatures. The test results demonstrate excellent robustness in various switching conditions. In the application, the proposed gated driver is immune to the influence of the junction temperature and switching speed. It should be clarified that extra isolated power supply and isolated signal for the auxiliary clamping switch is required, which makes it a little complex and expensive compared with gate drivers without any clamping circuit. Fortunately, it can be integrated into a gate driver chip for reducing the complexity.

VI. Conclusion

A high OFF-state gate loop impedance driver has been proposed to eliminate the crosstalk voltage in a phase-leg configuration of SiC MOSFETs. It is pointed out that the crosstalk voltage is not only caused by the Miller capacitor but also by the common-source inductor of the package. The proposed method eliminates the influence of the common-source inductor with higher gate loop impedance. And a negative charge is prestored in the gate-source capacitor to eliminate the influence from the gate–drain capacitor. To ensure the reliable operation of the device, the requirements of the negative voltage of the gate source considering the voltage tolerance and junction temperature have been assessed. The calculation results of the negative voltage demonstrate that though the required negative voltage may be larger than the recommended negative voltage of the commercial device, this side effect can be canceled by the short negative voltage stress time of the gate electrode due to the proposed scheme. The proposed method is capable of driving most of the commercial devices. Moreover, thanks to the proposed high OFF-state impedance gate driver, the influence of the current change in the power loop can be neglected, which makes the induced crosstalk voltage is less influenced by the switching current and the junction temperature. Finally, the proposed scheme is verified through a set of experiments and demonstrates stable performance under different test conditions.

Appendix

The analytical model of the crosstalk voltage is provided here to describe the influence of the parasitic and nonlinear parameters. Since the crosstalk voltage is induced by the switching of the other device in the phase leg, it is controlled by the speed of the other device passively. Due to the nonlinearity of the device behavior, it is difficult to acquire the analytical model considering all the nonlinear behaviors. Here, we use an analytical model based on the analysis in [24] to describe the switching of the lower device. Then the crosstalk voltage is deduced based on the analysis.

The considered parasitic parameters include the common-source inductance, nonlinear junction capacitance and the reverse recovery of the diode. The oscillations in the power loop due to the leakage inductance and parasitic capacitance is ignored in the analysis for simplicity. In the given model, the voltage drop on the common-source inductor and the charging current of the junction capacitor are modeled with the average value in the transition duration. The transfer function of the SiC power MOSFET is described by

$$i_{\rm ch} = k_1(v_{gs} - V_{\rm th})^x + k_2 \tag{A1}$$

where $i_{\rm ch}$ is the channel current, the coefficients k_1, V_{th}, x, and k_2 can be acquired from the curve fitting in the datasheet. As demonstrated in Fig. 20, the turn-ON of the lower device is divided as current rising stage s_1 and voltage falling stage s_2, and the turn-OFF is divided as voltage rising stage s_3 and current falling stage s_4. In each stage, if the drain-source current is changing, the drain-source voltage is described by a constant average value, and vice versa. The equivalent circuit is given in the figure, the analytical model is deduced below in each stage separately.

Stage s_1*:* In this stage, the voltage on drain source of the upper device decreases from the bus voltage to the zero. There exists a discharging current to the drain-source capacitance. The average discharging current I_{oss} is acquired by numerically

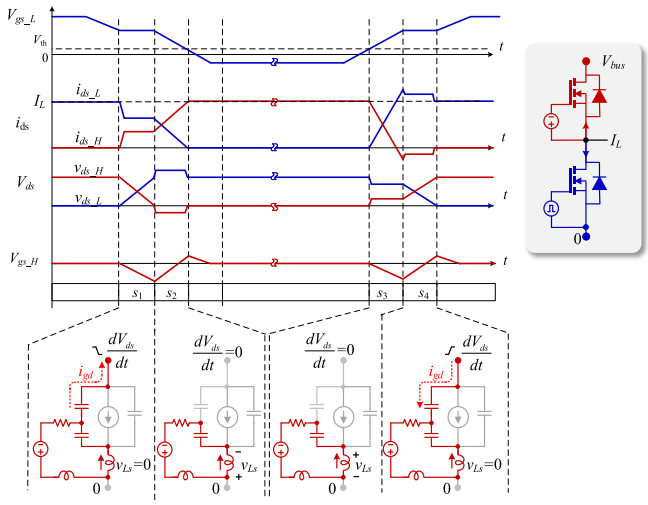


Fig. 20. Equivalent circuit of gate loop of the upper device at different switching stages of turn-ON/OFF of the lower device.

solving equation

$$\frac{2L_{s\_L}}{Q_{oss}R_{g\_L}}{I_{oss}}^2+\left(\frac{C_{gd}}{C_{gd}+C_{ds}}\right)I_{oss}-\frac{1}{R_{g\_L}}\left(\frac{I_L-2I_{oss}-k_2}{k_1}\right)^x+\frac{V_{g\_off}-V_{th}}{R_{g\_L}}=0 \quad \text{(A2)}$$

where Q_{oss} is the charge stored in the drain-source capacitance at bus voltage V_{DC}, C_{gd} and C_{ds} are the junction capacitance accordingly, and V_{th} is the threshold voltage of the device, I_L is load current. The duration of the stage s_1, represented by t_{s1}, is calculated by

$$t_{s1}=\frac{Q_{oss}}{I_{oss}}. \quad \text{(A3)}$$

The voltage of the Miller platform V_{miller} can be calculated by

$$V_{miller}=V_{th}+\left(\frac{I_L-2I_{oss}-k_2}{k_1}\right)^x. \quad \text{(A4)}$$

Since the voltage decreasing speed and current rising of the upper device and lower device are complementary, as demonstrated in Fig. 20. Due to the switching of the lower device, the average voltage drop V_{Ls_H} on the common-source inductance of the upper device is

$$V_{Ls\_H}=\frac{2L_{s\_H}{I_{oss}}^2}{Q_{oss}}. \quad \text{(A5)}$$

The displace current I_{gd_s1} of the gate–drain source capacitance of the upper device is

$$I_{gd\_s1}=\frac{V_{miller}-V_{g\_off}-V_{Ls\_H}}{R_{g\_L}}. \quad \text{(A6)}$$

Calculating the equivalent circuit in the stage s_1 in Fig. 20, the crosstalk voltage v_{gs_s1} in stage s_1 is

$$v_{gs\_s1}(t)=\left(V_{Ls\_H}-I_{gd\_s1}R_{g\_H}\right)\left(1-e^{-\frac{t}{\tau}}\right) \quad \text{(A7)}$$

where $\tau=R_{g\_H}C_{gs}$ is the response constant of the circuit. At the end of the stage s_1, the crosstalk voltage is $v_{gs\_s1}(t_{s1})$.

Stage s_2: The drain-source current of the upper device starts to increase to the load current, thus produce a voltage drop on the common-source inductor. The drain-source voltage keeps unchanged in this stage, thus, there is no feedback current to the gate loop. The time duration t_{s2} of this stage is controlled by the Miller plateau voltage of the lower device, namely

$$t_{s2}=-\ln\left(\frac{V_{g\_on}-V_{g\_off}}{V_{miller}-V_{g\_off}}\right)\cdot\left(\tau+g_{m\_s2}L_{s\_H}\right) \quad \text{(A8)}$$

where g_{m_s2} is the transconductance of the device and given by

$$g_{m\_s2}=\left(\frac{k_1(I_L-2I_{oss})^x}{I_L-2I_{oss}-k_2}\right)^{\frac{1}{x}}. \quad \text{(A9)}$$

Solving the equivalent circuit in Fig. 20, the crosstalk voltage v_{gs_s2} is

$$v_{gs\_s2}(t)=\left(\frac{L_{s\_H}\left(I_L-2I_{oss}\right)}{t_{s2}}\right)\left(1-e^{-\frac{t-t_{s1}}{\tau}}\right)+v_{gs\_s1}\left(t_{s1}\right)e^{-\frac{t-t_{ts1}}{\tau}}. \quad \text{(A10)}$$

Following the stage s_2, the crosstalk voltage will decrease to the negative driving voltage freely. The expression of the crosstalk voltage v_{gs_end} is

$$v_{gs\_end}(t)=-v_{gs\_s2}\left(t_{s1}+t_{s2}\right)e^{-\frac{t-t_{ts1}-t_{s2}}{\tau}}. \quad \text{(A11)}$$

Stage s_3: The lower device is turned ON, as a result, the current of the upper device will increase to the load current. Meanwhile, the drain-source voltage keeps the same. The transconductance g_{m_s3} is

$$g_{m\_s3}=\left(\frac{k_1{I_L}^x}{I_L-k_2}\right)^{\frac{1}{x}}. \quad \text{(A12)}$$

The current rising time t_{ri} is

$$t_{ri}=-\ln\left(1-\frac{I_L}{g_{m\_s3}\left(V_{g\_on}-V_{th}\right)}\right)\cdot\left(\tau+g_{s\_s3}L_{s\_H}\right). \quad \text{(A13)}$$

The current rising slop k_{ri} of the device is

$$k_{ri}=\frac{I_L}{t_{ri}}. \quad \text{(A14)}$$

When the drain-source current rises to the load current, the reverse recovery of the body diode occurs. In this article, the reverse recovery current and the charging current of the drain-source capacitance is modeled separately. The drain-source current of the lower devices will rise to the peak current at which the reverse recovery current reaches its peak value. During this stage, the drain-source voltage of the upper device remains zero due to the voltage clamping of the diode. The duration of the stage s_3 t_{s3} can be calculated by numerically solving

$$k_{ri}\tau_c\left(t_{ri}+\tau_c-t_{s3}-\tau_c e^{-\frac{t_{s3}}{\tau_c}}\right)+T_m\left(I_L-k_{ri}t_{ri}\right)=0 \quad \text{(A15)}$$

where τ_c and T_m are the parameters of the body diode of the power MOSFETs and can be acquired from the datasheet of the

device. The extraction procedure is given in [24]. The crosstalk voltage v_{gs_s3} can be calculated by

$$v_{gs\_s3}(t) = k_{\rm rise} L_{s\_H}\left(1 - e^{-\frac{t}{\tau}}\right). \tag{A16}$$

Stage s_4: When the current of the body diode falls from the peak reverse recovery current, the body diode starts to block voltage and the lower device enters the Miller plateau. The channel current of the lower device is composed of the charging current of the drain-source capacitance of both devices. The charging current I_{oss} is calculated by numerically solving

$$-\frac{2L_{s\_L}}{Q_{oss}R_{g\_L}}{I_{oss}}^2 + \left(\frac{C_{gd}}{C_{gd}+C_{ds}}\right) I_{oss} - \frac{1}{R_{g\_L}}\left(\frac{I_L - 2I_{oss} - k_2}{k_1}\right)^x + \frac{V_{g\_\rm on} - V_{\rm th}}{R_{g\_L}} = 0. \tag{A17}$$

The voltage rising time t_{s4} of the upper device is

$$t_{s4} = \frac{Q_{oss}}{I_{oss}}. \tag{A18}$$

The expression of the voltage drop of the common-source inductance and displacement current is the same as (A5) and (A6). In this phase, when the reverse recovery current falls from the peak current, there is a positive voltage $v_{gs\_s4\_\rm rr}$ induced, namely

$$v_{gs\_s4\_\rm rr}(t) = -\frac{L_{s\_H} I_{\rm rr}}{\tau_{\rm rr} - R_{g\_H}C_{gs}}\left(e^{-\frac{t-t_{s3}}{\tau}} - e^{-\frac{t-t_{s3}}{\tau_{\rm rr}}}\right) \tag{A19}$$

where $I_{\rm rr}$ is the peak reverse recovery current and given by

$$I_{\rm rr} = k_{\rm ri} t_{s3} - I_L. \tag{A20}$$

The crosstalk voltage v_{gs_s4} in this stage is expressed as

$$v_{gs\_s4}(t) = \left(V_{Ls\_H} + I_{gd\_s1}R_{g\_H}\right)\left(1 - e^{-\frac{t-t_{s3}}{\tau}}\right) + v_{gs\_s3}\left(t_{s3}\right)e^{-\frac{t-t_{s3}}{\tau}} + v_{gs\_s4\_\rm rr}(t). \tag{A21}$$

Following the stage s_4, the crosstalk voltage will decrease to the negative driving voltage freely. The expression of the crosstalk voltage $v_{gs\_\rm end}$ is

$$v_{gs\_\rm end}(t) = -v_{gs\_s4}\left(t_{s3} + t_{s4}\right)e^{-\frac{t-t_{ts3}-t_{s4}}{\tau}}. \tag{A22}$$

REFERENCES

[1] N. Kaminski, "The ideal chip is not enough: Issues retarding the success of wide band-gap devices," *Jpn J. Appl. Phys.*, vol. 56, no. 4, Feb. 2017, Art. no. 04CA03.

[2] J. Wang, H. S.-H. Chung, and R. T.-H. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 573–590, Jan. 2013.

[3] P. Venkataraghavan and B. Baliga, "The dV/dt capability of MOS-gated thyristors," *IEEE Trans. Power Electron.*, vol. 13, no. 4, pp. 660–666, Jul. 1998.

[4] N. McNeill, K. Sheng, and B. Williams, "Assessment of off-state negative gate voltage requirements for IGBTs," *IEEE Trans. Power Electron.*, vol. 13, no. 3, pp. 436–440, May 1998.

[5] Q. Zhao and G. Stojcic, "Characterization of Cdv/dt induced power loss in synchronous buck dc-dc converters," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1508–1513, Jul. 2007.

[6] L. Zhang, X. Yuan, X. Wu, C. Shi, J. Zhang, and Y. Zhang, "Performance evaluation of high-power SiC MOSFET modules in comparison to Si IGBT modules," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1181–1196, Feb. 2019.

[7] D. Peftitsis and J. Rabkowski, "Gate and base drivers for silicon carbide power transistors: An overview," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7194–7213, Oct. 2016.

[8] N. Idir, R. Bausiere, and J. Franchaud, "Active gate voltage control of turn-on *di/dt* and turn-off *dv/dt* in insulated gate transistors," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 849–855, Jul. 2006.

[9] H. C. P. Dymond *et al.*, "A 6.7-GHz active gate driver for GaN FETs to combat overshoot, ringing, and EMI," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 581–594, Jan. 2018.

[10] H. Xu, Y. Chang, H. Luo, W. Li, and X. He, "Turn-off performance optimization of press-pack IGBT with advanced active gate driver technique," in *Proc. 19th Eur. Conf. Power Electron. Appl.*, 2017, pp. P.1–P.6.

[11] I. Josifovic, J. Popovic, and J. A. Ferreira, "Improving SiC JFET switching behavior under influence of circuit parasitics," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3843–3854, Aug. 2012.

[12] Y. Li, M. Liang, J. Chen, T. Q. Zheng, and H. Guo, "A low gate turn-off impedance driver for suppressing crosstalk of SiC MOSFET based on different discrete packages," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 353–365, Mar. 2019.

[13] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active gate driver for cross talk suppression of SiC power devices in a phase-leg configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1986–1997, Apr. 2014.

[14] F. Gao, Q. Zhou, P. Wang, and C. Zhang, "A gate driver of SiC MOSFET for suppressing the negative voltage spikes in a bridge circuit," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2339–2353, Mar. 2018.

[15] J. Wang and H. S.-H. Chung, "A novel RCD level shifter for elimination of spurious turn-on in the bridge-leg configuration," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 976–984, Feb. 2015.

[16] B. Zhang, S. Xie, J. Xu, Q. Qian, Z. Zhang, and K. Xu, "A magnetic coupling based gate driver for crosstalk suppression of SiC MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9052–9063, Nov. 2017.

[17] K. Umetani, R. Matsumoto, and E. Hiraki, "Prevention of oscillatory false triggering of GaN-FETs by balancing gate-drain capacitance and common-source inductance," *IEEE Trans. Ind. Appl.*, vol. 55, no. 1, pp. 610–619, Jan. 2019.

[18] L. Dulau, S. Pontarollo, A. Boimond, J.-F. Garnier, N. Giraudo, and O. Terrasse, "A new gate driver integrated circuit for IGBT devices with advanced protections," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 38–44, Jan. 2006.

[19] Z. Zhang, J. Dix, F. Wang, B. J. Blalock, D. Costinett, and L. M. Tolbert, "Intelligent gate drive for fast switching and crosstalk suppression of SiC devices," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9319–9332, Dec. 2017.

[20] S. Yin *et al.*, "A novel gate assisted circuit to reduce switching loss and eliminate shoot-through in SiC half bridge configuration," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 3058–3064.

[21] B. Yang and J. Zhang, "Effect and utilization of common source inductance in synchronous rectification," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, vol. 3, Mar. 2005, pp. 1407–1411.

[22] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York, NY, USA: Springer, 2008.

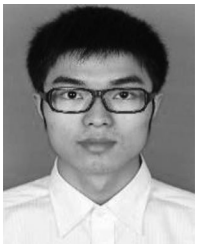
[23] K. Umetani, K. Aikawa, and E. Hiraki, "Straightforward measurement method of common source inductance for fast switching semiconductor devices mounted on board," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8258–8267, Oct. 2017.

[24] D. Christen and J. Biela, "Analytical switching loss modeling based on datasheet parameters for MOSFETs in a half-bridge," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3700–3710, Apr. 2019.

[25] H. Sakairi, T. Yanagi, H. Otake, N. Kuroda, and H. Tanigawa, "Measurement methodology for accurate modeling of SiC MOSFET switching behavior over wide voltage and current ranges," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7314–7325, Sep. 2018.

[26] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic mechanisms of threshold-voltage instability and implications for reliability testing of SiC MOSFETS," *IEEE Trans. Electron. Devices*, vol. 62, no. 2, pp. 316–323, Feb. 2015.

[27] S. Jahdi, O. Alatise, J. A. O. Gonzalez, R. Bonyadi, L. Ran, and P. Mawby,"Temperature and switching rate dependence of crosstalk in Si-IGBT and SiC power modules," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 849–863, Oct. 2015.



Chengmin Li (S'15) received the B.S. degree in electrical engineering from the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, China, in 2013. He is currently working toward the Ph.D. degree at the College of Electrical Engineering in Zhejiang University, Hangzhou, China.

His research interests include characterization of power devices and applications of SiC power MOSFETs in high-power converters.

Zhebie Lu (S'19) received the B.Sc. degree in electrical engineering from the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, China, in 2017. He is currently working toward the M.Sc. degree at Zhejiang University, Hangzhou, China.

His research interests include high-speed SiC devices driver circuit design and high-power medium-voltage soft-switching converters design.

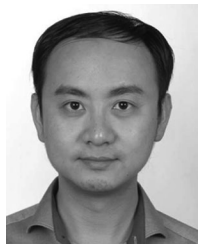
Ying Chen received the B.S. degree from the College of Information Science and Engineering, Central South University, Hunan, China, in 2017. She is currently working toward the M.Sc. degree from the College of Electrical Engineering, Zhejiang University, Zhejiang, China.

Her research interests include the modeling and the driver design of high-speed SiC devices.

Chushan Li (M'17) received the B.E.E. and Ph.D. degrees in electrical engineering from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 2008 and 2014, respectively.

He is currently an Assistant Professor in Zhejiang University–University of Illinois at Urbana-Champaign Institute, Zhejiang, China.

From April to September 2008, he was an Internship Student with the Power Application Design Center, National Semiconductor Co. Ltd., Hong Kong. From December 2010 to October 2011, he was a Visiting Scholar with the FREEDM Center, North Carolina State University. From December 2013 to June 2014, he was a Research Assistant with Hong Kong Polytechnic University. From July 2014 to July 2017, he was a Postdoctoral Fellow with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada. His research interest includes high power density power converter design and ac–dc power conversion.



Haoze Luo (M'15) received the B.S. and M.S. degrees from the Department of Electrical Engineering, Hefei University of Technology, Hefei, China, in 2008 and 2011, respectively, and the Ph.D. degree from Zhejiang University, Hangzhou, China, in 2015.

From January to April 2015, he was a Visiting Researcher with Newcastle University, Newcastle upon Tyne, U.K. From October 2015 to May 2018, he was a Postdoc with the Department of Energy Technology, Aalborg University, Aalborg, Denmark. His research interests include high-power converters and reliability of high-power modules.

Wuhua Li (M'09) received the B.Sc. and Ph.D. degree in power electronics and electrical engineering from Zhejiang University, Hangzhou, China, in 2002 and 2008, respectively.

From 2004 to 2005, he was a Research Intern, and from 2007 to 2008, a Research Assistant with GE Global Research Center, Shanghai, China. From 2008 to 2010, he joined the College of Electrical Engineering, Zhejiang University, as a Postdoctor. In 2010, he was promoted as an Associate Professor. Since 2013, he has been a Full Professor with Zhejiang University. From 2010 to 2011, he was a Ryerson University Postdoctoral Fellow with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada. He has authored or coauthored more than 200 peer-reviewed technical articles and holds more than 30 issued/pending patents. His research interests include power devices, converter topologies, and advanced controls for high-power energy conversion systems.

Dr. Li, due to his excellent teaching and research contributions, was the recipient of the 2012 Delta Young Scholar from Delta Environmental and Educational Foundation, the 2012 Outstanding Young Scholar from National Science Foundation of China, the 2013 Chief Youth Scientist of National 973 Program, the 2014 Young Top-Notch Scholar of National Ten Thousand Talent Program. He serves as the Associate Editor for the *Journal of Emerging and Selected Topics in Power Electronics*, *IET Power Electronics*, *CSEE Journal of Power and Energy Systems*, *Proceedings of the Chinese Society for Electrical Engineering*, Guest Editor of *IET Renewable Power Generation* for Special Issue "DC and HVDC system technologies," and member of Editorial Board for the *Journal of Modern Power System and Clean Energy*. He was the recipient of one National Natural Science Award and four Scientific and Technological Achievement Awards from Zhejiang Provincial Government and the State Educational Ministry of China. He was appointed as the Most Cited Chinese Researchers by Elsevier in 2014.

Xiangning He (M'95–SM'96–F'10) received the B.Sc. and M.Sc. degrees from Nanjing University of Aeronautical and Astronautical, Nanjing, China, in 1982 and 1985, respectively, and the Ph.D. degree from Zhejiang University, Hangzhou, China, in 1989.

From 1985 to 1986, he was an Assistant Engineer with the 608 Institute of Aeronautical Industrial General Company, Zhuzhou, China. From 1989 to 1991, he was a Lecturer with Zhejiang University. In 1991, he received a Fellowship from the Royal Society of U.K., and conducted research in the Department of Computing and Electrical Engineering, Heriot-Watt University, Edinburgh, U.K., as a Postdoctoral Research Fellow for two years. In 1994, he joined Zhejiang University as an Associate Professor. Since 1996, he has been a Full Professor with the College of Electrical Engineering, Zhejiang University. He was the Director of the Power Electronics Research Institute, the Head of the Department of Applied Electronics, the Vice Dean of the College of Electrical Engineering, and he is currently the Director of the National Specialty Laboratory for Power Electronics, Zhejiang University. His research interests include power electronics and their industrial applications.

Dr. He was appointed as the IEEE Distinguished Lecturer by the IEEE Power Electronics Society in 2011. He is also a Fellow of the Institution of Engineering and Technology (formerly IEE), U.K.