High-Efficiency Three-Level DC–DC Converter With Reduced Circulating Current and Rectifier Voltage Stress

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***Abstract*—This paper proposes a high-efficiency three-level (TL) dc–dc converter with reduced circulating current and rectifier voltage stress by using coupled inductor in the rectifier circuit. Because of decreased circulating current, the conduction loss in the primary circuit is reduced. In addition, since the rectifier diodes with low forward voltage drop can be employed due to the small voltage stress, the conduction loss of rectifier diodes can be reduced. Therefore, the efficiency can be increased due to the reduction of the conduction losses in the primary circuit and rectifier diodes. The characteristics of the proposed converter are analyzed and compared with other TL converters. The validity of the proposed converter is verified by the experimental results of the prototype with 540–600 VDC input and 750 W (48 V/15.625 A) output.**

***Index Terms*—Coupled inductor, reduced circulating current, small rectifier voltage stress, three-level (TL) converter.**

I. Introduction

OVER the past several years, high input voltage dc–dc converter has become a very important issue in medium to high-power applications such as fuel cell systems, ship-electric-power-distribution system, and high-voltage charging system, etc. [1]–[4]. Generally, insulated-gate bipolar transistors (IGBTs) and metal-oxide-semiconductor FETs (MOSFETs) are utilized for the primary switches. First, IGBTs are preferred for high input voltage application due to high-voltage blocking capability. However, IGBTs cannot be utilized with high switching frequency. Second, although MOSFETs can be used with high switching frequency, high-voltage-rating MOSFETs result in high cost and poor efficiency. Therefore, to achieve high efficiency with high switching frequency, decreasing the voltage stress of the primary switches and using MOSFETs are the best candidates.

In order to decrease the voltage stress of the primary switches, three-level (TL) dc–dc converters are widely used [5]–[14]. TL dc–dc converters are very suitable in high input voltage applications because the voltage stress of the primary switches becomes half of the input voltage. However, in TL dc–dc converters, there are two significant problems. At first, the large circulating current in the primary circuit causes a large conduction loss. Because the circulating current flows through the primary switches and clamping diodes without transferring the power, it results in large conduction loss in the primary circuit. Second, high-voltage-rating rectifier diodes lead to large conduction loss. Due to the resonance between the leakage inductor and parasitic capacitor, rectifier diodes have large voltage ringing, and the voltage across the rectifier diodes becomes high. Because high-voltage-rating diodes have large forward voltage drop, it results in large conduction loss in the rectifier diodes. Thus, it is necessary to minimize the circulating current and voltage ringing across the rectifier diodes for high efficiency.

In order to reduce the circulating current and voltage ringing across the rectifier diodes, many research works have been studied [15]–[21]. The work in [15] reduces the circulating current in the primary circuit. However, the converter requires additional switches and still has large voltage ringing across the rectifier diodes. Research in [16] decreases the voltage ringing across the rectifier diodes. However, the converter still suffers from the large conduction loss due to the circulating current, and this scheme only can be utilized in full-bridge TL converters. In [17]–[19], the voltage stress across the rectifier diodes is decreased, and the circulating current is reduced in the primary circuit. The converters utilize MOSFETs for leading switches to achieve zero-voltage switching (ZVS) operation and IGBTs for lagging switches to achieve zero current switching operation. However, IGBTs suffer from the current tailing phenomenon, and they limit the switching frequency. The works in [20]–[21] reduce the voltage stress across the rectifier diodes, and the circulating current is decreased in the primary circuit. However, lagging switches cannot achieve the ZVS operation under light-load condition. Although large leakage inductance can extend the ZVS range of lagging switches, it leads to large duty cycle loss.

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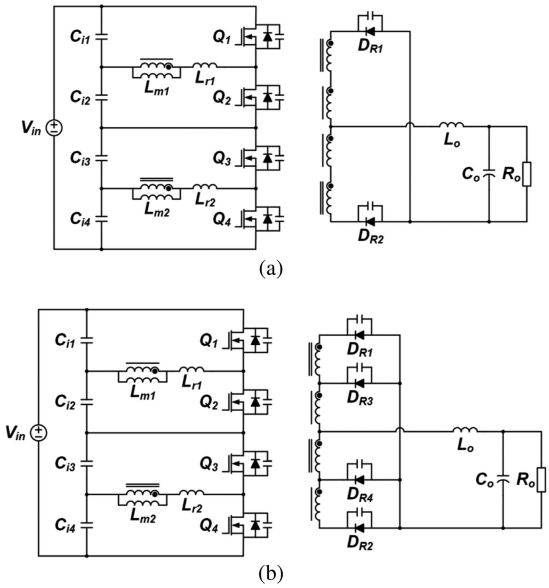

Fig. 1. Conventional TL dc–dc converters. (a) DHBC TL dc–dc converter. (b) Converter in [26].

Furthermore, the aforementioned studies [15]–[21] all have the clamping diodes in the primary circuit, which increase the cost and complexity of the circuit. Thus, to remove the clamping diodes, dual half-bridge cascaded (DHBC) TL dc–dc converter is suggested as shown in Fig. 1(a) [22]–[24]. In DHBC converter, one dc-blocking capacitor is added, but two clamping diodes are removed in comparison with the conventional TL dc–dc converter. Due to low cost and compact circuit structure, DHBC converter is widely used for industrial applications. However, DHBC TL dc–dc converter still has the circulating current in the primary switches and large voltage ringing problem across the rectifier diodes such as the conventional TL dc–dc converter. Therefore, to decrease the circulating current and voltage ringing across the rectifier diodes, several studies have been studied [25], [26]. In [25], the circulating current is reduced, and the soft switching of the primary switches can be achieved from full-load to light-load conditions. However, there is still large voltage ringing across the rectifier diodes. The work in [26] added two diodes in the rectifier circuit as shown in Fig. 1(b). It decreases the voltage stress across the rectifier diodes and the circulating current in the primary switches. However, because only half of the circulating current is removed, the circulating current flows through either Q_2 or Q_3. Also, the ZVS operation of the lagging switch cannot be achieved under light-load conditions.

In this paper, high-efficiency DHBC TL dc–dc converter is proposed by using a coupled inductor in the rectifier circuit. The circulating current flowing through the primary switches is decreased, and the voltage ringing across the rectifier diodes is reduced. Because the circulating current in the primary switches is decreased, the conduction loss in the primary switches is reduced. In addition, because of using the rectifier diodes having low forward voltage drop, the conduction loss of the rectifier diodes is reduced. Therefore, due to the small conduction losses

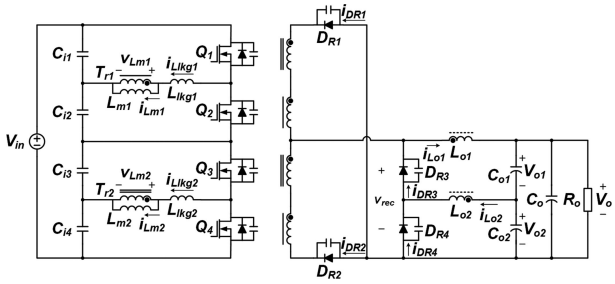

Fig. 2. Proposed DHBC TL dc–dc converter.

in the primary switches and rectifier diodes, the efficiency of the proposed converter is improved. Compare with [27], the improvements are expressed as follows.

1) Optimum design of coupled inductor is achieved.
2) Current stresses of primary switches are analyzed and compared with other TL dc–dc converters.
3) Experimental results of comparison between the proposed converter and DHBC TL dc–dc converter is added.
4) More detailed analysis of characteristics is added.

The validity of the proposed converter is confirmed by 540–600 VDC input and 750 W(48 V/15.625 A) output prototype.

II. Operational Principle

Fig. 2 shows the circuit diagram of the proposed DHBC TL dc–dc converter. The turn-ON time of Q_1 is complementary to that of Q_2 with dead time. The same gate signals are applied to Q_3 and Q_4 with a 180° phase difference. Fig. 3 shows the key operating waveforms of the proposed converter in the steady state. There are five modes in each half-switching period. The operating circuit of each mode is shown in Fig. 4. For simple analysis, the following assumptions are made as follows.

1) Input capacitances, C_{i1}, C_{i2}, C_{i3}, and C_{i4}, are large enough to be regarded as voltage sources. The voltage across the input capacitors, V_{Ci1}, V_{Ci2}, V_{Ci3}, and V_{Ci4} are calculated as follows:

$$V_{Ci1} = V_{Ci4} = \frac{(1-D)V_{\rm in}}{2} \tag{1}$$

$$V_{Ci2} = V_{Ci3} = \frac{DV_{\rm in}}{2} \tag{2}$$

where $V_{\rm in}$ is the input voltage and D is the duty ratio of Q_1 and Q_4.
2) The output capacitance is large enough that output voltage, V_o, is constant.
3) Turns ratio of the two transformers, T_{r1} and T_{r2}, is the same.

Mode 1 [t_0–t_1]: When Q_1 is turned ON, and i_{DR3} becomes zero, mode 1 starts. This mode is the powering mode because the power is transferred from the primary side to secondary side. The voltage across the primary winding of T_{r1}, v_{Lm1}, is (1–D)$V_{\rm in}$/2, and that of T_{r2}, v_{Lm2}, is $DV_{\rm in}$/2. Thus, the rectifier circuit voltage, $V_{\rm rec}$, is $V_{\rm in}$/2n regardless of D. In the rectifier circuit, the output current flows through D_{R2}. The current flows

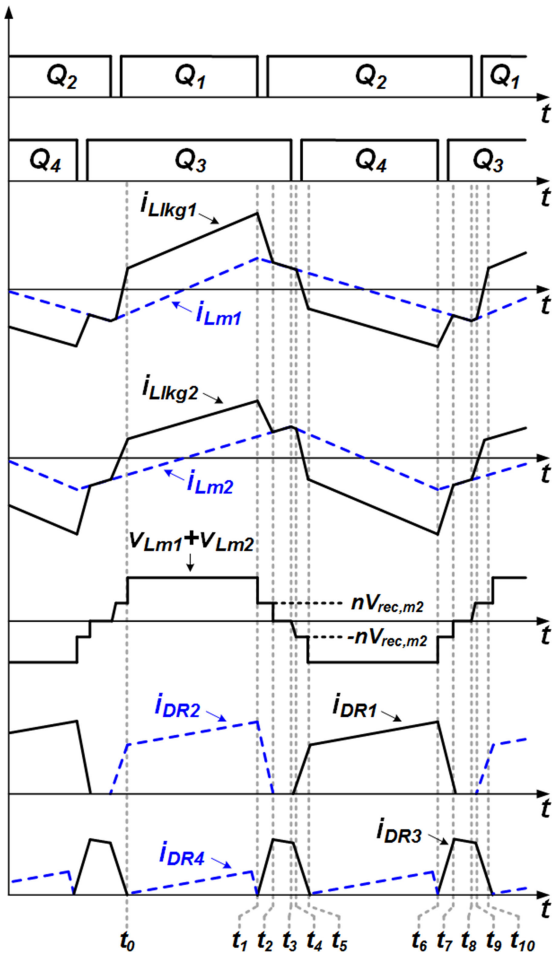

Fig. 3. Key operating waveforms of the proposed converter in steady state.

through D_{R4} discharges the upper side output capacitor, C_{o1}, and charges bottom side output capacitor, C_{o2}.

Mode 2 [t_1–t_2]: When Q_1 is turned OFF, mode 2 starts. During this mode, the output capacitors of Q_1 and Q_2 are charged and discharged. Until the leakage inductor current of T_{r1}, i_{lkg1}, becomes the same with the magnetizing inductor current of T_{r1}, i_{Lm1}, the leakage inductor helps in the ZVS operation of Q_2. After i_{lkg1} becomes the same with i_{Lm1}, the magnetizing inductor helps the ZVS operation. Thus, the ZVS operation of Q_2 can be easily achieved with sufficient energy.

During the mode 2, the circulating current decreases according to the voltage across the leakage inductors, L_{lkg1} and L_{lkg2}. At first, the relationships among the voltage across the magnetizing inductor of T_{r1}, v_{Lm1}, the voltage across the magnetizing inductor of T_{r2}, v_{Lm2}, the voltage across the leakage inductor of T_{r1}, v_{lkg1}, and the voltage across the leakage inductor of T_{r2}, v_{lkg2} are obtained as follows:

$$v_{Lm1} + v_{lkg1} = -0.5DV_{\text{in}} \tag{3}$$

$$v_{Lm2} + v_{lkg2} = 0.5DV_{\text{in}} \tag{4}$$

$$v_{Lm1} + v_{Lm2} = nV_{\text{rec},m2} \tag{5}$$

where n is turns ratio of the transformer.

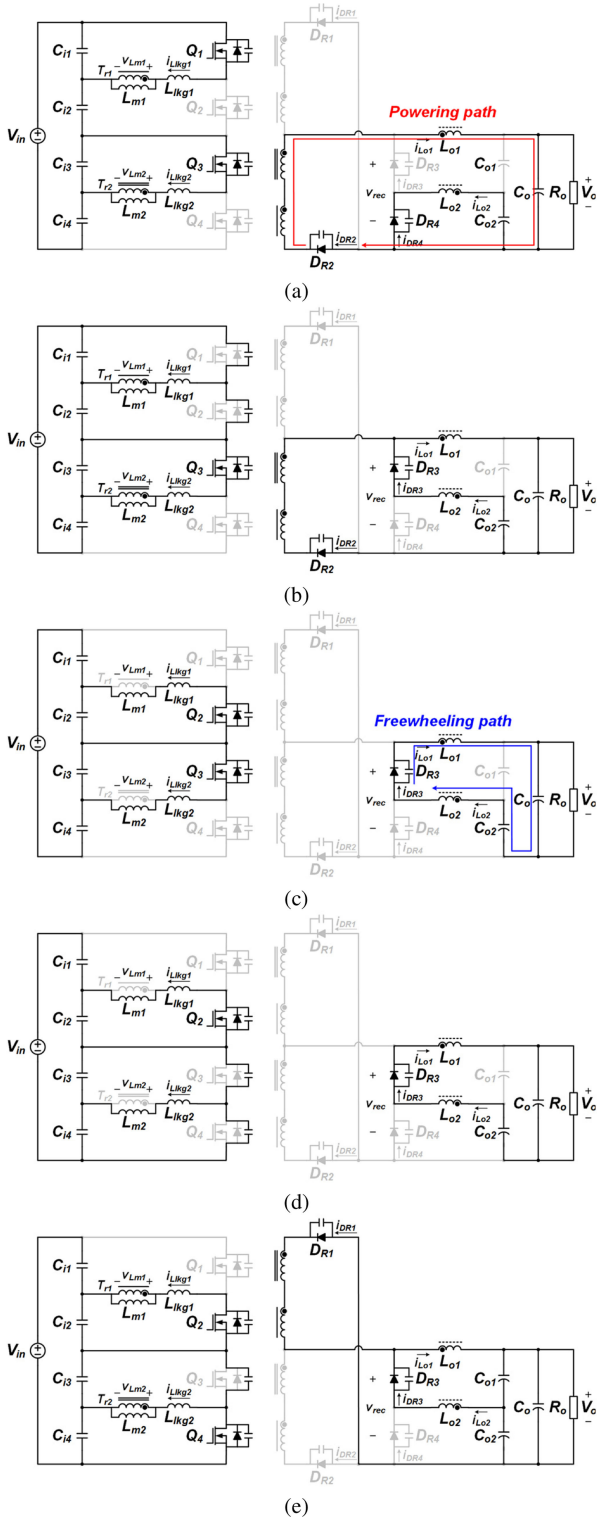

Fig. 4. Operating circuits of the proposed converter. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5.

The rectifier circuit voltage during the mode 2, $V_{\text{rec},m2}$, can be calculated as follows:

$$V_{\text{rec},m2} = \frac{V_{\text{in}}}{2n(n_c + 1)} \tag{6}$$

where n_c is turns ratio of the coupled inductor.

With the assumption that L_{lkg1} is the same with L_{lkg2}, v_{lkg1} is equal to v_{lkg2}. Then, using (3)–(6), the voltage across the leakage inductors can be obtained as follows:

$$v_{lkg1} = v_{lkg2} = -\frac{V_{\text{in}}}{4\,(n_c+1)}. \tag{7}$$

According to (7), the voltage across the leakage inductor is negative. Thus, the circulating current decreases, and the current flowing through D_{R2} decreases.

Mode 3 [t_2–t_3]: When Q_2 is turned ON, and i_{DR2} becomes zero, mode 3 begins. This mode is the freewheeling mode. Because the circulating current decreases during mode 2, only the magnetizing inductor current flows through the primary switches. In the rectifier circuit, the output inductor current flows through D_{R3} and coupled inductor.

Mode 4 [t_3–t_4]: When Q_3 is turned OFF, mode 4 begins. During this mode, the magnetizing inductor helps the ZVS operation of Q_4. Because D_{R1} and D_{R2} are reverse-biased, the output inductor current is not transferred to the primary side, and the voltage across Q_4 is discharged by the magnetizing inductor energy. When $(v_{Lm1}+v_{Lm2})$ becomes $-nV_{\text{rec},m2}$, D_{R1} becomes forward-biased, and mode 4 ends.

Mode 5 [t_4–t_5]: When $(v_{Lm1}+v_{Lm2})$ becomes $-nV_{\text{rec},m2}$, mode 5 starts. During this mode, the output capacitor of Q_4 is discharged by the leakage inductor energy, and the ZVS operation of Q_4 is achieved.

III. Analysis of the Proposed Converter

In Section III, the characteristics and design example of the proposed converter are presented with following specifications: input voltage = 540–600 V, output voltage = 48 V, rated output power = 750 W, and switching frequency = 100 kHz.

A. Voltage Gain

With assumption that the duty cycle loss is negligible, the voltage gain can be obtained from the voltage-second balance of the output inductor. In the proposed converter, the average voltage across the output inductor, $v_{Lo,\text{avg}}$, is calculated as follows:

$$v_{Lo,\text{avg}} = \left(\frac{V_{\text{in}}}{2n} - V_o\right) DT_s + \left(-\frac{n_c}{1+n_c}V_{o1}\right)(0.5-D)\,T_s = 0 \tag{8}$$

where V_o is the output voltage and T_s is the switching period.

The voltage across the output inductor during mode 1 in Section II is $(V_{\text{in}}/2n–V_o)$. Because V_{o2} is the same with the opposite side voltage of the output inductor, V_{o2} can be calculated as follows:

$$V_{o2} = \frac{1}{n_c}\left(\frac{V_{\text{in}}}{2n} - V_o\right). \tag{9}$$

Since $V_{o1} = V_o–V_{o2}$, using (8) and (9), the voltage gain of the proposed converter, M_{prop}, is expressed as follows:

$$M_{\text{prop}} = \frac{V_o}{V_{\text{in}}} = \frac{1+2Dn_c}{2n(1+n_c)}. \tag{10}$$

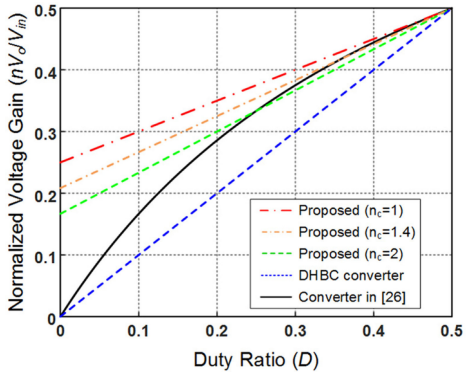

Fig. 5. Normalized voltage gain according to the duty ratio.

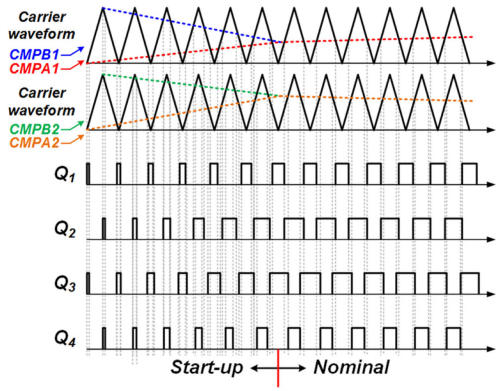

Fig. 6. Control scheme during the start-up operation.

In the same way, the voltage gain of DHBC converter, M_{conv1} and the converter in [26], M_{conv2}, can be obtained as follows:

$$M_{\text{conv1}} = \frac{V_o}{V_{\text{in}}} = \frac{D}{n} \tag{11}$$

$$M_{\text{conv2}} = \frac{V_o}{V_{\text{in}}} = \frac{D(3-2D)}{2n}. \tag{12}$$

Using (10)–(12), the normalized voltage gain of the proposed converter, DHBC converter, and the converter in [26] are compared in Fig. 5. Because the output voltage of the converter should be regulated at the minimum input voltage, n is designed considering the maximum voltage gain. According to (10), the maximum voltage gain of the proposed converter is $(1/2n)$ when $D = 0.5$. Thus, considering the duty cycle loss and parasitic components, n of the proposed converter is designed as 4.8.

According to (10), the voltage gain of the proposed converter cannot become 0. Thus, another control scheme is required to build up the initial output voltage. If the duty cycle of every primary switch is 0, the voltage gain of the proposed converter can become 0. Thus, during the start-up operation, the duty cycle of Q_1 and Q_3 increase from 0 to D, and the duty cycle of Q_2 and Q_4 increase from 0 to (1–D) with 180° phase difference as shown in Fig. 6. Because the duty cycle of every primary switch increases from 0, the voltage gain of the proposed converter also increases from 0. After that, during the nominal operation, the proposed converter regulates the output voltage by changing the duty ratio of the primary switches. Although the primary switches suffer

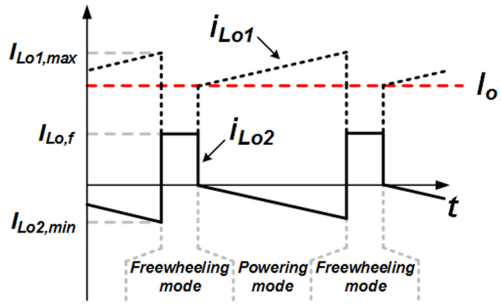

Fig. 7. Current flowing through the output inductor.

from hard switching during the start-up operation, it has little impact on the performance of the converter due to its short period.

B. Coupled Inductor Design

There are three guidelines to design the coupled inductor. First, the minimum turns of the coupled inductor, $N_{c,\min}$, should be designed to prevent the saturation of the output inductor [28], [29]. Assuming that the ripple current of the output inductor and duty cycle loss are negligible, the current flowing through L_{o1}, i_{Lo1}, and current flowing through L_{o2}, i_{Lo2}, are shown in Fig. 7. During the freewheeling mode, the constant current flows to D_{R3}, L_{o1}, and L_{o2}, and the amplitude of i_{Lo1} and i_{Lo2} become equal. Due to the coupled inductor structure, the relationship between i_{Lo1} and i_{Lo2} can be expressed as follows:

$$i_{Lo2}(t) = \frac{1}{n_c}\left(I_o - i_{Lo1}(t)\right) \tag{13}$$

where I_o is the output current.

Because i_{Lo1} and i_{Lo2} are the same during the freewheeling mode, by using (13), the current flowing through coupled inductor during the freewheeling mode, $I_{Lo,f}$, can be calculated as follows:

$$I_{Lo,f} = \frac{n_c}{n_c+1} I_o. \tag{14}$$

During the powering mode, the resonance among the leakage inductor of the coupled inductor, C_{o1}, and C_{o2} determines the shape of i_{Lo2}. Due to large C_{o1} and C_{o2}, i_{Lo1} and i_{Lo2} are formed as triangle shape as shown in Fig. 7. By applying the current-second balance of C_{o2}, the minimum current of i_{Lo2}, $I_{Lo2,min}$, can be calculated as follows:

$$\left(\frac{n_c}{n_c+1} I_o\right)(0.5-D)\,T_s + \left(0.5 I_{Lo2,\min}\right) DT_s = 0 \tag{15}$$

$$I_{Lo2,\min} = -\frac{n_c}{n_c+1}\left(\frac{1-2D}{D}\right) I_o. \tag{16}$$

In order to prevent the inductor saturation, $N_{c,\min}$ should be designed with considering the maximum current of i_{Lo1}, $i_{Lo1,max}$. Because i_{Lo1} has the maximum value when the i_{Lo2} has the minimum value, by utilizing (13) and (16), $i_{Lo1,max}$ can be obtained. Thus, $i_{Lo1,max}$ and $N_{c,\min}$ can be calculated as follows:

$$I_{Lo1,\max} = I_o + \frac{1}{n_c+1}\left(\frac{1-2D}{D}\right) I_o \tag{17}$$

$$N_{c,\min} = \frac{L_o I_{Lo1,\max}}{A_e B_{\text{sat}}} \tag{18}$$

where A_e is the effective cross-sectional area, and B_{sat} is the saturation flux density.

Second, n_c should be selected to design the winding area, $A_{w,Lo}$, smaller than the winding window area of the output inductor core [28], [29]. To calculate $A_{w,Lo}$, the rms value of i_{Lo1} and i_{Lo2} should be obtained. In case of i_{Lo1}, the current increases linearly during powering mode, and the current has constant value, $I_{Lo,f}$, during the freewheeling mode. In case of i_{Lo2}, the current decreases linearly during the powering mode, and the current has constant value, $I_{Lo,f}$, during the freewheeling mode. Thus, the rms value of i_{Lo1}, $i_{Lo1,\text{RMS}}$, and the rms value of i_{Lo2}, $i_{Lo2,RMS}$, can be calculated as follows: (19) and (20) shown at the bottom of this page.

Finally, $A_{w,Lo}$ is total area of wire wound on output inductor core, and by using (18)–(20), it can be calculated as follows:

$$A_{w,Lo} = k_u N_{c,\min}\left(\frac{i_{Lo1,\text{RMS}}}{J_{Lo}} + \frac{1}{n_c}\frac{i_{Lo2,\text{RMS}}}{J_{Lo}}\right) \tag{21}$$

where k_u is the window utilization factor, and J_{Lo} is the current density of the wire.

$$\begin{aligned} i_{Lo1,\text{RMS}} &= \sqrt{\frac{1}{0.5T_s}\left[\int_0^{DT_s}\left(I_o + \frac{1}{n_c+1}\frac{1-2D}{D^2T_s} I_o t\right)^2 dt + \int_{DT_s}^{0.5T_s}\left(\frac{n_c}{n_c+1} I_o\right)^2 dt\right]} \\ &= \sqrt{2\left[DI_o^2 + \frac{(1-2D)I_o}{n_c+1} + \left\{\frac{(1-2D)\,I_o}{n_c+1}\right\}^2\left(\frac{1}{3D} + \frac{n_c^2}{2}\right)\right]} \end{aligned} \tag{19}$$

$$\begin{aligned} i_{Lo2,\text{RMS}} &= \sqrt{\frac{1}{0.5T_s}\left[\int_0^{DT_s}\left(\frac{n_c}{n_c+1}\frac{1-2D}{D^2T_s} I_o t\right)^2 dt + \int_{DT_s}^{0.5T_s}\left(\frac{n_c}{n_c+1} I_o\right)^2 dt\right]} \\ &= \sqrt{\left(\frac{n_c}{n_c+1} I_o\right)^2 \frac{(1-2D)\,(2-D)}{3D}} \end{aligned} \tag{20}$$

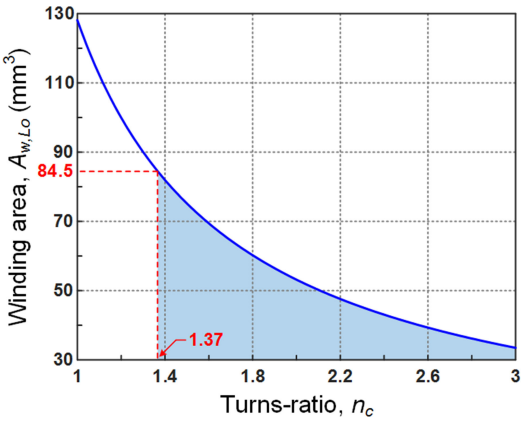

Fig. 8. Winding area of the output inductor according to n_c.

Third, n_c should be designed to minimize the circulating current. The circulating current decreases depending on v_{lkg1} and v_{lkg2}. Using (7), the duty ratio of mode 2 in Section II, D_{mode2}, can be calculated as follows:

$$\frac{|v_{lkg1}|}{L_{lkg1}} D_{\mathrm{mode2}} T_s = \frac{I_o}{n} \tag{22}$$

$$D_{\mathrm{mode2}} = \frac{I_o L_{lkg1}}{n\,|v_{lkg1}|\,T_s} = \frac{4\,(n_c+1)\,L_{lkg1} I_o}{n V_{in} T_s}. \tag{23}$$

From (23), according to decrease of n_c, D_{mode2} decreases. Because large D_{mode2} results in rapid decline of the circulating current, small n_c should be selected to reduce the circulating current.

In this design example, to calculate n_c, the output inductor inductance, L_o, is 13 μH, the core is PQ2625 whose winding window area is 84.5 mm^3, and J_{Lo} is 7 A/cm^2. Using (21), $A_{w,Lo}$ according to n_c is expressed in Fig. 8. According to the second design guideline, $A_{w,Lo}$ should smaller than the winding window area of PQ2625. Thus, n_c should be larger than 1.37 as shown in Fig. 8. Also, according to the third design guideline, small n_c should be chosen to reduce the circulating current. Therefore, considering the design guidelines of coupled inductor, n_c is designed as 1.4.

C. ZVS Condition of the Primary Switches

In the proposed converter, the ZVS condition of the lagging switches and leading switches are different. The output capacitor of the leading switch is charged and discharged by the energy stored in the output inductor and magnetizing inductor. Even at no-load condition, the ZVS operation can be achieved due to the sufficient magnetizing inductor energy. Thus, the ZVS operation of the leading switches can be performed under entire load conditions.

In case of the lagging switches, the ZVS condition is determined by the energy stored in the magnetizing inductor and leakage inductor. As mentioned earlier, the voltage across the lagging switch is discharged by the magnetizing inductor energy during D_{R1} and D_{R2} are reverse biased. Thus, until the voltage across the lagging switch becomes $(V_{\mathrm{in}}/2–nV_{\mathrm{rec},f})$, the magnetizing inductor current discharges the output capacitor of the lagging switch. After that, the energy stored in the leakage inductor involves in the ZVS operation. Therefore, the leakage inductor current should be large enough when the ZVS operation is started. Because the leakage inductor current is the same with the magnetizing inductor current during the mode 3 in Section II, the leakage inductor current at the initial point of the ZVS operation is equal to the peak magnetizing inductor current, $I_{Lm,pk}$. Thus, $I_{Lm,pk}$ can be calculated, and the converter should satisfy following conditions:

$$I_{Lm,pk} = \frac{D\,(1-D)\,V_{\mathrm{in}}}{4 L_m f_s} \tag{24}$$

$$\frac{1}{2}\,(L_{lkg1}+L_{lkg2})\,{I_{Lm,pk}}^2 \geq \frac{1}{2}\,(2C_{oss})\left(\frac{V_{\mathrm{in}}}{2} - nV_{\mathrm{rec},f}\right)^2 \tag{25}$$

where L_m is the magnetizing inductance, f_s is the switching frequency, and C_{oss} is the output capacitance of the primary switches.

Using (24) and (25), to achieve the ZVS operation of the lagging switches under entire load conditions, the maximum value of the magnetizing inductance can be obtained as follows:

$$L_m \leq \sqrt{\frac{(L_{lkg1}+L_{lkg2})}{2C_{oss}}}\left(1+\frac{1}{n_c}\right)\left(\frac{D(1-D)}{2f_s}\right). \tag{26}$$

Compared with the conventional converters, the proposed converter has a smaller peak current due to the reduced circulating current. However, the ZVS operation of lagging switches can be achieved because the proposed converter has larger energy for the ZVS operation. From (26), L_m is designed as 300 μH to achieve the ZVS operation of lagging switches. Therefore, the proposed converter guarantees the ZVS operation of the primary switches under entire load conditions.

D. Current Stress of the Primary Switches

Compared with the DHBC converter and the converter in [26], the proposed converter has smaller circulating current in the primary switches. With the assumption that the duty cycle loss and output inductor current ripple are negligible, the current waveforms flowing through the primary switches are shown in Fig. 9. There are no circulating current in Q_1 and Q_4 for every converter. The sum of the reflected output current and magnetizing inductor current flows through Q_1 and Q_4, and the rms current flowing through Q_1 and Q_4, $i_{Q1,Q4\_\mathrm{rms}}$, is calculated as follows:

$$i_{Q1,Q4\_\mathrm{rms}} = \sqrt{\frac{1}{T_s}\int_0^{DT_s}\left(\frac{(1-D)\,V_{\mathrm{in}}}{2L_m}t + \frac{I_o}{n} - I_{Lm,pk}\right)^2 dt}$$

$$= \sqrt{D\left[\frac{1}{3}{I^2}_{Lm,pk} + \left(\frac{I_o}{n}\right)^2\right]}. \tag{27}$$

For Q_2 and Q_3, the circulating current flows from t_0 to t_1 and from t_2 to t_3. For DHBC converter, the sum of the reflected output current and magnetizing inductor current flows. For the converter in [26], the magnetizing inductor current flows from t_0 to t_1, and the sum of the reflected output current and

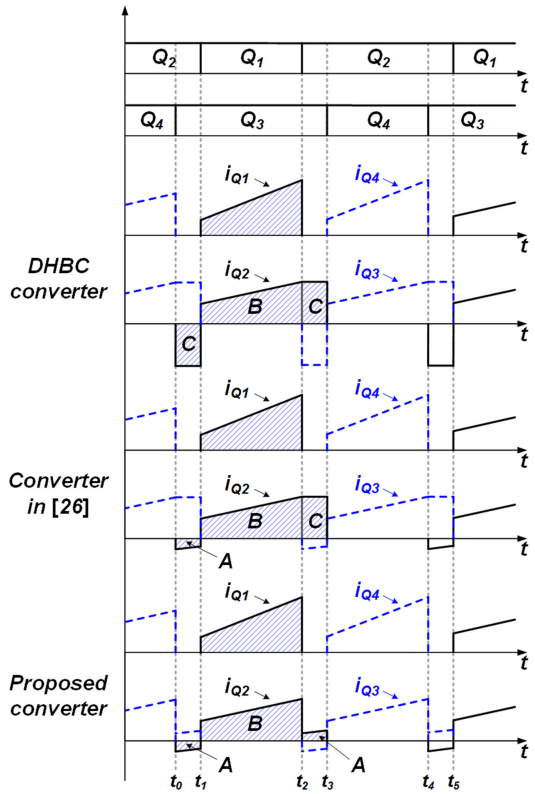

Fig. 9. Current waveforms flowing through the primary switches.

magnetizing inductor current flows from t_2 to t_3. In the proposed converter, only the magnetizing inductor current flows. To calculate the rms current in Q_2 and Q_3 for the proposed converter, $i_{Q2,Q3\_\mathrm{rms\_prop}}$, area A and B should be considered as shown in Fig. 9. Thus, $i_{Q2,Q3\_\mathrm{rms\_prop}}$ can be obtained as follows:

$$i_{Q2,Q3\_\mathrm{rms},A} = \int_0^{DT_s} \left(\frac{DV_{\mathrm{in}}}{2L_m}t - I_{Lm,pk}\right)^2 dt$$
$$= (0.5-D)\left[\frac{4}{3}\left(\frac{0.5-D}{D}I_{Lm,t2}\right)^2 - 2\left(\frac{0.5-D}{D}I_{Lm,t2}\right)I_{Lm,pk} + I_{Lm,pk}^2\right] \quad (28)$$

$$i_{Q2,Q3\_\mathrm{rms},B} = \int_0^{DT_s} \left(\frac{DV_{\mathrm{in}}}{2L_m}t + \frac{I_o}{n} - I_{Lm,t2}\right)^2$$
$$= D\left[\frac{1}{3}I_{Lm,t2}^2 + \left(\frac{I_o}{n}\right)^2\right] \quad (29)$$

$$i_{Q2,Q3\_\mathrm{rms\_prop}} = \sqrt{\frac{1}{T_s}\left(2i_{Q2,Q3\_\mathrm{rms},A} + i_{Q2,Q3\_\mathrm{rms},B}\right)} \quad (30)$$

where $I_{Lm,t2} = D^2V_{\mathrm{in}}/(4L_mf_s)$.

Using (10), (27), and (30), the rms current in the primary switches of the proposed converter can be calculated. Similarly, the rms current of the conventional converters can be obtained. For the current flowing through Q_1 and Q_4, the duty ratio and magnetizing inductance are changed. Therefore, the rms current in Q_1 and Q_4 of DHBC converter and the converter in [26] can be obtained by using (11), (12), and (23). However, in the case of the current flowing through Q_2 and Q_3, the circulating current is increased. To calculate the rms current in Q_2 and Q_3 for DHBC converter, $i_{Q2,Q3\_rms\_conv1}$, area B and C should be considered as shown in Fig. 9. Also, to calculate the rms current in Q_2 and Q_3 for the converter in [26], $i_{Q2,Q3\_rms\_conv2}$, areas A, B, and C should be considered. Thus, $i_{Q2,Q3\_rms\_conv1}$ and $i_{Q2,Q3\_rms\_conv2}$ can be expressed as follows:

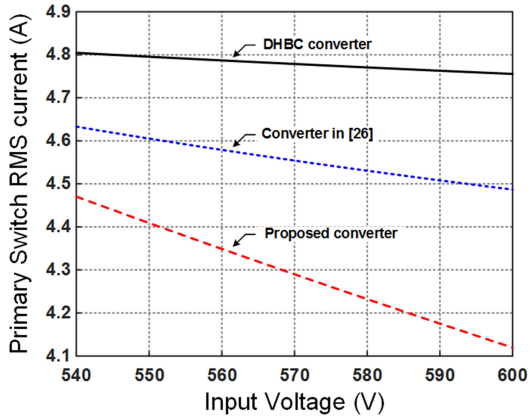

Fig. 10. Total rms current in the primary switches according to the input voltage at full load condition.

$$i_{Q2,Q3\_\mathrm{rms},C} = \int_0^{DT_s}\left(\frac{I_o}{n} + I_{Lm,pk1}\right)^2 dt$$
$$= \left(\frac{I_o}{n} + I_{Lm,pk1}\right)^2 (0.5-D) \quad (31)$$

$$i_{Q2,Q3\_\mathrm{rms\_conv1}} = \sqrt{\frac{1}{T_s}\left(i_{Q2,Q3\_\mathrm{rms},B} + 2i_{Q2,Q3\_\mathrm{rms},C}\right)} \quad (32)$$

$$i_{Q2,Q3\_\mathrm{rms\_conv2}}$$
$$= \sqrt{\frac{1}{T_s}\left(i_{Q2,Q3\_\mathrm{rms},A} + i_{Q2,Q3\_\mathrm{rms},B} + i_{Q2,Q3\_\mathrm{rms},C}\right)}. \quad (33)$$

Therefore, the current stress on primary switches of DHBC converter, converter in [26], and proposed converter can be calculated, and they are compared in Table I. Fig. 10 shows the comparison of the total rms current in the primary switches of the proposed converter and conventional converters at the full-load condition. Because the proposed converter has a smaller amount of the circulating current, the proposed converter has smaller conduction loss compared with the conventional converters.

E. Voltage Stress of the Rectifier Diodes

Due to the resonance between the leakage inductor and junction capacitor of the rectifier diodes, there is a voltage ringing problem across the secondary rectifier diodes. The equivalent circuit at the secondary side of the proposed converter during mode 1 in Section II is shown in Fig. 11(a). The voltage across

TABLE I
CURRENT STRESS ON PRIMARY SWITCHES OF THE PROTOTYPE CONVERTERS

	DHBC converter	Converter in [26]	Proposed converter
Primary switch (Q_1, Q_4)	$\sqrt{D\left[\frac{1}{3}I_{Lm,t2}^2+\left(\frac{I_o}{n}\right)^2\right]}$		
Primary switch (Q_2, Q_3)	$\sqrt{\frac{1}{T_s}\left(2i_{Q2,Q3\_rms,A}+i_{Q2,Q3\_rms,B}\right)}$	$\sqrt{\frac{1}{T_s}\left(i_{Q2,Q3\_rms,B}+2i_{Q2,Q3\_rms,C}\right)}$	$\sqrt{\frac{1}{T_s}\left(i_{Q2,Q3\_rms,A}+i_{Q2,Q3\_rms,B}+i_{Q2,Q3\_rms,C}\right)}$

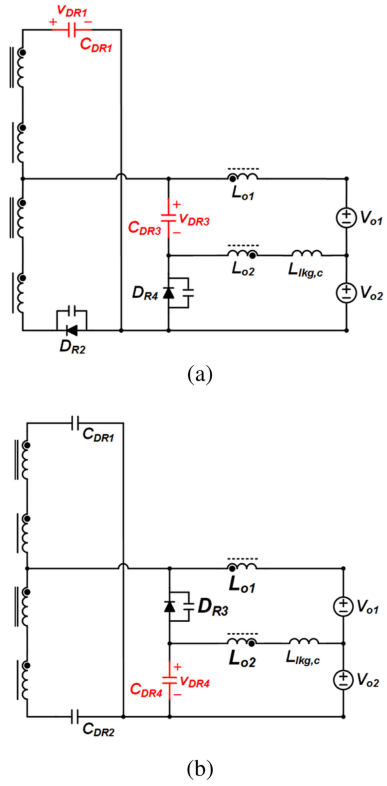

Fig. 11. Equivalent circuit at the secondary side of the proposed converter. (a) During mode 1 in Section II. (b) During mode 3 in Section II.

TABLE II
VOLTAGE STRESS OF RECTIFIER DIODES OF THE PROTOTYPE CONVERTERS

	DHBC converter	Converter in [26]	Proposed converter
Rectifier diode (D_{R1},D_{R2})	$\left(\frac{2V_{in}}{n}\right)$	$\left(\frac{2V_{in}}{n}-V_o\right)$	$2\left(\frac{V_{in}}{n}-V_o\right)$
Rectifier diode (D_{R3})	-	$2\left(\frac{V_{in}}{n}-V_o\right)$	$\left(\frac{V_{in}}{n}-V_o\right)$
Rectifier diode (D_{R4})			$\left(\frac{(n_c-1)V_{in}}{2nn_c(n_c+1)}-\frac{V_o}{n_c}\right)$

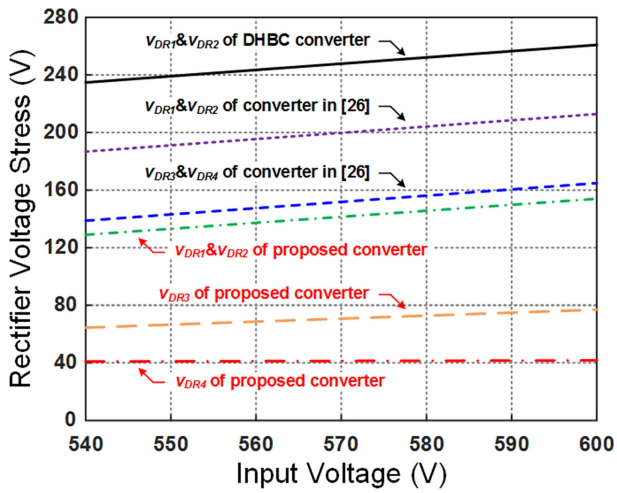

Fig. 12. Voltage stress of the rectifier diodes according to the input voltage.

D_{R3}, v_{DR3}, is the sum of V_{o1} and V_{o2} is V_o, and the voltage across L_{o1} is $(V_{\text{in}}/2n–V_o)$, v_{DR3} is calculated as follows:

$$v_{DR3}(t) = V_o + \left(\frac{V_{\text{in}}}{2n} - V_o\right)\cos(\omega_c t) \tag{34}$$

where C_D is the junction capacitance of the rectifier diodes, $L_{lkg,c}$ is the leakage inductance of the coupled inductor, and $\omega_c = (L_{lkg,c}C_D)^{1/2}$.

In addition, due to the center-tapped structure of the rectifier circuit, the voltage across D_{R1}, v_{DR1} is twice as v_{DR3}. Thus, v_{DR1} is obtained as follows:

$$v_{DR1}(t) = 2v_{DR3}(t) = 2\left(V_o + \left(\frac{V_{\text{in}}}{2n} - V_o\right)\cos(\omega_c t)\right). \tag{35}$$

The equivalent circuit at the secondary side of the proposed converter during mode 3 in Section II is shown in Fig. 11(b). During this period, the circulating current flows through D_{R3}.

The voltage across D_{R4}, v_{DR4}, is the sum of V_{o2} and the voltage across L_{o2}. Because the sum of the voltage across L_{o1} and L_{o2} is V_{o1}, the voltage across L_{o2} is $(V_{o1}/(n_c+1))$. Also, V_{o1} and V_{o2} can be obtained by using (9), and v_{DR4} is expressed as follows:

$$\begin{aligned} v_{DR4}(t) &= V_{o2} + \frac{V_{o1}}{n_c+1}\cos(\omega_c t) \\ &= \frac{1}{n_c}\left(\left(\frac{V_{\text{in}}}{2n} - V_o\right) + \left(V_o - \frac{V_{\text{in}}}{2n(n_c+1)}\right)\cos(\omega_c t)\right). \end{aligned} \tag{36}$$

According to (34)–(36), the maximum voltage across the rectifier diodes can be obtained when $\cos(\omega_c t)$ is 1. Similarly, the maximum voltage across the rectifier diodes of the conventional converters can be calculated. As a result, the voltage stress of the rectifier diodes comparing DHBC converter, converter in [26], and the proposed converter is shown in Table II.

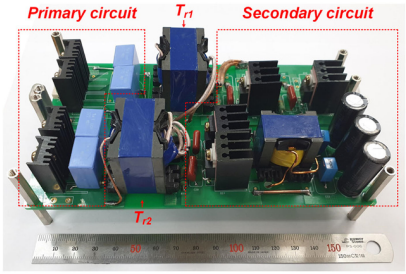

Fig. 13. Prototype of the proposed converter.

TABLE III
COMPONENT LIST OF THE PROTOTYPE CONVERTERS

	DHBC converter	Converter in [26]	Proposed converter
Primary switch (Q_1, Q_2, Q_3, Q_4) [volume, cost]	SPA12N50C3 ($V_{ds,max}$ = 500V, $I_{D,avg}$ = 11.6A) [680 mm^3 * 4, $2.23 * 4]		
Transformer (L_m, turns-ratio) [volume, cost]	PQ3230 (720 μH, 23:5:5) L_{lkg}=5.5 μH [12500 mm^3, $5.44]		PQ3230 (300 μH, 24:5:5) L_{lkg}=5.5 μH [12500 mm^3, $5.44]
Additional inductor (L_{r1}, L_{r2}) [volume, cost]	CM127125 (7.5 μH) [356 mm^3 * 2, $0.98 * 2]		-
Rectifier diode (D_{R1},D_{R2}) [volume, cost]	FFA60UP30DN (V_R=300 V, V_F=1.5 V) [680 mm^3 * 2, $1.88 * 2]	MBR40250TG (V_R=250 V, V_F=0.86 V) [680 mm^3 * 2, $1.72 * 2]	MBR20200CT (V_R=200 V, V_F=0.8 V) [680 mm^3 * 2, $0.98 * 2]
Rectifier diode (D_{R3}) [volume, cost]	-	MBR20200CT (V_R=200 V, V_F=0.8 A) [680 mm^3 * 2, $0.98 * 2]	MBR20H100CTG (V_R=100 V, V_F=0.77 V) [680 mm^3 * 2, $0.91 * 2]
Rectifier diode (D_{R4}) [volume, cost]			MBR20L60CTG (V_R=60 V, V_F=0.53 V) [680 mm^3 * 2, $0.9 * 2]
Output inductor (L_o, turns-ratio) [volume, cost]	PQ2620 (13 μH, 7 turn) [5470 mm^3, $2.99]		PQ2625 (13 μH, 7:5) [6530 mm^3, $3.19]
Output capacitor (C_o) [volume, cost]	Rubycon ZLH series (270 μF, 100 V) [1004 mm^3, $0.21]		Rubycon ZLH series (270 μF, 100 V) [1004 mm^3 * 3, $0.21 * 3]
Output capacitor (C_{o1}, C_{o2}) [volume, cost]	-		R82DC4100AA60J (1 μF, 63 V) [80 mm^3 * 2, $0.21 * 2]
Total volume	21726 mm^3	23086 mm^3	25602 mm^3
Total cost	$23.28	$24.92	$22.37

Fig. 12 shows the voltage stresses of the rectifier diodes according to the input voltages. Compared with the conventional converters, the proposed converter has lower voltage stresses. Thus, the proposed converter can use the rectifier diodes with smaller forward voltage drop, and the conduction loss of rectifier diodes is decreased.

IV. EXPERIMENTAL RESULTS

The proposed converter is implemented with 750-W DHBC TL converter with a Texas Instruments digital power controller TMS320F28069 to verify the performance. The design specifications are as followings: input voltage = 540–600 VDC, output voltage = 48 V, switching frequency = 100 kHz. The prototype of the proposed converter is shown in Fig. 13, and the detailed component list is presented in Table III.

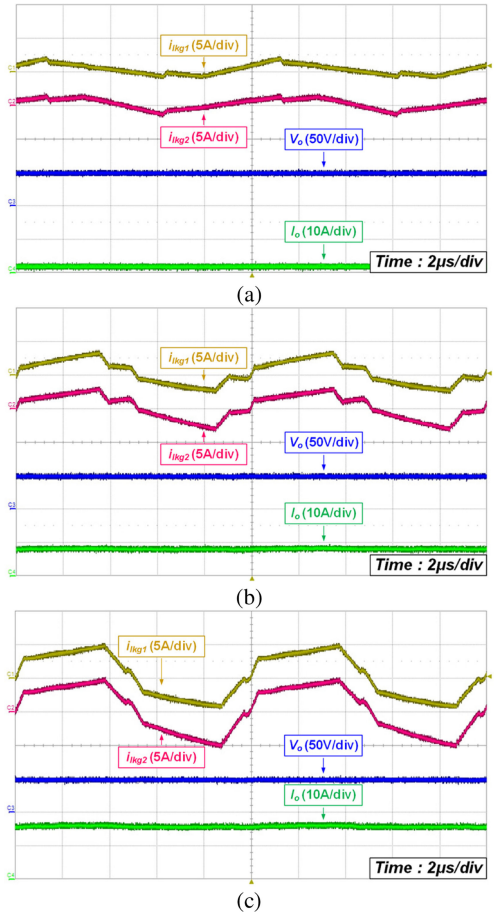

Fig. 14. Experimental waveforms of the proposed converter. (a) At 10% load condition. (b) At 50% load condition. (c) At 100% load condition.

Fig. 14 shows the experimental waveforms of the proposed converter. As load condition is increased, the duty ratio of the proposed converter is extended to regulate the output voltage. The proposed converter can regulate the output voltage under entire load conditions. Fig. 15 shows the experimental waveforms of DHBC converter, the converter in [26], and the proposed converter at the full-load condition. For the conventional converters, the leakage inductance is designed to achieve the ZVS operation of the lagging switches from 50% load condition to 100% load condition. Voltage across the rectifier diodes are clamped by RCD snubber circuit with 50% margin. For DHBC converter and the converter in [26], the circulating current remains, as shown in Fig. 15(a) and Fig. 15(b). However, for the proposed converter, the circulating current is reduced as shown in Fig. 15(c). In addition, the rectifier voltage stress of the proposed converter is smaller compared with the rectifier voltage stress of the conventional converters. Also, the voltage spike on D_{R3} and D_{R4} is very small due to small leakage inductance of the coupled inductor.

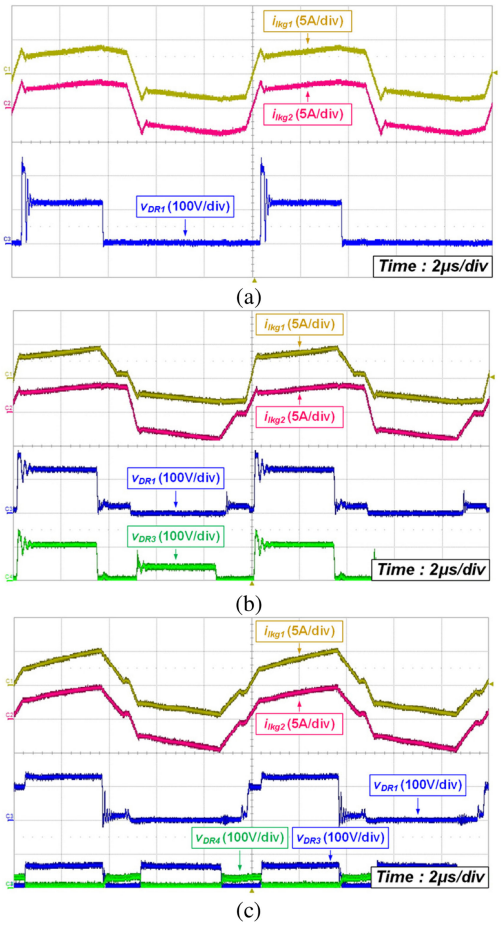

Fig. 15. Key waveforms at 100% load condition. (a) DHBC converter. (b) Converter in [26]. (c) Proposed converter.

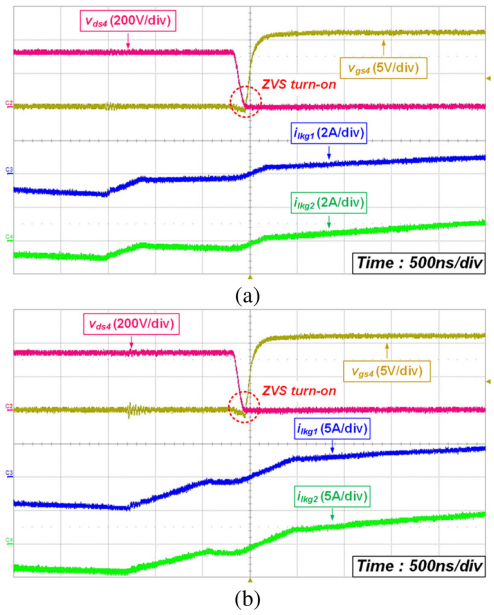

Fig. 16. ZVS waveforms at the lagging switch of the proposed converter. (a) Under 10% load condition. (b) Under 100% load condition.

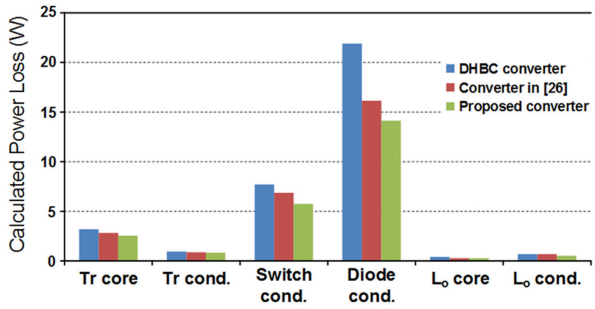

Fig. 17. Calculated power loss distribution at the full-load condition when $V_{\text{in}} = 600$ V.

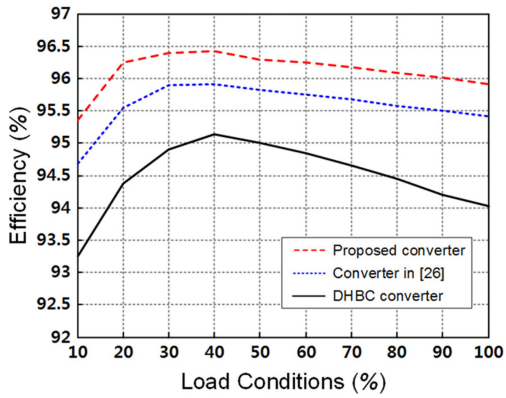

Fig. 18. Measured efficiency of the proposed converter, converter in [26], and DHBC converter.

Fig. 16 shows ZVS waveforms at the lagging switch Q_4 of the proposed converter. Because, for the proposed converter, the circulating current is the same with the magnetizing inductor current, the proposed converter has almost same ZVS energy regardless of the load conditions. The proposed converter can achieve the soft switching under entire load conditions.

Fig. 17 shows the calculated power loss distribution at the full-load condition when $V_{\text{in}} = 600$ V. Conduction loss of the primary switches is decreased in the proposed converter because of the reduced circulating current in the primary circuit. Also, the proposed converter can reduce the conduction loss of rectifier diodes due to employing the low-voltage-rating rectifier diodes.

Fig. 18 shows the measured efficiency of the proposed converter and conventional converters when $V_{\text{in}} = 600$ V. Due to the reduced circulating current in the primary circuit and small conduction loss in the rectifier diodes, the proposed converter can achieve higher efficiency compare with DHBC converter and the converter in [26]. Also, power density and hardware cost are an important factor to compare the converters. In Table III, the volume and cost of each component in the prototype converters are compared. Because the output inductor size is increased, and the additional output capacitors are added, the total volume of the proposed converter is a little bit increased. However, due to the low price of the rectifier diodes in the proposed converter, the total cost becomes the smallest. Although the power density of the proposed converter is smaller compared with the prototype converters, the efficiency is the highest, and hardware cost is the cheapest among the prototype converters.

V. Conclusion

This paper proposes high-efficiency DHBC TL dc–dc converter with reduced circulating current and rectifier voltage stress by using the coupled inductor in the rectifier circuit. Due to reduced circulating current, the rms current flowing through the primary switches is decreased. In addition, each rectifier diodes have small voltage stress, and it allows using diodes with low forward voltage drop. Consequently, the proposed converter is suitable for high input voltage applications requiring high efficiency.

Acknowledgment

The additional analysis and experimental results are included in a current version.

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