Control and Admittance Modeling of an AC/AC Modular Multilevel Converter for Railway Supplies

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***Abstract*—Modular multilevel converters (MMCs) can be configured to perform ac/ac conversion, which makes them suitable as railway power supplies. In this paper, a hierarchical control scheme for ac/ac MMCs for railway power supplies is devised and evaluated, considering the requirements and the operating conditions specific to this application. Furthermore, admittance models of the ac/ac MMC are developed, showing how the suggested hierarchical control scheme affects the three-phase and the single-phase side admittances of the converter. These models allow for analyzing the stability of the interconnected system using the impedance-based stability criterion and the passivity-based stability assessment. Finally, the findings presented in this paper are validated experimentally, using a down-scaled MMC.**

***Index Terms*—AC/AC converters, admittance, current control, frequency-domain analysis, linearization techniques, modular multilevel converters (MMCs), railway engineering, stability, voltage control.**

I. Introduction

MODULARITY, scalability, low power losses, and low harmonic distortion are several properties that make modular multilevel converters (MMCs) [1], [2] increasingly used in high-power applications, such as voltage source converter (VSC) based high-voltage dc systems, static synchronous compensators, and medium-voltage motor drives [3]–[6]. MMCs can be configured to perform ac/ac conversion, which makes them suitable as railway power supplies [7]–[10], especially in European countries with a low-frequency railway grid, e.g., Germany (16.7 Hz) and Sweden ($16\,^2/_3$ Hz). Compared with other VSCs for railway power supplies, the MMC is a particularly attractive solution because it can operate without the $16\,^2/_3$ Hz transformer and the 33-Hz filter, which are costly and bulky [7]. As stated in [8], the first MMC-based plant, consisting of two 37.5 MVA converters, was commissioned in 2011 in Nuremberg, Germany, while additional plants for Germany energy suppliers and the Swedish infrastructure company were planned.

As concluded in [9] and [10], MMCs will be the main future solution for ac railway power supplies. However, being a relatively recent and unconventional subject, the existing literature on ac/ac MMCs for railway power supplies and similar applications is somewhat scarce. The basic operation of the converter, comparing its direct (ac/ac) and indirect (ac/dc/ac) variants, are discussed in [7]. A control scheme based on capacitor voltage estimation is proposed in [11]. The converter operation focusing on wind turbine generation systems are analyzed in [12]. A study on how the energy variations can be reduced by an appropriate choice of voltage ratio is presented in [13]. The converter operation under asymmetric grid conditions are examined in [14]. The back-to-back operation of two ac/ac MMCs with a medium frequency link are analyzed in [15]. A modulation concept that minimizes the harmonic coupling between the two sides of the converter is presented in [16]. Different semiconductor technologies suitable for railway power supplies are compared in [17]. Overall, being scattered on a wide range of topics, the literature on ac/ac MMCs for railway power supplies is sparse and it offers a limited coverage of the subject. Related research topics on which recent studies have been presented are as follows. The control of the modular multilevel matrix converter, including capacitor voltage balancing, is presented in [18] and [19]. The control of the modular multilevel matrix converter under branch fault conditions is discussed in [20]. Capacitor voltage balancing strategies for MMC applications based on model predictive control are proposed in [21].

Differently from their ac/ac variant, the literature on ac/dc MMCs is extensive, as they have been widely studied in recent years. Notably, the two following subjects are particularly relevant and of significance.

1) A hierarchical control scheme is now a well established and mature solution [5], [22], which allows for a decoupled control of the ac-side, the dc-side, and the internal quantities. This scheme can be adapted to the ac/ac MMC for railway power supplies, resulting in a thorough design that improves the existing literature on control of ac/ac MMCs.
2) Admittance modeling of ac/dc MMCs is an increasingly studied subject [23]–[26], typically with focus on the

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three-phase side of the converter. These models allow for analyzing the stability of the interconnected system using the impedance-based stability criterion [27] and the passivity-based stability assessment [28]. So far, admittance models for ac/ac MMCs have not been investigated, meaning that an adaptation of the models proposed for ac/dc MMCs is a timely task. Moreover, this subject combines well with the design of the control system, which has a significant shaping effect on the converter admittances [26].

This paper aims to adapt the aforementioned concepts, originally proposed for the ac/dc configuration, to the ac/ac MMC for railway power supplies. Clearly, the adaptation is not straightforward due to the dc quantities being replaced by ac quantities, which has several implications on the operation of the converter. The studied application concerns several European countries, and Sweden is used as reference case [8], [9]. The novelty in this paper and its original contributions are summarized as follows.

1) A hierarchical control scheme for ac/ac MMCs for railway power supplies is devised and evaluated, considering the requirements and the operating conditions specific to this application. Particular care is devoted to designing the internal control, discussing its effects on steady-state harmonics, stability, and dynamic response.
2) Admittance models of the converter, both for the three-phase and the single-phase sides, are developed. These models are derived by adapting the method proposed in [26], [29] to the present application, adjusting the choice of frequency components and including the devised control scheme.

The paper is organized as follows. The system model and the control scheme are presented in Sections II and III, respectively, whereas the verification is made in Section V-A. The admittance models are derived in Section IV, with their experimental validation and discussion presented in Section V-B. Finally, Section VI summarizes this study and its conclusions.

II. System Model

In the Swedish railway power supplies, the converters act as an energy interface between the three-phase 50-Hz utility grid, with phase voltages given ideally as

$$e_a = e_1 \cos(\omega_1 t) \tag{1}$$

$$e_b = e_1 \cos\left(\omega_1 t - \frac{2}{3}\pi\right) \tag{2}$$

$$e_c = e_1 \cos\left(\omega_1 t - \frac{4}{3}\pi\right) \tag{3}$$

and the single-phase $16\,{}^{2}/_{3}$-Hz railway grid, with voltage

$$v_r = v_{1/3} \cos\left(\frac{\omega_1}{3} t + \psi\right) \tag{4}$$

which is tuned at strictly one-third of the utility fundamental frequency [8], [9]. Fig. 1 shows a typical interface point between the two grids, which features several converters operated in parallel [30]. Three main types of converters are used: 1) rotary converters, consisting of a 12-pole synchronous motor connected to a 4-pole synchronous generator through a common shaft; 2) cycloconverters, based on thyristors; and 3) VSCs, such as two-level VSCs and MMCs.

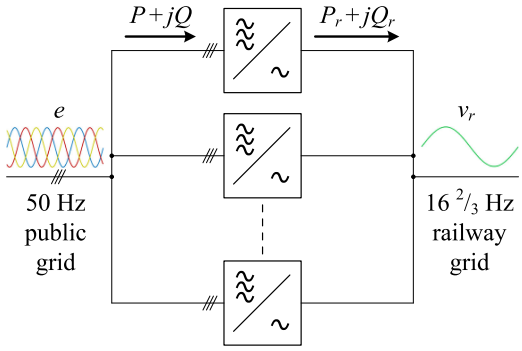

Fig. 1. Interface point between the three-phase grid and the Swedish railway grid, featuring several converters operated in parallel.

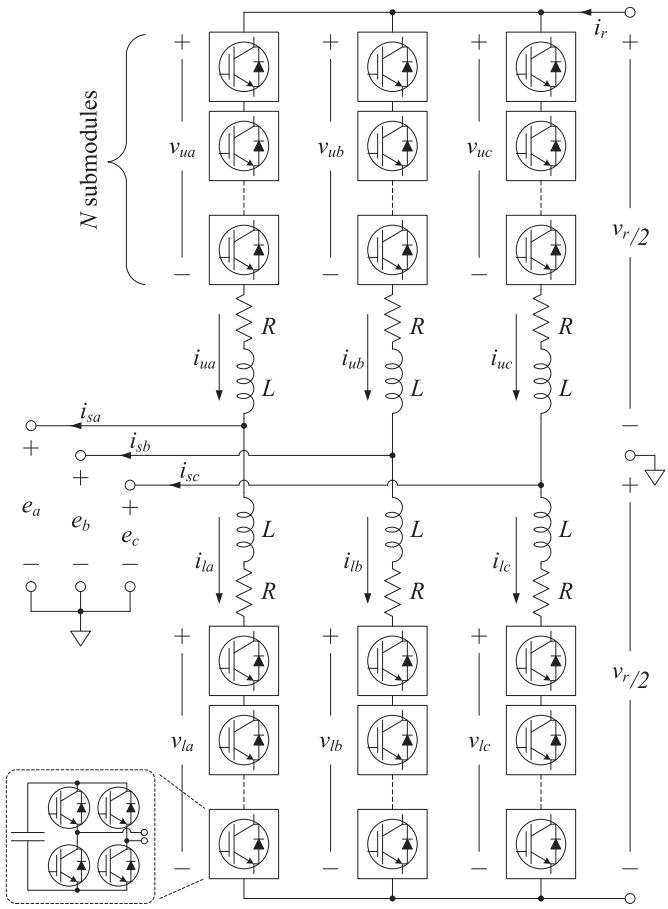

Fig. 2. Modular multilevel converter topology with full-bridge submodules.

A. Dynamic Model of the MMC

The MMC analyzed in this paper, shown in Fig. 2, performs a direct ac/ac conversion, i.e., without dc link, converting the three-phase voltage e into the single-phase voltage v_r. The MMC topology consists of three upper arms and three lower arms, each equipped with N submodules and an arm inductor L. Full-bridge submodules are used, which allow for inserting bipolar arm voltages, necessary for the direct ac/ac conversion. Moreover, a resistance R is included to account for the losses in the arm.

This study adopts the MMC time-averaged model [31], which neglects the switching operations, and assumes balanced submodule capacitances within the arm. The converter is modeled on a per-phase basis, dropping the subscript denoting the phase when not needed.

The arm-current dynamics are described using Kirchhoff's voltage law as follows:

$$L\frac{di_u}{dt} + Ri_u = \frac{v_r}{2} - v_u - e \tag{5}$$

$$L\frac{di_l}{dt} + Ri_l = \frac{v_r}{2} - v_l + e \tag{6}$$

where i_u is the upper-arm current, i_l is the lower-arm current, v_u is the upper-arm voltage, and v_l is the lower-arm voltage.

The arm voltages are obtained using time averaging, which allows for neglecting the switching operations, resulting in

$$v_{u,l} = n_{u,l} v^{\Sigma}_{Cu,l} \tag{7}$$

where $n_{u,l}$ are the insertion indices and $v^{\Sigma}_{Cu,l}$ are the sum capacitor voltages.

The sum capacitor voltages are obtained as described in [31], assuming balanced capacitor voltages and using time averaging, i.e.,

$$v^{\Sigma}_{Cu,l} = \frac{1}{C}\int n_{u,l} i_{u,l} dt + v^{\Sigma}_{C0} \tag{8}$$

where v^{Σ}_{C0} is the average sum capacitor voltage and C is the arm capacitance, defined as the submodule capacitance divided by N.

The insertion indices are the signals used for controlling the converter, obtained as final output of the control scheme, which is described in the following section. They are used for generating the converter switching signals, typically through nearest level modulation or phase-shifted carrier pulsewidth modulation [4], [5].

III. Control Scheme

The control scheme of the converter is divided into three parts: 1) three-phase side control; 2) single-phase side control; and 3) internal control. In order to enable the use of different controllers for the three-phase and single-phase sides, the following transformation of the arm currents is used [4], [31]:

$$i_s = i_u - i_l \qquad i_c = \frac{i_u + i_l}{2} \tag{9}$$

where i_s is the three-phase side current and i_c is the circulating current, which comprises one-third of the single-phase side current i_r. This transformation allows to rewrite (5) and (6) as

$$\frac{L}{2}\frac{di_s}{dt} + \frac{R}{2}i_s = v_s - e \quad \text{with} \quad v_s = \frac{-v_u + v_l}{2} \tag{10}$$

$$L\frac{di_c}{dt} + Ri_c = \frac{v_r}{2} - v_c \quad \text{with} \quad v_c = \frac{v_u + v_l}{2} \tag{11}$$

where v_s is the voltage driving i_s and v_c is the voltage driving i_c. The different parts of the control scheme of the converter are described in the following and are shown in Fig. 3.

A. Three-Phase Side Control

Since the converter is connected to the 50-Hz utility grid, which can be assumed strong, current control is a suitable choice for controlling the transferred power and the current dynamics. Synchronous-frame vector current control is a well established control scheme that is often applied to grid-connected inverters, including ac/dc MMCs [22]. This control scheme is a suitable choice for the present application and it operates as follows. The measured three-phase side voltage and current are transformed into the synchronous frame (i.e., the dq frame) and used in the controller, shown in Fig. 3(a), which consists of: 1) a proportional controller, which sets the closed-loop-system bandwidth to α_s; 2) an integral controller, for accurate tracking of the three-phase side current references $i^{\star}_{sd}$ and $i^{\star}_{sq}$; 3) a feedforward of the dq components of the three-phase side voltage; and 4) a decoupling term, i.e.,

$$v^{\star}_{sd} = F_{dq}(s)(i^{\star}_{sd} - i_{sd}) + H_{dq}(s)e_d - \omega_1 \frac{L}{2} i_{sq} \tag{12}$$

$$v^{\star}_{sq} = F_{dq}(s)(i^{\star}_{sq} - i_{sq}) + H_{dq}(s)e_q + \omega_1 \frac{L}{2} i_{sd} \tag{13}$$

where $s = d/dt$, $F_{dq}(s)$ is the proportional–integral controller

$$F_{dq}(s) = \alpha_s \frac{L}{2}\left(1 + \frac{2\alpha_1}{s}\right) \tag{14}$$

and $H_{dq}(s)$ is a low-pass filter with bandwidth α_f

$$H_{dq}(s) = \frac{\alpha_f}{s + \alpha_f}. \tag{15}$$

The current references $i^{\star}_{sd}$ and $i^{\star}_{sq}$ are set from the active- and reactive-power references $P^{\star}$ and $Q^{\star}$ as

$$i^{\star}_{sd} = -\frac{2P^{\star}}{3e_1} \qquad i^{\star}_{sq} = \frac{2Q^{\star}}{3e_1} \tag{16}$$

where $P^{\star}$ and $Q^{\star}$ are provided by the transmission system operator and e_1 is assumed known. After (12)–(13), the voltage references $v^{\star}_{sd}$ and $v^{\star}_{sq}$ are reverted into stationary coordinates, obtaining $v^{\star}_s$ for each phase, which are used for calculating the insertion indices.

The synchronization with the three-phase grid is achieved using a phase-locked loop (PLL), which outputs an estimate $\hat{\vartheta}(t)$ of the three-phase side voltage angle $\vartheta(t)$. The PLL, shown in Fig. 3(b), consists of a feedback loop built around an abc/dq transformation of e, which drives e_q to zero as $\hat{\vartheta}(t)$ tracks $\vartheta(t)$. The PLL feedback loop includes: 1) a second-order Butterworth low-pass filter

$$H_{\mathrm{lp}}(s) = \frac{\alpha^2_{\mathrm{lp}}}{s^2 + \sqrt{2}\alpha_{\mathrm{lp}} s + \alpha^2_{\mathrm{lp}}} \tag{17}$$

with bandwidth α_{lp}; 2) a proportional controller, which sets the closed-loop-system bandwidth to α_p; 3) a feedforward of the nominal fundamental angular frequency ω_1; and 4) an integrator.

B. Single-Phase Side Control

The frequency of the single-phase side voltage is strictly one-third of the fundamental frequency, as defined in (4). On the

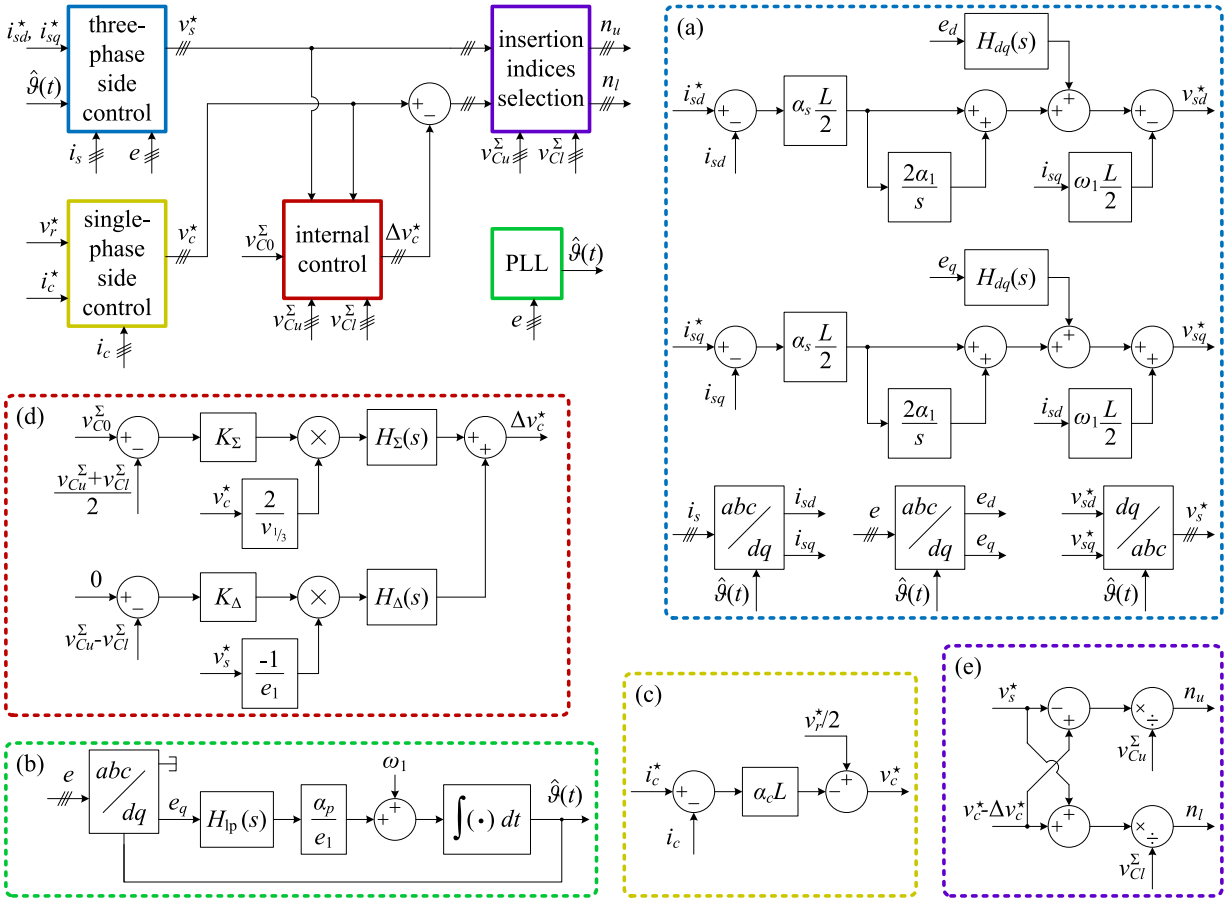

Fig. 3. Block diagram of the MMC control scheme. (a) Three-phase side control. (b) PLL. (c) Single-phase side control. (d) Internal control. (e) Insertion indices selection. For the block diagrams (c), (d), and (e), only one phase is shown.

other hand, the voltage amplitude $v_{1/3}$ and the phase shift ψ represent two degrees of freedom which are used for operating the parallel-connected converters in synergy, as shown in Fig. 1. The voltage amplitude $v_{1/3}$ is set as a function of the reactive power using a droop controller [9], while the phase shift ψ is used to emulate the behavior of the rotary converters, where ψ is a function of the active power [30]. In this paper, $v_{1/3}$ and ψ are kept constant for simplicity, omitting the dependence on active and reactive power, which are relevant when studying the parallel operation of several converters.

In order to operate the parallel-connected converters in synergy, the single-phase side controller is designed for providing a stiff voltage in a grid-forming fashion. In addition, the controller can improve the circulating current dynamic response by including a proportional current controller, as shown in Fig. 3(c), which sets the closed-loop-system bandwidth to α_c, i.e.,

$$v_c^\star = \frac{v_r^\star}{2} - \alpha_c L(i_c^\star - i_c) \tag{18}$$

where $v_r^\star$ and $i_c^\star$ are the single-phase side voltage reference and the circulating current reference, respectively, which are set as

$$v_r^\star = v_{1/3}\cos\left[\frac{\hat{\vartheta}(t)}{3} + \psi\right] \tag{19}$$

$$i_c^\star = \frac{2|S_r^\star|}{3v_{1/3}}\cos\left[\frac{\hat{\vartheta}(t)}{3} + \psi - \angle(-S_r^\star)\right] \tag{20}$$

where $S_r^\star = P_r^\star + jQ_r^\star$ is the single-phase side complex power reference, provided by the transmission system operator. The parameter α_c can be set to increase the damping of the circulating current dynamics from R/L to $\alpha_c + R/L$. However, excessively high values of α_c should be avoided, as that would cause the single-phase side to be current stiff, rather than voltage stiff, hindering the synergetic operation of the parallel-connected converters (cf. Fig. 1). For the same reason, the circulating current controller does not include a resonant part, meaning that a steady-state error in i_c is allowed.

The circulating current reference (20) is obtained expressing the complex power reference using the definitions of Figs. 1 and 2, i.e.,

$$S_r^\star = -\frac{V_r^\star \overline{I_r^\star}}{2} \quad \text{with } V_r^\star = v_{1/3}e^{j\psi} \tag{21}$$

where $V_r^\star$ and $I_r^\star$ are the phasors of $v_r^\star$ and $i_r^\star$, respectively, and the overline denotes the complex conjugate of the phasor. Since $i_r^\star$ splits equally among the three phases, the phasor of $i_c^\star$ results

$$I_c^\star = \frac{I_r^\star}{3} = \frac{2\overline{(-S_r^\star)}}{3\overline{V_r^\star}} = \frac{2|S_r^\star|}{3v_{1/3}}e^{j[\psi - \angle(-S_r^\star)]}. \tag{22}$$

It can be observed that the proposed controller does not require the actual value of the single-phase voltage v_r, since neither a single-phase PLL, nor a voltage controller, nor a feedforward of v_r are used in (18). This is a useful feature, which makes the controller immune to disturbances in v_r and improves the passivity properties of the single-phase side admittance [28], [32].

C. Internal Control

The last step in the control scheme is the computation of the insertion indices, which are obtained by normalizing the voltage references $v_s^\star$ and $v_c^\star$ with respect to the sum capacitor voltage. Two solutions are typically used [22]: an open-loop scheme, where the constant reference value v_{C0}^Σ is used in the division; and a closed-loop scheme, where the measured sum capacitor voltages are used instead.

The open-loop scheme inherently gives asymptotically stable sum capacitor voltages, meaning that an arm-balancing controller is not required. However, since the capacitor voltage ripple is not taken into account during the computation of the insertion indices, the multiplication in (7) produces undesired harmonics in the arm voltages. This effect propagates to the arm currents, which are proportional to the arm voltages via the arm impedance as shown in (5) and (6). Even though this phenomenon is acceptable in ac/dc MMCs, where the second-order harmonic in the arm currents is suppressed [22], it becomes particularly pronounced in the present application. The $16\,^2/_3$ and the 50-Hz components of $n_{u,l}$ and $i_{u,l}$ multiply in (8), generating frequency components in $v_{Cu,l}^\Sigma$ at $33\,^1/_3$, $66\,^2/_3$, and 100 Hz. These components produce numerous undesired harmonics in the arm currents that are difficult to suppress effectively. Therefore, using the open-loop scheme is not recommended for this application.

The closed-loop scheme computes ideal insertion indices, which generate arm voltages that match their references, except for the control system time delay. However, this also produces marginally stable sum capacitor voltages, meaning that an arm-balancing controller is required for controlling the average and the imbalance sum capacitor voltages, defined as

$$v_C^\Sigma = \frac{v_{Cu}^\Sigma + v_{Cl}^\Sigma}{2} \qquad v_C^\Delta = v_{Cu}^\Sigma - v_{Cl}^\Sigma \tag{23}$$

to v_{C0}^Σ and 0, respectively. Hence, an arm-balancing controller suitable for the present application is devised.

The first part of the controller drives a $16\,^2/_3$ Hz term in i_c, which is in phase with n_u and n_l. This term multiplies the $16\,^2/_3$ Hz component of n_u and n_l in (8), resulting in a dc term in the sum capacitor voltages that controls v_C^Σ. Similarly, the second part of the controller drives a 50-Hz term in i_c, which is in phase with n_u and in antiphase with n_l. This term multiplies the 50-Hz component of n_u and n_l in (8), resulting in a dc term in the sum capacitor voltages that controls v_C^Δ. The arm-balancing controller, shown in Fig. 3(d), produces the voltage reference

$$\Delta v_c^\star = K_\Sigma (v_{C0}^\Sigma - v_C^\Sigma)\frac{2v_c^\star}{v_{1/3}} H_\Sigma(s) - K_\Delta v_C^\Delta \left(-\frac{v_s^\star}{e_1^\star}\right) H_\Delta(s) \tag{24}$$

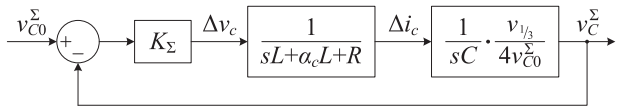

Fig. 4. Block diagram used for calculating the approximated closed-loop-system transfer function of the average capacitor voltage.

where K_Σ and K_Δ are proportional gains, $2v_c^\star/v_{1/3}$ produces a $16\,^2/_3$-Hz component in phase with n_u, $-v_s^\star/e_1^\star$ produces a 50-Hz component in phase with n_u, and $H_\Sigma(s)$ and $H_\Delta(s)$ are band-pass filters

$$H_\Sigma(s) = \frac{\alpha_\Sigma s}{s^2 + \alpha_\Sigma s + (\frac{\omega_1}{3})^2} \qquad H_\Delta(s) = \frac{\alpha_\Delta s}{s^2 + \alpha_\Delta s + \omega_1^2} \tag{25}$$

with bandwidths α_Σ and α_Δ, and centered at $\omega_1/3$ and ω_1, respectively. Finally, the insertion indices are computed as

$$n_u = \frac{v_c^\star - \Delta v_c^\star - v_s^\star}{v_{Cu}^\Sigma} \qquad n_l = \frac{v_c^\star - \Delta v_c^\star + v_s^\star}{v_{Cl}^\Sigma}. \tag{26}$$

The proposed arm-balancing controller presents a drawback. Since $\Delta v_c^\star$ is obtained using $v_{Cu,l}^\Sigma$, the capacitor voltage ripple tends to introduce undesired harmonics in i_c through $\Delta v_c^\star$. This effect is mitigated using the band-pass filters $H_\Sigma(s)$ and $H_\Delta(s)$; however, these filters also impact the dynamic performance of the controller, causing a malfunction if the filter bandwidths are excessively low. Ultimately, the undesired harmonics in i_c cannot be entirely removed when this control scheme is used. Further discussion about the spectra of i_s and i_c is presented in Section V-A.

An approximated closed-loop-system transfer function of the average capacitor voltage is obtained from the block diagram shown in Fig. 4, which is composed as follows. The arm-balancing controller is represented by the block K_Σ. The voltage Δv_c drives the current Δi_c through a transfer function that embeds the current controller (18) into the dynamic law (11). The current Δi_c controls v_C^Σ via (8), where $v_{1/3}/(2v_{C0}^\Sigma)$ is the approximated steady-state value of n_u. Moreover, since the dc term controlling v_C^Σ results from the multiplication of two $16\,^2/_3$ Hz terms, a factor $1/2$ is added. The following are the closed-loop-system transfer function results:

$$\frac{v_C^\Sigma}{v_{C0}^\Sigma} = \frac{\omega_\Sigma^2}{s^2 + s(\alpha_c + \frac{R}{L}) + \omega_\Sigma^2} \qquad \text{with } \omega_\Sigma^2 = \frac{K_\Sigma v_{1/3}}{4v_{C0}^\Sigma LC}. \tag{27}$$

The devised control scheme is compared with the solution proposed in [14], which is the only reference presenting a complete control scheme for ac/ac MMCs for railway power supplies. In the present paper, the sum capacitor voltages and the circulating currents are controlled independently via $\Delta v_c^\star$ and $v_c^\star$, respectively. Instead, in [14] the arm balancing controller modifies the circulating current reference $i_c^\star$ including additional ac components for capacitor voltage balancing. This method heavily relies on an effective filtering of the sum capacitor voltages, because any undesired component that appears in $i_c^\star$ is amplified by the circulating current controller, which drives i_c to match its reference. This could explain why the measurements

presented in [14] show distorted current waveforms. Hence, the control scheme devised in this paper is preferable.

IV. Admittance Modeling

Power converters can be modeled in the frequency domain as an admittance, which allows for using the impedance-based stability criterion [27] for assessing the stability of the interconnected system, formed by a power converter connected to a grid. Then, this stability analysis can be used for evaluating the design of the control system, which has a significant shaping effect on the converter admittances [26].

The three-phase side admittance of the studied MMC is calculated by superimposing a small-signal perturbation on the 50-Hz grid voltage

$$e = e_1\cos(\omega_1 t) + e_p\cos(\omega_p t) \qquad E(f_p) \ll E(f_1) \tag{28}$$

where $E(f_1) = e_1/2$ denotes the Fourier coefficient of e at f_1. Then, the admittance is obtained as the ratio between the current response to the applied voltage perturbation, i.e.,

$$Y_{3\mathrm{ph}}(f_p) = -\frac{I_s(f_p)}{E(f_p)}. \tag{29}$$

Similarly, the single-phase side admittance of the converter is calculated by superimposing a small-signal perturbation on the $16\,^2/_3$ Hz grid voltage, leading to

$$Y_{1\mathrm{ph}}(f_p) = \frac{I_r(f_p)}{V_r(f_p)} = \frac{3I_c(f_p)}{V_r(f_p)} \tag{30}$$

which assumes $I_r(f_p) = 3I_c(f_p)$.

A. Three-Phase Side Admittance

As discussed in Section III-C, the closed-loop scheme computes ideal insertion indices, producing

$$v_s = v_s^\star e^{-sT_d} \tag{31}$$

where T_d is the time delay of the control system. Equation (31) links $v_s^\star$ to i_s through (10), meaning that neither the sum capacitor voltages nor the single-phase side quantities appear in the admittance calculation. Effectively, the admittance of the ac/ac MMC coincides with the admittance of an ac/dc MMC with analogous settings [26], and also with the admittance of a two-level VSC [33], with a VSC phase inductance of $L/2$. Therefore, the findings presented in [26] can be extended to the present study, i.e.,

$$Y_{3\mathrm{ph}}(f_p) = \frac{1 + \left(H_{\mathrm{PLL}} - H_{dq}[j(\omega_p - \omega_1)]\right)e^{-j\omega_p T_d}}{\frac{j\omega_p L + R}{2} + \left(F_{dq}[j(\omega_p - \omega_1)] - \frac{j\omega_1 L}{2}\right)e^{-j\omega_p T_d}} \tag{32}$$

where H_{PLL} groups the effects of the PLL on the admittance (see the Appendix).

B. Single-Phase Side Admittance

The closed-loop scheme produces a voltage v_c that matches its reference, i.e.,

$$v_c = (v_c^\star - \Delta v_c^\star)e^{-sT_d} \tag{33}$$

TABLE I
Analyzed Frequency Components

Variable	Steady-State	Perturbation
i_u, v_u, n_u	$f_1/3$	$f_p - 2f_1$
	f_1	$f_p - 2f_1/3$
		f_p
v_{Cu}^Σ	0	$f_p - f_1$
		$f_p - f_1/3$
		$f_p + f_1/3$
		$f_p + f_1$

which links $v_c^\star$ and $\Delta v_c^\star$ to i_c through (11). However, $\Delta v_c^\star$ is a function of the sum capacitor voltages, which complicates the calculation of the single-phase side admittance.

The authors of the present paper have developed in [26], [29] a method for calculating the admittance of an MMC, obtaining a linear model by analyzing the main perturbation frequency components of the converter variables individually. This method can be adapted to the present application by adjusting the choice of frequency components and by including the employed arm-balancing controller. This results in an accurate admittance model.

In the derivation of $Y_{1\mathrm{ph}}$, the converter variables are analyzed at specific frequency components, listed in Table I, which are selected as the minimum amount necessary to achieve an accurate result.

1) Steady-State Components: Approximated solutions are used for simplicity, as they do not compromise the accuracy of the final result

$$I_u(\tfrac{f_1}{3}) = I_c^\star(\tfrac{f_1}{3}) \quad I_u(f_1) = \frac{i_{sd}^\star + j i_{sq}^\star}{4} \tag{34}$$

$$V_u^\star(\tfrac{f_1}{3}) = \frac{V_r^\star(\frac{f_1}{3})}{2} \quad V_u^\star(f_1) = -E(f_1) \tag{35}$$

$$N_u(\tfrac{f_1}{3}) = \frac{V_u^\star(\frac{f_1}{3})}{v_{C0}^\Sigma} \quad N_u(f_1) = \frac{V_u^\star(f_1)}{v_{C0}^\Sigma} \tag{36}$$

$$V_{Cu}^\Sigma(0) = v_{C0}^\Sigma. \tag{37}$$

2) Upper-Arm Current: The Kirchhoff's voltage law (5) is evaluated at the desired frequencies as

$$I_u(f_p - 2f_1) = -\frac{V_u(f_p - 2f_1)}{j(\omega_p - 2\omega_1)L + R} \tag{38}$$

$$I_u(f_p - 2\tfrac{f_1}{3}) = -\frac{V_u(f_p - 2\frac{f_1}{3})}{j(\omega_p - 2\frac{\omega_1}{3})L + R} \tag{39}$$

$$I_u(f_p) = -\frac{V_u(f_p)}{j\omega_p L + R} + \frac{V_r(f_p)}{2(j\omega_p L + R)}. \tag{40}$$

3) Upper-Arm Insertion Index: Equation (26) shows that n_u is a function of i_u through $v_c^\star$ and a function of v_{Cu}^Σ through $\Delta v_c^\star$. Due to the symmetries of the MMC topology, $v_{Cu}^\Sigma = v_{Cl}^\Sigma$ for $f = f_p \pm \frac{f_1}{3}$, while $v_{Cu}^\Sigma = -v_{Cl}^\Sigma$ for $f = f_p \pm f_1$. The frequency shift terms in (24) are approximated to ideal cosine waves at steady-state frequencies, in phase with e and $v_r^\star$, respectively.

The division by v_{Cu}^{Σ} in (26) is linearized as

$$\frac{1}{v_{Cu}^{\Sigma}} \simeq \frac{1}{v_{C0}^{\Sigma}} - \frac{v_{Cu}^{\Sigma}}{(v_{C0}^{\Sigma})^2}. \tag{41}$$

Including the effects of the control system time delay, the perturbation frequency components of n_u result

$$\begin{aligned} N_u(f_p-2f_1) = e^{-j(\omega_p-2\omega_1)T_d}\Bigg[&\frac{\alpha_c L}{v_{C0}^{\Sigma}} I_u(f_p-2f_1) \\ &- \frac{K_\Delta H_\Delta[j(\omega_p-2\omega_1)]}{v_{C0}^{\Sigma}} V_{Cu}^{\Sigma}(f_p-f_1) \\ &- \frac{\overline{V_u^{\star}(f_1)}}{(v_{C0}^{\Sigma})^2} V_{Cu}^{\Sigma}(f_p-f_1)\Bigg] \end{aligned} \tag{42}$$

$$\begin{aligned} N_u(f_p-2\tfrac{f_1}{3}) = e^{-j(\omega_p-2\frac{\omega_1}{3})T_d}\Bigg[&\frac{\alpha_c L}{v_{C0}^{\Sigma}} I_u(f_p-2\tfrac{f_1}{3}) \\ &+ \frac{K_\Sigma H_\Sigma[j(\omega_p-2\frac{\omega_1}{3})]}{v_{C0}^{\Sigma}} \frac{\overline{V_r^{\star}(\frac{f_1}{3})}}{v_{1/3}} V_{Cu}^{\Sigma}(f_p-\tfrac{f_1}{3}) \\ &- \frac{V_u^{\star}(\frac{f_1}{3})}{(v_{C0}^{\Sigma})^2} V_{Cu}^{\Sigma}(f_p-f_1) \\ &- \frac{\overline{V_u^{\star}(f_1)}}{(v_{C0}^{\Sigma})^2} V_{Cu}^{\Sigma}(f_p+\tfrac{f_1}{3})\Bigg] \end{aligned} \tag{43}$$

$$\begin{aligned} N_u(f_p) = e^{-j\omega_p T_d}\Bigg[&\frac{\alpha_c L}{v_{C0}^{\Sigma}} I_u(f_p) \\ &- \frac{K_\Delta H_\Delta(j\omega_p)}{v_{C0}^{\Sigma}} V_{Cu}^{\Sigma}(f_p-f_1) \\ &+ \frac{K_\Sigma H_\Sigma(j\omega_p)}{v_{C0}^{\Sigma}} \frac{V_r^{\star}(\frac{f_1}{3})}{v_{1/3}} V_{Cu}^{\Sigma}(f_p-\tfrac{f_1}{3}) \\ &+ \frac{K_\Sigma H_\Sigma(j\omega_p)}{v_{C0}^{\Sigma}} \frac{\overline{V_r^{\star}(\frac{f_1}{3})}}{v_{1/3}} V_{Cu}^{\Sigma}(f_p+\tfrac{f_1}{3}) \\ &- \frac{K_\Delta H_\Delta(j\omega_p)}{v_{C0}^{\Sigma}} V_{Cu}^{\Sigma}(f_p+f_1) \\ &- \frac{V_u^{\star}(f_1)}{(v_{C0}^{\Sigma})^2} V_{Cu}^{\Sigma}(f_p-f_1) - \frac{V_u^{\star}(\frac{f_1}{3})}{(v_{C0}^{\Sigma})^2} V_{Cu}^{\Sigma}(f_p-\tfrac{f_1}{3}) \\ &- \frac{\overline{V_u^{\star}(\frac{f_1}{3})}}{(v_{C0}^{\Sigma})^2} V_{Cu}^{\Sigma}(f_p+\tfrac{f_1}{3}) \\ &- \frac{\overline{V_u^{\star}(f_1)}}{(v_{C0}^{\Sigma})^2} V_{Cu}^{\Sigma}(f_p+f_1)\Bigg]. \end{aligned} \tag{44}$$

4) Upper-Arm Voltage: The multiplication in (7) combines the frequency components of n_u and v_{Cu}^{Σ} through addition and subtraction, generating

$$V_u(f_p-2f_1) = V_{Cu}^{\Sigma}(0)N_u(f_p-2f_1) + \overline{N_u(f_1)}V_{Cu}^{\Sigma}(f_p-f_1) \tag{45}$$

$$\begin{aligned} V_u(f_p-2\tfrac{f_1}{3}) = &V_{Cu}^{\Sigma}(0)N_u(f_p-2\tfrac{f_1}{3}) + N_u(\tfrac{f_1}{3})V_{Cu}^{\Sigma}(f_p-f_1) \\ &+ \overline{N_u(\tfrac{f_1}{3})}V_{Cu}^{\Sigma}(f_p-\tfrac{f_1}{3}) \\ &+ \overline{N_u(f_1)}V_{Cu}^{\Sigma}(f_p+\tfrac{f_1}{3}) \end{aligned} \tag{46}$$

$$\begin{aligned} V_u(f_p) = &V_{Cu}^{\Sigma}(0)N_u(f_p) + N_u(f_1)V_{Cu}^{\Sigma}(f_p-f_1) \\ &+ N_u(\tfrac{f_1}{3})V_{Cu}^{\Sigma}(f_p-\tfrac{f_1}{3}) \\ &+ \overline{N_u(\tfrac{f_1}{3})}V_{Cu}^{\Sigma}(f_p+\tfrac{f_1}{3}) \\ &+ \overline{N_u(f_1)}V_{Cu}^{\Sigma}(f_p+f_1) \end{aligned} \tag{47}$$

where the overline denotes the complex conjugate of the Fourier coefficient.

5) Upper-Arm Sum Capacitor Voltage: The multiplication in (8) combines the frequency components of n_u and i_u through addition and subtraction, generating

$$\begin{aligned} V_{Cu}^{\Sigma}(f_p-f_1) = \frac{1}{j(\omega_p-\omega_1)C}\Big[&N_u(f_1)I_u(f_p-2f_1) \\ &+ \overline{N_u(\tfrac{f_1}{3})}I_u(f_p-2\tfrac{f_1}{3}) + \overline{N_u(f_1)}I_u(f_p) \\ &+ I_u(f_1)N_u(f_p-2f_1) + \overline{I_u(\tfrac{f_1}{3})}N_u(f_p-2\tfrac{f_1}{3}) \\ &+ \overline{I_u(f_1)}N_u(f_p)\Big] \end{aligned} \tag{48}$$

$$\begin{aligned} V_{Cu}^{\Sigma}(f_p-\tfrac{f_1}{3}) = \frac{1}{j(\omega_p-\frac{\omega_1}{3})C}\Big[&N_u(\tfrac{f_1}{3})I_u(f_p-2\tfrac{f_1}{3}) \\ &+ \overline{N_u(\tfrac{f_1}{3})}I_u(f_p) + I_u(\tfrac{f_1}{3})N_u(f_p-2\tfrac{f_1}{3}) \\ &+ \overline{I_u(\tfrac{f_1}{3})}N_u(f_p)\Big] \end{aligned} \tag{49}$$

$$\begin{aligned} V_{Cu}^{\Sigma}(f_p+\tfrac{f_1}{3}) = \frac{1}{j(\omega_p+\frac{\omega_1}{3})C}\Big[&N_u(f_1)I_u(f_p-2\tfrac{f_1}{3}) \\ &+ N_u(\tfrac{f_1}{3})I_u(f_p) + I_u(f_1)N_u(f_p-2\tfrac{f_1}{3}) \\ &+ I_u(\tfrac{f_1}{3})N_u(f_p)\Big] \end{aligned} \tag{50}$$

$$\begin{aligned} V_{Cu}^{\Sigma}(f_p+f_1) = \frac{1}{j(\omega_p+\omega_1)C}\Big[&N_u(f_1)I_u(f_p) \\ &+ I_u(f_1)N_u(f_p)\Big] \end{aligned} \tag{51}$$

6) Solution: The expressions (38)–(51) are used to build a linear system with 13 equations and 13 unknown variables of the form

$$A\mathbf{x} = B \tag{52}$$

where the matrix A contains the coefficients of the linear system, the vector B contains the constant terms, and the vector $\mathbf{x}$ contains the system variables

$$\begin{aligned} \mathbf{x} = \big[&I_u(f_p-2f_1), I_u(f_p-2\tfrac{f_1}{3}), I_u(f_p), \\ &N_u(f_p-2f_1), N_u(f_p-2\tfrac{f_1}{3}), N_u(f_p), \\ &V_u(f_p-2f_1), V_u(f_p-2\tfrac{f_1}{3}), V_u(f_p), \\ &V_{Cu}^{\Sigma}(f_p-f_1), V_{Cu}^{\Sigma}(f_p-\tfrac{f_1}{3}), \\ &V_{Cu}^{\Sigma}(f_p+\tfrac{f_1}{3}), V_{Cu}^{\Sigma}(f_p+f_1)\big]^T. \end{aligned} \tag{53}$$

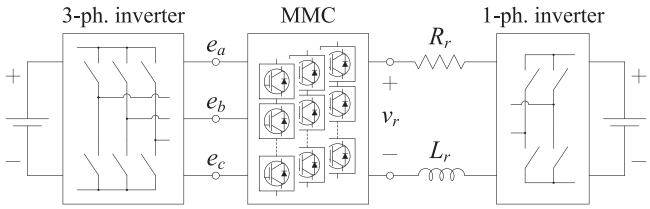

Fig. 5. Configuration of the experimental setup.

This linear system is solved, for instance, in MATLAB using the operation "x = A\B". Finally, the single-phase side admittance is obtained using (30), with $I_c(f_p) = I_u(f_p)$, due to the symmetries of the MMC topology.

7) Simplified Expression: A simplified expression of the single-phase side admittance can be obtained by neglecting $\Delta v_c^\star$ in (33), which allows to substitute (18) into (11), leading to

$$\hat{Y}_{1\text{ph}}(f_p) = \frac{3}{2(j\omega_p L + R + \alpha_c L e^{-j\omega_p T_d})}. \tag{54}$$

Although this expression is not correct in the whole frequency range, it serves as a useful approximation of the aforementioned accurate model.

The control system time delay affects the admittance only when the angle $\omega_p T_d$ becomes noticeable, e.g., $\omega_p > \omega_d$, with $\omega_d = \pi/(10T_d)$. If $\alpha_c < \omega_d$, then the term $j\omega_p L$ becomes the dominant term in the denominator of (54) for $\omega_p > \omega_d$, meaning that the control system time delay has a little impact on the admittance.

V. Verification and Discussion

The control scheme presented in Section III and the admittance models derived in Section IV are tested and validated through experiments, using a down-scaled MMC prototype. The experimental setup, shown in Fig. 5, consists of: 1) a three-phase inverter, which produces a 50-Hz voltage and, if needed, a small-signal perturbation; 2) a down-scaled MMC with five full-bridge submodules per arm, shown in Fig. 6 and described in detail in [34]; 3) a resistive-inductive load, connected to the single-phase terminals of the MMC; and 4) a single-phase inverter, which produces, if needed, a small-signal perturbation at the single-phase side of the converter. The parameters of the experimental setup are given in Table II. The values of L and C are selected as described in [22], i.e., the arm inductance limits the switching-frequency component of the arm currents, whereas the arm capacitance limits the sum capacitor voltage ripple. Table III shows the parameter values used in the experiments in relation to their full-scale values. It can be observed that the scaling is consistent, meaning that in per unit (p.u.) the experimental setup and a full-scale converter have the same parameter values.

A. Performance of the Control Scheme

The down-scaled MMC is controlled using a Xilinx Zynq-7000 system-on-chip, which integrates programmable logics with a processing system. The control scheme presented in Section III is implemented in the processing system, which operates in discrete-time steps. Therefore, the continuous-time transfer functions are discretized, using the prewarped Tustin method for the second-order transfer functions [35], and the backward Euler method for the first-order transfer functions.

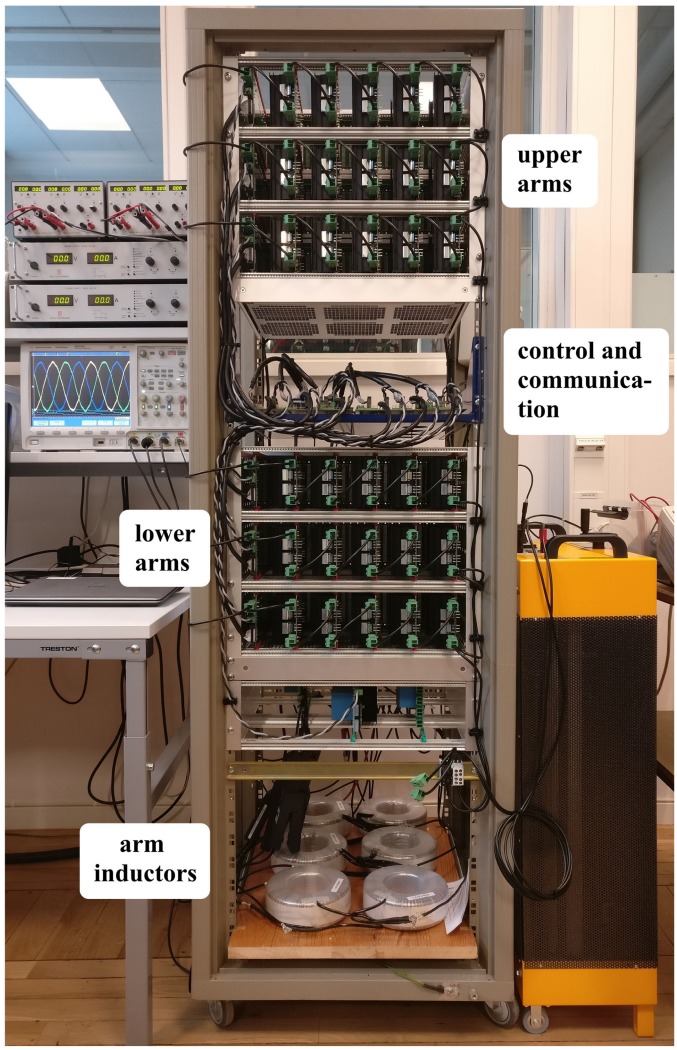

Fig. 6. Photograph of the down-scaled MMC prototype.

TABLE II
Parameters of the Experimental Setup

PCC voltage amplitude	e_1	48 V
Fundamental frequency	f_1	50 Hz
Arm inductance	L	5.7 mH
Arm resistance	R	0.55 Ω
Arm capacitance	C	0.54 mF
Submodules per arm	N	5
Load inductance	L_r	72.5 mH
Load resistance	R_r	11.3 Ω
Perturbation amplitude	e_p, v_p	0.8 V
Perturbation frequency	f_p	1.67 Hz – 1 kHz

TABLE III
PARAMETERS SCALING

Parameter	Symbol	Experiment	Full scale
PCC voltage amplitude	e_1	48 V	$15\sqrt{2/3}$ kV
Sum capacitor voltage	v_{C0}^{Σ}	98 V	25 kV
Single-ph. voltage amplitude	$v_{1/3}$	91.5 V	$16.5\sqrt{2}$ kV
Complex power amplitude	$\|S\|$	307 VA	20 MVA
Load impedance amplitude	$\|Z_r\|$	13.6 Ω	13.6 Ω

TABLE IV
SETTINGS OF THE MMC CONTROLLER

Three-ph. active-power reference	$P^{\star}$	255 W
Three-ph. reactive-power reference	$Q^{\star}$	0 VAr
Three-ph. current closed-loop-system bandwidth	α_s	1200 rad/s
Three-ph. current integral controller gain	α_1	100 rad/s
Three-ph. voltage feedforward filter bandwidth	α_f	1000 rad/s
PLL closed-loop-system bandwidth	α_p	50 rad/s
PLL low-pass filter bandwidth	α_{lp}	250 rad/s
Single-ph. voltage reference amplitude	$v_{1/3}$	91.5 V
Single-ph. voltage reference phase	ψ	0 rad
Single-ph. active-power reference	$P_r^{\star}$	255 W
Single-ph. reactive-power reference	$Q_r^{\star}$	171 VAr
Circulating current closed-loop-system bandwidth	α_c	1000 rad/s
Sum capacitor voltage reference	v_{C0}^{Σ}	98 V
Arm-balancing contr. average-part gain	K_{Σ}	0.5
Arm-balancing contr. imbalance-part gain	K_{Δ}	1
Arm-balancing contr. band-pass filter bandwidth	α_{Σ}	105 rad/s
Arm-balancing contr. band-pass filter bandwidth	α_{Δ}	105 rad/s
Carrier frequency	f_c	763 Hz
Control system delay time	T_d	65.5 μs

The insertion indices are transmitted to the programmable logic, where the modulation scheme is implemented. Phase-shifted carrier pulsewidth modulation is used, which ensures the balancing of the individual capacitor voltages and symmetrical operating conditions between the arms, given that the carrier frequency is a noninteger multiple of f_1 [36].

The MMC is first operated in the steady state, using the controller settings given in Table IV. The measured waveforms, presented in Fig. 7, show that the conversion from three-phase 50 Hz to single-phase $16\,^2/_3$ Hz is successfully achieved. It can be observed how the single-phase side current (green) splits equally among the three phases and thus the circulating currents (blue, red, and yellow) comprise one third of the single-phase side current.

The current waveforms are then analyzed in the frequency domain, comparing the insertion index selection methods discussed in Section III-C. Fig. 8 clearly shows that the $16\,^2/_3$ Hz and the $83\,^1/_3$ Hz components of i_s are greatly reduced when the closed-loop scheme is used instead of the open-loop scheme, which agrees with the theoretical analysis. On the contrary, undesired harmonics still appear in i_c as a side effect of the arm-balancing controller. Nonetheless, most of these harmonics do not propagate to the single-phase side current i_r, which only exhibits a 0.01 p.u. harmonic at 50 Hz.

The arm-balancing controller is tested by means of a step change in the reference v_{C0}^{Σ}. Since the resistive-inductive load affects the circulating current dynamics, (27) is modified as follows:

$$\frac{v_C^{\Sigma}}{v_{C0}^{\Sigma}} = \frac{\omega_{\Sigma}^2}{s^2 + s\left(\frac{\alpha_c L + R + R_r/2}{L + L_r/2}\right) + \omega_{\Sigma}^2} \tag{55}$$

with

$$\omega_{\Sigma}^2 = \frac{K_{\Sigma} v_{1/3}}{4 v_{C0}^{\Sigma}(L + \frac{L_r}{2})C}. \tag{56}$$

Fig. 9 shows that the sum capacitor voltages converge to the new reference value and that the transfer function (55) effectively models the average capacitor voltage dynamics.

The current controllers are tested by applying a step change in the current references amplitude. This particular test cannot be performed using the experimental setup, because the passive load binds the single-phase side current to the single phase-side voltage according to the Ohm's law. Therefore, varying the load current amplitude while keeping a constant load voltage amplitude is not possible, because the passive load allows operation on a specific operating point. Instead, this test is performed by simulating the MMC time-averaged model in SIMULINK, with the single-phase side connected to a voltage source of value v_r. For this test the full-scale parameters listed in Table III are used. In addition, since full-scale converters typically have low parasitic arm resistance [22], R is lowered to 0.1 Ω. Fig. 10 shows that the currents i_s and i_r respond to the step changes with the desired bandwidths, i.e., α_s and α_c, respectively. Moreover, the sum capacitor voltages track their reference v_{C0}^{Σ}.

B. Validation of the Admittance Models

The three-phase side admittance of the down-scaled MMC is measured by superimposing a small-signal perturbation on the 50 Hz voltage, using the three-phase inverter shown in Fig. 5. Since the perturbation frequency is programmable, several measurements are made to acquire the frequency-domain plot of the admittance. At every iteration, e and i_s are measured to extract their component at f_p, obtaining the corresponding admittance value using (29). Fig. 11 shows the result of this experiment, comparing the measured values with the analytical expression (32). The two curves are in agreement, which validates the proposed analytical model.

In order to measure the single-phase side admittance of the down-scaled MMC, the $16\,^2/_3$ Hz voltage is perturbed using the single-phase inverter, shown in Fig. 5. Again, a set of measurements is performed, changing the perturbation frequency at every iteration, and extracting the admittance value using (30). Fig. 12 shows the result of this experiment, comparing the measured values with the accurate analytical model, described in Section IV-B, and with the simplified expression (54). The accurate analytical model is in agreement with the measured values in the whole frequency range, which validates the proposed derivation. The simplified expression, which neglects the arm-balancing controller, does not capture the admittance profile in the 8–100 Hz range. Nonetheless, it can be used outside this

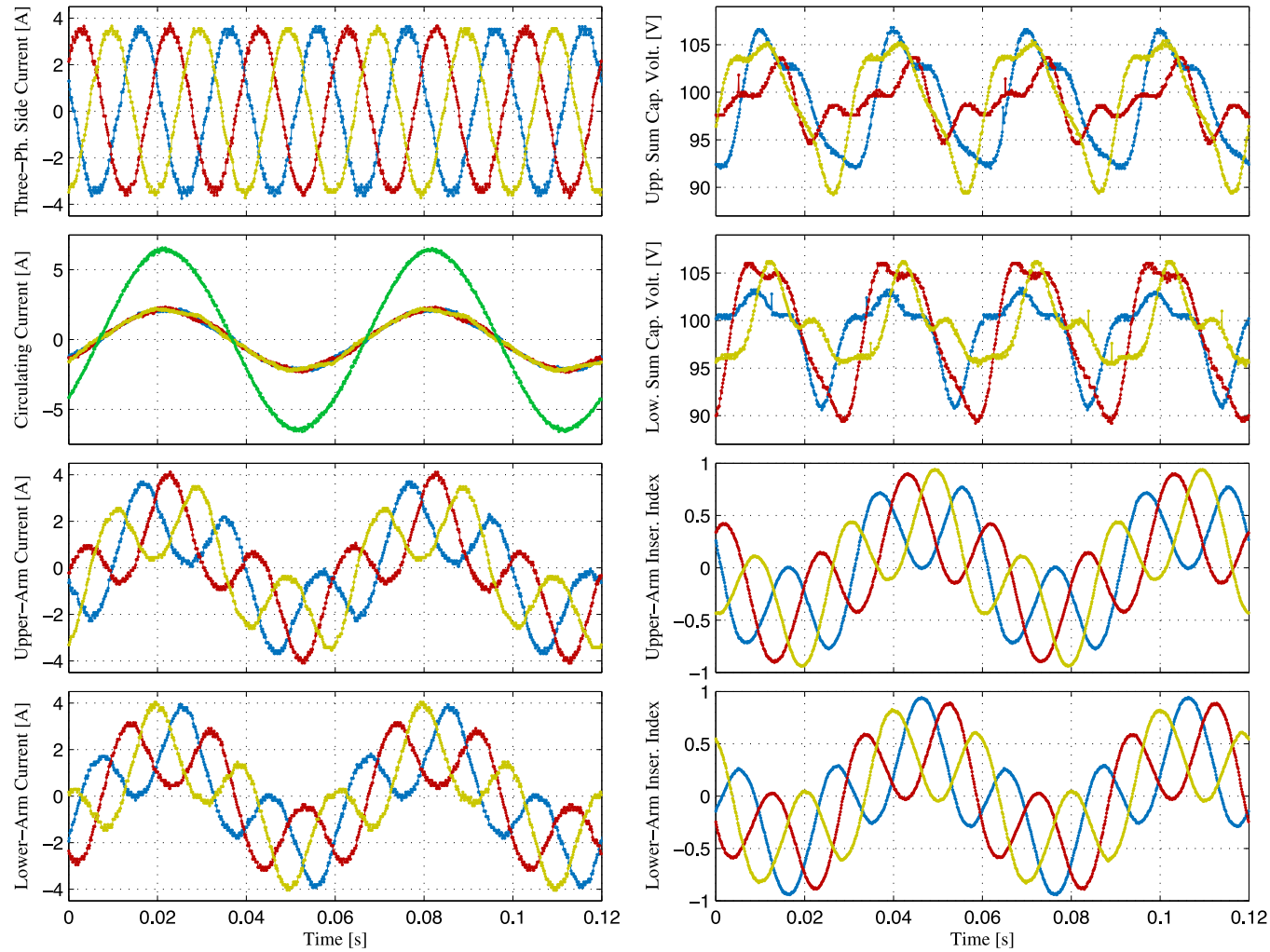

Fig. 7. Measured waveforms during steady-state operation: phase a (blue), phase b (red), phase c (yellow), and single-phase side current (green).

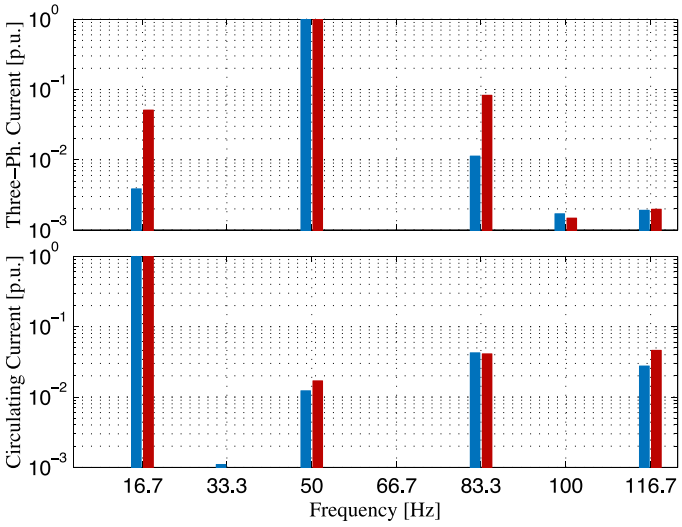

Fig. 8. Measured spectra of the converter currents for different insertion index selection methods: closed-loop scheme (blue) and open-loop scheme (red).

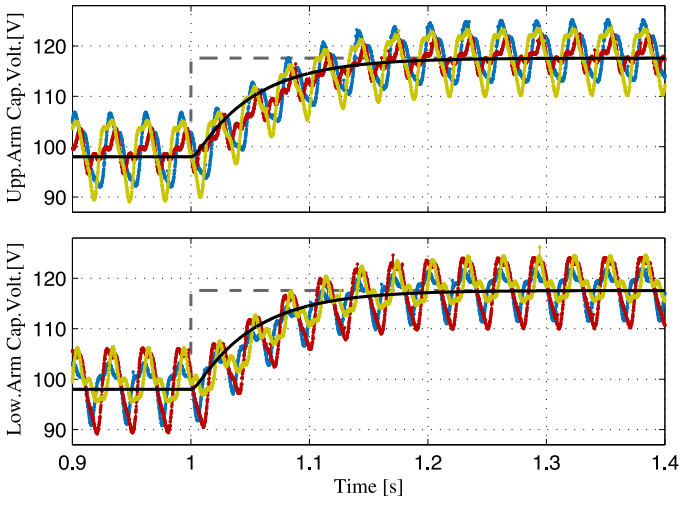

Fig. 9. Measured sum capacitor voltage waveforms during a step change in the average sum capacitor voltage reference (grey-dashed), which is increased by 20% at $t = 1$ s. The response of the average capacitor voltage is calculated analytically using (55) and plotted in black.

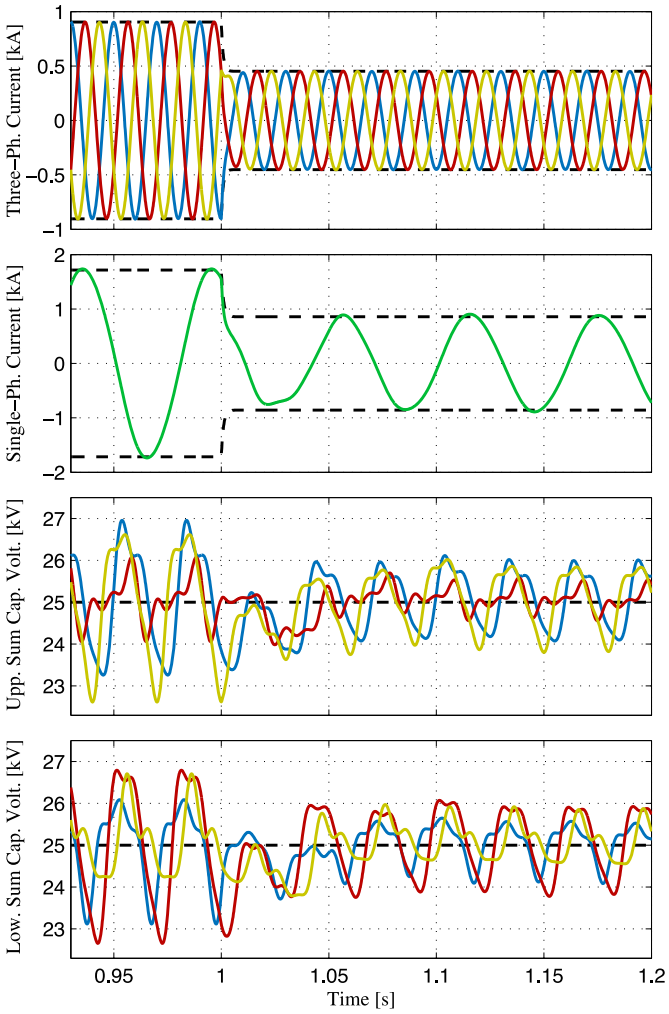

Fig. 10. Simulated current and sum capacitor voltage waveforms during a step change in the current references amplitude, which are reduced to 50% at $t = 1$ s. To verify whether the current controllers respond with the desired bandwidths, the current reference amplitudes are low-pass filtered, using $\alpha_s/(s+\alpha_s)$ for i_s and $\alpha_c/(s+\alpha_c)$ for i_r, and plotted in black. In the two lower plots the sum capacitor voltage reference v_{C0}^{Σ} is shown in black.

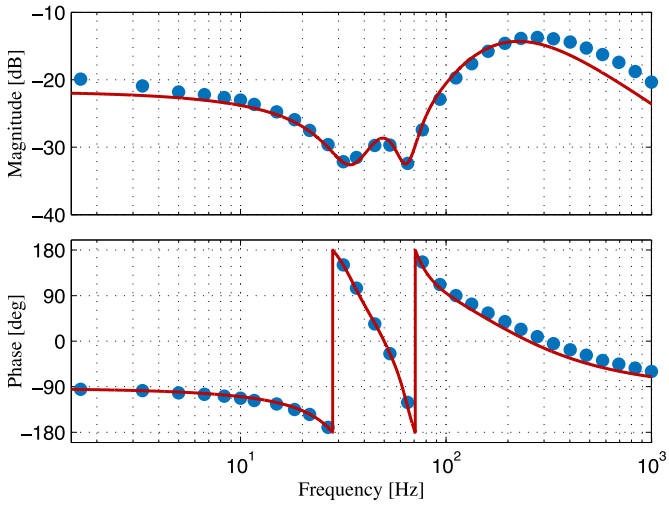

Fig. 11. Bode diagram of the MMC three-phase side admittance: measured values (blue dots) and analytical model (red line).

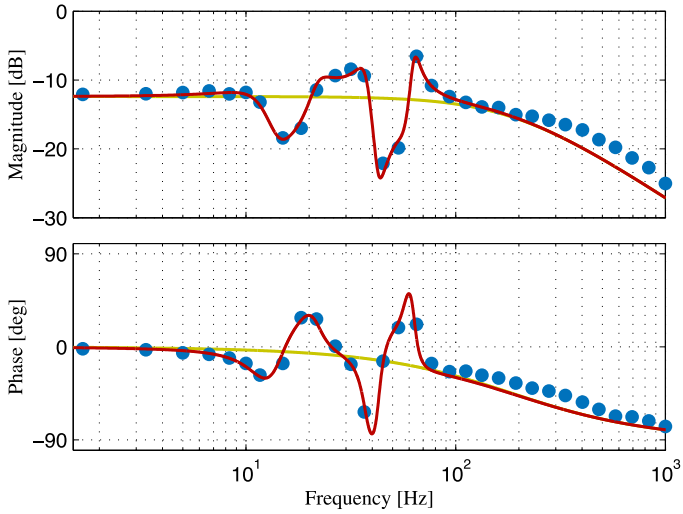

Fig. 12. Bode diagram of the MMC single-phase side admittance: measured values (blue dots), accurate analytical model (red line), and simplified analytical model (yellow line).

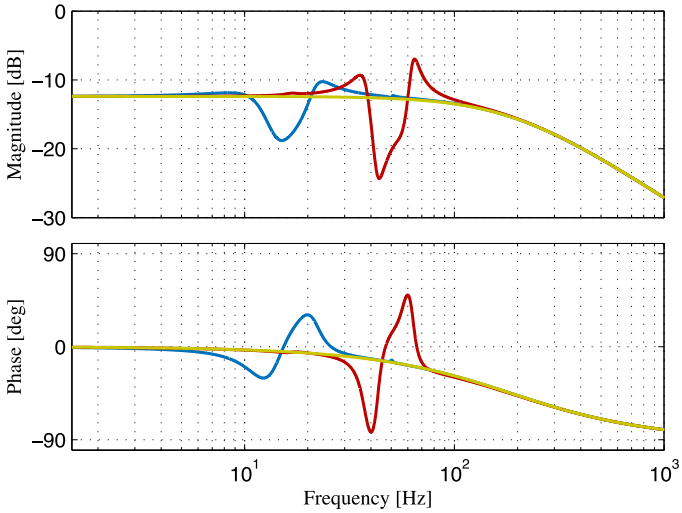

Fig. 13. Bode diagram of the MMC single-phase side admittance, obtained using the accurate analytical model: $K_\Sigma = 0.5$ and $K_\Delta = 0$ (blue), $K_\Sigma = 0$ and $K_\Delta = 1$ (red), and $K_\Sigma = K_\Delta = 0$ (yellow).

range as an approximation of the accurate model. Furthermore, comparing the two models shows how the arm-balancing controller shapes the admittance in the 8–100 Hz range. This effect is analyzed in detail in Fig. 13, evaluating the accurate analytical model for different values of K_Σ and K_Δ. It is observed that K_Σ causes the magnitude notch and phase rotation centered at $16\,^2/_3$ Hz, while K_Δ has similar effects centered at 50 Hz. Therefore, it is recommended to consider these admittance-shaping effects when selecting the control parameters K_Σ and K_Δ.

From Fig. 12, it is observed that $Y_{1\mathrm{ph}}$ has a nonnegative real part in the whole frequency range, i.e., it has a passive behavior. This is a highly beneficial feature, which generally allows for preventing destabilization of critical grid resonances [28], [32]. The passivity of $Y_{1\mathrm{ph}}$ is achieved through the controller design

(18). In comparison, Fig. 11 shows that $Y_{3\mathrm{ph}}$ has a negative real part for some frequencies, as a result of the more aggressive current control scheme and the presence of the PLL [26].

VI. Conclusion

In this paper, the ac/ac MMC for railway power supplies is studied, focusing on its control scheme and admittance models. The three-phase side control can adopt standard solutions used for grid-connected inverters, while the single-phase side must provide a stiff voltage, in a grid-forming fashion. The closed-loop scheme is the recommended choice for computing the insertion indices, as it prevents the generation of undesired harmonic components in the arm voltages and currents. An arm-balancing controller is however required, which causes harmonics to appear in the circulating current as a drawback of its design.

The three-phase side admittance coincides with the admittance of other grid-connected inverters, because neither the sum capacitor voltages nor the single-phase side quantities appear in the admittance calculation, given that the closed-loop scheme is used. The single-phase side admittance can be obtained by solving a linear system, which expresses the main perturbation frequency components of the converter variables. Its plot shows that, as a result of the chosen control scheme, passivity is achieved in the whole frequency range.

Appendix

A. Abbreviation List

MMC	Modular multilevel converter
VSC	Voltage source converter
PLL	Phase-locked loop
p.u.	per unit

B. Effects of the PLL on the Three-Phase Side Admittance

The function H_{PLL}, derived in [26], groups the effect of the PLL on the admittance, introduced by the dq transformation and its inverse, i.e.,

$$H_{\mathrm{PLL}} = \Bigg[\left(-F_{dq}[j(\omega_p - \omega_1)] + \frac{j\omega_1 L}{2} \right) I_s(f_1) + H_{dq}[j(\omega_p - \omega_1)] E(f_1) - V_s^{\star}(f_1) \Bigg] j H_p[j(\omega_p - \omega_1)] \tag{57}$$

where

$$I_s(f_1) = \frac{i_{sd}^{\star} + j i_{sq}^{\star}}{2} \tag{58}$$

$$V_s^{\star}(f_1) = E(f_1) + \frac{j\omega_1 L + R}{2} I_s(f_1) \tag{59}$$

are the 50-Hz Fourier coefficient of i_s and $v_s^{\star}$, respectively, and $H_p(s)$ is the PLL closed-loop transfer function, defined as

$$H_p(s) = \frac{-j\alpha_p H_{\mathrm{LP}}(s)}{e_1[s + \alpha_p H_{\mathrm{LP}}(s)]}. \tag{60}$$

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