

Analysis and Design of an RC Snubber Circuit to Suppress False Triggering Oscillation for GaN Devices in Half-Bridge Circuits

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Abstract—Wide bandgap devices such as gallium nitride (GaN) devices are being widely used due to their low ON-resistance and parasitic parameters that can improve system performance compared to Si MOSFETs. However, these advantages mentioned above can sometimes lead to unexpected behavior in practical systems, such as false triggering oscillation. False triggering oscillation may cause overshoot, electromagnetic interference, shoot-through, and even device damage, which seriously affects the performance of the system. In this paper, an RC snubber circuit is proposed to suppress false triggering oscillation in a half-bridge circuit, and the design method of the RC parameters is proposed. The proposed oscillation suppression method is simpler, easier to implement, and more effective than the active gate driver. In addition, it can provide guidance for oscillation suppression design in high-order systems. First, the double pulse circuit is used as an example to analyze false triggering oscillation and its high-frequency equivalent circuit is obtained. Then, the RC region is established by scrutinizing the characteristic equations via a root locus method. The RC snubber circuit has better oscillation suppression effect when the RC parameters are within the region rather than outside the region. Finally, the RC region designed by the proposed method is verified by simulation and experiment results, and the proposed method indicates a substantial improvement of the switching characteristics of the controlled device at turn-OFF.

Index Terms—False triggering oscillation, GaN devices, half-bridge circuit, RC snubber circuit.

I. INTRODUCTION

THE wide bandgap devices such as gallium nitride (GaN) transistors have faster switching capacity, lower conduction and switching losses when compared with the state-of-the-art Si MOSFETs [1]–[3]. Accordingly, they are considered as a kind of promising devices to achieve high-frequency, high-efficiency, and high-power-density power conversion.

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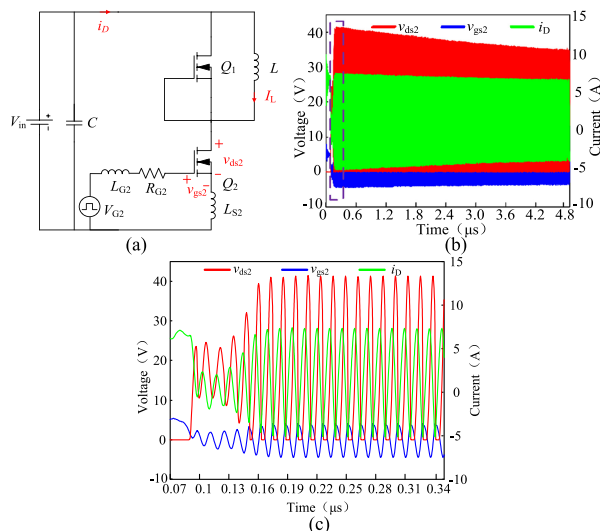


Fig. 1. False triggering oscillation of the half-bridge circuit. (a) GaN-based half-bridge circuit. (b) False triggering oscillation waveform. (c) Enlarged waveform.

Despite all its merits, low ON-resistance and capacitance of GaN devices can also cause false triggering pulse and even more severe false triggering oscillation as switching speed increases [4]–[7]. The false triggering oscillation mainly occurs when the active switch Q2 is OFF and the inactive switch Q1 conducts reversely, as shown in Fig. 1. It is noteworthy that the false triggering oscillation may cause overshoot, shoot-through, and even device damage, which seriously deteriorate its operational reliability. Furthermore, it may lead to serious electromagnetic interference (EMI) problem, and reduce conversion efficiency greatly since the false triggering oscillation frequency may reach tens to hundreds megahertz.

Commonly, there are two main reasons for false triggering pulse and even false triggering oscillation as follows [4], [6]–[10]. On the one hand, the negative voltage formed by the high di/dt at the common source inductance will lead to high gate–source voltage. On the other hand, high dv/dt induced displacement current flows through the Miller capacitor into the gate driving circuit, which will also result in Miller turn-ON if the gate–source voltage rises to its threshold voltage, and thus, false triggering pulse and even false triggering oscillation occur.

In [11] and [12], the Barkhausen criterion is adopted to analyze the oscillation occurrence condition, and explore the influence of some parameters on the false triggering oscillation, such as gate inductance, drain inductance, gate–drain capacitance, and common source inductance, etc. In [13] and [14], the principle of false triggering oscillation is analyzed, and some useful suggestions are given according to the analyzing results. For example, a small stray gate-loop inductance, a higher ON-resistance, and gate–source capacitance can reduce the risk of false triggering oscillation. In [15] and [16], the occurrence of false triggering oscillation can be avoided by a good printed circuit board (PCB) layout or by increasing the turn-ON gate resistance. However, it is very difficult to reduce these stray parameters due to device package limitations and PCB layout limitations in practice. Moreover, these suggestions mentioned above are qualitative, and how to determine these parameters to suppress the false triggering oscillation is not involved. An active gate driver and a clamped inductively loaded circuit are proposed to suppress false triggering oscillation in [17] and [18], respectively. Although these two methods mentioned above do have some useful effects, the circuit becomes quite complicated, and it is not conducive to circuit simplification.

RC snubber circuits are widely used to suppress the drain–source voltage ringing. However, the *RC* parameters are commonly fixed based on the designer’s experience [19]–[22]. Moreover, a sufficient level of ringing suppression cannot be guaranteed in the experimental design approach mentioned above. In [19] and [20], the second-order design is used to roughly estimate the *RC* snubber parameters, and then the parameters are experimentally determined. In fact, these approaches mentioned above do not have sufficient guidance for the design of the *RC* parameters quantitatively. In [23] and [24], an analytical technique for designing *RC* snubber circuits for the half-bridge configuration and the flyback converter has already been developed. In that technique, the characteristic equations of the high-frequency equivalent circuits are analyzed by using the root locus method, after which the *RC* snubber constants that eliminate the ringing caused by resonances between the parasitic inductance of the circuit and the parasitic capacitances of both the switching devices are derived. However, the mechanism of false triggering oscillation is quite different from that of the drain–source voltage ringing. Furthermore, this analytical method can only be applied to second-order or third-order circuits, it is quite difficult to simplify the system into a second-order or third-order circuit for false triggering oscillation suppression. Therefore, it is unclear whether the analytical technique used to design *RC* snubber circuits in [23] and [24] can be applied to deal with the false triggering oscillation.

According to the analysis mentioned above, there are mainly three problems as follows. First, the existing methods for false triggering oscillation suppression, such as active gate driver, are too complicated and their performance is not perfect. Second, although the *RC* snubber circuits are simple and have been widely used to suppress the ringing of the drain–source voltage, it is suspicious that the *RC* snubber circuits can be used to suppress the false triggering oscillation. Third, the existing *RC* design methods can only be used in second-order or third-order circuits,

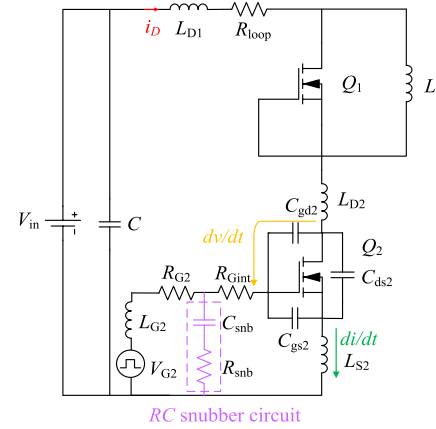


Fig. 2. Circuit diagram of a double pulse circuit with the *RC* snubber circuit. Q1 is the inactive device and Q2 is the active device.

it is very difficult to decide the *RC* parameters quantitatively for high-order systems.

In this paper, the *RC* snubber circuit is adopted to suppress the false triggering oscillation for GaN devices, which is simpler and more effective than other schemes. In addition, how to decide the *RC* parameters quantitatively is presented in detail, which can provide guidance for oscillation suppression design for high-order systems. This paper is organized as follows. In Section II, the analysis model of the false triggering oscillation based on the double pulse circuit is established at first. Then, the extraction of parasitic parameters and the analysis and design method of the *RC* parameter are presented in Section III. In Section VI, simulation and experimental platforms are built to validate theoretical analysis, respectively. In addition, a comparison of the proposed *RC* design method with the traditional *RC* design method is also shown in this section. Some conclusions driven from this study are described in Section V.

II. CIRCUIT MODELING SETTINGS AND DERIVATION

A. Assumptions and Equivalent Circuit Settings

A double pulse circuit, shown in Fig. 2, is taken as an example to obtain the analytical model for false triggering oscillation, and the *RC* snubber circuit is also included. This model can also be applied to other half-bridge circuits, such as the synchronous buck converter. As mentioned earlier, false triggering oscillation is caused by high *dv/dt* and *di/dt*, which occurs mainly when active GaN transistor Q2 is turned OFF and inactive GaN transistor Q1 is freewheeling. The definitions of the symbols used in Fig. 2 are shown below.

V_{in}	DC input power.
C	Capacitance of decoupling capacitor.
L_{D1}	Drain parasitic inductance of Q1.
R_{loop}	Power loop resistance of the double pulse circuit.
L_{D2}	Drain parasitic inductance of Q2.
C_{ds2}	Drain–source parasitic capacitance of Q2.
C_{gd2}	Gate–drain parasitic capacitance of Q2.
C_{gs2}	Gate–source parasitic capacitance of Q2.
L_{S2}	Common source parasitic inductance of Q2.
L	Inductance of load inductor.

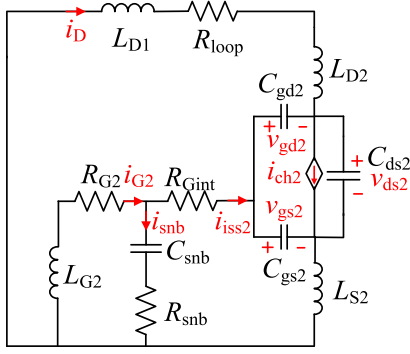


Fig. 3. Simplified circuit diagram of a double pulse circuit with the RC snubber circuit.

R_{Gint}	Gate parasitic resistance of Q2.
R_{G2}	Gate external resistance of Q2.
L_{G2}	Gate parasitic inductance of Q2.
V_{G2}	Gate drive power of Q2.
C_{snb}	Capacitance of snubber capacitor.
R_{snb}	Resistance of snubber resistor.

In order to simplify the equivalent circuit diagram shown in Fig. 2, the following assumptions are made.

- 1) Due to the large capacitance of the decoupling capacitor C , its high-frequency impedance is sufficiently smaller than the impedance of other parasitic parameters; therefore, it can be regarded as a short circuit.
- 2) Due to the large inductance of the load inductor L , its high-frequency impedance is sufficiently higher than the impedance of other parasitic parameters; therefore, it can be regarded as an open circuit.
- 3) Since the false triggering oscillation occurs after Q2 is turned OFF, the gate drive voltage of Q2 is at a low level of zero.
- 4) When Q2 exhibits false triggering oscillation, Q2 generates channel current. The existence of channel current is a necessary condition for false triggering oscillation [14].

According to the abovementioned assumptions, a simplified equivalent circuit diagram for analyzing false triggering oscillation is shown in Fig. 3. In addition, the definitions of symbols in Fig. 3 are shown below.

i_D	Drain current of Q1.
v_{gd2}	Gate–drain voltage of Q2.
v_{ds2}	Drain–source voltage of Q2.
v_{gs2}	Gate–source voltage of Q2.
i_{ch2}	Channel current of Q2.
i_{G2}	Gate input current of Q2.
i_{iss2}	Gate current of Q2.
i_{snb}	Current of snubber circuit.

B. Deriving Characteristic Equations Based on Equivalent Circuit

According to KCL and KVL, the following equations can be obtained from Fig. 3:

$$0 = L_D \frac{di_D}{dt} + L_{S2} \frac{d(i_{iss2} + i_D)}{dt} + v_{ds2} + R_{loop} i_D \quad (1)$$

$$i_D = C_{ds2} \frac{dv_{ds2}}{dt} - C_{gd2} \frac{dv_{gd2}}{dt} + i_{ch2} \quad (2)$$

$$v_{gd2} = v_{gs2} - v_{ds2} \quad (3)$$

$$i_{ch2} = g_m v_{gs2} \quad (4)$$

$$L_{S2} \frac{d(i_{iss2} + i_D)}{dt} + v_{gs2} + R_{Gint} i_{iss2} = \frac{1}{C_{snb}} \int i_{snb} dt + i_{snb} R_{snb} \quad (5)$$

$$i_{G2} = i_{snb} + i_{iss2} \quad (6)$$

$$L_{G2} \frac{di_{G2}}{dt} + i_{G2} R_{G2} + \frac{1}{C_{snb}} \int i_{snb} dt + i_{snb} R_{snb} = 0 \quad (7)$$

$$i_{iss2} = C_{gs2} \frac{dv_{gs2}}{dt} + C_{gd2} \frac{dv_{gd2}}{dt} \quad (8)$$

where L_D is the sum of L_{D1} and L_{D2} .

R_{snb} and C_{snb} are designed to suppress false triggering oscillations of v_{gs2} . Therefore, we perform the Laplace transform on the abovementioned equations and finally get the s-domain equation for v_{gs2} . The initial condition of the abovementioned variable is $i_D(0) = I_0$, $i_{G2}(0) = i_{snb}(0) = i_{iss2}(0) = 0$, $v_{gs2}(0) = V_0$, $v_{ds2}(0) = 0$. The following equations can be obtained from (1) to (8):

$$0 = (L_D + L_{S2})(s i_D(s) - I_0) + s L_{S2} i_{iss2}(s) + v_{ds2}(s) + R_{loop} i_D(s) \quad (9)$$

$$i_D(s) = s C_{oss2} v_{ds2}(s) - C_{gd2} (s v_{gs2}(s) - V_0) + g_m v_{gs2}(s) \quad (10)$$

$$s L_{S2} i_{iss2}(s) + L_{S2} (s i_D(s) - I_0) + v_{gs2}(s) + i_{iss2}(s) R_{Gint} = \frac{1}{s C_{snb}} i_{snb}(s) + i_{snb}(s) R_{snb} \quad (11)$$

$$R_{G2} (i_{snb}(s) + i_{iss2}(s)) + s L_{G2} (i_{snb}(s) + i_{iss2}(s)) + \frac{1}{s C_{snb}} i_{snb}(s) + i_{snb}(s) R_{snb} = 0 \quad (12)$$

$$i_{iss2}(s) = C_{iss2} (s v_{gs2}(s) - V_0) - s C_{gd2} v_{ds2}(s) \quad (13)$$

where $C_{oss2} = C_{gd2} + C_{ds2}$ and $C_{iss2} = C_{gs2} + C_{gd2}$. $i_D(s)$, $i_{iss2}(s)$, $i_{snb}(s)$, $v_{gs2}(s)$, and $v_{ds2}(s)$ are defined as the Laplace transform of i_D , i_{iss2} , i_{snb} , v_{gs2} , and v_{ds2} , respectively.

The gate–source voltage $v_{gs2}(s)$ can be expressed as

$$v_{gs2}(s) = \frac{N(s)}{D(s)} = \frac{a_0 s^5 + a_1 s^4 + a_2 s^3 + a_3 s^2 + a_4 s + a_5}{b_0 s^6 + b_1 s^5 + b_2 s^4 + b_3 s^3 + b_4 s^2 + b_5 s + b_6} \quad (14)$$

where b_i ($i = 0, 1, 2, 3, 4, 5, 6$) and a_j ($j = 0, 1, 2, 3, 4, 5$) are coefficients listed in the Appendix. It should be noted that this is a sixth-order system.

III. ANALYSIS AND DESIGN OF RC SNUBBER CIRCUITS FOR FALSE TRIGGERING OSCILLATION SUPPRESSION

In order to suppress false triggering oscillation of v_{gs2} , the best case is that v_{gs2} has no oscillation terms. When the solutions of the characteristic equation $D(s) = 0$ are all real numbers,

TABLE I
SPECIFICATIONS AND KEY CIRCUIT PARAMETER

Symbol	Value
L_D	5.95 nH
L_{G2}	5.2 nH
L_{S2}	3 nH
C_{iss2}	1.15 nF
C_{oss2}	0.75 nF
C_{gd2}	0.07 nF
R_{G2}	0.5 Ω
R_{Gint}	0.6 Ω
R_{loop}	0.1 Ω
g_m	27 S

then v_{gs2} has no oscillation terms. However, when $D(s) = 0$ is a third-order or lower order polynomial, all solutions of $D(s) = 0$ may be a real number. Since the order of the equation is the same as the number of roots, the third-order polynomial $D(s) = 0$ will appear in three solutions. These three solutions are either real numbers or a combination of a real number and two conjugate complex solutions. In the third-order polynomial, when the breakaway point γ is satisfied such that $D(\gamma) = 0$ and $dD(\gamma)/ds = 0$, the designed R_{snb} and C_{snb} can make $D(s)$ have no oscillation terms [23], [24]. However, this method cannot be applied to the fourth-order or higher order polynomials. Since in the fourth-order polynomial, the number of root loci of $D(s)$ is also four, a breakaway point exists when two of four root loci cross the real axis. However, the other two root loci do not always cross the real axis [25]. Accordingly, we cannot make all solutions real numbers by solving equations $D(\gamma) = 0$ and $dD(\gamma)/ds = 0$ simultaneously for the fourth-order polynomial.

Since the characteristic equation $D(s) = 0$ in this paper is a sixth-order polynomial, it is not possible to make all solutions of $D(s) = 0$ be real numbers. Therefore, the aforementioned method of utilizing the breakaway point is not applicable here. This paper uses the root locus method to confirm the R_{snb} and C_{snb} value regions for the sixth-order equation. From (14), the characteristic equation can be obtained as

$$D(s) = 0. \quad (15)$$

Considering the snubber capacitance C_{snb} as the variable parameter, we rearrange (15) as follows:

$$D(s) = P + C_{snb}Q = 0. \quad (16)$$

Transforming (16) into the following form:

$$D_1(s) = 1 + \frac{C_{snb}Q}{P} = 0 \quad (17)$$

where P and Q are listed in the Appendix.

Changing the value of the capacitance C_{snb} from zero to infinity according to $C_{snb}Q/P$, we can get the root loci of the characteristic equation $D(s) = 0$.

Table I lists the circuit parameters obtained from the experimental prototype. Parasitic inductances are extracted by ANSYS Q3D software according to the PCB layout. Fig. 4 shows the PCB layout and ANSYS Q3D extraction of Q2 drive circuit. Since the parasitic parameter extraction method of the driver loop is basically consistent with the power loop, we use the

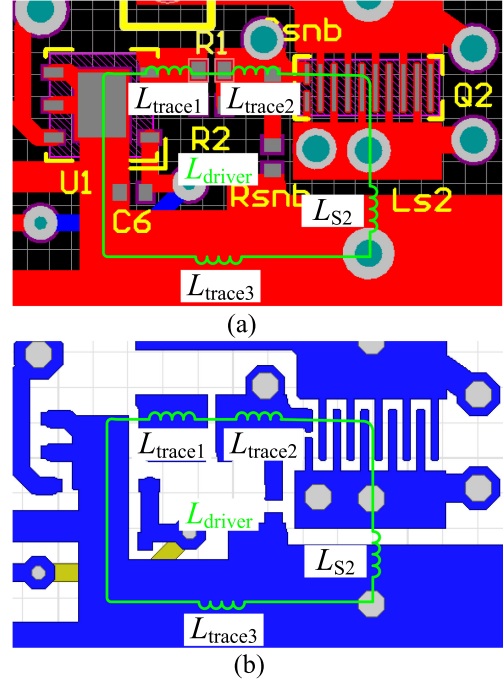


Fig. 4 Example of Q3D extraction. (a) PCB layout of the Q2 drive circuit. (b) ANSYS Q3D extraction of Q2 drive circuit.

TABLE II
DRIVER LOOP PARASITIC INDUCTANCE EXTRACTION USING Q3D

Parasitic Parameter	value	Parasitic Parameter	value
L_{trace1}	0.68 nH	L_{trace3}	3.55 nH
L_{trace2}	0.97 nH	L_{S2}	3 nH

driver loop of Q2 as an example to explore the extraction of parasitic parameters. The green line in Fig. 4 represents the entire driver loop. The parasitic inductance shown in Fig. 4 can be extracted through the ANSYS Q3D, which mainly includes L_{trace1} , L_{trace2} , and L_{trace3} . The gate inductance L_{G2} of Q2 is the sum of the inductances L_{trace1} , L_{trace2} , and L_{trace3} , which is 5.2 nH. In addition, L_{S2} is the common source inductance that is 3 nH. The final results are listed in Table II.

The transconductance and capacitances are obtained from the device's datasheet. The selection of the parasitic capacitance value is related to the drain-source voltage V_{ds2} , and the value of the transconductance is obtained near the threshold voltage V_{th} of the device.

As mentioned above, the best suppression of oscillation is achieved when all solutions of the characteristic equation $D(s) = 0$ are all real numbers. The damping ratio of all solutions is 1 when all solutions are real numbers. In the sixth-order equation, there is no guarantee that the damping ratio of all solutions is 1, but all damping ratios should be as large as possible to get the better oscillation suppression effect. To this end, we propose to make all the roots of the characteristic equation satisfy the relatively large damping when changing the range of RC . It will have better damping effect when the damping ratio is greater than 0.4 [26].

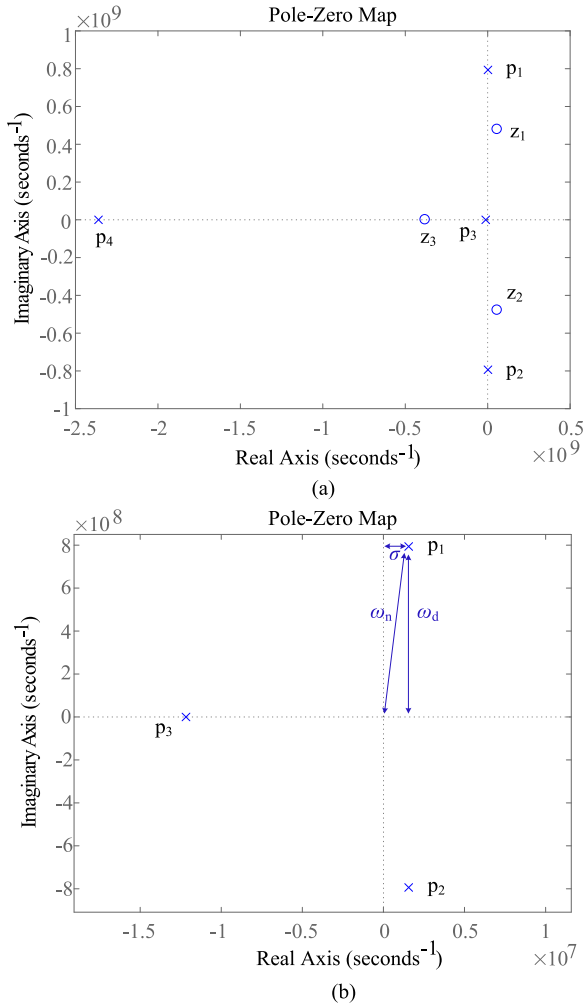


Fig. 5. (a) Pole-zero map of the $v_{gs2}(s)$. (b) Enlarged pole-zero map.

When no RC snubber circuit is added, the pole-zero map of v_{gs2} is plotted in Fig. 5(a). There are four poles, two negative real poles p_3, p_4 and two positive complex conjugate poles p_1, p_2 . Fig. 5(b) is the enlarged view and it shows that p_1 and p_2 are in the right-half plane of s . It can be seen that when there is no RC snubber circuit, the false triggering oscillation will occur.

The complex pole p_1 can be defined by its real and imaginary parts as

$$p_1 = \sigma + j\omega_d. \quad (18)$$

Since the complex pole p_1 is in the right-half plane of s , similar to the second-order system, the damping ratio is defined as [27]

$$\zeta = \frac{-\sigma}{\sqrt{\sigma^2 + \omega_d^2}} = \frac{-\sigma}{\omega_n}. \quad (19)$$

The ζ from (19) is less than 0, the pole has a positive real part, and the false triggering oscillation will occur. When $\zeta > 0$, the pole has a negative real part and that will not occur the false triggering oscillation.

When adding the RC snubber circuit, changing the value of the capacitance C_{snb} from zero to infinity according to $C_{snb}Q/P$,

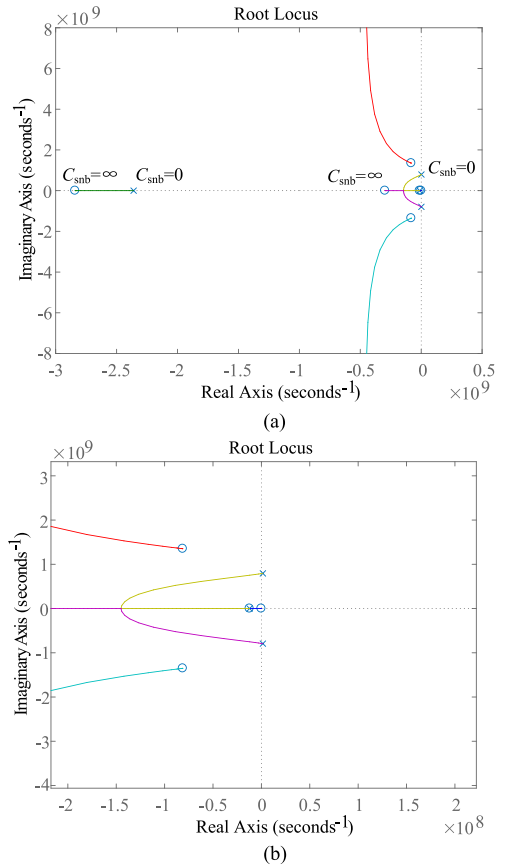


Fig. 6. (a) Root locus diagram of $D(s) = 0$ for parameter C_{snb} ($R_{snb} = 1 \Omega$). (b) Enlarged root locus diagram.

we can get the root loci of the characteristic equation $D(s) = 0$. Fig. 6 shows the root locus diagram when $R_{snb} = 1 \Omega$. After the RC snubber circuit is included, $D(s) = 0$ is a sixth-order equation with six solutions. These six solutions are biased toward the left-half plane of s as C_{snb} increases. It can be seen that after adding the RC snubber circuit, the false triggering oscillation tends to be suppressed.

In order to obtain the better oscillation suppression effect, it is required that all solutions of $D(s) = 0$ have a large damping ratio ζ . As mentioned earlier, when $\zeta > 0.4$, there will be better oscillation suppression. Fig. 7 shows the root locus diagram for parameter C_{snb} when R_{snb} is equal to 3Ω . This sixth-order equation has two negative real solutions with a damping ratio of 1 and two pairs of complex conjugate solutions. With the change of C_{snb} , $D(s) = 0$ always has two negative real solutions with a damping ratio of 1. Therefore, in order to make the damping ratio of all solutions of $D(s) = 0$ greater than 0.4, only the damping ratios of the other two pairs of complex conjugate solutions are greater than 0.4. Making the straight line with $\zeta = 0.4$, we can see that these two lines intersect with the other four root loci. Taking the red line and the yellow line root loci above the horizontal axis as an example, when the damping ratio of the red line root locus is $\zeta > 0.4$, the value range of C_{snb} is (0.17 nF, 0.7 nF). When the damping ratio of the yellow line root locus is $\zeta > 0.4$, the value range of C_{snb} is $C_{snb} > 0.55$ nF. In order to make the

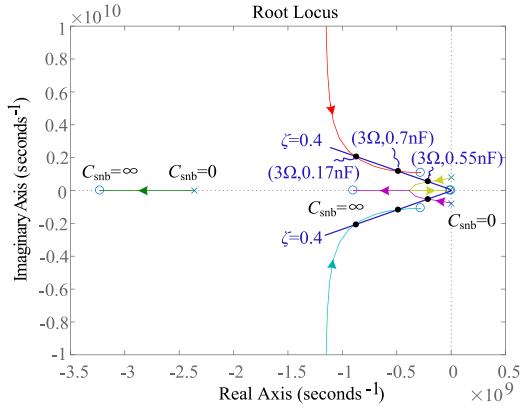


Fig. 7. Root locus diagram of $D(s) = 0$ for parameter C_{snb} ($R_{snb} = 3 \Omega$).

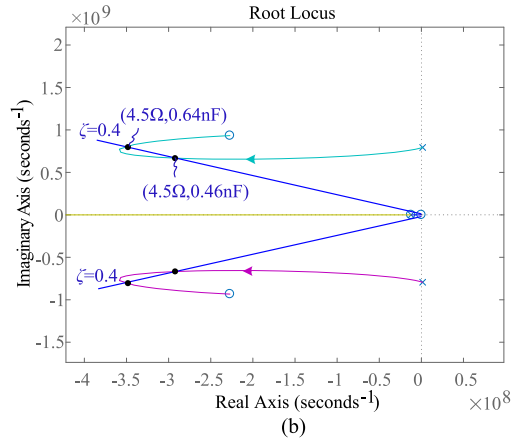
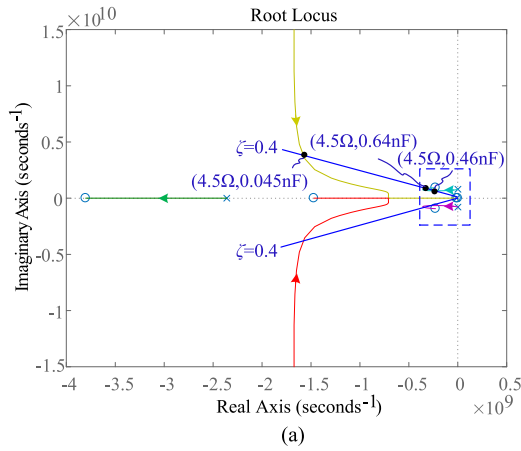


Fig. 8. (a) Root locus diagram of $D(s) = 0$ for parameter C_{snb} ($R_{snb} = 4.5 \Omega$). (b) Enlarged root locus diagram.

damping ratio of all solutions greater than 0.4, the intersection of the two C_{snb} value ranges is (0.55 nF, 0.7 nF). The root locus below the horizontal axis has the same C_{snb} value as above the horizontal axis. Therefore, when the snubber resistance R_{snb} is equal to 3 Ω and the value range of C_{snb} is (0.55 nF, 0.7 nF), the damping ratio of all solutions of $D(s) = 0$ can be made greater than 0.4.

Fig. 8 shows the root locus diagram for parameter C_{snb} when R_{snb} is equal to 4.5 Ω. As with R_{snb} equals 3 Ω, there are also

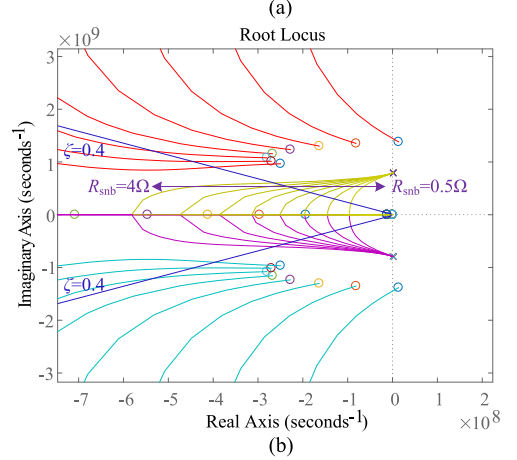
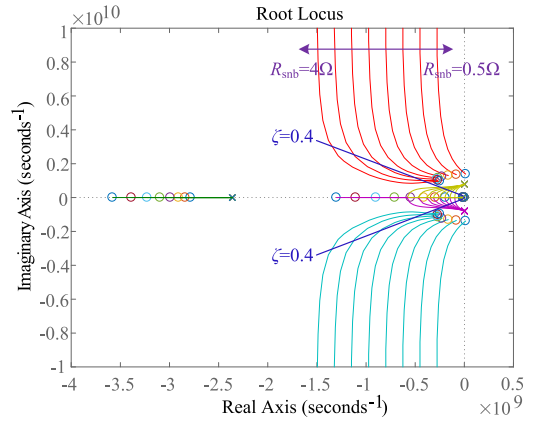


Fig. 9. (a) Root locus diagram of $D(s) = 0$ when the snubber resistance R_{snb} changes from 0.5 to 4 Ω. (b) Enlarged root locus diagram.

two pairs of complex conjugate solutions when R_{snb} is equal to 4.5 Ω. Similarly, draw the straight line of $\zeta = 0.4$, there are intersection points between these two lines and two pairs of complex conjugate solutions. Taking the two root loci above the horizontal axis as an example, when the damping ratio of the yellow line root locus is $\zeta > 0.4$, the value range of C_{snb} is $C_{snb} > 0.045$ nF. When the damping ratio of the other root locus is $\zeta > 0.4$, the range of C_{snb} is (0.46 nF, 0.64 nF). In order to make the damping ratio of all solutions greater than 0.4, the intersection of the two C_{snb} value ranges is (0.46 nF, 0.64 nF).

Fig. 9 shows the root locus of $D(s) = 0$ when the snubber resistance R_{snb} changes from 0.5 to 4 Ω. It can be seen that when R_{snb} is small, no matter how the value of C_{snb} changes, $D(s) = 0$ always has the root with a damping ratio less than 0.4. Therefore, these RC values can be excluded. Fig. 10 shows the root locus of $D(s) = 0$ when the snubber resistance R_{snb} changes from 4.5 to 6 Ω. It can be seen from Fig. 10(b) that when R_{snb} is large, no matter how the value of C_{snb} changes, $D(s) = 0$ always has the root with a damping ratio less than 0.4. These RC values can also be excluded.

As previously analyzed, in order to make the damping ratio of all solutions greater than 0.4, when the snubber resistance R_{snb} is equal to 3 and 4.5 Ω, the value ranges of C_{snb} are (0.55 nF, 0.7 nF) and (0.46 nF, 0.64 nF), respectively. In addition, when the snubber resistance R_{snb} is equal to 3.5 and 4 Ω, the value

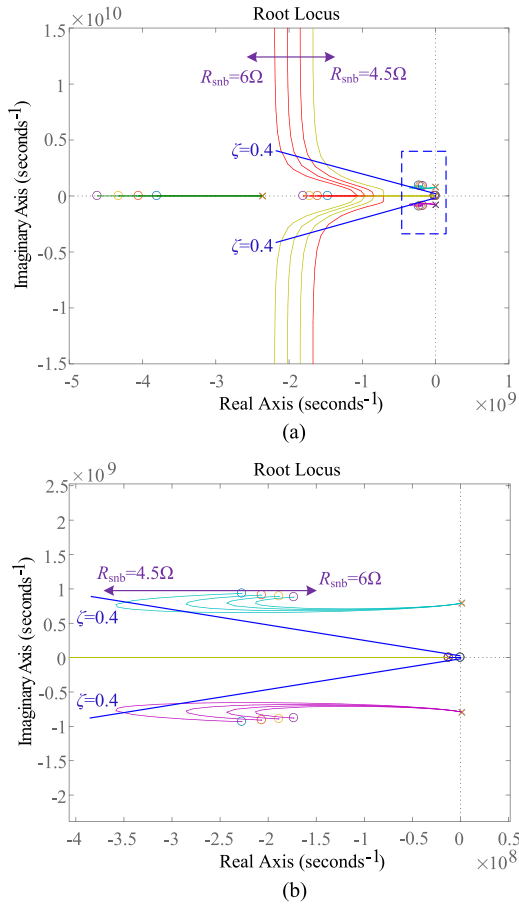


Fig. 10. (a) Root locus diagram of $D(s) = 0$ when the snubber resistance R_{snb} changes from 4.5 to 6 Ω . (b) Enlarged root locus diagram.

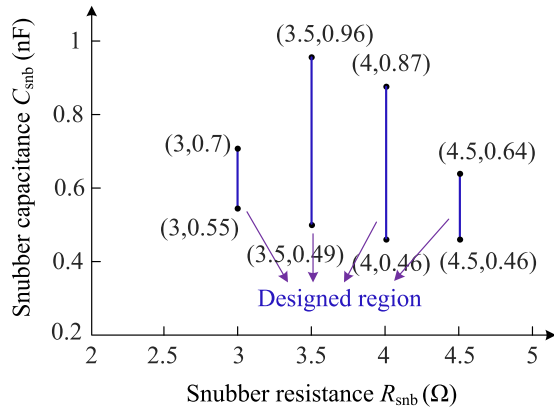


Fig. 11 R_{snb} - C_{snb} region when R_{snb} is equal to 3, 3.5, 4, and 4.5 Ω , respectively.

ranges of C_{snb} are (0.49 nF, 0.96 nF) and (0.46 nF, 0.87 nF), respectively. Fig. 11 shows the RC design region when R_{snb} is equal to 3, 3.5, 4, and 4.5 Ω , respectively. Using the same method, we can also get the corresponding snubber capacitance C_{snb} region when the snubber resistance R_{snb} is of other different values.

Finally, the designed region of C_{snb} and R_{snb} is shown in Fig. 12. The region enclosed by the blue line is the range of

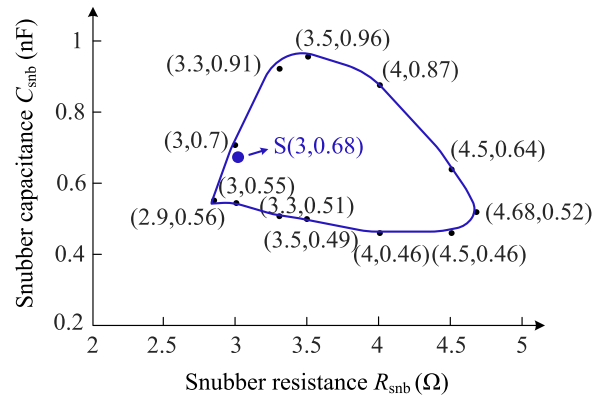


Fig. 12. R_{snb} - C_{snb} region where false triggering oscillation is considered to be better suppressed.

RC values, which can better suppress oscillation because the damping ratio of all solutions of $D(s) = 0$, are greater than 0.4. Through the abovementioned analysis, the flowchart of the proposed RC design method is shown in Fig. 13.

IV. SIMULATION AND EXPERIMENTAL VERIFICATION

A. Simulation Verification

The double pulse circuit with the RC snubber circuit is built with LTSpice software. The specifications and the key circuit parameters are listed in Table I. The input voltage V_{in} is 15 V, the inductor current I_L is 7 A, and the drive voltage V_{G2} is 5 V. Especially the switching device is EPC2015 using the manufacturer's device model [28]. Fig. 14 shows the voltage waveform of v_{gs2} without the RC snubber and with the RC snubber. It can be seen that the RC snubber circuit has a good suppression effect on the oscillation.

In order to further verify the suppression effect of the RC design region on the false triggering oscillation, the RC snubber constants outside the design region are examined. According to Fig. 12, the range of the snubber resistance R_{snb} within the design region is (2.9 Ω , 4.68 Ω). Due to the limitations of resistor selection in practice, we choose point S (3 Ω , 0.68 nF) within the design region and compared its oscillation suppression effect with that outside the RC design region. The RC values selected outside the RC design region are shown in Fig. 15, which mainly include point A (0.4 Ω , 0.68 nF), point B (8.2 Ω , 0.68 nF), point C (3 Ω , 0.22 nF), and point D (3 Ω , 1.8 nF). Point A and point B are compared with point S when the snubber resistance R_{snb} is small or large. Point C and point D are compared with point S when snubber capacitance C_{snb} is small or large.

Fig. 16 shows a comparison of the oscillation suppression effect within the RC design region and outside the RC design region. As can be seen from Fig. 16(a), when R_{snb} is small (point A), v_{gs2} has a larger amplitude and a longer oscillation time. When R_{snb} is large (point B), v_{gs2} has a larger overshoot, which will be more likely to cause false triggering conduction. According to Fig. 16(b), when C_{snb} is small or large, the point S has a better oscillation suppression effect than the points C and D. Thus, these results show that the analytically designed RC

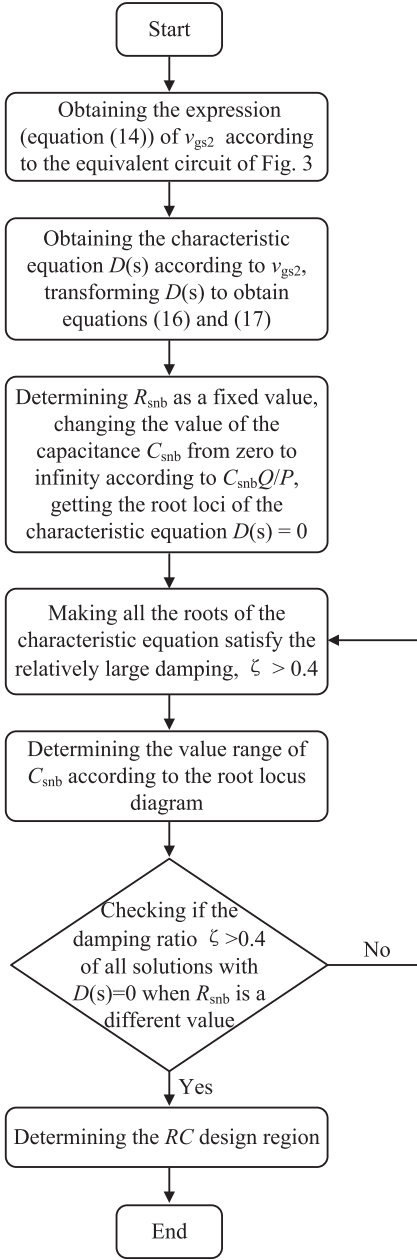


Fig. 13. Flowchart of the proposed RC design method.

snubber is more effective at suppressing oscillation when the RC parameters are within the region than outside of it.

B. Experimental Verification

An experimental prototype is built, as shown in Fig. 17. Its specifications and circuit parameters are the same as that listed in Table I. Similarly, the switching device is the EPC2015, the driver is the LM5114. In order to measure the switching current accurately, a coaxial current shunt (named SSDN-10) manufactured by T&M Research Products Inc. is adopted. The SSDN-10 has a high bandwidth (2000 MHz), small parasitic inductance (2 nH), and an accurate resistance (0.1 Ω); thus, it can be used to measure currents with very fast dynamic

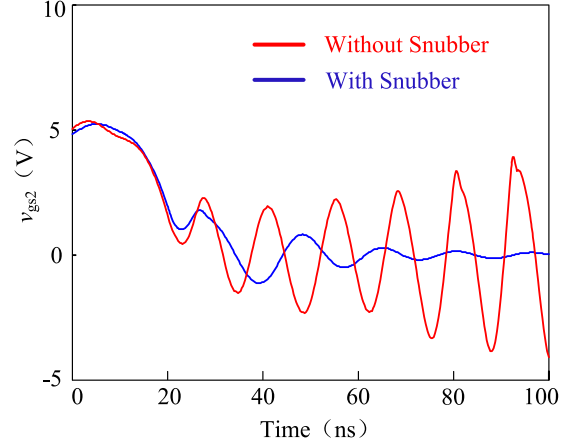
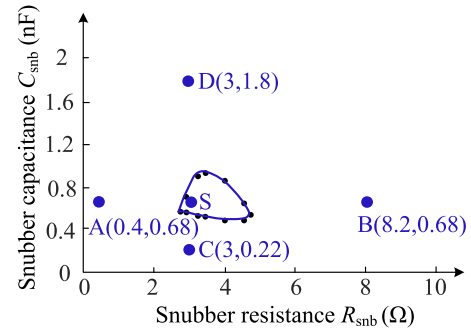
Fig. 14. Simulation waveform of v_{gs2} without and with the RC snubber.

Fig. 15. RC selection values outside the RC design region.

characteristics. Specific operation characteristic and schematic of the SSDN-10 are elaborated in [29] and [30].

Fig. 18 shows the experimental waveforms of v_{gs2} and i_D without the RC snubber and with the RC snubber. It can be seen that v_{gs2} will generate false triggering oscillation when there is no RC snubber circuit, which may affect operating reliability of the device. When the RC snubber is added, the false triggering oscillation can be significantly suppressed. Similar to the simulation, when $R_{snb} = 0.4 \Omega$ and $C_{snb} = 0.68 \text{ nF}$ (point A), $R_{snb} = 8.2 \Omega$ and $C_{snb} = 0.68 \text{ nF}$ (point B), $R_{snb} = 3 \Omega$ and $C_{snb} = 0.22 \text{ nF}$ (point C), and $R_{snb} = 3 \Omega$ and $C_{snb} = 1.8 \text{ nF}$ (point D), respectively, their suppression effect on oscillation is compared with that of $R_{snb} = 3 \Omega$ and $C_{snb} = 0.68 \text{ nF}$ (point S). Experimental results of the oscillation suppression effect within the RC design region and outside the RC design region are shown in Fig. 19. It can be seen that the RC value (point S) within the design region has a smaller oscillation amplitude and oscillation time than outside the design region. This result supports our conclusion that the better oscillation suppression effect can be obtained by an analytically designed RC snubber circuit.

As mentioned in this paper, RC snubber circuits are widely used to suppress the ringing of the drain-source voltage of the power loop. In this paper, we apply it to the driver loop to suppress the false triggering oscillation. Since the false triggering oscillation in this paper is a sixth-order system, the traditional RC design methods that mainly include second-order

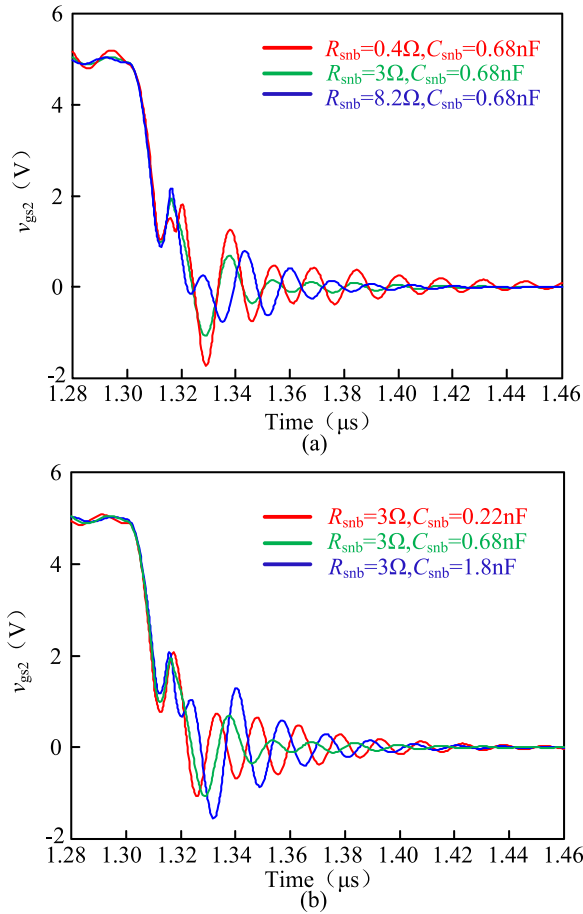


Fig. 16. Comparison of oscillation suppression effect within the RC design region and outside the RC design region. (a) Snubber resistance R_{snb} is 0.4, 3, and 8.2 Ω , respectively, when C_{snb} is 0.68 nF. (b) Snubber capacitance C_{snb} is 0.22, 0.68, and 1.8 nF, respectively, when R_{snb} is 3 Ω .

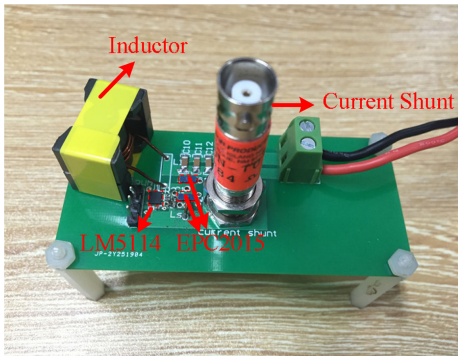


Fig. 17. Prototype of the double pulse test circuit.

design [19], [20] and third-order design [23], [24] are not applicable here. However, in order to verify the suppression effect of the traditional method and the proposed method on the false triggering oscillation, the proposed RC design method is compared with the two traditional RC design methods. The second-order design here is equivalent to not considering the influence of the power loop and does not distinguish between the gate inductance L_{G2} and the common source inductance

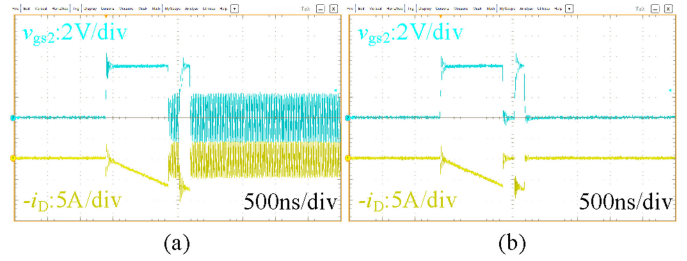


Fig. 18. Experimental results without RC snubber and with the RC snubber. (a) Without RC snubber. (b) With RC snubber.

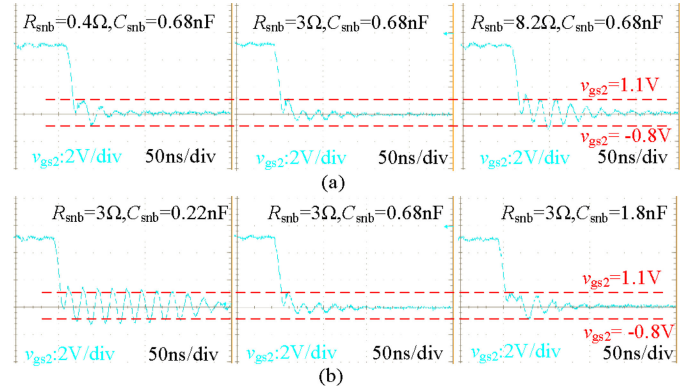


Fig. 19. Experimental results of oscillation suppression effect within the RC design region and outside the RC design region. (a) Snubber resistance R_{snb} is 0.4, 3, and 8.2 Ω , respectively, when C_{snb} is 0.68 nF. (b) Snubber capacitance C_{snb} is 0.22, 0.68, and 1.8 nF, respectively, when R_{snb} is 3 Ω .

L_{S2} . The third-order design here also does not take into account the influence of the power loop but distinguishes between L_{G2} and L_{S2} . However, the generation of false triggering oscillation is inseparable from the power loop, moreover, the magnitude of L_D and L_{G2} is comparative. Accordingly, obtaining the RC value of the snubber by the second-order or third-order design may lead to the oscillation suppression effect not good enough. In the second-order design, the RC snubber is designed using the following equations:

$$R_{snb}(s) = \frac{1}{2\zeta} \sqrt{\frac{L_p}{C_p}} \quad (20)$$

$$C_{snb}(s) = \frac{1}{2\pi R_{snb} f_r} \quad (21)$$

where ζ is the damping ratio, L_p is the parasitic inductance of the test circuit, which is the sum of L_{G2} and L_{S2} , C_p is the parasitic capacitance of the GaN device, and f_s is the oscillation frequency.

From (20) and (21), the RC values obtained by the second-order design are $R_{snb} = 1.5$ Ω and $C_{snb} = 1.8$ nF, which are outside our designed region. Similarly, in the third-order design, the values of RC are obtained by using the breakaway point to obtain a simultaneous equation. The obtained values are $R_{snb} = 1$ Ω and $C_{snb} = 10$ nF, which are also outside our designed region. The simulation and experimental results are shown in Fig. 20, it can be seen that the traditional RC design method has a certain

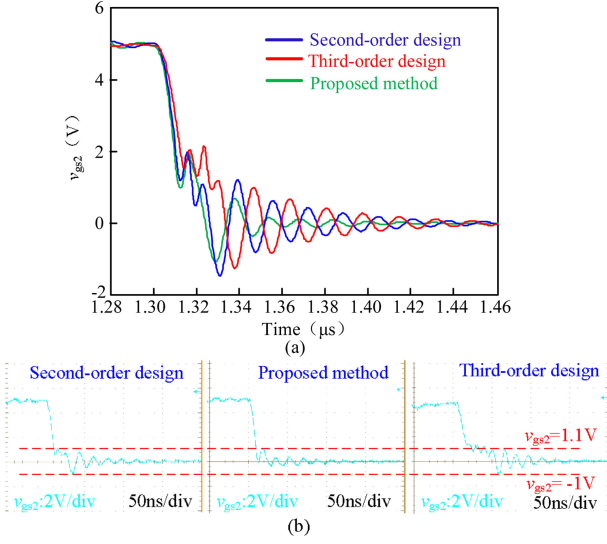


Fig. 20. Comparison of oscillation suppression effect among the second-order design, the third-order design, and the proposed method. (a) Simulation results. (b) Experimental results.

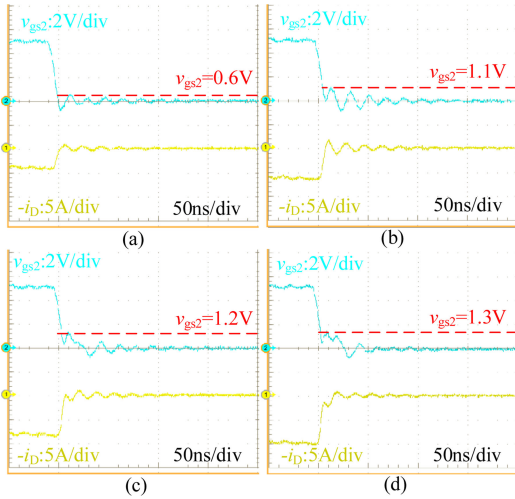


Fig. 21. False triggering oscillation suppression for the proposed RC design method under different inductor currents. (a) $I_L = 4$ A. (b) $I_L = 6$ A. (c) $I_L = 8$ A. (d) $I_L = 10$ A.

suppression effect on the false triggering oscillation. Compared with the traditional RC design method, the RC design method proposed in this paper has a smaller oscillation amplitude and oscillation time, which has better oscillation suppression effect.

Fig. 21 shows the suppression effect of the proposed RC design method on the false triggering oscillation under different inductor currents. It can be seen that when the inductor current changes from 4 to 10 A, the proposed RC design method can suppress the false triggering oscillation well.

V. CONCLUSION

In this paper, a design method for an RC snubber circuit is proposed to suppress false triggering oscillation in a half-bridge circuit. In the traditional analysis design, the RC design method can only be applied to systems with no more than three orders.

This paper proposes that the root locus method achieves optimal oscillation suppression in the sixth-order system. It can provide guidance for oscillation suppression design in high-order systems. The proposed method is verified by simulation and experiment. Moreover, the proposed RC design method is compared with the traditional RC design method, which proves that the proposed RC design region has better oscillation suppression effect. Accordingly, the proposed method indicates a substantial improvement of the switching characteristics of the controlled device at turn-OFF. In addition, the proposed oscillation suppression method is simpler, easier to implement, and more effective than the active gate driver.

APPENDIX

The coefficients in (14) are as follows:

$$\begin{aligned}
 a_0 &= C_{gd2}^2 C_{snb} L_D L_{G2} L_{S2} V_0 - C_{iss2} C_{oss2} C_{snb} L_D L_{G2} L_{S2} V_0 \\
 a_1 &= C_{gd2}^2 C_{snb} L_D L_{G2} R_{Gint} V_0 - C_{gd2} C_{snb} L_D L_{G2} L_{S2} I_0 \\
 &\quad + C_{gd2}^2 C_{snb} L_D L_{S2} R_{G2} V_0 + C_{gd2}^2 C_{snb} L_D L_{G2} R_{snb} V_0 \\
 &\quad + C_{gd2}^2 C_{snb} L_{G2} L_{E2} R_{Gint} V_0 \\
 &\quad + C_{gd2}^2 C_{snb} L_{G2} L_{S2} R_{loop} V_0 \\
 &\quad + C_{gd2}^2 C_{snb} L_D L_{S2} R_{snb} V_0 + C_{gd2}^2 C_{snb} L_{G2} L_{S2} R_{snb} V_0 \\
 &\quad - C_{iss2} C_{oss2} C_{snb} L_D L_{G2} R_{Gint} V_0 \\
 &\quad - C_{iss2} C_{oss2} C_{snb} L_D L_{S2} R_{G2} V_0 \\
 &\quad - C_{iss2} C_{oss2} C_{snb} L_D L_{G2} R_{snb} V_0 \\
 &\quad - C_{iss2} C_{oss2} C_{snb} L_{G2} L_{S2} R_{Gint} V_0 \\
 &\quad - C_{iss2} C_{oss2} C_{snb} L_{G2} L_{S2} R_{loop} V_0 \\
 &\quad - C_{iss2} C_{oss2} C_{snb} L_D L_{S2} R_{snb} V_0 \\
 &\quad - C_{iss2} C_{oss2} C_{snb} L_{G2} L_{S2} R_{snb} V_0 \\
 a_2 &= C_{gd2}^2 L_D L_{G2} V_0 + C_{gd2}^2 L_D L_{S2} V_0 + C_{gd2}^2 L_{G2} L_{S2} V_0 \\
 &\quad - C_{iss2} C_{oss2} L_D L_{G2} V_0 - C_{iss2} C_{oss2} L_D L_{S2} V_0 \\
 &\quad - C_{iss2} C_{oss2} L_{G2} L_{S2} V_0 \\
 &\quad + C_{gd2} C_{snb} L_{G2} L_{S2} V_0 - C_{iss2} C_{snb} L_{G2} L_{S2} V_0 \\
 &\quad - C_{gd2} C_{snb} L_D L_{G2} R_{Gint} I_0 \\
 &\quad - C_{gd2} C_{snb} L_D L_{S2} R_{G2} I_0 - C_{gd2} C_{snb} L_D L_{G2} R_{snb} I_0 \\
 &\quad - C_{gd2} C_{snb} L_{G2} L_{S2} R_{Gint} I_0 - C_{gd2} C_{snb} L_D L_{S2} R_{snb} I_0 \\
 &\quad - C_{gd2} C_{snb} L_{G2} L_{S2} R_{snb} I_0 \\
 &\quad - C_{oss2} C_{snb} L_{G2} L_{S2} R_{loop} I_0 \\
 &\quad + C_{gd2}^2 C_{snb} L_D R_{G2} R_{Gint} V_0 \\
 &\quad + C_{gd2}^2 C_{snb} L_{G2} R_{Gint} R_{loop} V_0 \\
 &\quad + C_{gd2}^2 C_{snb} L_D R_{G2} R_{snb} V_0 \\
 &\quad + C_{gd2}^2 C_{snb} L_D R_{Gint} R_{snb} V_0 \\
 &\quad + C_{gd2}^2 C_{snb} L_{S2} R_{G2} R_{Gint} V_0
 \end{aligned}$$

$$\begin{aligned}
& + C_{gd2}^2 C_{snb} L_{S2} R_{G2} R_{loop} V_0 \\
& + C_{gd2}^2 C_{snb} L_{G2} R_{loop} R_{snb} V_0 \\
& + C_{gd2}^2 C_{snb} L_{S2} R_{G2} R_{snb} V_0 \\
& + C_{gd2}^2 C_{snb} L_{S2} R_{Gint} R_{snb} V_0 \\
& + C_{gd2}^2 C_{snb} L_{S2} R_{loop} R_{snb} V_0 \\
& - C_{iss2} C_{oss2} C_{snb} L_D R_{G2} R_{Gint} V_0 \\
& - C_{iss2} C_{oss2} C_{snb} L_{G2} R_{Gint} R_{loop} V_0 \\
& - C_{iss2} C_{oss2} C_{snb} L_D R_{G2} R_{snb} V_0 \\
& - C_{iss2} C_{oss2} C_{snb} L_D R_{Gint} R_{snb} V_0 \\
& - C_{iss2} C_{oss2} C_{snb} L_{S2} R_{G2} R_{Gint} V_0 \\
& - C_{iss2} C_{oss2} C_{snb} L_{S2} R_{G2} R_{loop} V_0 \\
& - C_{iss2} C_{oss2} C_{snb} L_{G2} R_{loop} R_{snb} V_0 \\
& - C_{iss2} C_{oss2} C_{snb} L_{S2} R_{G2} R_{snb} V_0 \\
& - C_{iss2} C_{oss2} C_{snb} L_{S2} R_{Gint} R_{snb} V_0 \\
& - C_{iss2} C_{oss2} C_{snb} L_{S2} R_{loop} R_{snb} V_0 \\
a_3 = & C_{gd2}^2 L_D R_{G2} V_0 - C_{gd2} L_D L_{S2} I_0 \\
& - C_{gd2} L_{G2} L_{S2} I_0 \\
& - C_{snb} L_{G2} L_{S2} I_0 - C_{gd2} L_D L_{G2} I_0 \\
& + C_{gd2}^2 L_D R_{Gint} V_0 + C_{gd2}^2 L_{G2} R_{loop} V_0 \\
& + C_{gd2}^2 L_{S2} R_{G2} V_0 + C_{gd2}^2 L_{S2} R_{Gint} V_0 \\
& + C_{gd2}^2 L_{S2} R_{loop} V_0 \\
& - C_{iss2} C_{oss2} L_D R_{G2} V_0 - C_{iss2} C_{oss2} L_D R_{Gint} V_0 \\
& - C_{iss2} C_{snb} L_{G2} R_{Gint} V_0 \\
& - C_{iss2} C_{oss2} L_{G2} R_{loop} V_0 - C_{iss2} C_{oss2} L_{S2} R_{G2} V_0 \\
& - C_{iss2} C_{oss2} L_{S2} R_{Gint} V_0 \\
& + C_{gd2} C_{snb} L_{S2} R_{G2} V_0 - C_{iss2} C_{snb} L_{S2} R_{G2} V_0 \\
& - C_{iss2} C_{snb} L_{G2} R_{snb} V_0 \\
& - C_{iss2} C_{oss2} L_{S2} R_{loop} V_0 + C_{gd2} C_{snb} L_{S2} R_{snb} V_0 \\
& - C_{iss2} C_{snb} L_{S2} R_{snb} V_0 \\
& - C_{gd2} C_{snb} L_D R_{G2} R_{Gint} I_0 \\
& - C_{gd2} C_{snb} L_D R_{G2} R_{snb} I_0 \\
& - C_{gd2} C_{snb} L_D R_{Gint} R_{snb} I_0 \\
& - C_{gd2} C_{snb} L_{S2} R_{G2} R_{Gint} I_0 \\
& - C_{gd2} C_{snb} L_{S2} R_{G2} R_{snb} I_0 \\
& - C_{gd2} C_{snb} L_{S2} R_{Gint} R_{snb} I_0 \\
& - C_{oss2} C_{snb} L_{S2} R_{G2} R_{loop} I_0 \\
& - C_{oss2} C_{snb} L_{S2} R_{loop} R_{snb} I_0
\end{aligned}$$

$$\begin{aligned}
& + C_{gd2}^2 C_{snb} R_{G2} R_{Gint} R_{loop} V_0 \\
& + C_{gd2}^2 C_{snb} R_{G2} R_{loop} R_{snb} V_0 \\
& + C_{gd2}^2 C_{snb} R_{Gint} R_{loop} R_{snb} V_0 \\
& - C_{iss2} C_{oss2} C_{snb} R_{G2} R_{Gint} R_{loop} V_0 \\
& - C_{iss2} C_{oss2} C_{snb} R_{G2} R_{loop} R_{snb} V_0 \\
& - C_{iss2} C_{oss2} C_{snb} R_{Gint} R_{loop} R_{snb} V_0 \\
a_4 = & C_{gd2} L_{S2} V_0 - C_{iss2} L_{G2} V_0 \\
& - C_{iss2} L_{S2} V_0 - C_{gd2} L_D R_{G2} I_0 \\
& - C_{gd2} L_D R_{Gint} I_0 - C_{gd2} L_{S2} R_{G2} I_0 \\
& - C_{gd2} L_{S2} R_{Gint} I_0 - C_{snb} L_{S2} R_{G2} I_0 \\
& - C_{oss2} L_{S2} R_{loop} I_0 - C_{snb} L_{S2} R_{snb} I_0 \\
& + C_{gd2}^2 R_{G2} R_{loop} V_0 \\
& + C_{gd2}^2 R_{Gint} R_{loop} V_0 - C_{iss2} C_{snb} R_{G2} R_{Gint} V_0 \\
& - C_{iss2} C_{oss2} R_{G2} R_{loop} V_0 \\
& - C_{iss2} C_{oss2} R_{Gint} R_{loop} V_0 - C_{iss2} C_{snb} R_{G2} R_{snb} V_0 \\
& - C_{iss2} C_{snb} R_{Gint} R_{snb} V_0 \\
a_5 = & -L_{S2} I_0 - C_{iss2} R_{G2} V_0 - C_{iss2} R_{Gint} V_0 \\
b_0 = & C_{gd2}^2 C_{snb} L_D L_{G2} L_{S2} - C_{iss2} C_{oss2} C_{snb} L_D L_{G2} L_{S2} \\
b_1 = & C_{gd2}^2 C_{snb} L_D L_{G2} R_{Gint} + C_{gd2}^2 C_{snb} L_D L_{S2} R_{G2} \\
& + C_{gd2}^2 C_{snb} L_D L_{G2} R_{snb} + C_{gd2}^2 C_{snb} L_{G2} L_{S2} R_{Gint} \\
& + C_{gd2}^2 C_{snb} L_{G2} L_{S2} R_{loop} + C_{gd2}^2 C_{snb} L_D L_{S2} R_{snb} \\
& + C_{gd2}^2 C_{snb} L_{G2} L_{S2} R_{snb} \\
& - C_{iss2} C_{oss2} C_{snb} L_D L_{G2} R_{Gint} \\
& - C_{iss2} C_{oss2} C_{snb} L_D L_{S2} R_{G2} \\
& - C_{iss2} C_{oss2} C_{snb} L_D L_{G2} R_{snb} \\
& - C_{iss2} C_{oss2} C_{snb} L_{G2} L_{S2} R_{Gint} \\
& - C_{iss2} C_{oss2} C_{snb} L_{G2} L_{S2} R_{loop} \\
& - C_{iss2} C_{oss2} C_{snb} L_D L_{S2} R_{snb} \\
& - C_{iss2} C_{oss2} C_{snb} L_{G2} L_{S2} R_{snb} \\
& - C_{gd2} C_{snb} L_D L_{G2} L_{S2} g_m \\
b_2 = & C_{gd2}^2 L_D L_{G2} + C_{gd2}^2 L_D L_{S2} + C_{gd2}^2 L_{G2} L_{S2} \\
& - C_{iss2} C_{oss2} L_D L_{G2} \\
& - C_{oss2} C_{snb} L_D L_{G2} - C_{iss2} C_{oss2} L_D L_{S2} \\
& - C_{iss2} C_{oss2} L_{G2} L_{S2} \\
& + 2C_{gd2} C_{snb} L_{G2} L_{S2} - C_{iss2} C_{snb} L_{G2} L_{S2} \\
& - C_{oss2} C_{snb} L_{G2} L_{S2} \\
& + C_{gd2}^2 C_{snb} L_D R_{G2} R_{Gint} + C_{gd2}^2 C_{snb} L_{G2} R_{Gint} R_{loop}
\end{aligned}$$

$$\begin{aligned}
& - C_{iss2}C_{oss2}L_{G2}L_{S2})s^4 + (C_{gd2}^2L_D R_{G2} \\
& + C_{gd2}^2L_D R_{Gint} + C_{gd2}^2L_{G2}R_{loop} \\
& + C_{gd2}^2L_{S2}R_{G2} + C_{gd2}^2L_{S2}R_{Gint} \\
& + C_{gd2}^2L_{S2}R_{loop} - C_{iss2}C_{oss2}L_D R_{G2} \\
& - C_{iss2}C_{oss2}L_D R_{Gint} \\
& - C_{iss2}C_{oss2}L_{G2}R_{loop} - C_{iss2}C_{oss2}L_{S2}R_{G2} \\
& - C_{iss2}C_{oss2}L_{S2}R_{Gint}C_{iss2}C_{oss2}L_{S2}R_{loop} \\
& - C_{gd2}L_D L_{G2}g_m - C_{gd2}L_D L_{S2}g_m \\
& - C_{gd2}L_{G2}L_{S2}g_m)s^3 \\
& + (2C_{gd2}L_{S2} - C_{oss2}L_D - C_{iss2}L_{G2} \\
& - C_{iss2}L_{S2} - C_{oss2}L_{S2} + C_{gd2}^2R_{G2}R_{loop} \\
& + C_{gd2}^2R_{Gint}R_{loop} - C_{iss2}C_{oss2}R_{G2}R_{loop} \\
& - C_{iss2}C_{oss2}R_{Gint}R_{loop} - C_{gd2}L_D R_{G2}g_m \\
& - C_{gd2}L_D R_{Gint}g_m - C_{gd2}L_{G2}R_{loop}g_m \\
& - C_{gd2}L_{S2}R_{G2}g_m - C_{gd2}L_{S2}R_{Gint}g_m \\
& - C_{gd2}L_{S2}R_{loop}g_m)s^2 + (-L_{S2}g_m \\
& - C_{iss2}R_{G2} - C_{iss2}R_{Gint} - C_{oss2}R_{loop} \\
& - C_{gd2}R_{G2}R_{loop}g_m - C_{gd2}R_{Gint}R_{loop}g_m)s - 1 \\
Q = & (C_{gd2}^2L_D L_{G2}L_{S2} - C_{iss2}C_{oss2}L_D L_{G2}L_{S2})s^6 \\
& + (C_{gd2}^2L_D L_{G2}R_{Gint} + C_{gd2}^2L_D L_{S2}R_{G2} \\
& + C_{gd2}^2L_D L_{G2}R_{snb} \\
& + C_{gd2}^2L_{G2}L_{S2}R_{Gint} + C_{gd2}^2L_{G2}L_{S2}R_{loop} \\
& + C_{gd2}^2L_D L_{S2}R_{snb} \\
& + C_{gd2}^2L_{G2}L_{S2}R_{snb} - C_{iss2}C_{oss2}L_E L_{G2}R_{Gint} \\
& - C_{iss2}C_{oss2}L_D L_{S2}R_{G2} \\
& - C_{iss2}C_{oss2}L_D L_{G2}R_{snb} - C_{iss2}C_{oss2}L_{G2}L_{S2}R_{Gint} \\
& - C_{iss2}C_{oss2}L_{G2}L_{S2}R_{loop} \\
& - C_{iss2}C_{oss2}L_D L_{S2}R_{snb} - C_{iss2}C_{oss2}L_{G2}L_{S2}R_{snb} \\
& - C_{gd2}L_D L_{G2}L_{S2}g_m)s^5 \\
& + (2C_{gd2}L_{G2}L_{S2} - C_{oss2}L_D L_{G2} - C_{iss2}L_{G2}L_{S2} \\
& - C_{oss2}L_{G2}L_{S2} \\
& + C_{gd2}^2L_D R_{G2}R_{Gint} + C_{gd2}^2L_{G2}R_{Gint}R_{loop} \\
& + C_{gd2}^2L_D R_{G2}R_{snb} \\
& + C_{gd2}^2L_D R_{Gint}R_{snb} + C_{gd2}^2L_{S2}R_{G2}R_{Gint} \\
& + C_{gd2}^2L_{S2}R_{G2}R_{loop} \\
& + C_{gd2}^2L_{G2}R_{loop}R_{snb} + C_{gd2}^2L_{S2}R_{G2}R_{snb} \\
& + C_{gd2}^2L_{S2}R_{Gint}R_{snb} \\
& + C_{gd2}^2L_{S2}R_{loop}R_{snb} - C_{iss2}C_{oss2}L_D R_{G2}R_{Gint} \\
& - C_{iss2}C_{oss2}L_D R_{G2}R_{snb} - C_{iss2}C_{oss2}L_D R_{Gint}R_{snb} \\
& - C_{iss2}C_{oss2}L_{S2}R_{G2}R_{Gint} \\
& - C_{iss2}C_{oss2}L_{S2}R_{G2}R_{loop} - C_{iss2}C_{oss2}L_{S2}R_{Gint}R_{snb} \\
& - C_{iss2}C_{oss2}L_{S2}R_{loop}R_{snb} - C_{gd2}L_D L_{G2}R_{Gint}g_m \\
& - C_{gd2}L_D R_{G2}R_{snb}g_m - C_{gd2}L_{G2}R_{Gint}R_{loop}g_m \\
& - C_{gd2}L_{S2}R_{G2}R_{snb}g_m - C_{gd2}L_{S2}R_{Gint}R_{snb}g_m \\
& - C_{gd2}L_{S2}R_{loop}R_{snb}g_m)s^3 \\
& + (-L_{G2} - C_{iss2}R_{G2}R_{Gint} \\
& - C_{oss2}R_{G2}R_{loop} \\
& - C_{iss2}R_{G2}R_{snb} - C_{iss2}R_{Gint}R_{snb} \\
& - C_{oss2}R_{loop}R_{snb} \\
& - L_{S2}R_{G2}g_m - L_{S2}R_{snb}g_m \\
& - C_{gd2}R_{G2}R_{Gint}R_{loop}g_m \\
& - C_{gd2}R_{G2}R_{loop}R_{snb}g_m - C_{gd2}R_{Gint}R_{loop}R_{snb}g_m)s^2 \\
& + (-R_{G2} - R_{snb})s.
\end{aligned}$$

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