Analysis and Design of a Novel Thyristor-Based Circuit Breaker for DC Microgrids

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***Abstract*—DC microgrids have attracted increasing concern in industrial applications due to a simple and efficient integration with renewable energy sources, battery energy storage, and variable speed generators and motors. However, extensive application of dc architecture is still restricted by fault protection challenges posed by the absence of natural current zero-crossing. This paper has proposed a novel thyristor-based dc circuit breaker with a one-shot triggering commutating circuit, which maintains a compact size as no additional power supply is required to precharge the commutating capacitors. Considering di/dt limitation of the triggering thyristor in the commutating circuit, a saturable inductor is utilized to avoid hot spot failure in the thyristor. Moreover, saturation characteristic of the inductor allows a sharp-rising commutating current which can provide zero-crossing for the main thyristor with a shorter delay. A real-time analog protecting unit is also introduced to interrupt fault current accurately and rapidly. Furthermore, detailed breaker topology analysis and circuit design guidelines are provided through mathematical modeling. Finally, the proposed breaker design method is verified by simulation studies over two cases and further validated by a 400 V/4 kW laboratory prototype.**

***Index Terms*—Analog processing circuits, circuit breakers, circuit topology, microgrids, power system protection.**

I. Introduction

DIRECT current microgrids and power distribution are showing attractive features with the development of power electronics. First, lots of renewable energy sources, such as photovoltaics and fuel cells, are inherently dc sources. The integration of such sources is much easier and more efficient for a dc architecture as no conversion from dc to ac is needed [1], [2]. Second, when variable speed generators and motor loads interface with a dc grid instead of a 50/60 Hz ac one, frequency synchronization is no longer required, and thus their speed can be optimized for power efficiency [3], [4]. Additionally, dc systems are rather convenient for embedding readily available energy storage devices, which can provide essential voltage and power support for grids with relatively weak power sources and impact loads, such as a marine power grid [5], [6]. Furthermore, dc distribution possesses a much larger power transfer capability limited by voltage stability than ac distribution [7]. These features have promoted dc applications in urban transportation, data centers, and marine vessels [8]–[14].

However, the lack of a natural voltage or current zero-crossing is still an obstacle restricting further application of dc grid. Unlike ac systems, using a mechanical breaker to interrupt dc fault current typically causes arc erosion due to the absence of a natural zero-crossing, thus leading to a higher maintenance cost and complexity [2], [8]. Moreover, the smaller impedance in dc lines usually brings a sharper rising fault current, which can exceed the power rating of semiconductor-based converters in tens of microseconds [15]. Therefore, an arcless breaker with fast tripping response is needed for dc fault protection and can further improve the cost-effectiveness and extensive application of dc grids, especially for dc microgrids.

Semiconductor switches can well meet this requirement with a rapid arcless interruption. Solid-state dc breakers were first introduced using half-controlled thyristors requiring a commutating circuit to trip the main thyristor [16]–[20], followed by breakers using full-controlled power electronic devices, such as gate turn-off thyristors (GTOs) and insulated gate bipolar transistors (IGBTs) [21]–[23]. Compared with full-controlled-switch-based breakers, thyristor-based circuit breakers (TBCBs) maintain smaller ON-state resistances and stronger tolerance to current and voltage surges [24], but need extra commutating circuits. Such commutating circuits can be roughly divided into three categories: 1) active circuit with additional power supply [16], [17]; 2) passive circuit with tripping switches and energy storage elements, such as capacitors and inductors [18]–[20]; 3) Z-source-type passive circuit which can automatically respond to fault current [2], [11]–[14]. Compared with the first type of breaker, the last two types do not require additional power supply, thus decreasing costs and control complexity. Z-source breakers can perform an automatic interruption but may malfunction to load variations, which limits the application. It is easy for the second type of TBCBs to integrate more flexible protecting rules as well as guarantee a reliable fault isolation.

The previously proposed two-stage TBCB uses three thyristors in the commutating circuit and two switching operations

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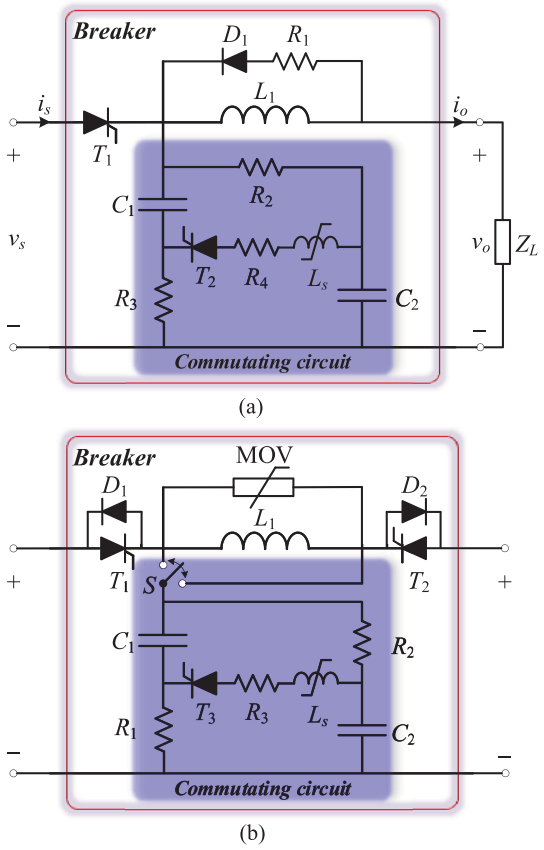

Fig. 1. Novel thyristor-based circuit breaker. (a) Unidirectional topology. (b) Bidirectional topology.

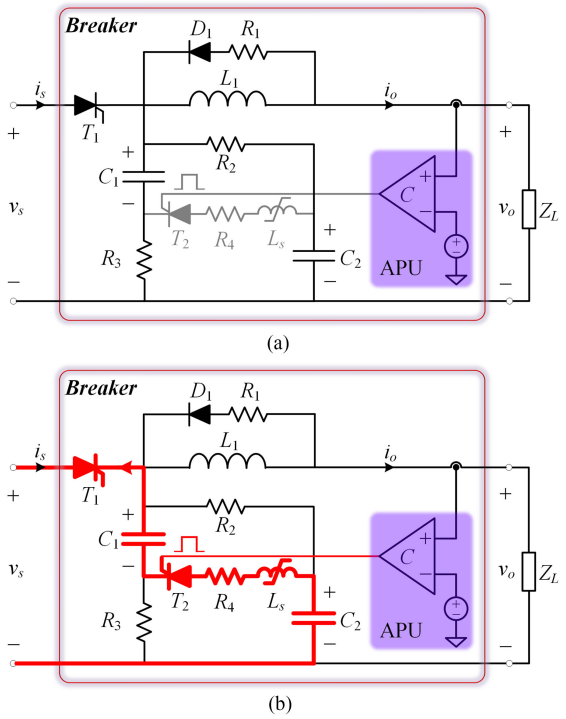

Fig. 2. Proposed breaker with an analog protecting unit during. (a) Normal operation. (b) Protecting operation.

to isolate fault with a decreased interrupting overvoltage [18]. However, the switching between the two stages needs extra state detection, leading to a complex interrupting control and more response time. Also, the dependence on the source inductance will limit its application only to load protections with long feeding cables. Other proposed TBCBs with a passive commutating circuit are also based on the commutation-forced turn-OFF principle using parallel capacitors [5], [19], [20]. Compared with the two-stage TBCB, these breakers are easier to design and control. However, the tripping of the main thyristor will introduce a current surge to the feeding side, which usually needs an oversized limiting inductor to keep the surge under permitted level. Also, turn-ON di/dt of thyristors in the commutating circuit has not been properly limited, which may cause hot spots and result in thyristor failure [25].

A novel TBCB oriented toward dc microgrid protection with an easy-controlled passive commutating circuit is proposed in this paper, as illustrated in Fig. 1. Using only one main inductor (L_1) and two capacitors (C_1 and C_2) for both unidirectional and bidirectional topology, this breaker can provide a more compact size and better OFF-state isolation compared with the existing passive TBCBs [5], [19]. A saturable inductor is adopted to avoid hot spot in the commutation thyristor (T_2 or T_3). Moreover, tripping with one-shot triggering makes it possible for the breaker to be controlled by an all-analog circuit with a submicrosecond delay, thus interrupting fault current rapidly and accurately. The bidirectional topology in Fig. 1(b) allows power flow in both directions with two diodes (D_1 and D_2) antiparallel to the main thyristors (T_1 and T_2). Contactor S should switch to the left contact when power flow is from left to right while to the right contact for flow in the opposite direction. Then, both topologies in Fig. 1 are based on the same operating principle, so circuit analysis and design method in the following paper will just focus on the unidirectional one. Breaker topology and a simple analog-protecting unit are first introduced in Section II. Based on detailed mathematical modeling, Section III proceeds with the discussion on circuit design and component sizing. In Section IV, two design cases are carried out and verified by SPICE simulation and laboratory experiments following the design guidelines provided in Section III. Finally, practical considerations are discussed in Section V.

II. Proposed Breaker With Real-Time Protection

The proposed breaker contains two thyristors T_1 and T_2, as illustrated in Fig. 2. T_1 is in the main path for fault isolation. T_2 locates in the commutating circuit as a trigger to generate reverse voltage and current needed for T_1 blocking, with a saturable inductor L_s limiting the turn-ON di/dt. Considering fault current of a critical dc short-circuit may increase very sharply and go beyond the blocking capability of T_1 even before the zero-crossing, an inductor L_1 is applied in the main path to limit the fault current rising. A real-time analog protecting unit (APU), made up of a comparator circuit, can be adopted to shorten the response time of the breaker. Moreover, D_1 and R_1 compose the snubber circuit, which can provide a low-resistance channel for reversed voltage impulses on L_1 to guard T_1 against severe voltage spikes.

During the normal operation, T_1 is ON while T_2 is OFF, as illustrated in Fig. 2(a). Both C_1 and C_2 are fully charged and keep

the same voltage level as the source. Hence, T_2 is forward biased by the voltage of C_2. With an APU, the main path current is continuously sensed and compared with a preset threshold. When a short-circuit or overcurrent fault occurs, the output current will increase and exceed the threshold value. Then, the APU will generate a T_2 triggering signal, which will be further amplified by the thyristor driver to turn ON T_2, as illustrated in Fig. 2(b). After that, C_1 and C_2 will be connected in series, and their total voltage is nearly twice of the source voltage. Consequently, T_1 will get reverse biased. A large transient discharge current, which is produced from C_1 and C_2 and limited by L_s and R_4, will flow reversely through T_1 and force its current to cross zero. As a result, T_1 turns OFF and isolates the fault. With saturable inductor L_s, the discharging current will increase at a limited rate before the saturation point, leaving time for propagation of conduction across the thyristor junction. After that, a sharp current rise will be allowed to offer T_1 a zero-crossing. After tripping, a resonance will start among the breaker passive circuit and the fault path. All the energy stored in the inductors and capacitors will be consumed by circuit resistors, mainly R_1 and R_4, so power resistors with a good performance for high peak power and high-energy pulses should be selected, such as noninductive ceramic resistors.

III. Circuit Analysis and Component Sizing

In this section, protection mechanism of the proposed breaker is modeled and analyzed in detail. Mathematical model is established to analyze the fault isolation and provide design guidelines for component sizing. To simplify the analysis, ON-state voltage drops of thyristors, internal resistance and saturation effect of inductor L_1, as well as time delay of the APU and thyristor driver are all neglected. Also, by selecting L_s with proper saturation current and a much smaller inductance than L_1, typically 5%–10% the rated current of T_2 and 5%–10% the inductance of L_1, the combination of T_2 and L_s can be simplified as an ideal switch. Detailed design of L_s can refer to [26] and [27].

A. Fault Protection Modeling

The most severe dc fault is the short-circuit fault because of the highest current rising rate. The isolation must be rapid enough to prevent the current exceeding the blocking capability of the breaker. Therefore, a short-circuit fault at the output port is considered in the following design, as shown in Fig. 3.

According to the overload capacity of power source and load circuit, current protecting threshold I_{th} can be determined. This threshold is usually a little larger than the rated value. Once it is exceeded by the output current in a short-circuit condition, the APU will instantly trigger thyristor T_2 and turn it ON. At this moment, the inductor current equals to I_{th}, while capacitors C_1 and C_2 both maintain the source voltage V_s. In this design, C_1 and C_2 are selected with the same capacitance C, considering their same function. Similarly, R_2 and R_3 maintain the same resistance R. All the variables are defined with polarities illustrated in Fig. 3.

According to Kirchhoff's voltage law (KVL), one can obtain

$$V_s = L_1 \frac{di_1}{dt}. \tag{1}$$

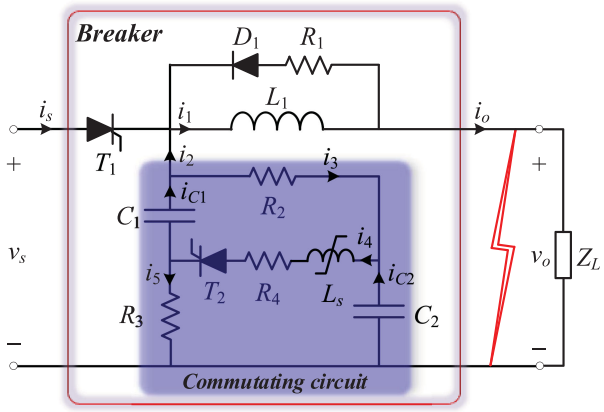

Fig. 3. Fault protection modeling under short-circuit condition.

Solving (1) with the initial current I_{th} yields

$$i_1 = I_{th} + \frac{V_s}{L_1} t. \tag{2}$$

So i_1 keeps rising at a constant rate until T_1 turns off. Then i_2 still remains to be solved. Due to the symmetry of the commutating circuit, it can be derived by Kirchhoff's current law (KCL) and KVL

$$\begin{cases} i_3 = i_5 \\ i_{C1} = i_{C2}. \end{cases} \tag{3}$$

In the commutating circuit, KVL also states

$$\begin{cases} V_s = V_{C0} - \frac{1}{C}\int_0^t i_{C1} d\tau + R i_5 \\ V_{C0} - \frac{1}{C}\int_0^t i_{C1} d\tau = R i_3 + R_4 i_4 \end{cases} \tag{4}$$

where V_{C0} indicates the initial voltage of two capacitors and equals to V_s.

It can be further obtained by KCL

$$i_5 = i_4 - i_{C1}. \tag{5}$$

Substitution of (3) and (5) into (4) leads to the differential equation

$$\frac{di_{C1}}{dt} + \frac{2R + R_4}{RR_4C} i_{C1} = 0. \tag{6}$$

Deriving the initial current of i_{C1} with (3), (4), and (5) and solving (6), one obtains

$$i_{C1} = \frac{V_s}{R_4} e^{-\frac{2R+R_4}{RR_4C}t}. \tag{7}$$

Substituting (3) and (7) into (4), i_3 can be derived as

$$i_3 = \frac{V_s}{2R + R_4}\left(1 - e^{-\frac{2R+R_4}{RR_4C}t}\right). \tag{8}$$

Then, according to KCL

$$i_2 = i_{C1} - i_3 = -\frac{V_s}{2R + R_4} + \frac{2V_s(R + R_4)}{R_4(2R + R_4)} e^{-\frac{2R+R_4}{RR_4C}t} \tag{9}$$

which indicates that i_2 decreases exponentially with time.

Because diode D_1 in the snubber circuit remains reverse biased, the source current, also the current of thyristor T_1, can

be calculated as

$$i_s = i_1 - i_2. \tag{10}$$

Considering that a large discharge current is necessary for current zero-crossing, we should choose R_4 with a much smaller resistance than R. Substituting (2) and (9) into (10), i_s can be further simplified as

$$i_s \approx I_{th} + \frac{V_s}{L_1}t + \frac{V_s}{2R} - \frac{V_s}{R_4}e^{-\frac{2}{R_4C}t}. \tag{11}$$

From (11), we know that i_s increases with time. To turn OFF T_1, i_s must have a negative initial value and remain negative until T_1 finishes its reverse recovery. Typically, this recovery time is a little shorter than the rated thyristor turn-OFF time t_q. Therefore, reliable turn-OFF of T_1 can be guaranteed by

$$i_s|_{t=t_q} = I_{th} + \frac{V_s}{L_1}t_q + \frac{V_s}{2R} - \frac{V_s}{R_4}e^{-\frac{2}{R_4C}t_q} \le 0. \tag{12}$$

Referring to (12), L_1 should satisfy the inequality

$$L_1 \ge \frac{V_s t_q}{\frac{V_s}{R_4}e^{-\frac{2}{R_4C}t_q} - \frac{V_s}{2R} - I_{th}}. \tag{13}$$

To design the breaker with a more compact size, the partial derivative of (13) with respect to the R_4 is taken, which reveals that the minimum of L_1 exists only when

$$R_4 C = 2t_q. \tag{14}$$

And the corresponding minimum inductance needed is

$$L_{\min} = \frac{V_s t_q}{\frac{V_s}{R_4}e^{-1} - \frac{V_s}{2R} - I_{th}}. \tag{15}$$

As the inductance must be a positive value, the denominator of (15) must be greater than zero, which leads to

$$R_4 < \frac{2RV_s e^{-1}}{V_s + 2RI_{th}}. \tag{16}$$

Once R_4 is selected, L_1 and C can be chosen as

$$\begin{cases} L_1 \ge \frac{V_s t_q}{\frac{V_s}{R_4}\mathrm{e}^{-1} - \frac{V_s}{2R} - I_{th}} \\ C \ge \frac{2t_q}{R_4}. \end{cases} \tag{17}$$

From (17), both L_1 and C are directly proportional to t_q. Therefore, adopting a fast recovery thyristor in the main path can not only accelerate the tripping speed but also considerably reduce the breaker size. Moreover, delays of the current sensor, APU, and thyristor driver are all neglected here because they are much smaller than t_q. However, APU can only offer simple threshold protection and is not the only option for controllers. It is also possible for the proposed breaker topology to adopt a digital controller, such as a field-programmable gate array (FPGA) or digital signal processor (DSP), which is suitable for rather complex load conditions and fault types; however, since it requires A/D conversion, the nonnegligible delays caused by A/D conversion and digital signal sampling and processing should be considered and added into t_q. Furthermore, the proposed breaker topology can also operate as a dc switch, which means manual tripping of the breaker and coordinated protection between breakers are both allowed. If the proposed breaker is used in complicated networks under a centralized or distributed control structure, then the communication time delays should be further counted into t_q.

In summary, the proposed breaker can be designed with the following guidelines:

1) Determine the current threshold I_{th} considering the overload capacity of power source and load circuit and design the control circuit. If a threshold protection can well meet the requirement, APU-based controller is recommended.
2) Select semiconductor devices according to the power rating (typically with $U_{\mathrm{DRM}} \ge 2V_s$ and $I_{T(AV)M} > I_{th}$) and efficiency requirement. If efficiency is less important than a compact size or a rapid tripping, a fast recovery thyristor is the first choice for T_1. A cheaper thyristor with enough surge capability is suggested for T_2 especially for high-power applications.
3) Choose R_1 with a resistance less than 20% of the load resistance to bypass the overvoltage on T_1; choose R (R_2 and R_3) as 5–20 times the load resistance to limit the capacitor charging current when starting or reenergizing the breaker.
4) Determine R_4, L_1, and C (C_1 and C_2) referring to (16) and (17), where the saturation current of L_1 should be greater than

$$i_{\mathrm{sat}} = I_{th} + \frac{V_s}{L_1}t_q. \tag{18}$$

B. Voltage Transfer Function

To ensure a stable voltage transfer characteristic, voltage transfer function of the proposed breaker is derived here.

In the normal operation state, diode D_1 in the snubber circuit is maintained reverse biased. According to KVL,

$$v_s(s) = sL_1 i_1(s) + v_o(s). \tag{19}$$

On the load side, Ohm's law states

$$v_o(s) = Z_L i_1(s). \tag{20}$$

Combining (19) and (20) together leads to the input–output voltage transfer function

$$\frac{v_o(s)}{v_s(s)} = \frac{Z_L}{sL_1 + Z_L}. \tag{21}$$

From (21), the voltage transfer function shows a first-order low-pass characteristic when the load is resistive, as illustrated in Fig. 4. The proposed breaker features unity gain at low frequencies and decaying gain at high frequencies, which is preferred especially for applications with filtering requirements [2], [5].

IV. Breaker Design and Verification

In this section, two breaker cases are designed following the provided guidelines and verified by SPICE simulation and laboratory experiments. Since SPICE-embedded thyristor model inherits an exaggerated reverse recovery current for forced-commutated applications [28], modified thyristor model in [29] is applied in the following simulation to provide a more accurate result.

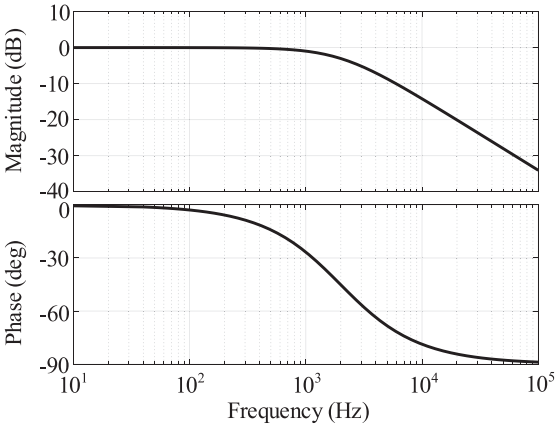

Fig. 4. Low-pass voltage transfer characteristic of the proposed breaker.

A. Low-Voltage Design

DC microgrids have already been applied in commercial buildings with a voltage of 380 V [30], [31]. A 400 V/4 kW breaker is first designed to validate the performance of the commutating circuit and APU. The rated current is 10 A with a resistive load of 40 Ω, and I_{th} here is set to 12 A (for illustrative purpose), i.e., 120% of the rated current. To provide a fast protection, thyristors were selected as high-frequency thyristor (KG30A-800 V) with a turn-OFF time $t_q = 20\,\mu$s. Following design guidelines in Section III, the rest circuit components were chosen with parameters listed in Table I. Saturation current of L_s is 2 A.

According to the design, a maximum overload of 20% is allowed for this breaker. Hence, three tests were performed by introducing a 13% overload, 80% overload, and output short-circuit, respectively. The SPICE simulation results are shown in Fig. 5.

The 13% overload test was carried out by paralleling a 300 Ω resistor to the 40 Ω load resistor. The simulation waveform is shown in Fig. 5(a). When the extra load is added, output resistance decreases immediately. As the inductor current cannot leap, the output voltage shows a sag. After that, the output current as well as the source current increases to 11.3 A, which is still lower than I_{th} without triggering the breaker.

For the 80% overload test, a 50 Ω resistor was paralleled to the 40 Ω load resistor. As shown in Fig. 5(b), a deeper sag appears on the output voltage, followed by the output current surge. After T_1 turns OFF, rest energy left in the commutating circuit and L_1 will swing between the load and commutating circuit, which arises surges in the output current and voltage. Such surges are sometimes unfavorable and can be reduced by properly increasing the resistance of R_4 or the ratio of $R_4/R_{\rm L}$, which also means a large L_1 and smaller C_1 and C_2 according to (17), then breaker volume and cost should be evaluated and within the restriction. Furthermore, paralleling a capacitor filter or a metal oxide varistor (MOV) to the load can also well suppress the load voltage surge. For this design, the voltage peak is 722 V for no suppression and can be reduced to 600 and 499 V by using a 20D471K MOV and 40 μF capacitor, respectively. During the interruption, T_1 voltage remains negative for 280 μs to guarantee a reliable turn-OFF. Finally, the output voltage decays to zero, and T_1 withstands the whole dc voltage.

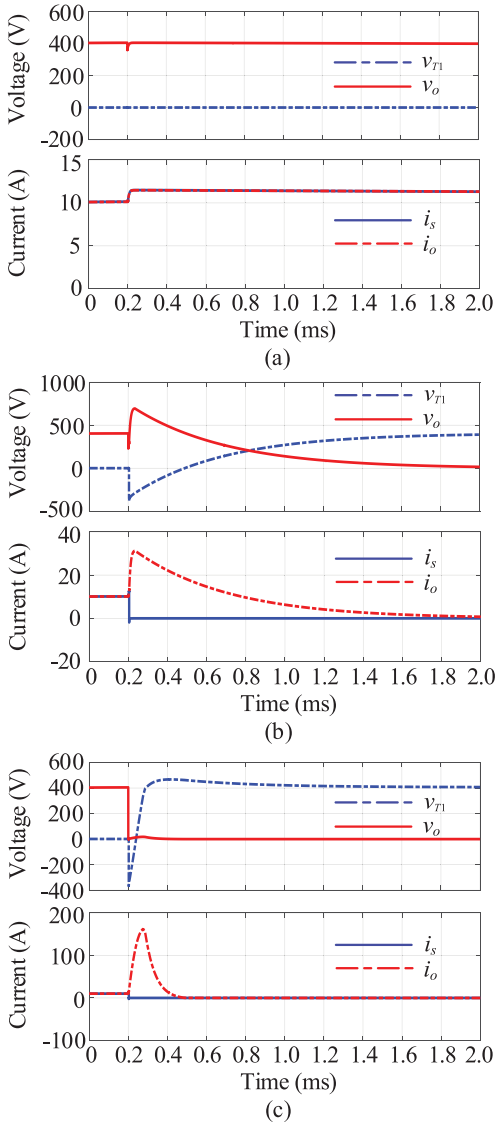

Fig. 5. Simulation waveforms of the 400 V/4 kW breaker for (a) 13% overload, (b) 80% overload, and (c) short-circuit fault.

The short-circuit test was realized with another thyristor to short the output. The result is shown in Fig. 5(c). As the output gets shorted, output voltage drops to zero followed by a higher output current surge with a peak of 187 A. However, this surge introduces little voltage surge due to the short-circuit and decays to zero in less than 250 μs. During the interruption, T_1 voltage remains negative for over 30 μs to guarantee a reliable turn-OFF and finally equals to the source voltage with a 20% overshoot.

B. Experimental Verification

A 400 V/4 kW experimental prototype of the proposed breaker has been built with the same parameters designed in Table I, as shown in Fig. 6. To endure current pulses and consume the residual energy after tripping, all resistors are selected as aluminum-housed resistors in the prototype. The APU is designed and implemented with analog devices. A LEM current

TABLE I
PARAMETERS OF THE 400 V/4 kW PROTOTYPE

R_1	$R_2(R_3)$	R_4	$C_1(C_2)$	L_1	L_s	Z_L
0.5 Ω	500 Ω	1 Ω	40 μF	200 μH	20 μH	40 Ω

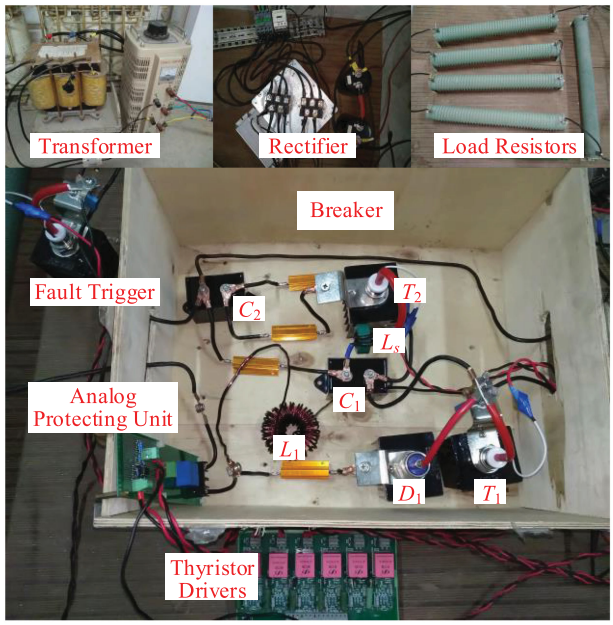

Fig. 6. Laboratory prototype of the proposed TBCB.

sensor LA25-NP using Hall effect is adopted for current sensing. LA25-NP produces a current signal, which is proportional to the output current and further transformed into a voltage signal with a resistor. A nano-farad or subnano-farad capacitor can be added parallel to the resistor to filtering high-frequency noise especially for industrial field. This voltage signal then compares with the threshold voltage using an LM393 comparator. When the output current exceeds I_{th}, the voltage signal will be higher than the threshold voltage, then LM393 will generate a triggering signal to the driver of T_2. The driver provides voltage isolation with a KCB419 triggering transformer and amplifies the triggering signal to turn ON T_2. It should be noted that power supplies of the APU and the thyristor driver are better unified, otherwise a voltage level conversion circuit will be further needed.

The 400 V dc source is rectified from a 285 V three-phase ac source, which transformed from a 380 V three-phase ac source with an adjustable transformer. As shown in Fig. 6, an isolation transformer is also used to offer an ungrounded arrangement, which is usually recommended for dc microgrids to allow continuing operation under less severe faults such as a pole-to-ground fault [32], [33]. Moreover, corrugated power resistors are used as the testing load and a Tektronix oscilloscope DPO4034B is used to record experimental waveforms.

The lab breaker was tested under the same three load conditions as the simulation, and Fig. 7 shows the waveforms. Comparing Fig. 7 with Fig. 5, the measured waveforms have shown remarkable consistency with the simulated results. The breaker designed for a 20% overload tripping offers rapid isolation for both the 80% overload and short-circuit tests while allowing a 13% slight overload. The good matching of waveforms between

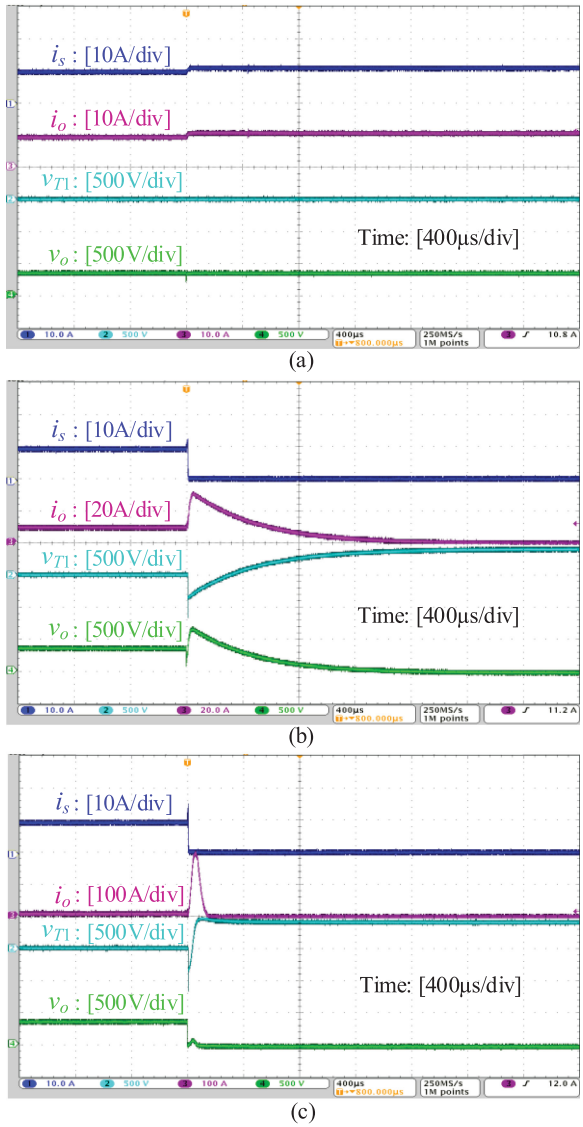

Fig. 7. Experimental waveforms of the designed breaker for (a) 13% overload, (b) 80% overload, and (c) short-circuit fault.

experiment and simulation also has demonstrated the validity of the proposed breaker and accuracy of SPICE models. It should be noted that negative voltage spikes may appear on T_1 during its tripping, which are caused by nonlinear turn-OFF impedance of the thyristor and parasitic inductances in the commutating circuit. An *RC* snubber can well absorb this part of energy and suppress the voltage spikes. For example, a 10 nF capacitor and 40 Ω resistor are used as T_1 snubber in the prototype and can reduce the peak voltage spike to −670 V from −1320 V for no suppression.

More detailed waveforms during the steady state and fault period are included in Fig. 8. At the moment the short-circuit fault occurs, L_1 withstands the source voltage and its current i_1 starts to increase. When i_1 exceeds I_{th}, T_2 is triggered to commutate T_1 accompanied by the discharging of C_1 and C_2. As shown in the waveforms, i_4, i_{C1}, and i_{C2} are almost the same during the discharging, which corresponds well to the analysis in Section II. The saturable inductor L_s endures voltage during the turn-ON process of T_2 to provide di/dt limitation and begins to

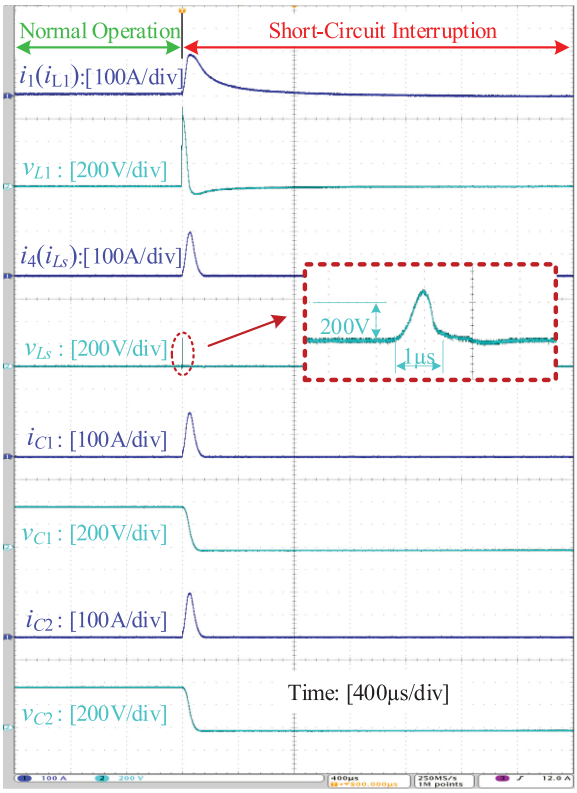

Fig. 8. Detailed breaker waveforms before and after the short-circuit fault.

saturate in less than 1 μs. After rapidly entering deep saturation, L_s withstands zero voltage, just performing as a piece of wire.

Response time of the APU has also been measured. Time delay from $i_o = I_{th}$ to the moment that APU finishes inversing the driver input signal is 1.592 μs, including 0.92 μs delayed by the LEM current sensor and 0.672 μs for LM393 to flip the triggering level. Then it takes another 0.89 μs to finish turning on thyristor T_2. Since the total time is considerably smaller than the thyristor turn-OFF time, the neglected delay caused by the current sensor, APU, and thyristor driver in the modeling of Section III is acceptable. Considering that current sensor and semiconductor driver are always required for either the APU-based or digital-controller-based protection [21], using APU instead of digital controllers can save the time for A/D conversion and delay caused by limited sampling frequency. Moreover, a comparator chip is much cheaper than an ADC and digital controller. The simplicity of the control circuit and integration of current sensor and comparator circuit on one board with a compact arrangement is also beneficial for noise immunity.

A manual tripping test was also carried out to investigate the breaker performing as a dc switch. This functionality can also be easily integrated into the APU using a manual button and a logic gate. The measured waveforms, as shown in Fig. 9, are much like the results in the overload protection except for the transient caused by the extra load. The turn-OFF is very fast with a considerably smaller output current surge than the overload and short-circuit fault. One-shot triggering characteristic of the commutating circuit makes it an easy-controlled switch for the proposed breaker, which leaves flexibilities for a comprehensive protection against various fault conditions and coordinated protection in a rather complicated network under a centralized or distributed control.

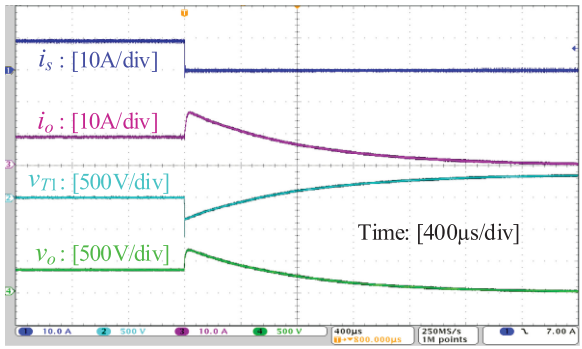

Fig. 9. Manual tripping waveforms of the designed breaker.

TABLE II
PARAMETERS OF THE 1.5 kV/4.5 MW BREAKER

R_1	$R_2(R_3)$	R_4	$C_1(C_2)$	L_1	L_s	Z_L
0.1 Ω	5 Ω	0.1 Ω	8000 μF	700 μH	50 μH	0.5 Ω

C. Medium-Voltage Design

City subway systems generally utilize dc power supplies with a common voltage level of 1.5 kV, which has also been applied for dc microgrids in Finland [33]. Hence, a 1.5 kV/4.5 MW breaker is designed as an illustration for high-power medium-voltage design. The rated current is 3 kA, and I_{th} here is set to 4.5 kA (for illustrative purpose), i.e., 150% of the rated current. Thyristors of ABB 5STP 45Q2800 with $t_q = 400$ μs are selected to optimize for conduction efficiency. Following design guidelines in Section III, the rest of the circuit components are chosen with parameters listed in Table II. Saturation current of L_s here is set to 300 A.

The designed breaker is modeled in SPICE and tested with three different load conditions.

1) 25% Overload: The simulation waveform is shown in Fig. 10(a). When the extra load is added, the resistive load changes immediately. Because the inductor current cannot leap, the output voltage shows a sag. After that, the output current as well as the source current increases to a higher value. However, the final current is 3.75 kA, which is still lower than I_{th} without triggering the breaker.

2) 100% Overload: This time, the extra load added has the same resistance as the rated load, i.e., 0.5 Ω. As shown in Fig. 10(b), a deeper sag appears on the output voltage, which is followed by the rising current. When the output current exceeds the threshold, the APU triggers the commutating circuit to interrupt the current. During the interruption, the T_1 voltage remains negative for over 700 μs to guarantee a reliable turn-OFF. Meanwhile, as R_4/R_L is much higher than the 400 V/4 kW design, the output voltage surge gets much smoother. After T_1 turns OFF, the load voltage decays to zero, and T_1 withstands the whole dc voltage. A voltage overshoot may emerge on T_1, then the snubber circuit will conduct to smooth down this overshoot.

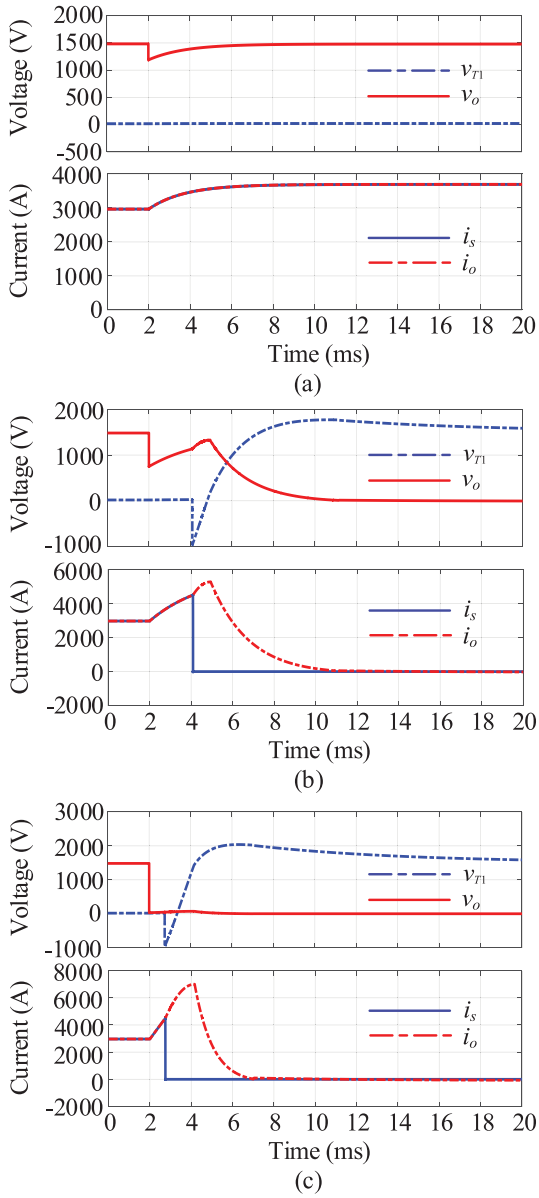

Fig. 10. Simulation waveforms of the 1.5 kV/4.5 MW breaker for (a) 25% overload, (b) 100% overload, and (c) short-circuit fault.

3) Short-Circuit: Short-circuit condition is similar to the 100% overload condition, but with a sharper rising current, as shown in Fig. 10(c). The fault current is interrupted rapidly in less than 1 ms with a 33% voltage overshoot.

D. Effect of the Saturable Inductor

Fig. 11 illustrates the functionality of L_s. By using such an inductor, the turn-ON current first rises at a limited rate, introducing a zero-voltage switching, followed by a sharp rising after saturation. A considerable power pulse can then be avoided by such a current delay. Considering that all the energy in such a power pulse will be dissipated in a small volume of activated thyristor junction, very high temperature spots may be produced and cause a thyristor failure. Therefore, the adoption of L_s can significantly improve the robustness and reliability of

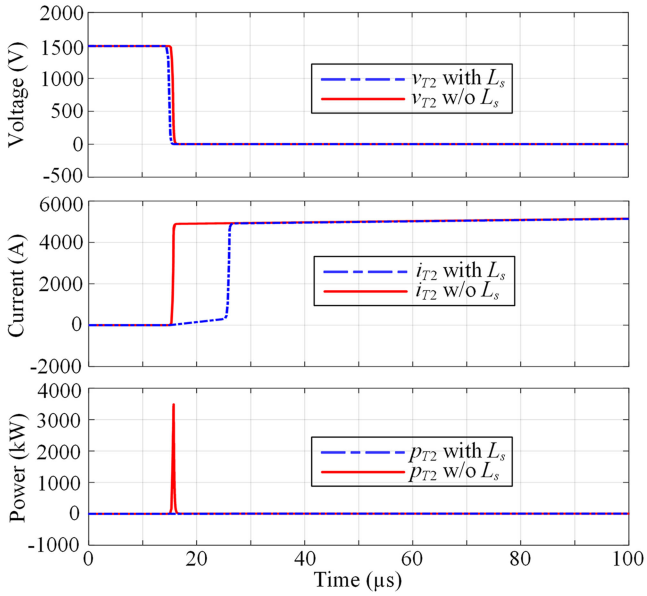

Fig. 11. T_2 triggering waveforms of the 1.5 kV/4.5 MW breaker demonstrating the effect of L_s.

TBCBs. Although saturable inductors are widely used for di/dt limitations [34]–[36], the determination of proper inductance and saturation point for a matched thyristor has not yet been covered in existing literatures and still deserves further research.

V. Practical Considerations

Power efficiency and cost-effectiveness of the proposed breaker are analyzed in this section.

A. Power Loss Evaluation

It is important for breakers to maintain low power losses, especially for high-power designs, since a simplified cooling system and higher power efficiency can be achieved. Typically, the main contact resistance in a mechanical breaker with a current rating of several kilo-amps should be in the order of 100 $\mu\Omega$ [37], and a maintenance to replace the contact will be required once its resistance exceeds 200 $\mu\Omega$ [38]. Hence, the maximum allowable contact resistance for a 1.5 kV/4.5 MW level mechanical breaker is assumed as 200 $\mu\Omega$ here. In the medium-voltage design, thyristor 5STP 45Q2800 of ABB with a slope resistance of 70 $\mu\Omega$ and threshold voltage drop below 0.86 V is selected as the main switch, which means a maximum ON-state resistance of 357 $\mu\Omega$, while injection-enhanced gate transistor (IEGT) ST3000GXH24A and IGBT 5SNA 3000K452300 [39] can also be used as the main switch representing the pinnacle of available full-controlled semiconductor switches with an equivalent resistance of 1283 and 1317 $\mu\Omega$, respectively. Thus, both of them maintain a considerably higher ON-state resistance as well as conduction losses than mechanical and thyristor switch, as shown in Table III.

Other components in the main circuit should also be considered, such as load commutation switches in hybrid breakers [39] and current-limiting inductors. For the proposed design, the

TABLE III
POWER LOSSES FOR DIFFERENT SWITCHES

Switch Type	Mechanical contact	*SCR* 5STP45 Q2800	*IEGT* ST3000 GXH24A	*IGBT* 5SNA3000 K452300
U_{DRM}/U_{CES}	-	2800 V	4500 V	4500 V
$I_{T(AV)M}/I_C$	-	5490 A	3000 A	3000 A
Surge current (10 ms/125°C)	-	77 kA	-	21 kA
On-state voltage (3 kA/125°C)	0.6 V	1.07 V	3.85 V	3.95 V
Maximum on-state resistance	200 μΩ	357 μΩ	1283 μΩ	1317 μΩ
Conduction loss	1800 W	3210 W	11550 W	11850 W

resistance of L_1 will also increase the power loss. However, the proposed breaker only needs one inductor in the main circuit rather than two for Z-source breakers [11]–[14]. Furthermore, this inductor can also be shared as the input filter for dc load. As the inductance is proportional to the thyristor turn-OFF time according to (17), inductor L_1 and thyristor T_1 can be flexibly selected to get the optimized power efficiency.

B. Cost Analysis

Breaker cost varies for different topologies at different power rating. Unlike mechanical breakers, solid-state and hybrid breakers require little maintenance and provide more control flexibilities, and thus suitable for applications requiring a high supply reliability at low maintenance cost. As a promising candidate for HVdc, hybrid breakers typically cost considerably more than solid-state breakers due to a more complex circuit and control. Solid-state breakers using full-controlled semiconductor switches still seem attractive in low-power applications which are more sensitive to costs rather than power efficiency. However, since the one-shot tripping characteristic allows a cheap APU as the controller, the proposed breaker can maintain a total cost comparable to IGBT-based breakers even for low-power applications. As power rating increases, a thyristor will be much cheaper than an IGBT or IEGT. For example, the IEGT and IGBT in Table III cost approximately five and nine times, respectively, of the thyristor. Also, an antiparallel fast-recovery diode will be further needed for the IEGT, which has no diode or reverse conducting capacity integrated. Moreover, costs of the commutating circuit and current-limiting inductor will be considerably decreased as the thyristor turn-OFF time decreases, so a fast switching thyristor is recommended for cost-sensitive applications. This also applies to Z-source breakers [5] in which one more current-limiting inductor would be further required. Low-pass characteristic integrated in these breakers can reduce power filter cost as well. The available thyristors with different turn-OFF time and prices will also provide more selecting and design flexibilities for applications in a wider power rating.

VI. CONCLUSION

A novel dc breaker using a thyristor as the main switch to reduce the conduction losses is presented for dc microgrid protection. The one-shot triggering characteristic of the commutating circuit makes it simple and reliable to trip the breaker. Besides conventional digital control unit, a simple APU can be adopted for a faster response. The proposed breaker also remains a low-pass voltage transfer characteristic. Moreover, a saturable inductor is utilized to limit the turn-ON di/dt and avoid hot spot in the commutation thyristor. The saturation characteristic also allows a sharp-rising commutating current, which can provide zero-crossing for the main thyristor with a shorter delay. As the core of the dc breaker, the commutating circuit features a compact size and simple structure, which can be conveniently integrated into other breaker topologies with zero-crossing requirements. Furthermore, a detailed mathematical modeling as well as simulation and experimental results verifying the feasibility of the proposed breaker is provided. The modeling method and the breaker topology can both offer valuable references for design and further application of dc circuit breakers.

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