An Overview and Comprehensive Comparative Evaluation of Current-Fed-Isolated-Bidirectional DC/DC Converter

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***Abstract*—Renewable energy generations have been attracting sustained attentions in academic and industry. Current-fed-isolated-bidirectional dc/dc converters (CF-IBDCs) are widely adopted in low-voltage high-current applications such as solar photovoltaic fuel cell with energy storage. This paper gives an overview and a comprehensive comparative evaluation of CF-IBDCs. The active clamped, dual half-bridge, *L-L* type dual active bridge, resonant-type, naturally clamped, and other type topologies of CF-IBDCs are investigated, analyzed, and compared regarding their circuit topological structures, operation characteristics, modulation methods, and soft-switching technologies. In addition, component cost models and loss models of converters are deduced and presented. On this basis, quantitative and comprehensive performance comparison of seven typical CF-IBDC topologies selected from each type is conducted in terms of costs, losses, weight, volume, and power density for the given system specifications and design constraints. Finally, the application range of different CF-IBDCs and future trend are presented to encourage further development.**

***Index Terms*—Active clamped, cost models, current-fed-isolated-bidirectional dc/dc converter (CF-IBDC), dual half-bridge, *L-L* type, loss models, naturally clamped, power density, resonant, volume, weight.**

I. Introduction

THE development of renewable energy sources and distributed generations requires new strategies for the operation of a grid-connected generation system. The power electronic technology plays an important role in the integration of renewable energy generation into the power grid and is widely used and rapidly expanded [1]–[3]. In order to realize the connection of low-voltage generating sides and high-voltage bus and meanwhile maintain or improve the power-supply quality and reliability, it is necessary to implement a power electronic converter with high voltage gain as a mediation module.

Current-fed power electronic converters are boost-derived topologies and have been justified to be suitable for low-voltage high-current applications. Renewable energy sources such as solar photovoltaic and fuel cell generate low-voltage and high-current output; thus, current-fed converters are good candidates to interface them with high-voltage dc bus. In the distributed generation system, the energy storage devices such as battery and supercapacitor are key elements which are able to absorb the reverse power flow and also output power as auxiliary sources. Therefore, current-fed converters with bidirectional power transfer capability are required [4]–[8].

Compared to conventional voltage-fed-isolated-bidirectional dc/dc converters (VF-IBDCs), current-fed-isolated-bidirecti onal dc/dc converter (CF-IBDCs) are meritorious owing to lower input current ripples, inherent short circuit protection, lower high-frequency (HF) transformer turns ratio, high step-up ratio, no duty cycle loss, and easier current controllability [9]–[11]. Current limiting through the components and short-circuit protection becomes significant for high-current applications. In addition, the inductor at input side of CF-IBDC is more reliable and has longer lifetime compared with the electrolytic capacitor employed in VF-IBDC. However, CF-IBDCs have inherent defects as well. The main drawbacks of CF-IBDCs are charging the inductor at start-up and the voltage spike across the turning OFF switches caused by current mismatch between the input boost inductor and the leakage inductance of an HF transformer. Lots of literatures have been focusing on overcoming these problems by the innovation and modification of topologies with new modulation and control methods and soft-switching techniques. Novel modulation and auxiliary components or circuits are often investigated to solve the intrinsical problems associated with the topologies and enhance the converter performance for specific applications.

In view of the state-of-the-art research, this paper will present the classification of various CF-IBDCs as shown in Fig. 1. Active clamped, dual half-bridge, *L-L* type dual active bridge, resonant-type, naturally clamped, and other type topologies of CF-IBDCs

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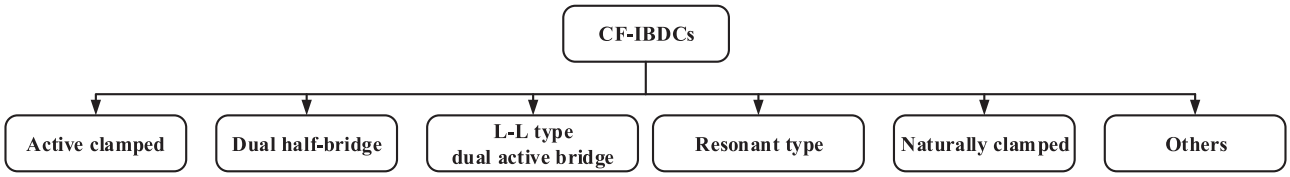

Fig. 1. Classification of CF-IBDCs.

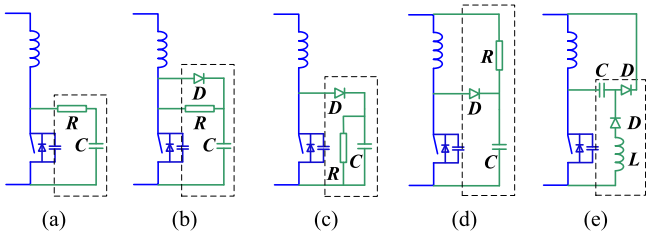

Fig. 2. Snubbers for suppressing the voltage spike [12]–[15]. (a) Dissipative *RC* snubber [13]. (b)–(d) Dissipative RCD snubber [13], [14]. (e) Nondissipative energy recovery *LC* snubber [15].

are reviewed and studied. Cost models for MOSFET, transformer, inductor, capacitor, heatsink, and gate-driver integrated circuits (ICs) will be derived. Loss models for switching and conduction losses of MOSFET, core loss and winding loss of inductor and transformer will be presented as well. Based on the quantitative data from the simulation for the same specification, a virtual prototype of each topology has been designed for several typical topologies of CF-IBDCs. A systematic performance comparison is presented for these selected topologies from the aspects of power density, costs, weight, volume, and efficiency.

This paper is organized as follows. Section II gives the six types of CF-IBDCs and discusses their characteristics in detail. Component cost models and loss models are derived and presented in Section III. Section IV compares and evaluates various CF-IBDCs qualitatively in different aspects. Section V discusses the application range of different types of CF-IBDCs. Finally, Section VI discusses the future trends.

II. Traditional and Advanced CF-IBDC Topologies

In current-fed circuits, hard commutation is the major issue as it results into device voltage overshoot, which is caused by current mismatch between the input boost inductor and the leakage inductance of HF transformer. Snubbers are generally required to limit the voltage spike to prevent the switching device from a permanent breakdown. Different snubber circuits such as dissipative snubbers and regenerative snubbers have been utilized as shown in Fig. 2 [12]–[15]. These snubbers are employed to accommodate the whole boost inductor current until the HF transformer current is fully built up to the level of the boost inductor current.

Dissipative snubbers lead to low efficiency owing to the energy dissipated in snubber resistor. To improve the efficiency, energy recovery *LC* snubbers have been proposed as shown in Fig. 2(e). The *LC* snubber stores the surge energy in the snubber capacitor during device turn-OFF. During the interval before the switch turns OFF, the capacitor is charged to the reverse input voltage due to the resonance between the snubber inductor and capacitor. During switch turn-OFF, the boost inductor current is commuted through the snubber capacitor and the commutation diode; thus, the switch is turned OFF in a zero-voltage switching (ZVS). Once the switch is turned ON, the capacitor is reset and energy stored in the inductor is fed back to the input instead of being dissipated [15]. However, the conventional *LC* snubber has several problems like complex structure, difficult optimal design, and do not assist in soft switching.

Recently, a lot of new studies of CF-IBDCs are emerged in the aspect of innovation of topologies and modulations. The classification of various CF-IBDC topologies is shown in Fig. 1 and more details about each topology will be given next.

A. Active Clamped CF-IBDC

A simple way to suppress the voltage spike inherited in the current-fed converter is to utilize power semiconductor devices and a large HF film capacitor to provide an additional commutation path. It allows the current flowing through the leakage inductance to rise to the input inductor current in a controllable manner. The voltage spike can be considered to be clamped by the HF film capacitor. Thus, this is called an active clamp technique.

Active clamp has been implemented in many fundamental topologies [16]–[19], such as full-bridge current-fed topology as shown in Fig. 3(a). A path consisting of a capacitor C_a and switch S_a in series is used to clamp the voltage spike when the main switches turn OFF and store the energy in auxiliary clamp capacitor C_a through the antiparallel body diodes D_{ax} of the auxiliary switch S_a. The corresponding operating waveforms are shown in Fig. 3(b). In boost mode, the duty cycle of the main switches is larger than 0.5 and the gating signals of switches in the same leg are phase shifted by 180° with an overlap. The auxiliary switch S_a is in ON state during the nonconduction interval of the main switches. S_a will achieve ZVS if it is turned ON before the clamp capacitor current i_{Ca} decreases to zero. When the current i_{Ca} is reversed, the energy stored in the capacitor will be released back to the main circuit. Similarly, the main switches can also be gated for ZVS turn ON. Thus, ZVS soft-switching operation is achieved for all switches and high efficiency can be achieved. In buck mode, synchronous rectification is implemented in current-fed side to reduce the conduction loss, while the phase-shift control strategy is applied in voltage-fed side. The freewheeling current is reset by activating the auxiliary switch S_a and at the same time, zero-current switching (ZCS) of S_7 and S_8 is realized. But current-fed side switches are turned ON twice in one switching

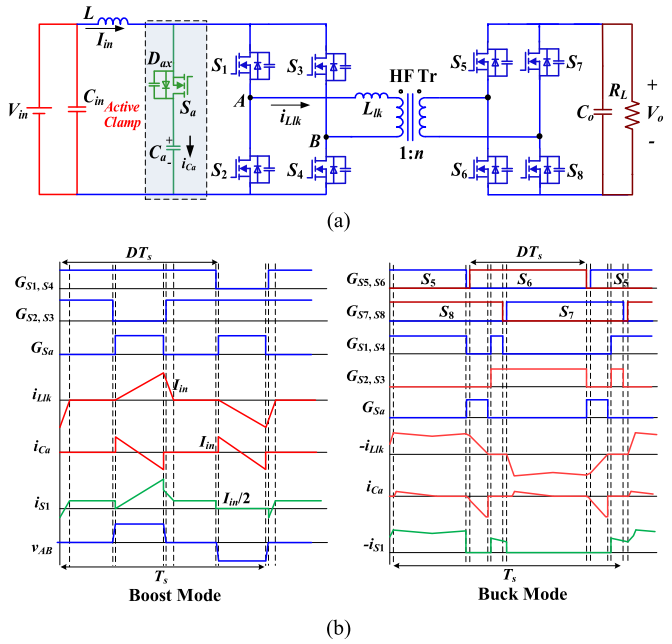

Fig. 3. (a) Topology with the simplest active clamp [18]. (b) Key operating waveforms.

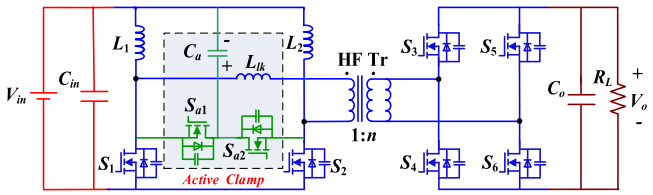

Fig. 4. Topology proposed in [20].

cycle along with different duty ratios, increasing the control complexity. The problem of this fundamental active clamped topology is that the soft switching cannot be maintained for light-load condition.

Rathore *et al.* [20] propose a *L*-*L* type active-clamped current-fed converter shown in Fig. 4 with wide/extended ZVS range design. As shown in Fig. 4, the active clamp circuit is composed of two switches and a capacitor, and the switches provide access for the clamping capacitor C_a to absorb and release the energy from the current mismatch during commutation. Similar operating process to aforementioned topology in Fig. 3 is appeared in this converter. The difference is that two auxiliary switches are gated ON once in turns during one switching cycle while the auxiliary switch in Fig. 3 is gated ON twice one cycle. Compared with active clamped full-bridge topology, *L*-*L* type half-bridge has less number of active switches and potential lower input current ripple with interleaving effect. The clamping capacitor C_a can also be connected to the ground of primary side [21]. It is intensively researched in the literature and will be discussed separately in Section II-C.

The *L*-*L* type active-clamped converter can achieve higher boost ratio on account of equivalent dual boost converters on primary side. Moreover, magnetizing inductance of the HF

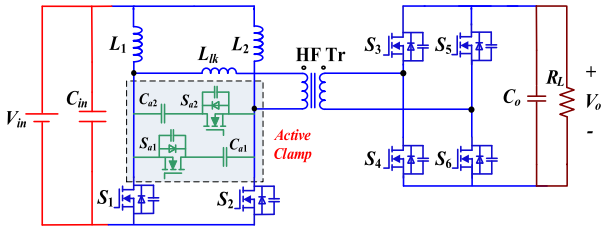

Fig. 5. Topology proposed in [22].

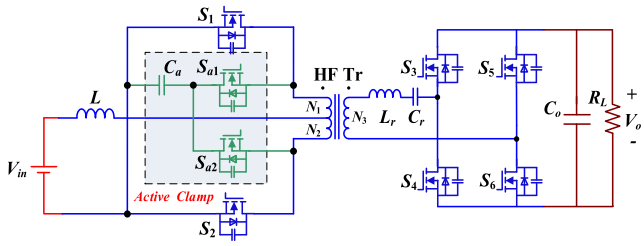

Fig. 6. Topology proposed in [23].

transformer has been used to extend the soft-switching range. It maintains soft switching over a wide voltage range and wide load range. All the switches realize soft switching even under light-load conditions. It is worthy of mentioning that a tradeoff should be considered between the conduction loss and range of soft switching for the primary switches.

Another novel active clamp circuit as given in Fig. 5 can achieve ZVS both at turn-ON and turn-OFF, but the voltages across the auxiliary switches are twice as those of the main switches [22]. The active clamp circuits need floating active device(s) and high value of HF clamp capacitor for accurate and effective clamping.

In addition to the above converters, clamp circuit has also been introduced in other current-fed topologies [23]–[25]. A new topology with active clamped push–pull current-fed circuit at low-voltage side and *LC* resonant hybrid full-bridge circuit at high-voltage side is proposed in [23], as shown in Fig. 6. Two novel control methods are presented to achieve the ZVS soft switching and higher power handling capacity in both power transferring directions. In buck mode, commutation overlap period is reduced to expand the max duty cycle. In boost mode, active commutation is accelerated through utilizing the reflected voltage from high-voltage side. The power transferring capacity is increased 1.5 times in buck mode operation and 3.6 times in boost mode operation. In [24], similar control method has been studied for active-clamped current-fed full-bridge topology at low-voltage side. At high-voltage side, a fast recovery dc-link diode with a parallel switch is introduced to allow the use of high-voltage MOSFETs and achieve low switching loss. In boost mode, the added parallel switch is in OFF state and the dc-link diode reduces large reverse current from high voltage terminal. In buck mode, the parallel switch is turned ON and high-voltage side full bridge works as an inverter.

In summary, the active clamp technique can be applied to three basic double-ended topologies push–pull, *L*-*L* type half-bridge

TABLE I
COMPARISON OF THREE ACTIVE CLAMPED TOPOLOGIES

Topologies	Full-bridge	L-L type half-bridge	Push-pull
Numbers of low voltage switch	5	4	4
Voltage stress of low voltage switch	$\frac{V_{in}}{2(1-D)}$	$\frac{V_{in}}{(1-D)}$	$\frac{V_{in}}{2(1-D)}$
Current stress of low voltage switch	I_{in}	I_{in}	I_{in}
Transformer windows utilization	Good	Good	Poor
Input current ripple	Moderate	Good	Moderate

and full bridge. All of them can achieve ZVS soft switching in bidirectional energy transferring and have higher efficiency compared to dissipative/passive snubbers. They all suffer from the demerits of additional floating devices, driver, and large HF capacitor adding to volume. The main features of these three topologies are compared in Table I, and they all have advantages and disadvantages.

Similar techniques have been reported for three-phase current-fed active clamped topologies [26]–[33]. It should be noted that although some of studied converters are unidirectional, it is feasible to replace the diodes on high-voltage side with active switches allowing bidirectional power transferring capability. Three-phase converter not only inherits the advantages of aforementioned single-phase current-fed converters but also increases the power transfer capability for switches with the same voltage and current rating compared to single-phase one. In addition, reduced rms current per phase and low conduction loss and smaller size of passive components are achieved for the same power compared to the single-phase converter. A three-phase full-bridge current-fed converter with active clamp and delta–delta connected transformer is shown in Fig. 7(a) [26]. The ideal waveforms of the pulsewidth modulation (PWM) control strategy applied to this converter are shown in Fig. 7(b). As shown, the duty ratio of switches' gating signal is varying so that it increases the complexity of control. Three-phase half-bridge active-clamped topology with three input inductors and Y–Y connected transformers is shown in Fig. 8 [27], [28]. Due to the three-phase interleave operation, the frequency of input current is triple of switching frequency and its current ripple is minimized. The current ripple is much smaller than the converter in Fig. 7(a) and single-phase topologies with the same inductor design. In addition, the adopted PWM control with fixed duty ratio under steady state is easier compared to the former three-phase converter. If the duty cycle D is less than 0.66, then the auxiliary clamp capacitor current I_c is continuous. The counterpart topology with delta–delta connected transformer is studied in [29].

The active clamp technique is also applied to basic three-phase current-fed push-pull converter [30] as well. The three-phase push–pull topology has benefits of simplest structure in its power and gate driver circuits, leading to high system reliability. Three-phase push–pull converter with active clamp is

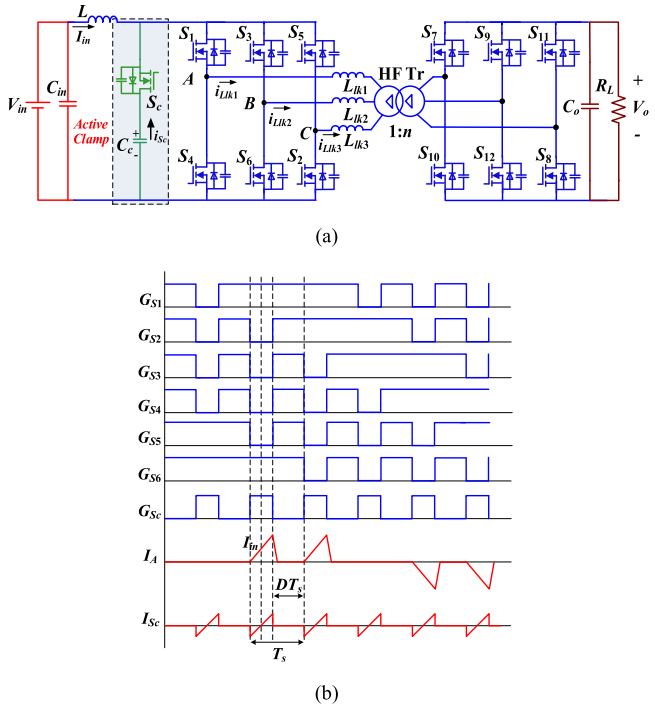

Fig. 7. (a) Topology proposed in [26]. (b) Key operating waveforms.

shown in Fig. 9 [31], [32]. A full three-phase bridge is used at low-voltage side like Figs. 7 and 8, which is meritorious for modular design. Similar PWM control method in [27] is adopted, of which the major advantage is that the switching frequency of clamp switches and main switches is identical. Three different operating regions depending on the duty cycle D ($D > 0.66$, $0.33 < D < 0.66$, and $D < 0.33$) are studied. For $D > 0.66$, the RMS current through the leakage inductances is larger compared to that in [26] and [27]. For $D < 0.33$, ZVZCS soft switching of clamp switches is achieved.

A new three-phase push–pull converter employing a simple active clamp circuit with rearrangement of three main switches is presented in [33] as shown in Figs. 10. The topology inherits the similar characteristics in [26], [31], and [32] with simplest structure. In this topology, PWM control with $D > 0.66$ is employed to ensure enough voltage step-up ratio. The disadvantage of this topology is that the voltage stress of main switches is higher than that of topologies studied in [26], [31], and [32].

In buck operating mode for three-phase active clamped converters, the operating process is similar to that of single-phase active clamped topology. The auxiliary switch is only activated briefly after the execution of high voltage switch to reset the leakage inductor current which otherwise circulates in voltage-fed side.

B. Dual Half-Bridge CF-IBDC

Peng *et al.* proposed a novel type of CF-IBDC with boost half-bridge as shown in Fig. 11(a) [34], [35]. The converter is configured with dual half-bridge structure placed at both sides of the HF transformer and an inductor at the input of

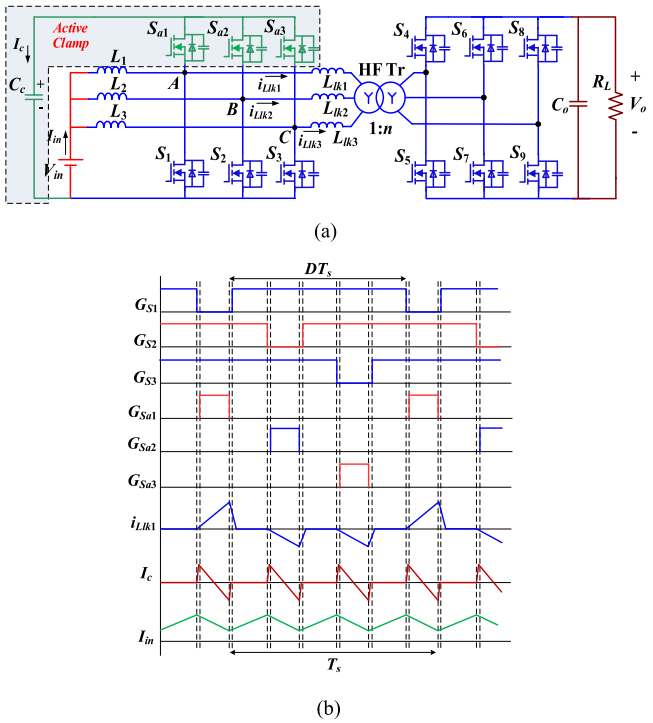

Fig. 8. (a) Topology proposed in [27]. (b) Key operating waveforms.

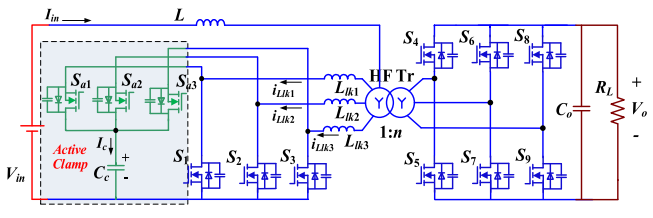

Fig. 9. Topology proposed in [31] and [32].

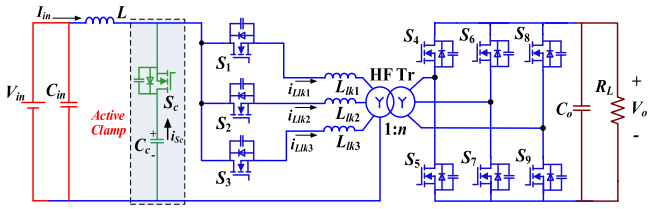

Fig. 10. Topology proposed in [33].

the low-voltage side. This topology is a boost-type circuit and minimizes the devices count for the same power rating compared to full-bridge topology, which allows a compact packaging. Each switch and corresponding capacitor will serve as the active clamp for the complementary one. In addition, the start-up problem of the voltage-fed converter is inexistent, which eliminates the need for additional devices and reduces the complexity of converter.

Fig. 11(b) shows the idealized operating waveforms of the converter under different cases according to the phase shift Φ_1 and voltage relationships of V_1 and V_3 and V_2 and V_4. The optimum case happens when the duty cycle $D = 0.5$, $V_1 = V_3$ and

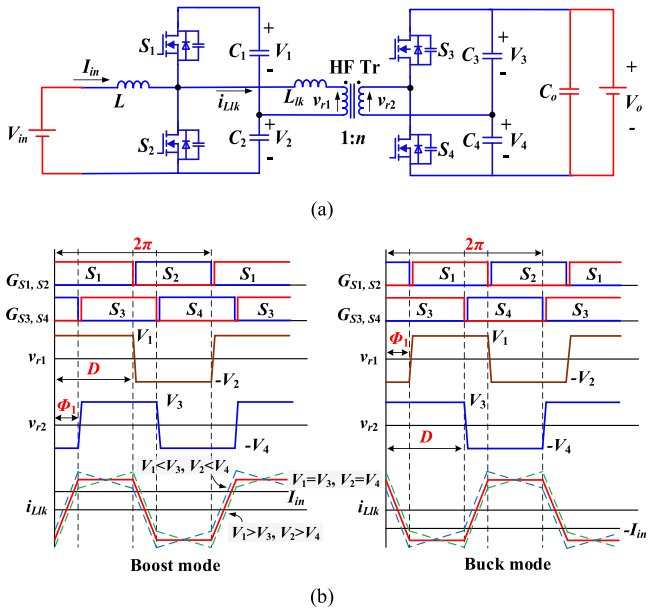

Fig. 11. (a) Conventional current-fed dual half-bridge topology [34], [35]. (b) Key operating waveforms.

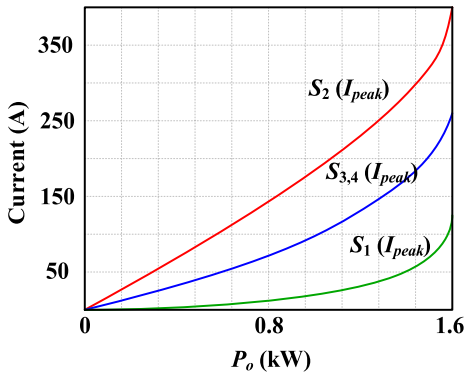

Fig. 12. Current stresses of switches versus output power [34].

$V_2 = V_4$, which minimizes the peak value of leakage inductor current. S_1 and S_3 are controlled with the same duty cycle, which is named as symmetrical duty cycle (SDC) control. The duty cycle D can be regulated to match the voltages across the both sides of the transformer. The power transferring and its direction are decided by the phase shift Φ_1 between two voltages across the transformer primary and secondary. When V_{r1} is leading V_{r2}, the converter is working at boost mode. Otherwise, the converter is working at buck mode. The current stresses of switches are also related with Φ_1. Decreased value of Φ_1 brings less current stress. ZVS of all switches is achieved in either direction of power flow. However, the current stresses of low-voltage side switches are asymmetric (shown in Fig. 12) and it is difficult to accommodate a wide range of voltage boost ratio as well. Practically, the ZVS soft switching cannot be maintained through full range of load. Another drawback of half-bridge topology is the requirement of split capacitors which have to deal with the full load current.

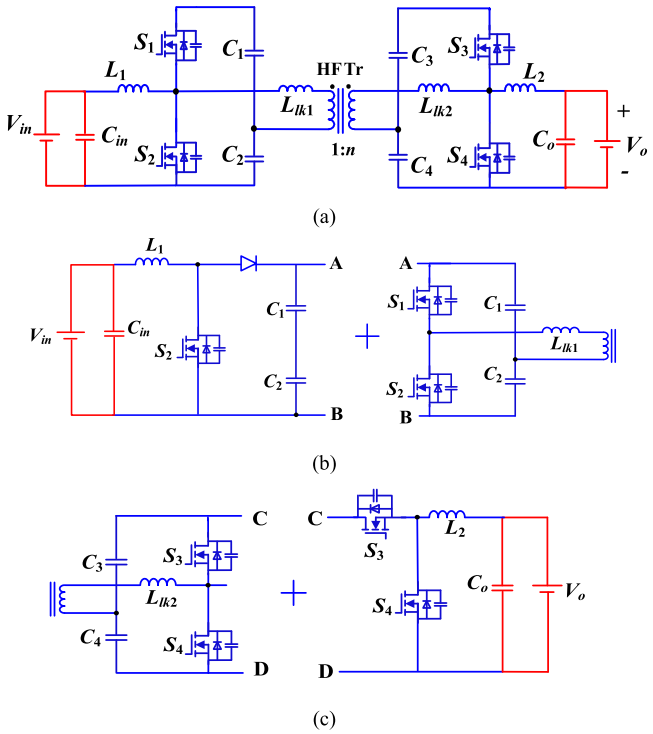

Fig. 13. (a) Topology proposed in [36]. (b) and (c) equivalent circuits.

The secondary side of the above topology in Fig. 11 has been modified in [36] as given in Fig. 13(a). The converter is bilaterally symmetrical and is also a variant of the boost circuit. In boost mode, the low-voltage side can be considered as a combination of a boost converter and a half-bridge converter as shown in Fig. 13(b). And for the high voltage side, the working principle of the converter can be regarded as a hybrid of a buck converter and a half-bridge converter as shown in Fig. 13(c).

Similarly, S_4 is the key switch. In order to avoid the unbalance voltage of C_1 and C_2 and the unsymmetrical voltage of the primary winding, the duty cycle of all switches is fixed at 50%. Similar to [34] and [35], this topology is operating at phase-shift control mode. Power flow, the output voltage and current, and soft switching are all controlled by the phase-shift angle between the transformer primary and secondary voltages with fixed 50% duty cycle. Compared to the half-bridge topology in Fig. 11, this modified topology achieves ZVS for all switches and zero current commutation for the rectifier diode over a wide load range. The control method, i.e., using a fixed duty cycle (FDC) with phase shift to control power flow, is simple and easy to implement. But the FDC control method is not suitable for wide input application. The current stress of switches stays asymmetric like topology in [34] and [35].

Based on the conventional dual half-bridge CF-IBDC [34], [35], Sun *et al.* [37] add one more identical secondary-side configuration and combines the two capacitor legs into one as shown in Fig. 14(a). The immediate effect of this change is that the secondary-side output voltage becomes three levels from two levels, and thus the converter can be optimized for low conduction loss design. PWM plus hybrid phase-shift modulation

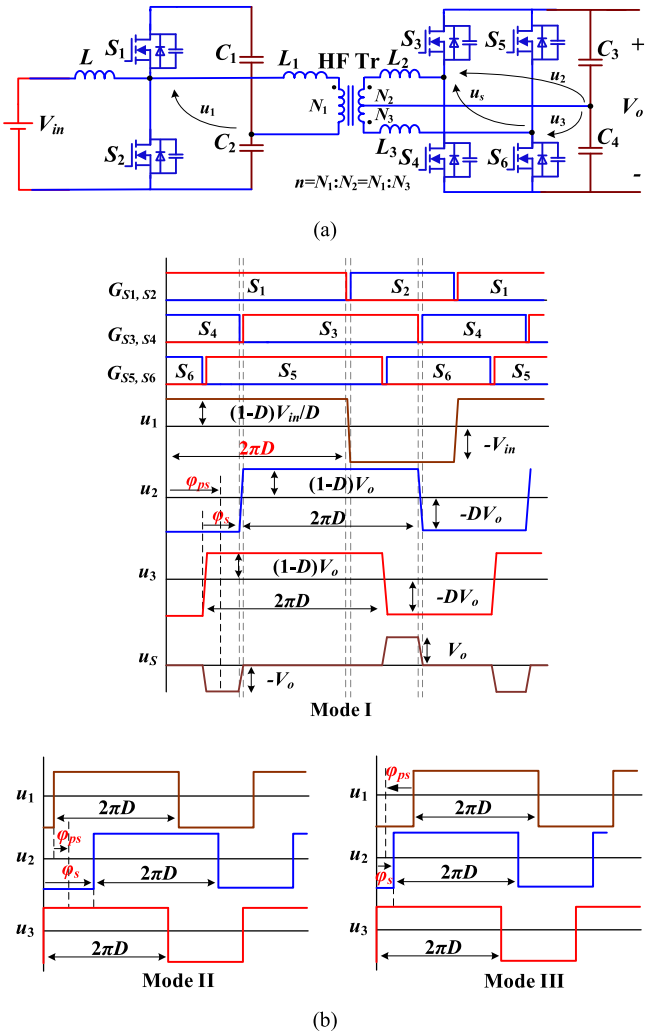

Fig. 14. (a) Topology proposed in [37]. (b) Three operating modes.

(PSM) are applied to this converter. As shown in Fig. 14(b), there are three control variables, namely the duty cycle D of S_1, S_3, and S_5, the phase-shift angle $\varphi_{\rm ps}$ between the primary and secondary switching units, and the secondary-side internal phase shift angle φ_s. Three different operating modes of converter are identified depending on the control of these variables. Boost operation occurs in Mode I and II, and buck operation exists in Mode II and III. The direction of power flow is controlled by $\varphi_{\rm ps}$ instead of φ_s.

In order to minimize the rms current, the duty cycles of the three half bridges are the same (SDC control). The duty cycle D can be regulated to match the voltages across the both sides of the transformer. In addition, the current stresses, rms current, and conduction losses of the converter are reduced with PWM control. Single phase-shift (SPS) modulation (modulation of $\varphi_{\rm ps}$) and dual phase-shift (DPS) modulation (modulation of φ_s and $\varphi_{\rm ps}$) are combined to form a hybrid PSM. The adoption of hybrid PSM can achieve practical ZVS operation of high-voltage side switches within wide input voltage and full power range, resulting in lower switching losses and higher

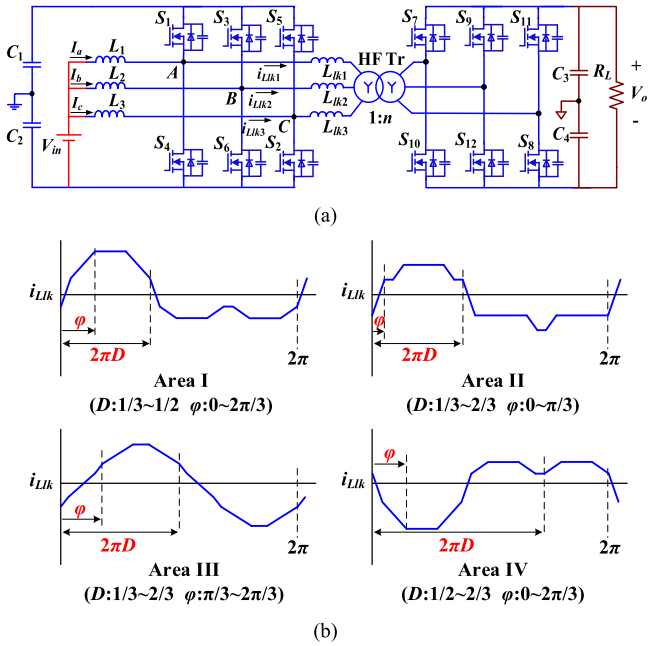

Fig. 15. (a) Topology proposed in [38]. (b) Four practical operating areas.

efficiency. Compared with the topologies and control scheme in [34]–[36], the proposed control strategy performs better under all modalities than SPS control and can better match the output voltage. However, this converter is more complex in terms of structure and control.

A number of new topologies based on the conventional dual half-bridge CF-IBDC have been proposed to fulfill different specific targets. In order to improve the converter power rating with reduced weight and size of passive components which are limitations in single-phase counterpart, a three-phase current-fed converter with Y-Y connected transformers as shown in Fig. 15(a) is proposed [38]. With the interleaving structure, dc-link capacitor can be reduced as well compared to single-phase topology. Simultaneously, the Y-Y connection of transformers has better current sharing capability compared with other types of connection. Similar to the control in single-phase topology, duty cycle plus phase-shift control is implemented, in which the varied SDC D accommodates the changes of input voltage. The phase angle φ between the switches on low-voltage and high-voltage sides controls the bidirectional power flow. The upper and bottom switches on each phase are conducted complementarily, with the phase angle 120° between phase legs on the same side. The varied duty cycle modulation (D is limited in 1/3–2/3) results in four practical operating areas in boost mode for the converter, which are shown in Fig. 15(b). The maximum power is located at $D = 1/2$ and $\varphi = \pi/2$. In buck mode, φ is less than zero and the operating waveforms are symmetrical. Soft switching and low rms current are maintained over a wide load range and wide input voltage range. Increased power rating and reduced size of passive components are the major merits of the three-phase design.

Three-port triple half-bridge CF-IBDCs have also been proposed to interface multiple dc sources [39], [40]. Unlike most

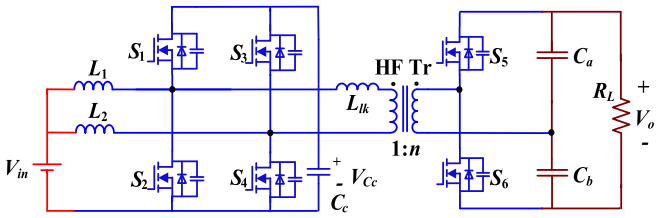

Fig. 16. Topology proposed in [41].

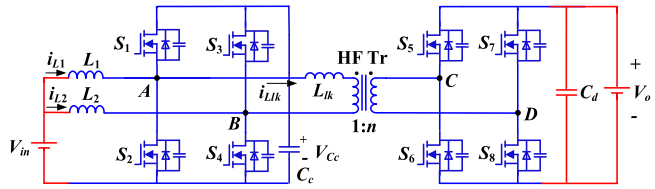

Fig. 17. Topology proposed in [21] and [42].

of control methods, Wang *et al.* [39] propose a novel asymmetrical duty cycle (ADC) control method for a three-port triple half-bridge dc–dc converter. Generally, with SDC and FDC control methods, two current-fed ports cannot maintain ZVS and the dc-bus voltage varies under wide input voltage variation. For ADC control, the duty cycles of two current-fed ports are adjusted according to the variation of respective input voltages and the duty cycle of voltage-fed port is fixed at 50%. With the ADC control method, constant dc-bus voltage and ZVS for all the ports within full input voltage range are maintained. The power flow between three ports is controlled by the phase-shift angles. Furthermore, the proposed ADC control reduces the converter peak current and rms current. Cao *et al.* [40] propose a similar three-port dc–dc converter while using two transformers. Focusing on the closed-loop feedback control of the converter, the virtual-output-impedance shaping technique and double PI feedback method are presented and designed to minimize the second-harmonic distortion on dc-bus voltage.

C. L-L Type Dual Active Bridge CF-IBDC

A novel type CF-IBDC has been introduced in [41] based on Peng's single half-bridge topology, as shown in Fig. 16. It can also be considered as one special type of active clamped *L-L* type current-fed converter. This *L-L* type dual active bridge CF-IBDC has drawn a lot of research efforts and is analyzed separately here.

In [41], the converter is controlled by phase-shift plus low-voltage-side PWM scheme and the high-voltage-side pulsewidth is fixed at 0.5. ZVS soft-switching over wide range of load under wide input voltage variation condition is achieved. The circulating current is also reduced considerably. However, the circulating energy is still relatively large with fixed high voltage side pulsewidth in boost mode and the realization of wide range of output voltage changing in buck mode is difficult. Hui *et al.* [21] modify Fig. 16 into three-level topology (full-bridge at high voltage side), as shown in Fig. 17. Therefore, the pulsewidth of high-voltage side can be modulated to obtain more operation

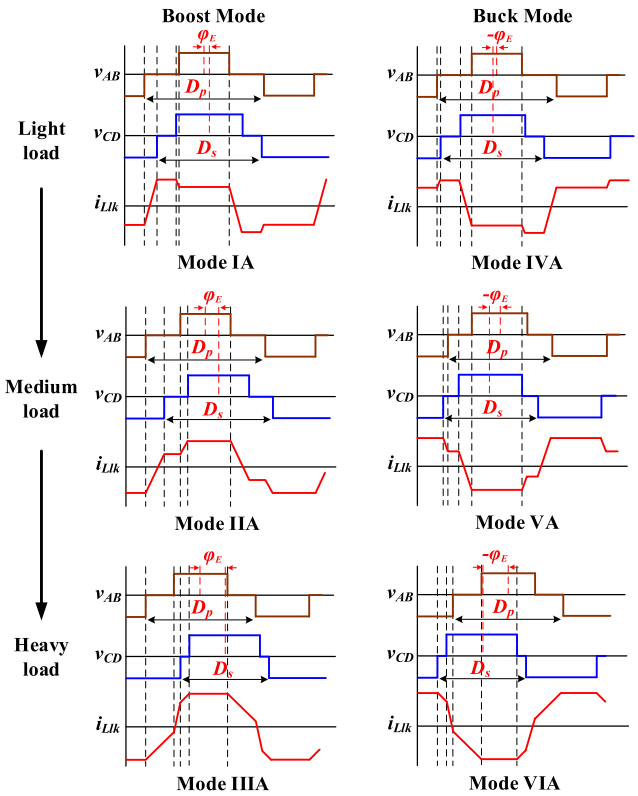

Fig. 18. Operating patterns for the topology in Fig. 17 [42].

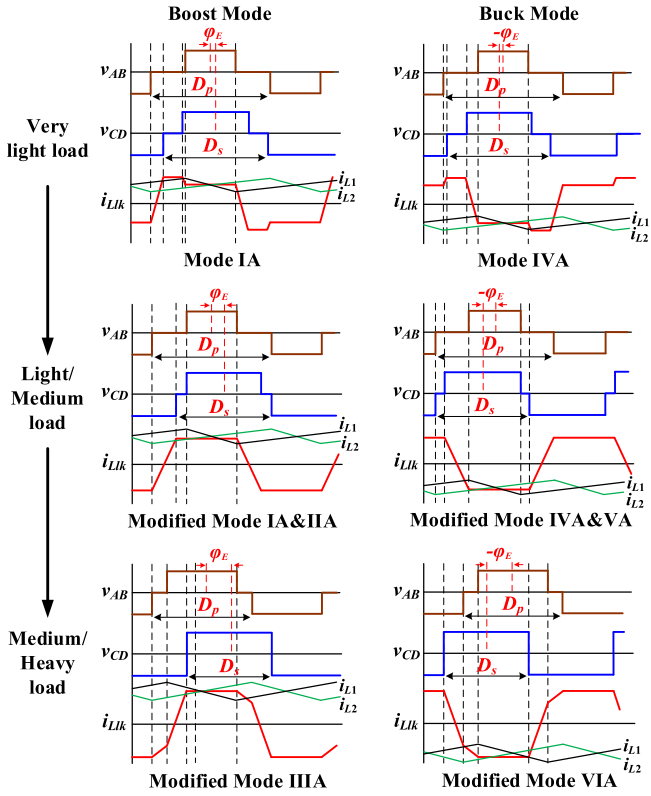

Fig. 19. Modified operating modes for the topology in Fig. 17 [43].

modes. PWM plus SPS is adopted, and the duty cycle of low-voltage side and high-voltage side are kept to be the same (SDC). Voltage mismatching control is employed, where voltage across clamp capacitor is not controlled to be equal to reflected high voltage ($V_{Cc} \neq V_o/n$). The studied converter minimizes the rms value of transformer current. But soft switching through full range of loads cannot be achieved, and the current stress is still relatively high.

Sha *et al.* [42] studied the control of this converter further. Unlike Hui's work, voltage matching control is implemented to avoid the high current stress caused by unmatched voltage control. All the possible and practical switching patterns on the premise of wide ZVS range, power controllability, and voltage matching control have been analyzed and compared with respect to three degrees of control freedom, i.e., the low-voltage side duty cycle D_p, the high-voltage side duty cycle D_s, and the phase-shift angle φ_E. The practical operating patterns are depicted in Fig. 18. To achieve ZVS for a wide load range, $D_p > D_s$ should be maintained. A new control strategy is proposed that D_p is always larger than D_s by a fixed value and the bidirectional power is monotonously controlled by φ_E in the range of $-\pi/2 \sim \pi/2$. The fixed value is designed as small as possible on the premise of ZVS achievement in order to reduce the circulation loss. Therefore, the independent control variables have been reduced from 3 to 2. The converter is optimally operating at different modes according to the load conditions and low voltage variations. The closed-loop control is simple while maintaining the advantages of minimized circulating current. The proposed control strategy allows the converter to achieve soft switching over the full load range including no load condition.

In [43], based on the operating modes shown by Fig. 18, corresponding modified modes are presented shown in Fig. 19 with the same three control freedoms D_p, D_s, and φ_E. It is clearly demonstrated that the modified modes in Fig. 19 are the boundary modes of that in Fig. 18, which reduces the peak current and rms current in the transformer. Compared to the previous control methods, lower conduction loss and core loss occur with this modified modulation strategy. However, the requirement of control precision is greatly increased.

Sha *et al.* [44] replace the two input inductors in Fig. 17 with magnetic-integrated inductors, thus improving the power density and the power conversion efficiency at light-load conditions. The duty cycle of low-voltage side bottom switches is controlled to be lower than 50% to reduce the conduction loss. Meanwhile, the voltage mismatching control with adaptive clamp voltage regulation helps achieve ZVS for all switches throughout full load range. However, proper dead time to achieve ZVS has to be designed precisely which brings difficulty of control.

To obtain both low conduction losses and circulating current, Zhang and Sha [45] proposed a new control method with double PWM plus double phase-shift (DPDPS). Gating signal of both side of HF transformer is controlled with DPS to achieve ZVS of low-voltage side switches and ZVS/ZCS of high-voltage side switches. Unlike Hui's work, voltage matching control is also implemented. The advantages of this control method are

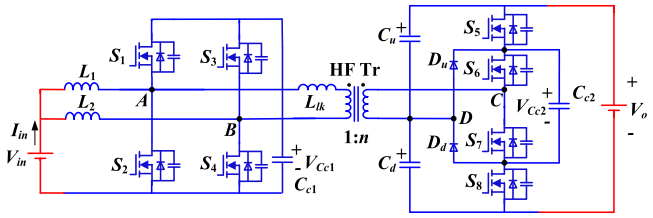

Fig. 20. Topology proposed in [46].

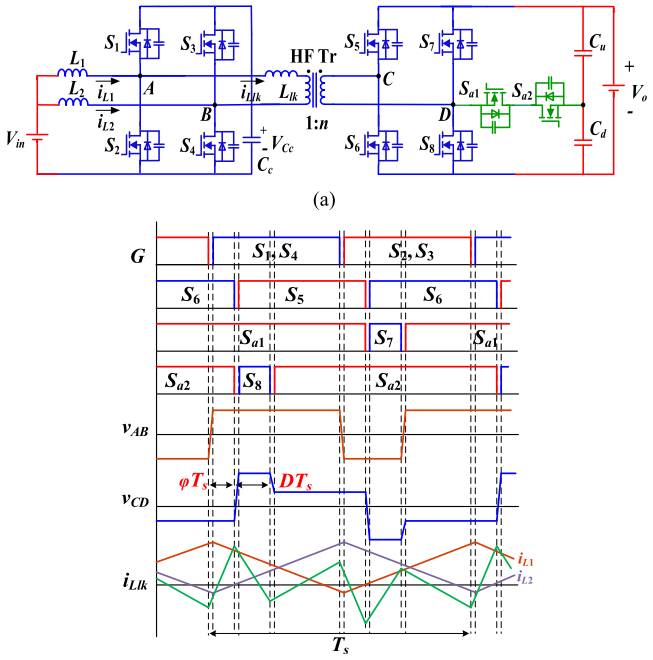

Fig. 21. (a) Topology proposed in [47]. (b) Key operating waveforms.

that the soft switching is maintained for wide variation of low input voltage. Thus, the conversion efficiency is higher than the PWM plus SPS control. Similar DPDPS technique has been implemented for the topology with a three-level neutral point clamped circuit at high voltage side [46], as shown in Fig. 20.

A novel *L-L* type hybrid dual active bridge converter is proposed in [47], as shown in Fig. 21(a). The high voltage side is a full bridge with an auxiliary half-bridge circuit, which allows five-level high-voltage operation at most. The theoretical operating waveforms are shown in Fig. 21(b). The low-voltage switches are conducted complementarily with 50% FDCs regardless of the input voltage and load variation. Therefore, the current ripples of L_1 and L_2 offset each other and the input current ripple can be reduced to zero theoretically. For high-voltage switches, the duty cycle of S_7 and S_8 is D and complementary to that of the auxiliary switches. The selection of D is related to the ZVS range for all switches, which is determined by the voltage conversion ratio and the phase shift angle φ. To achieve zero current ripple, this converter suffers from the issue of high number of active switches and high current stress with voltage mismatching control.

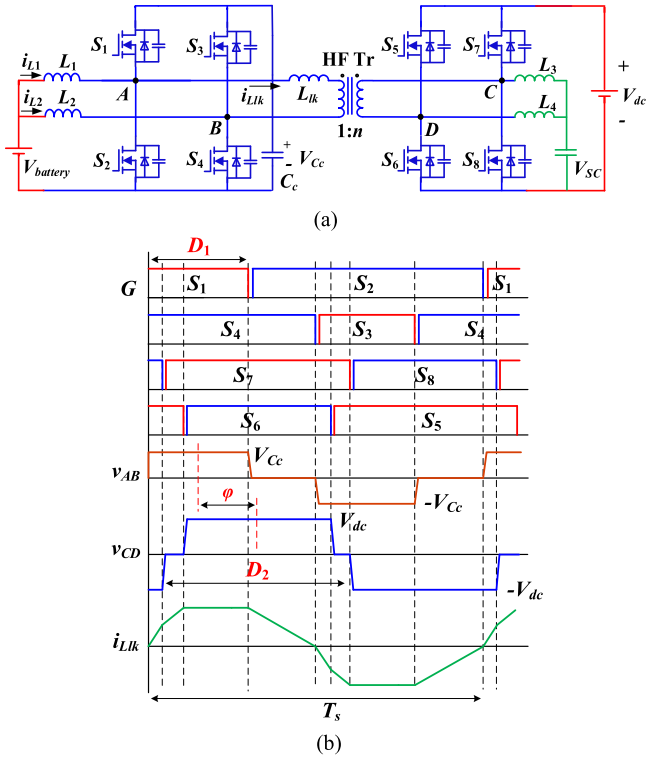

Fig. 22. (a) Topology proposed in [48]. (b) Key operating waveforms.

A multiport topology suitable for hybrid battery and supercapacitor applications is presented in [48]. The converter is symmetrical on both sides of transformer, shown in Fig. 22(a). As indicated in Fig. 22(b), the duty cycle D_1 controls the voltage across the clamp capacitor Cc and D_2 adjusts the voltage of dc bus. Similarly, the phase angle φ controls the power flow between the battery and dc bus. For ZVS achievement of switches on the battery side in full load range, D_1 is set less than 0.5, while for switches on the dc-bus side, the inductors L_3 and L_4 should be designed properly to achieve whole range's ZVS operation. Compared to the topologies without multiport, lower reactive power and circulating current are realized in this topology and it is potential to attain the port extension.

The operating patterns of above research work in boost mode and buck mode are symmetrical and the power transferring magnitude and direction can be generally controlled by the phase shift angle since they are piecewise related.

In [49], one active switch at low-voltage side is replaced with a diode, which leads to low size and cost of the converter. However, only two switches operate under ZVS within wide power range and the efficiency is low at light-load conditions. Dual transformers structure-based *L-L* type CF-IBDCs are introduced in [50] and [51]. With respective advanced modulations, input current ripple free is achieved in [50] and switching harmonics elimination and power sharing without transformer dc bias are realized in [51]. In [52] and [53], parallel connected *L-L* type dual active bridge CF-IBDCs are investigated with corresponding control strategies. Excellent power sharing can be achieved among the individual constituent converters not only in steady state but also in the dynamic process.

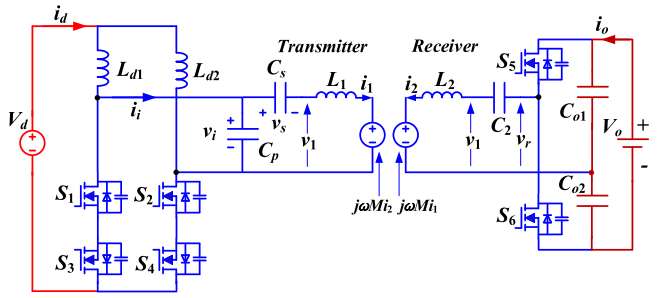

Fig. 23. Topology proposed in [62].

D. Resonant-Type CF-IBDC

Resonant-type current-fed converters make use of the transformer parasites (leakage inductor, parasitic capacitor) as resonant circuit elements and solve the problem of voltage/current spikes and high switching losses. Resonant converters are the earliest soft-switched converters. According to different types of resonances, resonant converters can be divided into series resonant, parallel resonant, and series–parallel resonant converters. Dozens of research work have applied these resonant techniques over current-fed converters. Many types of the resonating current-fed converter such as *LC*-type [54]–[57], *CLC*-type [58], *LLC*-type [59], *LCC*-type [60], *CLLC*-type [61], etc., have been reported, which were distinguished based on the components of the resonant circuit. Normally, the output voltage is regulated through varying frequency control and switches can be soft switched.

Samanta *et al.* [62] present a new current-fed resonant topology for the bidirectional wireless power transmission power electronics system. A series–parallel *CLC* resonant tank is formed through connecting a designed capacitor in series with the transmitter coil. The topology is shown in Fig. 23. Compared to the conventional current-fed topology with *LC* resonant tank, the voltage stress on the converter is much smaller. Variable frequency modulation is used to control the power flow. Regardless of the load current, the devices can obtain soft switching. The receiver-side voltage doubler acts as an uncontrolled rectifier in forward direction. To compensate the reactive power consumed by the receiver coil, a capacitor is connected with it in series. In backward direction, the voltage doubler circuit operates as voltage-fed inverter with a FDC 0.5. Varying frequency control brings difficulty to the optimized control and design of the converter [63].

To solve the issue of varying frequency control of resonating converter, some scholars focus on the study of fixed frequency or limited range frequency control. Fig. 24 shows a novel fixed-frequency PWM-controlled *LC* series-resonant tank-based CF-IBDC [63]. The primary side is an *L*-*L* type active bridge topology, while the secondary side is an active full-bridge circuit. The resonant tank, which is composed of a series inductor L_r, a capacitor C_r, and an HF transformer, is used to produce a nearly sinusoidal current at both sides of the transformer. This results in a lower switching loss of the switching devices. The auxiliary inductors L_a and magnetizing inductance L_m are employed to

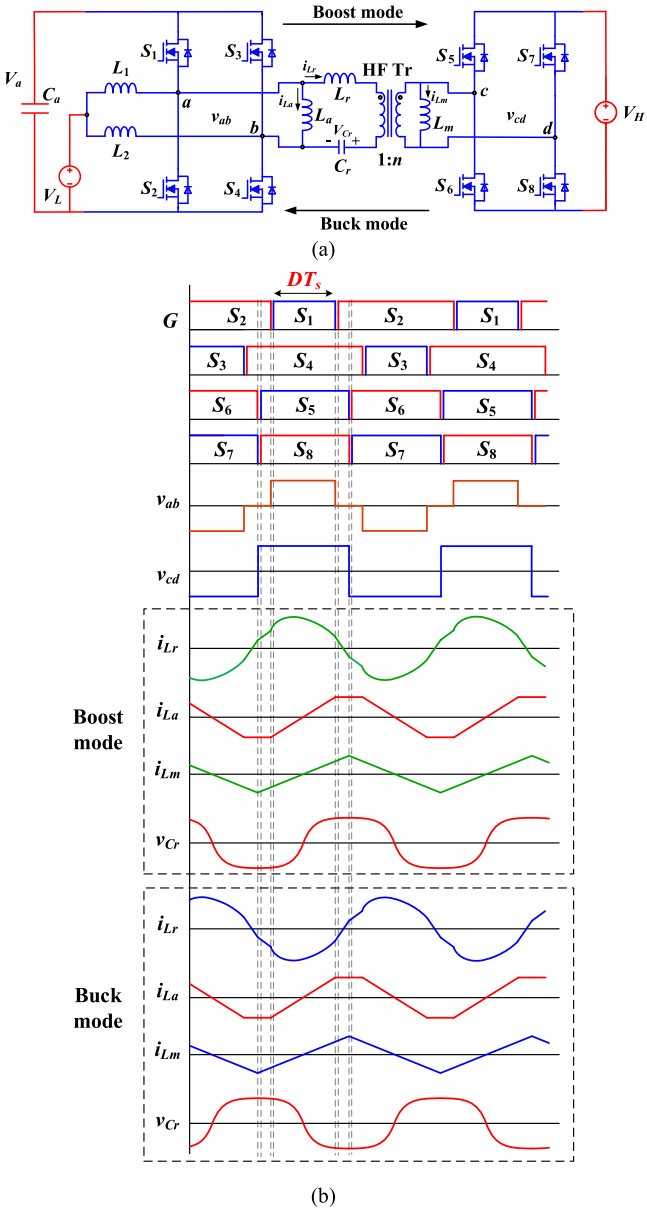

Fig. 24. (a) Topology proposed in [63]. (b) Key operating waveforms.

achieve ZVS for all the switches. Fig. 24(b) shows the operating waveforms in boost and buck modes. It can be seen that the gating signals of switches in boost and buck modes are exactly the same, as well as the inductor currents i_{La} and i_{Lm}. The only difference is the direction of i_{Lr} and v_{Cr}. The most attractive feature of this proposed series-resonant converter is that the voltage gain characteristic is very similar to the well-known PWM converters, whose voltage gain is only determined by the duty cycle *D* of switches S_1 and S_3. *D* is the only control variable and varying around 0.5 to accommodate the wide voltage applications. The amplitude and direction of the transferred power are regulated easily and smoothly through simple PWM control.

Fig. 25 shows a traditional *LLC* resonant converter with an optimal modulation strategy analyzed in [64]. Compared to the conventional pulse-frequency modulation (PFM) which is not

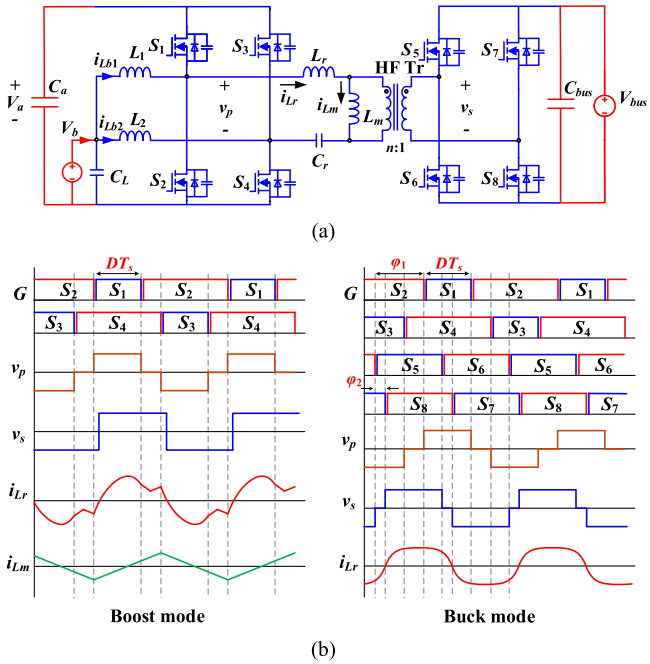

Fig. 25. (a) Topology proposed in [64]. (b) Key operating waveforms.

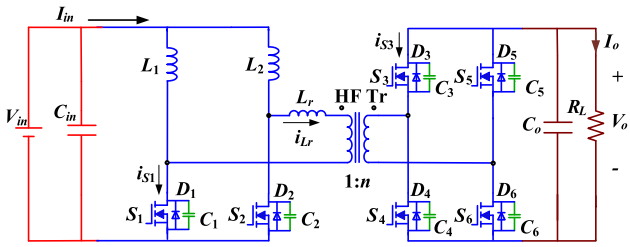

Fig. 26. Topology proposed in [65].

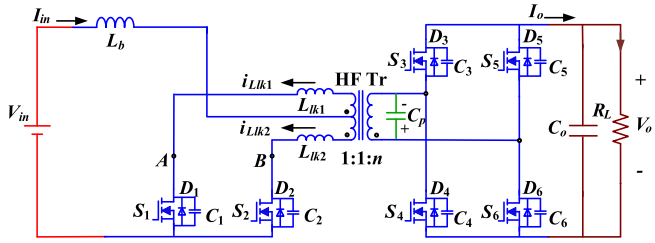

Fig. 27. Topology proposed in [68].

suitable for bidirectional operation within wide voltage range due to the requirement of wide frequency regulation range, this new control method employs narrow operation frequency range which is beneficial for the design of magnetic components and achieves high efficiency. In boost mode, PWM control is employed. The duty cycle D of S_1 and S_3 is changed to regulate the voltage of capacitor C_a and the high voltage side switches are synchronous rectified. The dc-bus voltage is controlled by PFM. While in buck mode, PWM plus PSM is adopted. The phase-shift angle φ_1 between S_5 and S_1 and duty cycle D regulate V_b and V_a, respectively. And the constant phase shift φ_2 between S_5 and S_8 helps to realize ZVS of all the switches. It should be noted that the converter parameters and control strategy need to be well designed and tradeoff must be made to ensure ZVS over a full operating range and better efficiency performance.

The disadvantages of the resonant-type CF-IBDCs are that the resonant tanks need extra inductors and capacitors, and the resonating voltage and current stress of these passive components are relatively large.

In addition to aforementioned converters with resonance in the whole cycle, there exist other types of resonant converters of which the resonance happens only for a part of the switching period. Instead of full resonance, partial resonance may obtain the advantages of soft commutation, limited device voltage, and current stress. Some of them are named as quasi-resonant converter [65]–[67]. The resonant components are the leakage inductor of HF transformer and the parasitic capacitor of the switches. The topology is shown in Fig. 26 and its corresponding boost mode operating waveforms are shown in Fig. 28. The resonance frequency should be selected several times the maximum switching frequency. The voltage gain is mainly affected by the resonant components and switching frequency, instead of high voltage side duty cycle. In buck mode operation, low-voltage side switches are operated same as that in boost mode. Although the proposed converter is operated under ZVS at both power directions, the voltage stress of low-voltage side switches is still too high.

Similar techniques called impulse commutated converters have been reported recently [68]–[70]. Impulse commutation utilizes transformer leakage inductance and interturn winding capacitance as the resonance tank, which allows the device voltage to rise gradually and therefore solve the issue of device turn-OFF voltage spike without increasing complexity and degrading performance of converters. The resonance happens only for a short period of time depending upon the overlap time and produces a resonance impulse. ZCS turn OFF operation of low-voltage switches and reduced peak current compared to full resonant converters are achieved and the voltage gain is immune to load variation. However, frequency modulation is still required to regulate the load voltage. Impulse commutation technique can be applied to three basic double-ended topologies push–pull, *L*-*L* type half-bridge, and full bridge [70]. Fig. 27 shows an impulse commutated push–pull topology (the operating waveforms are shown in Fig. 28). Reduced peak and circulating currents compared to resonant converters with identical *LC* tank are achieved for impulse commutated current-fed converter.

Fig. 29 shows an impulse commutated three-phase topology, which can implement two types of modulation schemes, i.e., 120° modulation and 180° modulation and offer high potential for low-voltage and high-current applications like fuel cell application. More details about comparison and evaluation of various three-phase current-fed impulse commutated converters such as three-phase half-bridge, three-phase full-bridge, and three-phase push–pull topologies, are presented in [70]. Although the studied topologies in [70] are unidirectional, it is feasible to replace

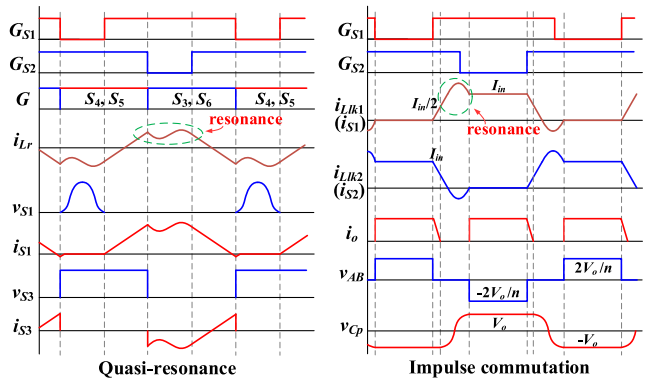

Fig. 28. Waveforms of quasi-resonant converter [65] and impulse commutated converter [68].

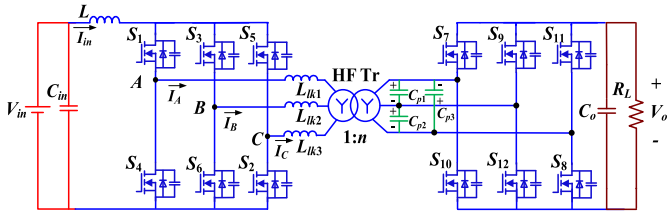

Fig. 29. Topology proposed in [69].

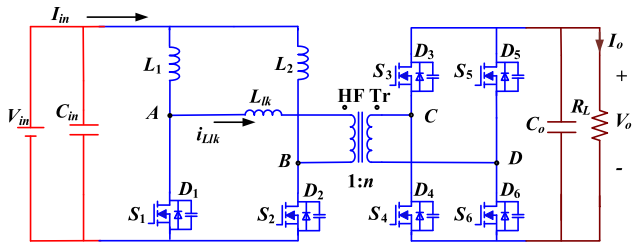

Fig. 30. Topology presented in [73].

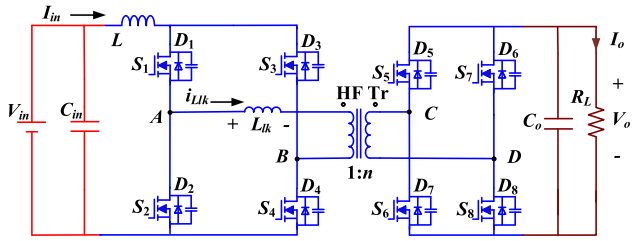

Fig. 31. Topology presented in [75] and [76].

the diodes on high voltage side with active switches allowing bidirectional power transferring capability. In buck operation, similar modulation schemes applied in conventional three-phase voltage-fed *LC* resonant dc/dc converters could be implemented for these current-fed impulse commutated converters.

E. Naturally Clamped CF-IBDC

For current-fed bidirectional converter, the voltage-fed (high voltage) side switches provide the flexibility to preset the current flowing through leakage inductance to the boost inductor current before the commutation of current-fed side switches thus reducing or eliminating the need of snubber circuits. This is referred as active commutation technique or natural clamping technique [71], [72]. For the soft-commutation method proposed by Zhu [71], the energy consumption of the passive snubber can be reduced but cannot be completely eliminated. In [72], the commutation time has to be precisely controlled which limits the practical applications.

Rathore *et al*. has contributed a lot in the development of new family of current-fed converters—active commutated or naturally clamped current-fed converters [73]–[78]. The main principle of a secondary-modulation-based naturally clamping technique is to utilize the reflected output voltage across the primary winding of the HF transformer. The reflected output voltage diverts the input boost inductor current from one switch (or switch pair) to the other switch (or switch pair) through the HF transformer. A minor circulating current allows body diode conduction to ensure ZCS and natural turn-OFF. Low-voltage side switches are naturally voltage clamped by reflected output voltage and achieve ZCS turn-OFF and nearly ZVS turn-ON, while the high-voltage-side switches realize ZVS turn-ON. Soft switching and voltage clamping are inherent and maintained independent of the load and voltage variations. Owing to the low clamped voltage of low-voltage-side devices, low-voltage-rating devices with low ON-state resistance can be used, resulting in low conduction losses and higher efficiency.

Two types of secondary modulation have been implemented over current-fed *L-L* type half bridge topology and full-bridge topology as shown in Fig. 30 [73] and Fig. 31 [75]. The key operating waveforms of these two secondary-modulation techniques have been displayed in Fig. 33(a) and (b). Low-voltage-side switches are controlled by identical gating signals (greater than 0.5) phase shifted by 180° with an overlap. Both of them can achieve natural voltage clamping while for [73] the current flowing through HF transformer is discontinuous unlike [75]. The continuity of leakage inductance current is determined by the gating signal of high-voltage-side switches. The turn-OFF moment of high-voltage switches is synchronous with the turn-OFF of corresponding low-voltage switches. While for [73], the duty cycle is necessarily less than $\varphi/2$ at full load and for [75], the duty cycle should be large enough even up to 0.5. Thus, the control method proposed in [73] suffers from the oscillation due to the resonance between the leakage inductance of HF transformer and device capacitances when current in the transformer reaches zero.

For both of these two techniques [73], [75], under light-loads conditions, the peak current through the leakage inductance of HF transformer and the low-voltage-side switches is much higher than the input current, i.e., the excess current or circulating current is relatively larger, compared to that at rated load. The value of this peak current is constant and fixed for a given operating condition, irrespective of any power level or load change. Such peculiarity leads to higher current available for soft switching than that required, high circulating current and high

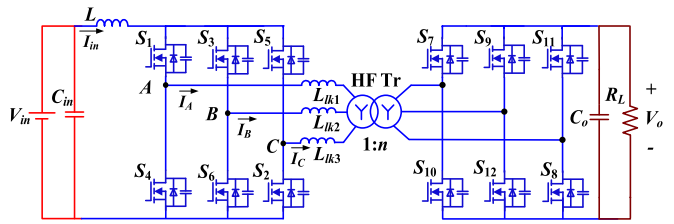

Fig. 32. Topology proposed in [77].

conduction and reverse recovery losses of primary switches' body diode at light loads. As a result, the performance of the converter is reduced at light loads.

The modulation methods implemented in [73]–[75] can be seen a SPS modulation as discussed in [76]. The control variable φ is the phase shift between the gating signals of the low-voltage switches and the corresponding high-voltage switches as shown in Fig. 33(b) and (c). The deficiency of the single variable control is the unregulated peak current especially under light-load condition as discussed above. Bal *et al*. [76] propose DPS modulation implemented over the same topology in Fig. 31. In addition to φ, the phase difference α_s between the diagonal switches on high voltage side is also controlled as shown in Fig. 33(c). With this modified modulation strategy, the value of aforementioned peak current is greatly reduced and thus the performance of the converter is improved at light-load conditions. For DPS modulation, the voltage across the secondary winding of the transformer is three level which is beneficial to reduce the circulating current and the power transfer is controlled by φ and α_s simultaneously.

In [77] and [78], naturally clamped bidirectional current-fed dual six-pack and three-phase push–pull topologies have been studied for high-power applications, which allows the reduction in the passive components and the enhancement of the power density. The dual six-pack topology is shown in Fig. 32. Similar to the single-phase topology, the duty ratios of low-voltage-side switches in one leg are more than 0.5 and 180° phase shifted with an overlap. Phase difference of 120° is maintained between three legs. The voltage across OFF-state switches in primary is naturally clamped at V_o/n. It should be noted that the peak value of currents through the leakage inductance and low voltage switches is $2\times$ input current.

In buck mode, the conventional PSM in high voltage side with synchronous rectification in low voltage side is implemented under high-load conditions. In order to maintain ZVS soft switching at lower loads, active controlled rectification is applied, where the duty cycle of low-voltage-side switches is greater than 0.5 to utilize the active devices for synchronous rectification for maximum conduction period. Hence, the overall performance of converter is improved. Note that some issues along with the bidirectional operation also exist, such as the seamlessly transition between two control schemes between boost mode and buck mode operation, which are associated with some resonant-type CF-IBDCs as well.

In summary, the merits of naturally clamping are no need of auxiliary circuits, ZVZCS for low-voltage-side devices and ZVS for high-voltage devices for wide operating range, inherent natural voltage clamping and higher efficiency and power density of the converter.

F. Other Type CF-IBDC

In addition to the topologies mentioned above, there are many other distinct types of current-fed converters which are out of common features [79]–[91]. These topologies realize their functions in specific applications but compromise on the complexity of the circuit. Some of them are introduced here.

Some authors utilize the auxiliary circuits to clamp the voltage spike during switching transition [79]–[84]. The flyback snubber was used to recycle the absorbed energy in the clamping capacitor [79]–[81]. The topology of CF-IBDC with a flyback snubber is shown in Fig. 34 [79]. Since the flyback snubber can be operated independently, it can be freely controlled according to the requirements of the converter. Therefore, it can clamp the voltage of low-voltage switches to a level slightly higher than the voltage across primary side of the transformer. Due to the existence of clamping branch (D_{au1} and $C_{\rm au}$) and the flyback circuit, the circulating current does not flow through the main switches and the voltage spike is avoided during switching commutation, consequently improving the reliability of converter. The clamping branch and the flyback snubber are activated in start-up process and regular boost mode operation. The circuit can be feasible by precharging the high voltage side capacitor through the flyback snubber at start-up thus realizing soft start and suppressing inrush current. In boost mode, low-voltage-side switches are controlled and high-voltage side is synchronous rectifying. While in buck mode, low-voltage side is operated as a rectifier and the topology is a phase-shift full-bridge converter without the participation of the flyback snubber. Sharon and Sathiyan [81] add two passive capacitor–diode snubbers at high-voltage side and the energy stored in flyback snubber is transferred to the buffer capacitors of added passive snubbers. As a result, the voltage and current spike as well as the voltage stress of the switches are reduced. In [82], external auxiliary buck circuits are utilized to achieve ZCS and reduce the circulating current for current-fed full-bridge topology as illustrated in Fig. 35.

In [86], a new switching control strategy taking advantage of the separated commutation is presented for the converter whose low-voltage side consists of four-quadrant switches comprising two MOSFETs each in backward connection, as shown in Fig. 36. It features natural clamping and ZCS soft switching at current-fed side with ZVS at voltage-fed side. A three-phase topology based on this structure is proposed in [87], which allows the converter to operate for higher power levels while maintains high efficiency.

In [88], an extended secondary universal current-fed converter is proposed based on Fig. 4 by modifying its secondary circuit. Hybrid modulation is proposed for this converter, where PWM in primary side with fixed secondary-side duty cycle under input voltage below 42 V and secondary side PWM for input voltage above 42 V are employed. With hybrid modulation, this converter accommodates load voltage regulation with wide input voltage variation (1:3) and load variation. In addition, ZVS for

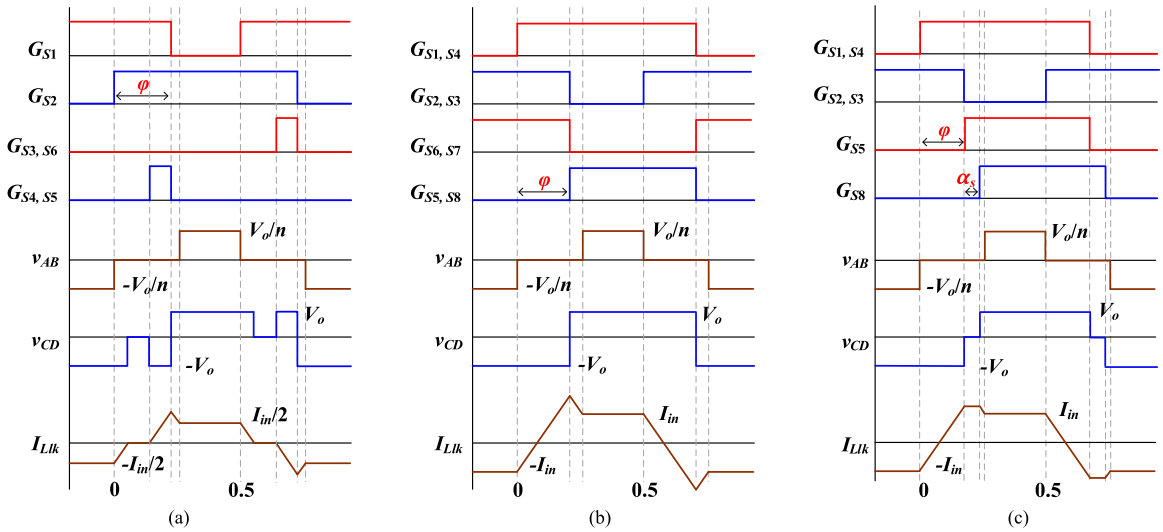

Fig. 33. Key operating waveforms of three types of secondary-modulation-based naturally clamping techniques [73], [75], [76].

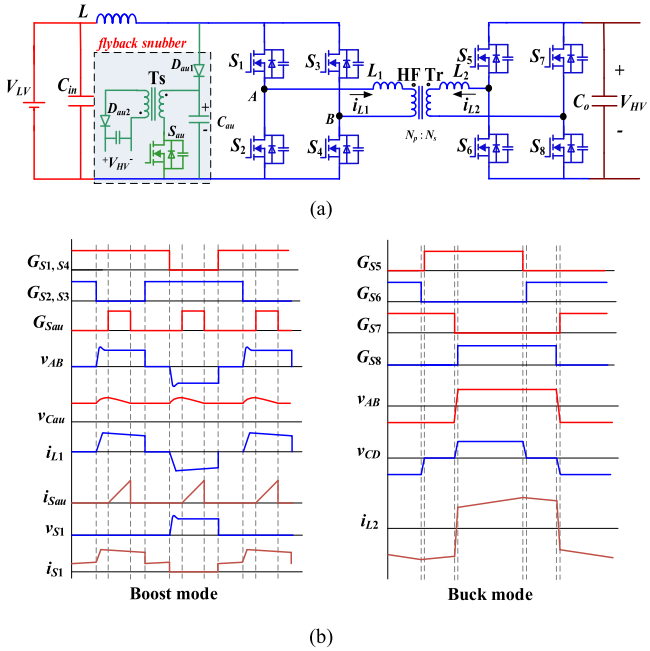

Fig. 34. (a) Topology proposed in [79]. (b) Key operating waveforms.

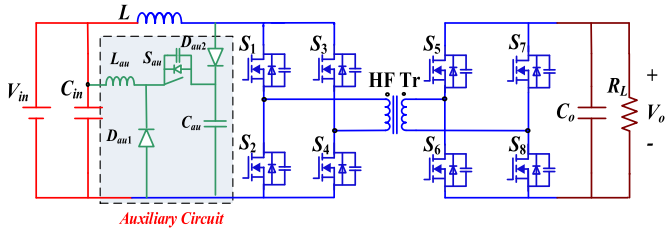

Fig. 35. Topology proposed in [82].

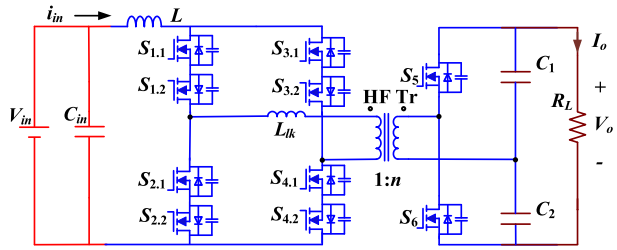

Fig. 36. Topology proposed in [86].

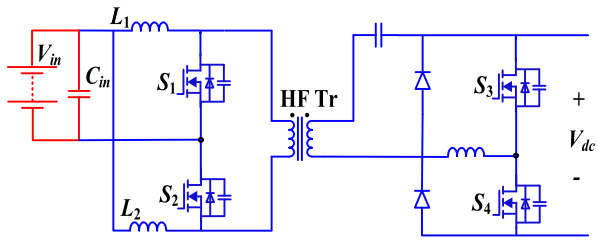

Fig. 37. Topology proposed in [90].

primary switches and ZCS for secondary switches are achieved under all operating conditions. Therefore, it can be universally adopted for interfacing different sources with different voltage ranges such as fuel cells, batteries, and solar panels.

Jwa *et al.* [89] integrate the conventional active clamped full-bridge with a half-bridge *LLC* converter and consequently further improve the converter performance. Low switch voltage stress at low voltage side owing to small duty ratio D and reduced peak currents through main switches and transformer primary due to two transformers structure are achieved compared to active clamped full-bridge converter. Fig. 37 shows an asymmetrical half-bridge bidirectional dc/dc converter [90]. Two inductors are used at the low voltage side and a series blocking capacitor is placed to prevent transformer saturation, which may limit the power transferring capacity of the circuit.

For a hybrid system consisting of renewable energy source and energy storage, it is very important to efficiently draw

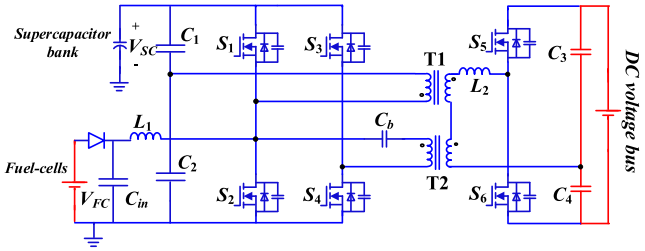

Fig. 38. Topology proposed in [91].

the energy form these two different power sources over wide range of input voltage and load variations. Zhang *et al.* [91] propose a fuel cell-based hybrid topology, shown in Fig. 38. By using two HF transformers, the topology combines a boost half-bridge circuit connecting fuel cell and a full-bridge circuit for supercapacitor which acts as an auxiliary power source on low-voltage side. Due to bidirectional power transfer capability, the proposed topology has three operating modes, i.e., boost mode, supercapacitor power mode, and supercapacitor recharge mode. A PWM plus PSM scheme is utilized to flexibly regulate the bidirectional power flow and achieve a quasi-optimal design that can minimize the RMS value of ac through inductance L_2 and extend the ZVS range.

III. Derivation of Component Cost Models and Loss Models

For the performance evaluation of power electronic converter, five significant aspects about converters are considered: cost, volume, weight, losses, and power density. The trends of development include the increase of the efficiency (reducing the losses) and power density while lowering the cost, weight, and volume. In this section, the component cost models for MOSFET, transformer, inductor, capacitor, heatsink, and gate-driver ICs of the converters are derived. Different loss models, including switching and conduction losses of MOSFET, inductor losses and transformer losses, are presented.

A. Cost Models

1) Power Semiconductors: Generally, the cost of a power semiconductor largely depends on its chip area and package which determine its electrical and thermal properties [92], [93]. The following cost model is established in [92]:

$$\sum_{\mathrm{SC}} = \sigma_{\mathrm{chip},x} A_{\mathrm{chip}} + \sum_{\mathrm{pack},x} \tag{1}$$

where Σ_{SC} is the total cost, $\sigma_{\mathrm{chip},x}$ is the price per chip area A_{chip}, and $\Sigma_{\mathrm{pack},x}$ is the package price. The parameters $\sigma_{\mathrm{chip},x}$ and $\Sigma_{\mathrm{pack},x}$ vary with different chip and packaging technologies. $\sigma_{\mathrm{chip},x}$ represents the sum of all processing and R&D costs for a specific chip technology. $\sigma_{\mathrm{chip},x}$ and $\Sigma_{\mathrm{pack},x}$ of specific chip technology can be obtained through investigating the prices of semiconductor products from its major manufacturer.

CF-IBDC is normally adopted for low-voltage high-current application, where MOSFETs are generally preferred in the engineering design. OptiMOS power MOSFET of Infineon Company are quite mature for the semiconductor devices within 200 V while its CoolMOS power MOSFET is advantageous for the semiconductor devices around 600–650 V. In this paper, OptiMOS and CoolMOS MOSFET of Infineon Company is selected to design the virtual prototype. The specific numerical values of $\sigma_{\mathrm{chip},x}$ and $\Sigma_{\mathrm{pack},x}$ can be obtained by multiparametric least square fitting based on the database samples [94]. Table II presents some numerical values of $\sigma_{\mathrm{chip},x}$ and $\Sigma_{\mathrm{pack},x}$ for different chip technologies and packaging types (ordering quantity is 5000+).

TABLE II
Numerical Values for the Cost Model of MOSFET

Chip technology	OptiMOS			CoolMOS	
	100V	120V	200V	600V	650V
$\sigma_{chip,x}$ (\$/cm^2)	4.9	8.8	12.3	3.8	5.2
Packaging technology	**TO220-3**		**TO263-3**	**TDSON-8**	
$\Sigma_{pack,x}$ (\$/unit)	0.3		0.25	0.4	

2) Transformers and Inductors: Transformers and inductors are both magnetic components, which consist of magnetic core and winding. Therefore, the cost models of transformer and inductor can be divided into two parts, i.e., core cost and winding cost.

For the HF transformers, in order to have a compact design, planar ER cores are used and copper foil or copper sheet is employed as the winding type for the virtual prototype in this study. Therefore, the following transformer cost model for the CF-IBDC is proposed:

$$\begin{aligned}\sum_{T} &= \sum_{\mathrm{core},T} + \sum_{\mathrm{wdg},T} \\ &= a_m W_{\mathrm{core},T}^2 + b_m W_{\mathrm{core},T} + c_m + \sigma_{\mathrm{wdg},T} W_{\mathrm{wdg},T}\end{aligned} \tag{2}$$

where $W_{\mathrm{core},T}$ is the core weight and a_m, b_m, and c_m are constant coefficients depending on the core material. $\sigma_{\mathrm{wdg},T}$ is the cost per winding weight and $W_{\mathrm{wdg},T}$ is the whole winding weight. The given model is applied to the core less than 1 kg. Winding cost should cover the copper cost and corresponding labor cost.

Ferrite core is suitable for the design of transformer operated under 100 kHz or higher frequency. According to the data from a leading supplier of ferrite components (Ferroxcube) for minimum ordering quantity larger than 5000, the numerical values of a_m, b_m, and c_m are 2.484×10^{-4} \$/g^2, 2.621×10^{-3} \$/g and 0.4696 \$, respectively, for 3C95 material [95]. With regard to $\sigma_{\mathrm{wdg},T}$, it is around 0.06 \$/g for copper foil (0.4 mm thickness).

For inductors, to minimize the core losses and reduce the HF skin effect, sendust toroid cores and litz wires are employed. The following cost model of inductor is supposed:

$$\begin{aligned}\sum_{L} &= \sum_{\mathrm{core},L} + \sum_{\mathrm{wdg},L} \\ &= \sigma_{\mathrm{core},L} W_{\mathrm{core},L} + \sum_{\mathrm{fix},L} + \sigma_{\mathrm{wdg},L} W_{\mathrm{wdg},L}\end{aligned} \tag{3}$$

TABLE III
NUMERICAL VALUES FOR THE COST MODEL OF CAPACITOR

	63V	100V	250V	400V	630V
a_f (\$/μF)	0.146	0.156	0.170	0.269	0.633
b_f (\$/unit)	0.049	0.081	0.230	0.186	0.283

where $\sigma_{\mathrm{core},L}$ and $\sigma_{\mathrm{wdg},L}$ are specific costs per weight $W_{\mathrm{core},L}$ and $W_{\mathrm{wdg},L}$. $\Sigma_{\mathrm{fix},L}$ can be considered as the fixed core manufacturing cost. By means of a multiparametric least square fitting of the data supplied by an inductor manufacturer (Micrometals), the parameters $\sigma_{\mathrm{core},L}$ and $\Sigma_{\mathrm{fix},L}$ are 9.429×10^{-3} \$/g and 0.1956 \$/unit [96]. If the winding type is AWG 26 litz wire, $\sigma_{\mathrm{wdg},L}$ is approximately 0.05 \$/g.

3) Capacitors: For the HF-operated CF-IBDC of several kW power level, thin film capacitors are sufficient for the power decoupling. The cost of metallized polyester or metallized polypropylene thin film capacitors is modeled in this section. Based on the study of the capacitor prices of different voltage ratings and capacitances, it can be observed that the unit cost of film capacitors scales linearly with its capacitance value (*C*) for a specific voltage rating. The capacitor model for each specific voltage rating can be expressed in the following:

$$\sum_{C} = a_f C + b_f. \tag{4}$$

Table III shows values of a_f and b_f for several typical voltage ratings. These fitted parameters are obtained based on the data from a major capacitor manufacturer (Kemet) [97].

4) Heatsinks: Generally, the cost of heatsinks largely depends on the material, volume/weight, and manufacturing cost. Aluminium (Al) is widely used as heatsink material. And different manufacturing processes result in various heatsink types, e.g., extruded and hollow-fin. The heatsink cost model can be supposed as follows:

$$\sum_{hs} = \sigma_{hs} V_{hs} + \sum_{\mathrm{fix},hs} \tag{5}$$

where σ_{hs} denotes the cost per volume V_{hs} for a specific heatsink type and $\Sigma_{\mathrm{fix},hx}$ is the fixed cost independent from the volume. For the extruded Al heatsink, σ_{hs} is 0.009 \$/cm^3 and $\Sigma_{\mathrm{fix},hx}$ is 0.27 \$/unit.

5) Gate-Driver ICs: The normal operation of power electronic converters depends on a variety of ICs such as gate-driver ICs. It is difficult to develop a relatively accurate cost model for such ICs due to the dispersion. Consequently, unit costs of gate driver ICs are fixed separately and total costs are determined based on the driving requirement and quantity.

B. Loss Models

1) MOSFET Switching Losses: Due to the equivalent MOSFET input capacitance and Miller effect, switching transients consist of rise time t_r and fall time t_f. The drain–source voltage V_{DS} and the drain current I_D change with a certain slope during these time periods, and the overlap of voltage and current results in power loss. The charge stored in the MOSFET parasitic output capacitor C_{oss} during the switch-off process causes another power loss. In addition, the product of the total gate charge Q_g and gate voltage V_g can be seen as a part of switching losses. The occurrence of reverse recovery of the body diode during the switch-on period generates another loss. Therefore, the MOSFET switching losses consist of four major elements: power loss due to the overlap of current and voltage, parasitic output capacitance loss, gate charge loss, and reverse recovery loss of the body diode [98], [99]. The following loss model is given:

$$\begin{aligned} P_S = f_s \times (&\sigma_1 \times 0.5 \times V_{\mathrm{DS}} \times I_{D\mathrm{on}} \times t_r + \sigma_2 \times 0.5 \times V_{\mathrm{DS}} \\ &\times I_{D\mathrm{off}} \times t_f + 0.5 \times C_{\mathrm{oss}} \times V_{\mathrm{DS}}^2 \\ &+ Q_g V_g + \sigma_3 \times Q_{\mathrm{rr}} V_{\mathrm{rr}}) \end{aligned}$$

$$\sigma_1 = \begin{cases} 1, & \mathrm{hard-switching} \\ 0, & \mathrm{ZVS\ turn-on} \end{cases} \quad \sigma_2 = \begin{cases} 1, & \mathrm{hard-switching} \\ 0, & \mathrm{ZCS\ turn-off} \end{cases}$$

$$\sigma_3 = \begin{cases} 1, & \mathrm{hard-switching} \\ 0, & \mathrm{soft-switching} \end{cases} \tag{6}$$

where f_s is the switching frequency, Q_{rr} is the reverse recovery charge, and V_{rr} is the reverse recovery voltage. The rise time t_r and fall time t_f of switching transient and output capacitance C_{oss} can be read from the diagrams or tables in the MOSFET datasheet. V_{DS}, $I_{D\mathrm{on}}$, $I_{D\mathrm{off}}$ can be obtained from characteristic equations related to the converter's operation or from simulation results. Since the soft-switching operation is achieved in most of aforementioned CF-IBDCs, the switching losses can be reduced compared to those undergoing hard switching. If soft-switching is realized, the current through MOSFET body diode can decrease gradually and commutate with zero current; thus, the reverse recovery effect can be lessened. The variables σ_1, σ_2, and σ_3 are equal to 0 or 1 according to the specific soft-switching conditions (ZVS turn-ON or ZCS turn-OFF).

2) MOSFET Conduction Losses: The instantaneous conduction losses of MOSFET are

$$p_c(t) = V_{\mathrm{DS}}(t) \cdot I_D(t) = R_{\mathrm{DSon}} \cdot I_D^2(t) \tag{7}$$

R_{DSon} is the on-state resistance of MOSFET. By integrating the instantaneous value of $p_c(t)$ over a switching cycle, the average MOSFET conduction losses are expressed as follows:

$$\begin{aligned} P_C &= \frac{1}{T_S}\int_0^{T_S} p_c(t)dt = \frac{1}{T_S}\int_0^{T_S} (R_{\mathrm{DSon}} \cdot I_D^2(t))dt \\ &= R_{\mathrm{DSon}} \cdot I_{D\mathrm{rms}}^2 \end{aligned} \tag{8}$$

where $I_{D\mathrm{rms}}$ is the rms value of the drain current. R_{DSon} can be read from the MOSFET datasheet as well.

3) Inductor Losses: The inductor losses are split into the winding losses (copper losses) and core losses

$$P_L = P_{\mathrm{wdg},L} + P_{\mathrm{core},L}. \tag{9}$$

The copper losses can be calculated as

$$P_{\mathrm{wdg},L} = R_{\mathrm{DC}} \cdot I_{L,\mathrm{avg}}^2 + R_{\mathrm{AC}} \cdot \left[I_{L,\mathrm{avg}}^2 + \frac{1}{12}(\Delta I)^2 \right] \tag{10}$$

where $R_{\rm DC}$ and $R_{\rm AC}$ are the dc resistance and ac resistance of the winding, respectively. $I_{L,\rm avg}$ is the average current through the inductor and ΔI is the current ripple associated with operating condition of converter. $R_{\rm DC}$ can be calculated based on the winding geometry as shown in (11). The existence of $R_{\rm AC}$ is due to the frequency dependent skin effect and proximity effect in the winding, which is much complicated to calculate for litz wires. The analytical model of the round litz wire winding can be found in [100]

$$R_{\rm DC} = \frac{4 \cdot \rho \cdot l_{{\rm wdg},L}}{n_s \cdot \pi \cdot d_s^2} \tag{11}$$

where ρ is the resistivity of litz wire (expressed in Ω·m), $l_{{\rm wdg},L}$ denotes the length of winding, n_s is the number of strands, and d_s is the diameter of the strand. If the ac component of inductor current is negligible, winding loss is mainly determined by $R_{\rm DC}$.

The core losses are computed based on the calculated ac flux density B (expressed in G) and frequency f_s (expressed in Hz). The ac flux density B is related with the inductance L, the inductor current ripple ΔI, the winding turns N, and the core cross-sectional area A_c as (12). ΔI is different among different CF-IBDCs within the same operating condition, which depends upon the numbers of input boost inductors and corresponding modulation schemes

$$B = \frac{L \cdot \Delta I}{N \cdot A_c} \times 10^4. \tag{12}$$

Since the input boost inductors are relatively large with limited small current ripple in most of current-fed dc–dc converters, the core loss of inductor is low compared to the winding loss. The empirical formula of inductor core losses given by Micrometals Company is shown as follows [101]:

$$P_{{\rm core},L} = \left(\frac{f_s}{\frac{a}{B^3} + \frac{b}{B^{2.3}} + \frac{c}{B^{1.65}}} + d \cdot f_s^2 \cdot B^2 \right) \cdot V_{{\rm core},L} \tag{13}$$

where $V_{{\rm core},L}$ is the core volume (cm^3). The loss coefficients a, b, c, and d are listed in manufacturer's catalog. For sendust core with 60 permeability, a, b, c, and d are 7.89×10^9, 7.11×10^8, 8.98×10^6, and 2.85×10^{-14}, respectively.

4) Transformer Losses: The estimation of transformer losses is similar to that of inductor, i.e., the total losses are equal to the winding losses plus the core losses

$$P_T = P_{{\rm wdg},T} + P_{{\rm core},T}. \tag{14}$$

The winding losses include the losses in the primary ($P_{{\rm wdg},Tp}$) and the secondary windings ($P_{{\rm wdg},Ts}$). Copper foils or copper sheets are utilized in virtual prototype design in Section IV and their thickness (δ) design is optimized according to the skin depth at operating switching frequency. Then, the winding losses can be calculated using winding resistance

$$\begin{aligned} P_{{\rm wdg},T} &= P_{{\rm wdg},Tp} + P_{{\rm wdg},Ts} \\ &= \frac{\rho_{\rm Cu} \cdot l_{{\rm wdg},Tp}}{w_{Tp} \cdot \delta} \cdot I_{Tp,\rm rms}^2 + \frac{\rho_{\rm Cu} \cdot l_{{\rm wdg},Ts}}{w_{Ts} \cdot \delta} \cdot I_{Ts,\rm rms}^2 \end{aligned} \tag{15}$$

where $\rho_{\rm Cu}$ is the copper resistivity constant, w_{Tp} and w_{Ts} are primary and secondary winding widths, δ is the winding thickness, and $I_{Tp,\rm rms}$ and $I_{Ts,\rm rms}$ are the rms values of currents through the transformer primary and secondary, respectively.

The core losses are generated by the changing magnetic flux field within the core, which can be approximately calculated by means of the Steinmetz equation. The generalized Steinmetz equation [102]–[104] is very straightforward to use but its corresponding parameters are only valid for sinusoidal excitation, which is not suitable for power electronic applications. For CF-IBDCs analyzed in this paper, the improved Steinmetz equation can be applied, which is efficient to any piecewise linear model with arbitrary nonsinusoidal excitation [105]. The equation is

$$P_{{\rm core},T} = V_{{\rm core},T} \cdot 4^\alpha \cdot k \cdot f_s^\alpha \cdot B_{\rm pk}^\beta \tag{16}$$

where $V_{{\rm core},T}$ is the core volume (cm^3), $B_{\rm pk}$ is defined as half of the peak ac flux density (T), and f_s the switching frequency (kHz). The parameters k, α, and β are constants obtained from curve fitting for a given material with relative permeability. $B_{\rm pk}$ is calculated as

$$B_{\rm pk} = \frac{B_{\rm ac,max} - B_{\rm ac,min}}{2}. \tag{17}$$

$B_{\rm pk}$ can be determined by first calculating H (A·T/cm) at each ac extreme

$$H_{\rm ac,max} = \frac{N \cdot I_{\rm ac,max}}{l_m} \quad H_{\rm ac,min} = \frac{N \cdot I_{\rm ac,min}}{l_m} \tag{18}$$

where N is the number of winding turns and l_m is the magnetic path length. From $H_{\rm ac,max}$, $H_{\rm ac,min}$ and the B–H curve, $B_{\rm ac,max}$ and $B_{\rm ac,min}$ can be derived and therefore $B_{\rm pk}$ is determined. For example, k, α, and β are 6.14×10^{-4}, 1.95, and 3.11, respectively, for 3C95 material given by Ferroxcube Company [95].

Loss calculations of different reviewed topologies have been done assisted by the simulation results and the designed virtual prototypes. The virtual prototypes are designed under the same defined design principles, which provides us the selection of the MOSFETs, inductor/transformer cores, and windings as illustrated in Table V. Components-related parameters like MOSFET's $C_{\rm oss}$, Q_g, Q_{rr}, t_r, t_f, $R_{\rm DSon}$ and empirical formula of inductor/transformer core loss calculation parameters can be obtained from corresponding technical datasheet. Converter operation-related parameters like device voltage/current during switching $V_{\rm DS}$, $I_{D\rm on}$, $I_{D\rm off}$, input current ripple, rms current and peak current flowing through inductor/transformer/switches can be obtained from characteristic equations or from simulation results. Then, the loss of the different reviewed topologies can be calculated based on the presented loss models.

IV. Comparison and Analysis

In this section, a quantitative and comprehensive performance comparison is conducted for the seven typical converters (Figs. 3, 8, 14, 20, 25, 30, and 31), which are selected from each type of all reviewed CF-IBDC topologies. In order to have a fair comparison of these topologies, a virtual prototype of each topology has been designed for the same specification: 20–40 V

TABLE IV
COMPARISON OF COMPONENTS' COUNT AND RATINGS OF DIFFERENT CF-IBDC TOPOLOGIES

Topology	Single-Phase Active Clamped (Fig. 3)	Dual Half-Bridge (Fig. 14)	L-L Type Dual Active Bridge (Fig. 20)	Resonant Type (Fig. 25)	Naturally Clamped Full-Bridge (Fig. 31)	L-L Type Naturally Clamped (Fig. 30)	Three-Phase Active Clamped (Fig. 8)
No. of switches	Primary: 5 Secondary: 4	Primary: 2 Secondary: 4	Primary: 4 Secondary: 4	Primary: 4 Secondary: 4	Primary: 4 Secondary: 4	Primary: 2 Secondary: 4	Primary: 6 Secondary: 6
RMS currents of switches	Primary: 4×67A, 1×40.2A Secondary: 2×6.8A, 2×6.5A	Primary: 43.7A, 135A Secondary: 2×5.4A, 2×5A	Primary: 2×6.9A, 2×63A Secondary: 2×9A, 2×10.9A	Primary: 2×11.54A, 2×68A Secondary: 4×3.98A	Primary: 4×65A Secondary: 4×6.94A	Primary: 2×62.6A Secondary: 4×5.62A	Primary: 3×48A, 3×22A Secondary: 6×3.5A
Voltage stresses of switches	Primary: 65.5V Secondary: 400V	Primary: 60V Secondary: 400V	Primary: 88V Secondary: 200V	Primary: 59V Secondary: 400V	Primary: 50V Secondary: 400V	Primary: 88.9V Secondary: 400V	Primary: 65.5V Secondary: 400V
No. of passive components	1 inductor (8μH/100.24A), 2 capacitors (20μF/64.9V, 4μF/400V)	1 inductor (15μH/102A), 4 capacitors (60μF/40V, 180μF/20V, 6.6μF/267.4V×2)	2 inductors (12μH/51.1A×2), 4 capacitors (6μF/79.7V, 10μF/204.5V, 4μF/203.8V×2)	4 inductors (2μH/53.8A×2, 15μH/44.77A, 30μH/2.4A), 4 capacitors (12μF/55V, 185μF/19.9V, 169nF/597V, 1.5μF/400V)	1 inductor (7μH/103.5A), 1 capacitor (5μF/400V)	2 inductors (12μH/51.2A×2), 1 capacitor (4μF/400V)	3 inductors (2μH/38.9A×3), 2 capacitors (20μF/65.5V, 1.2μF/400V)
Transformer turns ratio	1:8	1:6.67	1:2.25	1:8	1:8	1:4.5	1:6
Leakage inductance (rms current)	0.1μH (79.5A)	0.28μH (97.6A)	0.93μH (38.7A)	--	0.76μH (78A)	0.98μH (35.8A)	0.15μH (28A)
Types of Soft-switching (primary/ secondary)	ZVS/ZVZCS	ZVS/ZVS	ZVS/ZVS	ZVS/ZVZCS	ZVZCS/ZVS	ZVZCS/ZVS	ZVS/ZVZCS
Modulation	PWM	PWM+PSM	PWM+PSM	PWM	PWM+PSM	PWM+PSM	PWM
Additional components	1 switch and gate driver, 1 capacitor	Nil	1 capacitor	2 inductors, 2 capacitors	Nil	Nil	1 capacitor

low-voltage input, 400-V high-voltage output, 2-kW power rating, 100-kHz switching frequency, 10-A input current ripple, and 4-V output voltage ripple. To verify the design parameters of each virtual prototype and assure them coincide closely with the original papers, simulations have been performed on PSIM 9.1 as well.

Table IV shows the components count and ratings of different topologies of CF-IBDCs in boost mode operation (20-V input voltage, 400-V output voltage, 2-kW power transferring). Soft-switching characteristics have also been listed. From Table IV, it can be seen that active clamped (single-phase and three-phase), *L-L* type dual active bridge and resonant-type CF-IBDCs require additional switches or passive components to achieve soft switching and suppress voltage spikes. The current stresses of low-voltage-side switches of CF-IBDCs with single half-bridge (see Fig. 14) or two parallel half-bridges configuration (Figs. 20 and 25) are considerably different. The rms current flowing through primary low-side switches is much higher than primary high-side switches since the primary low-side switches are main switches while the high-side switches play the role of auxiliary clamp switches. Such situation brings difficulty to the thermal design of the system. For the three-phase active clamped CF-IBDC, the rms current of switches at both sides are significantly reduced. Nevertheless, higher quantities of switches are required. *L-L* type converters (Figs. 20 and 30) have higher boost capacity than the full-bridge converters (Figs. 3 and 31) and single half-bridge converter (see Fig. 14), while the voltage stress of primary side switches in *L-L* type topologies is higher than that of full-bridge and single half-bridge topologies. This feature is lost for the resonant-type converter (Fig. 25). Due to the voltage doubling effect of the neutral point clamped circuit on high voltage side, the transformer turns ratio of *L-L* type dual active bridge is the lowest. For passive components, the sizes of input inductors and output capacitor of the three-phase topology are significantly reduced compared with single-phase topologies due to the interleaving structure. The resonant-type converter needs additional inductors and capacitors to form a resonant tank. With regard to soft-switching characteristics, naturally clamped CF-IBDCs can realize ZVZCS of low-voltage-side switches featuring low switching loss which will be analyzed

TABLE V
COMPARISON OF THE DESIGN SPECIFICATIONS AND COMPONENT COSTS OF DIFFERENT CF-IBDC TOPOLOGIES

Topology / Costs ($)	Single-Phase Active Clamped (Fig. 3)	Dual Half-Bridge (Fig. 14)	L-L Type Dual Active Bridge (Fig. 20)	Resonant Type (Fig. 25)	Naturally Clamped Full-Bridge (Fig. 31)	L-L Type Naturally Clamped (Fig. 30)	Three-Phase Active Clamped (Fig. 8)
	33.06	**25.24**	**22.68**	**25.34**	**24.6**	**21.16**	**39.99**
MOSFETs	4×IPP023N10N5 (100V, 120A) 1×IPD050N10N5 (100V, 80A) 4×IPP60R060C7 (650V, 35A)	1×IPD050N10N5 (100V, 80A) 2×IPP023N10N5 (100V, 120A) 4×IPP60R060C7 (650V, 35A)	2×BSZ240N12NS3 (120V, 37A) 2×IPB038N12N3 (120V, 120A) 4×IPP60R060C7 (650V, 35A)	2×IPA180N10N3 (100V, 28A) 2×IPP023N10N5 (100V, 120A) 4×IPP60R060C7 (650V, 35A)	4×IPP023N08N5 (80V, 120A) 4×IPP60R060C7 (650V, 35A)	2×IPB038N12N3 (120V, 120A) 4×IPP60R060C7 (650V, 35A)	3×IPP023N10N5 (100V, 120A) 3×IPD050N10N5 (100V, 80A) 6×IPP60R060C7 (650V, 35A)
Gate driver ICs	**8.38**	**6.67**	**6.6**	**6.64**	**6.64**	**3.88**	**9.96**
	3×IR2010S 2×IRS2113	1×IR2010S 1×AUIR08152S 2×IRS2113	2×IRS2181S 2×IR2010S	2×IR2010S 2×IRS2113	2×IR2010S 2×IRS2113	1×IRS4426S 2×IRS2113	3×IR2010S 3×IRS2113
	7.52	**18.4**	**6.97**	**7.66**	**7.52**	**6.74**	**12.42**
Transformer (planar ER core & copper foil winding)	Core: ER51/10/38-3C95 Winding: 0.4mm×10mm×4, 2 turns (primary) 0.4mm×5mm, 16 turns (secondary)	Core: ER64/13/51-3C95 Winding: 0.4mm×10mm×5, 2 turns (primary) 0.4mm×4mm, 13 turns (secondary ×2)	Core: ER51/10/38-3C95 Winding: 0.4mm×9mm×2, 4 turns (primary) 0.4mm×8mm, 9 turns (secondary)	Core: ER51/10/38-3C95 Winding: 0.4mm×10mm×2, 4 turns (primary) 0.4mm×3mm, 32 turns (secondary)	Core: ER51/10/38-3C95 Winding: 0.4mm×10mm×4, 2 turns (primary) 0.4mm×5mm, 16 turns (secondary)	Core: ER51/10/38-3C95 Winding: 0.4mm×8mm×2, 4 turns (primary) 0.4mm×4mm, 18 turns (secondary)	3×Core: ER41/7.6/32-3C95 3×Winding: 0.4mm×8mm×2, 5 turns (primary) 0.4mm×2mm, 30 turns (secondary)
	18.42	**27.49**	**19.9**	**49.17**	**15.72**	**19.9**	**21.87**
Inductor (sendust toroid core & litz wire)	Core: MS-250060-2 Winding: #26AWG×300, 8 turns	Core: MS-292060-2 Winding: #26AWG×300, 11 turns	Core: MS-226060-2 (×2) Winding: #26AWG×150, 11 turns (×2)	a. Core: MS-200026-2 (×2) Winding: #26AWG×300, 8 turns (×2) b. Core: MS-292014-2 Winding: #26AWG×10, 25 turns c. Core: ER64/13/51-3C95 Winding: 0.4mm×10mm×2, 13 turns	Core: MS-250060-2 Winding: #26AWG×300, 7 turns	Core: MS-226060-2 (×2) Winding: #26AWG×150, 11 turns (×2)	Core: MS-185014-2 (×3) Winding: #26AWG×150, 11 turns (×3)
	6.27	**23.27**	**4.67**	**16.64**	**3.26**	**2.75**	**4.56**
Capacitor (metallized polyester/ polypropylene film capacitor)	100V DC / 22μF, 630V DC / 3.9μF	63V DC / 56μF, 63V DC / 180μF, 400V DC / 6.8μF (×2)	100V DC / 5.6μF, 250V DC / 3.9μF (×2), 250V DC / 10μF	900V AC / 0.18μF, 100V DC / 12μF, 63V DC / 180μF, 630V DC / 1.5μF	630V DC / 4.7μF	630V DC / 3.9μF	100V DC / 22μF, 630V DC / 1.2μF
Heatsink	**3.47**	**2.46**	**3.06**	**1.85**	**2.36**	**1.9**	**2.37**
Total	**77.12**	**103.53**	**63.88**	**107.3**	**60.1**	**56.33**	**91.17**

next, while other type topologies can only achieve ZVS. And the employed modulation methods in active clamped and resonant-type converters are PWM, and PWM plus PSM is adopted in the rest. This has been studied in detail in Section II.

To have a quantitative comparison in terms of multiple performance indices like cost, volume, weight, losses, and power density, a virtual hardware for each selected topology needs to be designed under the same design principle. The following selection and design principles of converter components are adopted. As for the selection of MOSFET, voltage rating is 1.5× voltage stress and current rating is 2× current stress, with low ON-state resistance. As regard to the design of HF transformer, the principle is to obtain the minimum overall transformer loss. The window fill factor of inductor is set to 0.4. For the capacitor selection, voltage rating is 1.5× its voltage stress. The heatsink volume is calculated for the case that the device junction temperature is maximum and the ambient temperature is 40 °C with natural convection.

The details of designed virtual hardware prototypes and corresponding costs have been listed in Table V. Fig. 39 depicts costs distribution and comparison of different type CF-IBDCs based on the aforementioned cost models. The cost of active components for active clamped topologies (see Figs. 3 and 8) is much higher than the rest due to the fact that they have the highest number of switches with high current rating, which is relevant to the chip area. Comparing the single-phase active clamped topology with the three-phase one, the latter costs more in the transformer design due to the three-phase transformer that is assembled using three single-phase transformers. Although the three-phase CF-IBDC contains three input boost inductors more than other compared converters, its cost of inductors is close to that of others owing to the reduced size of this passive

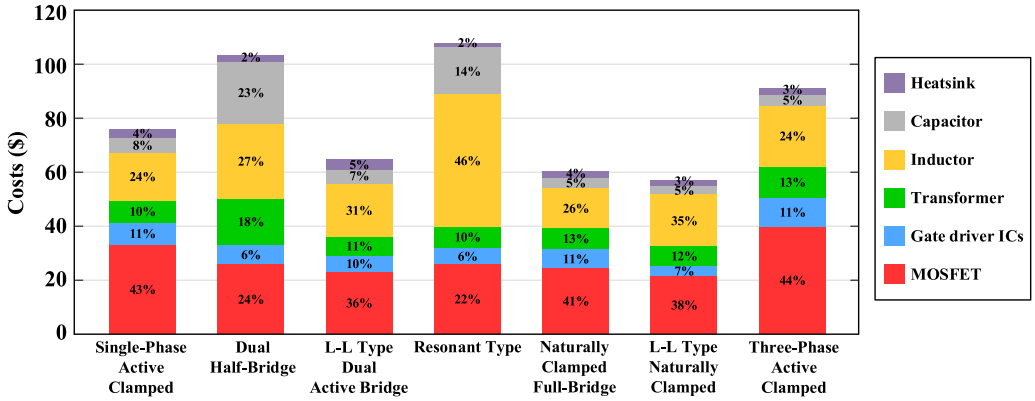

Fig. 39. Costs distribution and comparison of different type CF-IBDCs.

TABLE VI
PERFORMANCE COMPARISON OF DIFFERENT CF-IBDC TOPOLOGIES

Topology		Single-Phase Active Clamped (Fig. 3)	Dual Half-Bridge (Fig. 14)	L-L Type Dual Active Bridge (Fig. 20)	Resonant Type (Fig. 25)	Naturally Clamped Full-Bridge (Fig. 31)	L-L Type Naturally Clamped (Fig. 30)	Three-Phase Active Clamped (Fig. 8)
Losses (W)	Switching	33.15	23.19	13.42	12	7.28	6.55	29.24
	Conduction	52.06	32.03	48.18	25.92	43.8	31.65	23.9
	Transformer	3.59	5.45	3.65	4.6	3.61	3.45	8.22
	Inductor	6.68	7.87	9.04	30.26	5.62	10.06	19.13
Total		**95.48**	**68.54**	**74.29**	**72.78**	**60.31**	**51.71**	**80.49**
Volume (cm^3)	Transformer	33.23	64.68	32.2	33.5	33.23	31.77	53.15
	Inductor	99.29	155.45	103.74	253.78	91.78	103.74	100.79
	Capacitor	34.8	98.29	22.44	94.96	24.93	24.93	28.88
	Heatsink	325	213.3	250.1	145.2	202.7	151.7	202.4
Total		**492.32**	**531.72**	**408.48**	**527.44**	**352.64**	**312.14**	**385.22**
Weight (kg)	Transformer	0.21	0.39	0.2	0.21	0.21	0.19	0.34
	Inductor	0.63	0.97	0.66	1.47	0.57	0.66	0.61
	Capacitor	0.05	0.14	0.03	0.12	0.03	0.03	0.04
	Heatsink	0.88	0.58	0.68	0.39	0.55	0.41	0.55
Total		**1.77**	**2.08**	**1.57**	**2.19**	**1.36**	**1.29**	**1.54**
Power Density (W/cm^3)		**4.26**	**3.89**	**5.08**	**3.93**	**5.84**	**6.57**	**5.40**
Efficiency		**95.44%**	**96.69%**	**96.42%**	**96.49%**	**97.07%**	**97.48%**	**96.13%**

component. Considering the overall cost, dual half-bridge (see Fig. 14) and resonant-type (see Fig. 25) converters are much higher than the rest topologies. For the dual half-bridge topology, two capacitors with much larger capacitance are employed. Moreover, the three-winding transformer design with high current flowing through and the largest core size results in a higher cost. For the resonant-type topology, resonating components cause the raises of the overall cost since ac flows through the resonating inductor and capacitor. External inductor generally needs to be added in parallel connection with HF transformer, which causes extra costs. The costs of the rest single-phase CF-IBDC converters (see Figs. 20, 30, and 31) are competitive with each other and *L-L* type naturally clamped topology has the potential lowest cost.

Table VI lists the numerical values of other performance indices (losses, volume, weight, and power density) of designed virtual prototypes. Fig. 40 depicts the losses distribution and comparison based on the aforementioned loss models. The MOSFET switching losses and conduction losses dominate the total losses of the converters. The MOSFET switching loss of the active clamped topologies is top two among these seven converters owing to having the larger number of switches and higher voltage and current values of low-voltage-side switches at the turn-OFF transient. For the dual half-bridge topology, the turning-OFF current value of low-voltage-side switches is considerably high as well so that its switching loss is large. Note that the switching loss of three-phase active clamped topology with the highest number of MOSFETs is lower than the

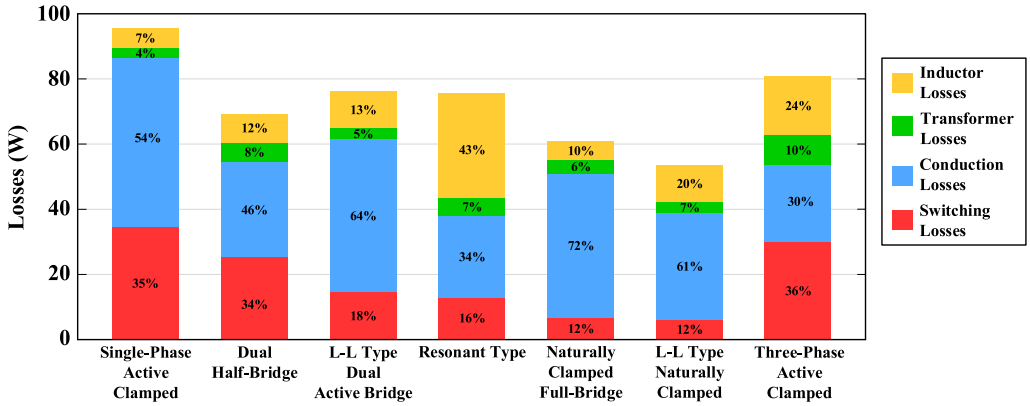

Fig. 40. Losses distribution and comparison of different type CF-IBDCs.

single-phase active clamped type because of lower turn-ON and turn-OFF currents through the switches. Due to ZCS turn-OFF for low-voltage-side switches which handles large current in naturally clamped topologies, the switching losses of these type CF-IBDCs are greatly reduced.

MOSFET conduction losses are mainly decided by the rms current, number of switches, and ON-state resistance, while ON-state resistances are highly influenced by device rating. RMS current and ON-state resistance are decided by the converter's operation, as clearly illustrated by Table IV. Single-phase active clamped, *L-L* type dual active bridge and naturally clamped full-bridge converters are higher than the rest because they have large amounts of MOSFETs with high rms current values. Generally, the MOSFET with lower current rating has higher ON-state resistance than that with higher current rating for the same voltage rating, which directly affects the conduction loss. As for the three-phase converter, although the applied MOSFET products in virtual prototype have the same ON-state resistances as the single-phase active clamped topology and the quantity used is large, its conduction loss is the lowest among these compared topologies owing to reduced rms current of switches. With both higher switching loss and conduction loss, the single-phase active clamped topology has the highest losses.

The total losses of active components of resonant-type topology are the lowest which is a remarkable merit. However, the inductor loss of resonant-type topology is much higher than the rest due to the large ac flowing through the resonating inductor, which causes large core loss and winding loss. The resonant-type topology may have better performance for low-current application. Except for resonant-type CF-IBDC, other topologies only have the inductors at input side. The inductor loss of *L-L* type topologies is higher than that of topologies assembling single input boost inductor. This is because applying the same design principle of 10-A input current ripple and each input inductor of *L-L* type topologies can deal with larger ripple due to the interleave structure, which in turn increases the loss. According to the overall losses, the efficiency of seven comparative topologies is all higher than 95%, and even reaches 97.5%. Naturally clamped CF-IBDCs achieve the highest efficiency due to both low switching loss and low passive component loss. Half-bridge type seems to have higher efficiency than its corresponding full-bridge type due to smaller amount of switches.

In addition to costs and losses, volume and weight of converters are also compared, as shown in Figs. 41 and 42. The numerical calculation of components' volume and weight are on the basis of the selection and design principles. The volume of heatsink is determined by the total losses of power semiconductors and it takes a main proportion of overall converter volume except for the resonant-type topology. Therefore, the single-phase active clamped converter requires the largest heatsink volume owing to its highest MOSFET losses while the resonant-type converter needs the smallest heatsink volume for its lowest MOSFET losses. Due to the usage of planar ER core and thin copper foil in the design of HF transformer, the transformer volume accounts for a small proportion of the overall converter volume. And the three-phase transformer and three-winding transformer design in three-phase active clamped and dual half-bridge CF-IBDCs, respectively, cause higher volume and weight of transformer than others. But the total volume and weight of three-phase active clamped topology is relatively small among these topologies compared, since it has advantages of smaller size of reactive components and higher power density. For the dual half-bridge and resonant-type converters, high passive components' counts and ratings result in larger volume and weight of passive components.

The components' weight distribution shows that the weight of magnetic components is the major part in the total weight of the virtual hardware as shown in Fig. 42. The volume and weight of naturally clamped topologies are lower in comparison with other type topologies because of no requirements of extra components. Since two input inductors are necessary in *L-L* type naturally clamped topology, the volume and weight of inductors of it are slightly larger than full-bridge type. However, owing to lower losses of switches which necessitate smaller size of heatsink, the overall volume and weight of *L-L* type naturally clamped topology are lower than naturally clamped full-bridge topology. The power density of a converter is defined as the total power divided by its volume. Fig. 43 shows the comparison of power densities with respect to selected CF-IBDCs. The comparison result of power density coincides closely with the comparison

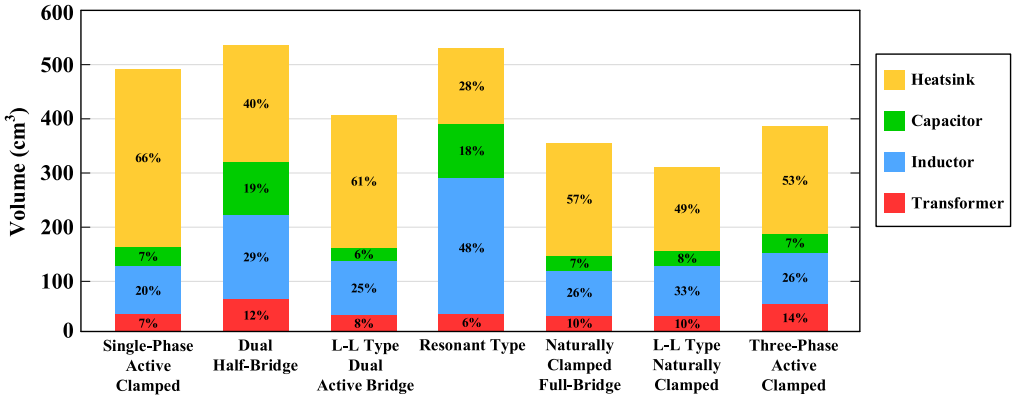

Fig. 41. Volume distribution and comparison of different type CF-IBDCs.

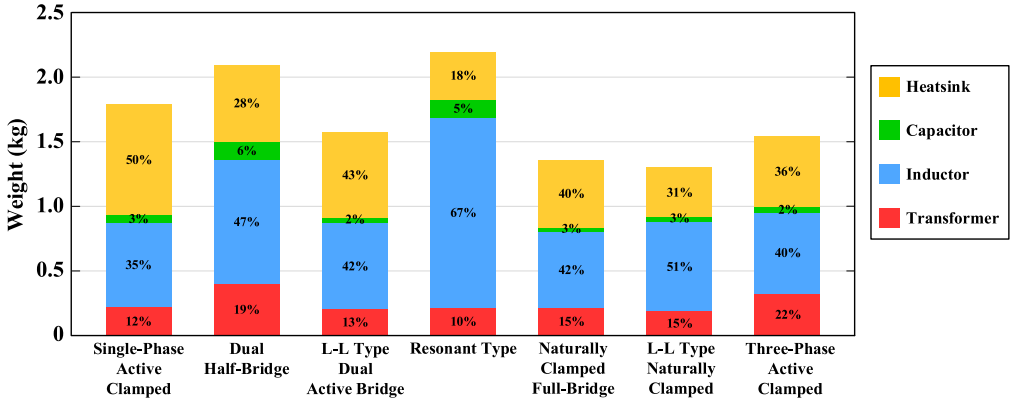

Fig. 42. Weight distribution and comparison of different type CF-IBDCs.

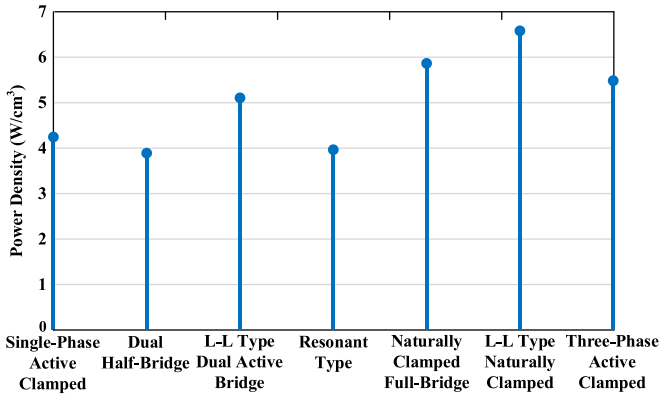

Fig. 43. Power density of different type CF-IBDCs.

of volume. Fig. 44 illustrates the comprehensive comparison of seven topologies regarding aforementioned five performance indices. Although the single-phase active clamped CF-IBDC features the highest overall losses compared with others, its total costs and power density are moderate. Half-bridge derived topology are meritorious than full-bridge derived topology, like *L-L* type dual active bridge versus full-bridge active clamped and *L-L* type naturally clamped versus full bridge naturally clamped. This is due to the reason that the performance is constrained by the low-voltage-side switches for low-voltage high-current application. With smaller amounts of active switches, half-bridge switches are advantageous to some extent. The performance of resonant-type topology is at the most disadvantageous place due to the limitation of passive components for low-voltage high-current application. For other application specification, its performance could be better with the lowest active components losses. Although the three-phase type costs more, it performs well in other aspects.

V. Applications

CF-IBDCs would be a smart choice for application with low voltage high current. Typical applications include auxiliary dc/dc converter to interface low-voltage energy storage (12/24/48 V) and high voltage dc bus in the range of 200–900 V for transportation electrification, renewable energy generation such as solar photovoltaic and fuel cell with low voltage energy storage, and hybrid dc microgrid with multiple voltage level. Different application scenario has different electrical specifications and performance requirements in terms of cost, efficiency, weight, volume, and reliability, which results in different selections of reviewed CF-IBDCs.

As illustrated by Fig. 39, naturally clamped and *L-L* type dual active bridge CF-IBDCs provide low-cost solutions.

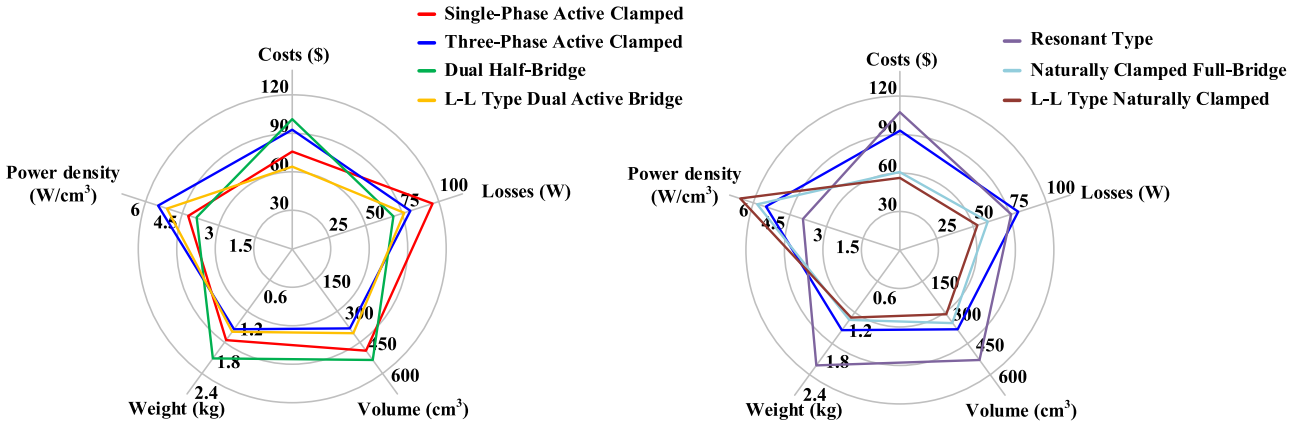

Fig. 44. Comparison of different type CF-IBDCs regarding costs, losses, volume, weight, and power density.

However, if efficiency and lifetime can be compromised, dual half-bridge CF-IBDC has the potential lowest cost. For the selected dual half-bridge CF-IBDC, capacitor, inductor, and transformer contribute to a large proportion of total cost. If electrolytic capacitor is allowed to be employed to mitigate input current ripple and achieve voltage clamping, the cost of capacitor and inductor can be reduced enormously. The topology of Fig. 11 can be chosen to achieve minimized devices count, although the wide range efficiency is scarified to some extent. Compared with dual half-bridge CF-IBDC in Fig. 14, the cost of devices and transformer can be much reduced. With the considerable reduction of capacitor, inductor, transformer, and devices, the dual half-bridge CF-IBDC is capable of achieving the lowest cost. Dual half-bridge CF-IBDC is suitable for the application like small urban city driving or residential driving (driving range of 100 km) where cost is valued more than the efficiency and lifetime.

The naturally clamped CF-IBDCs represent the optimal topologies among the selected options and for the given system specifications and design constraints as shown by Fig. 44. They can achieve high efficiency and high power density while saving a large part of costs without the need of external snubbers. Since the voltage clamping is achieved through completely software control, its reliability under different operating scenarios like extreme load, wide transient, and failure conditions needs to be researched and evaluated further. Another issue is that control schemes are different for bidirectional power transferring, and the seamlessly transfer between boost mode and buck mode has not yet been reported. Before these issues are solved, it is recommended to apply CF-IBDCs to the application like hybrid dc microgrid, where cost and efficiency are weighted more than reliability.

As the energy demand from low-voltage dc source on electrical vehicles (EVs)/more electric aircraft/all electric aircraft, etc., keeps increasing, the needs for bidirectional dc/dc converters capable of handling large current with high reliability, high efficiency, high power density, and low cost are growing. Compared with naturally clamped CF-IBDCs, the control of bidirectional power transferring of *L-L* type dual active bridge is symmetrical and easy to be implemented. *L-L* type dual active bridge can achieve high efficiency over wide range of input voltage/output voltage/loads variations, and hardware voltage clamping is more reliable. This is quite critical for a lot of applications. For example, voltage across the energy storages varies under different operating conditions, and in many cases the high-voltage dc bus is not fixed. In EVs, high-voltage dc bus varies in wide range to achieve the highest "fuel economy." For the renewable energy generation system, if the high voltage bus is directly connected with solar photovoltaic and fuel cell, its output voltage varies. Therefore, *L-L* type dual active bridge is quite advantageous for these applications. With the exception of naturally clamped topology, *L-L* type dual active bridge CF-IBDCs provide the optimized overall performances as shown by Fig. 44, which makes it the best candidate for the transportation electrification application and renewable energy generation system.

L-L type dual active bridge is quite flexible and can be easily modified into multiport structure as well [48]. This feature makes it suitable for the applications like the hybrid energy storage system or the hybrid renewable energy generation system.

For the resonant-type CF-IBDC, owing to circulating current, peak (above $2\times$) and rms current through the devices and components is high. This makes the ratings of the components high and their selection difficult for low-voltage high-current applications. In addition, its power density is limited by the passive elements of resonating bank especially for low-voltage high-current condition. This can be alleviated for high-voltage application. Therefore, the resonant-type CF-IBDC can be applied to interface high-voltage power battery in transportation electrification application. Or like wireless charging application in [62], the heavy and bulky devices are placed off the board.

For low-voltage high-current application, the voltage stress of primary switches is quite critical to achieve high efficiency. As given by the table, the voltage stress of half-bridge derived topology doubles the full-bridge derived topology and push–pull topology. Thus, for the low-voltage application less than 30 V (like 12/24 V storage), half-bridge-derived topology is competitive. Once the voltage specification goes higher than 30 V, the choice between half-bridge derived topology and full-bridge-derived topology needs to be evaluated comprehensively. Generally, *L-L* type dual active bridge is one special type of active clamped topologies. Other type active clamped CF-IBDCs have the potential to be applied to transportation

electrification application and renewable energy generation system as well with different design specification.

As discussed above, three-phase topology is promising for high-power applications with advantages of reduced current rating in active components, smaller size of reactive components compared with corresponding single-phase converter. Three-phase converter is capable of working with partial power even one of the phases fails, thus providing higher reliability. Three-phase CF-IBDCs play an important role in the high-power application that values more about reliability, efficiency, power density than the cost. Three-phase converters can be applied to transportation electrification application with need of heavy power and high reliability.

In practical design, it depends on the engineering design and markets constraints whether particular topogloies are favorable for the specific design specifications.

VI. Future Trend

In view of the discussion and evaluation about state-of-the-art CF-IBDCs in previous sections, many researches have focused on the topology, modulation strategy, soft-switching solution, and hardware design optimization. In future, the improvement of the converter efficiency and power density while lowering the costs and weight is the trend. In addition, the reliability and modularity are another two significant indicators, which are concerned with the development of smart grid and energy internet [106]. Furthermore, as the mediation module, converter should achieve wide input voltage variation and output voltage variation range on the premise of high efficiency. New topologies and corresponding modulation and soft-switching techniques are expected to be further researched for wide input voltage wide output voltage applications. The utilization of SiC/GaN power devices will allow the design of higher switching frequency and lower switching loss of converters, thus contributing to higher power density [107]. But it is worth noting that presently SiC/GaN-based power semiconductors cannot compete with Si devices in terms of the current rating, while the conduction loss plays a dominant role in low-voltage high-current applications instead of the switching loss. Therefore, a trade-off about the device selection and usage should be made in practice.

VII. Conclusion

CF-IBDCs have been widely used in low-voltage, high-current, and high-voltage gain applications. This paper has provided an overview of state-of-the-art researches of CF-IBDCs. The studied CF-IBDCs were divided into six types, including active clamped, dual half-bridge, *L-L* type dual active bridge, resonant-type, naturally clamped, and others. Different topologies with their circuit structures, modulation strategies, basic operation, soft-switching characteristics, and advantages and disadvantages have been reviewed and discussed in detail. In addition, the costs model and losses model of converter components have been presented in this paper. On this basis, comprehensive study and comparison of several typical types of CF-IBDCs with regard to quantized costs, volume, weight, losses, and power densities have been conducted for the given specification. At the end of this paper, several prospective and specific applications of different type CF-IBDCs have been presented as well. There exists a huge scope of further development of these topologies and this paper helps advanced and ongoing research.

References

[1] J. M. Carrasco *et al.*, "Power-electronic systems for the grid integration of renewable energy sources: A survey," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002–1016, Jun. 2006.

[2] M. Manojkumar, K. Porkumaran, and C. Kathirvel, "Power electronics interface for hybrid renewable energy system—A survey," in *Proc. Int. Conf. Green Comput. Commun. Elect. Eng.*, Coimbatore, India, 2014, pp. 1–9.

[3] P. V. Joshi, Y. S. Bhavsar, S. S. Dhamal, A. M. Lulhe, and T. P. Pandhi, "Grid interconnection of DC microgrid at distribution level using power electronic converter system-MATLAB/Simulink modeling and analysis," in *Proc. Int. Conf. Autom. Control Dyn. Optim. Techn.*, Pune, India, 2016, pp. 1056–1061.

[4] Z. Liao and X. Ruan, "Control strategy of bi-directional DC/DC converter for a novel stand-alone photovoltaic power system," in *Proc. IEEE Vehicle Power Propulsion Conf.*, Harbin, China, 2008, pp. 1–6.

[5] R.-J. Wai and R.-Y. Duan, "High-efficiency power conversion for low power fuel cell generation system," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 847–856, Jul. 2005.

[6] X. Li, W. Zhang, C. Du, K. Ma, X. Wu, and D. Xu, "Investigation to power conversion topology for fuel cell power generation system," in *Proc. Int. Power Electron. Conf.*, Sapporo, Japan, 2010, pp. 2637–2643.

[7] A. Mehdipour and S. Farhangi, "Comparison of three isolated bi-directional DC/DC converter topologies for a backup photovoltaic application," in *Proc. 2nd Int. Conf. Elect. Power Energy Convers. Syst.*, Sharjah, United Arab Emirates, 2011, pp. 1–5.

[8] A. Averberg, K. R. Meyer, C. Q. Nguyen, and A. Mertens, "A survey of converter topologies for fuel cells in the kW range," in *Proc. IEEE Energy 2030 Conf.*, Atlanta, GA, USA, 2008, pp. 1–7.

[9] A. K. Rathore and U. Prasanna, "Comparison of soft-switching voltage-fed and current-fed bi-directional isolated DC/DC converters for fuel cell vehicles," in *Proc. IEEE Int. Symp. Ind. Electron.*, Hangzhou, China, 2012, pp. 252–257.

[10] P. Xuewei and A. K. Rathore, "Comparison of bi-directional voltage-fed and current-fed dual active bridge isolated dc/dc converters low voltage high current applications," in *Proc. IEEE 23rd Int. Symp. Ind. Electron.*, Istanbul, Turkey, 2014, pp. 2566–2571.

[11] V. Fernão Pires, E. Romero-Cadaval, D. Vinnikov, I. Roasto, and J. F. Martins, "Power converter interfaces for electrochemical energy storage systems—A review," *Energy Convers. Manage.*, vol. 86, pp. 453–475, Oct. 2014.

[12] A. K. Rathore, "Current-fed DC/DC converters for high voltage gain and low voltage high current applications: An overview of topologies and modulation techniques," in *Proc. IEEE Int. Conf. Power Electron. Drives Energy Syst.*, Trivandrum, India, 2016, pp. 1–6.

[13] K. Harada and H. Sakamoto, "Switched snubber for high frequency switching," in *Proc. 21st Annu. IEEE Conf. Power Electron. Spec.*, San Antonio, TX, USA, 1990, pp. 181–188.

[14] L. Zhu, "A novel soft-commutating isolated boost full-bridge ZVS-PWM DC-DC converter for bidirectional high power applications," in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf.*, Aachen, Germany, vol. 3, 2004, pp. 2141–2146.

[15] E.-S. Kim, K.-Y. Joe, H.-Y. Choi, Y.-H. Kim, and Y.-H. Cho, "An improved soft switching bi-directional PSPWM FB DC/DC converter," in *Proc. 24th Annu. Conf. IEEE Ind. Electron. Soc.*, Aachen, Germany, vol. 2, 1998, pp. 740–743.

[16] S.-J. Jang, T.-W. Lee, W.-C. Lee, and C.-Y. Won, "Bi-directional dc-dc converter for fuel cell generation system," in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf.*, vol. 6, 2004, pp. 4722–4728.

[17] Y. Miura, M. Kaga, Y. Horita, and T. Ise, "Bidirectional isolated dual full-bridge dc-dc converter with active clamp for EDLC," in *Proc. IEEE Energy Convers. Congr. Expo.*, Atlanta, GA, USA, 2010, pp. 1136–1143.

[18] K. Wang, C. Y. Lin, L. Zhu, D. Qu, F. C. Lee, and J. S. Lai, "Bi-directional DC to DC converters for fuel cell systems," in *Proc. Power Electron. Transp.*, Dearborn, MI, USA, 1998, pp. 47–51.

[19] P. U R and A. K. Rathore, "Extended range ZVS active-clamped current-fed full-bridge isolated DC/DC converter for fuel cell applications: Analysis, design, and experimental results," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2661–2672, Jul. 2013.

[20] A. K. Rathore, A. K. S. Bhat, and R. Oruganti, "Analysis, design, and experimental results of wide range ZVS active-clamped L-L type current-fed DC/DC converter for fuel cells to utility interface," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 473–485, Jan. 2012.

[21] Y. Shi, R. Li, Y. Xue, and H. Li, "Optimized operation of current-fed dual active bridge DC-DC converter for PV applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6986–6995, Nov. 2015.

[22] S. Jang, C.-Y. Won, B.-K. Lee, and J. Hur, "Fuel cell generation system with a new active clamping current-fed half-bridge converter," *IEEE Trans. Energy Convers.*, vol. 22, no. 2, pp. 332–340, Jun. 2007.

[23] T. Shimada, H. Shoji, and K. Taniguchi, "Two novel control methods expanding input-output operating range for a bi-directional isolated DC-DC converter with active clamp circuit," in *Proc. IEEE Energy Convers. Congr. Expo.*, Raleigh, NC, USA, 2012, pp. 2537–2543.

[24] T. Shimada, H. Shoji, and K. Taniguchi, "A novel scheme for a bi-directional isolated DC-DC converter with a DC-link diode using reverse recovery current," in *Proc. 16th Eur. Conf. Power Electron. Appl.*, Lappeenranta, Finland, 2014, pp. 1–7.

[25] O. Y. K. Al-Atbee and J. A. M. Bleijs, "Improved modified active clamp circuit for a current fed DC/DC power converter," in *Proc. IEEE 6th Int. Symp. Power Electron. Distrib. Gener. Syst.*, Aachen, Germany, 2015, pp. 1–7.

[26] H. Cha, J. Choi, and P. N. Enjeti, "A three-phase current-fed DC/DC converter with active clamp for low-DC renewable energy sources," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2784–2793, Nov. 2008.

[27] Y. Song *et al.*, "A current-fed three-phase half-bridge dc-dc converter with active clamping," in *Proc. IEEE Energy Convers. Congr. Expo.*, San Jose, CA, USA, 2009, pp. 1362–1366.

[28] X. Liu and H. Li, "An electrolytic-capacitor-free single-phase high-power fuel cell converter with direct double-frequency ripple current control," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 297–308, Jan./Feb. 2015.

[29] H. Cha, J. Choi, and B.-M. Han, "A new three-phase interleaved isolated boost converter with active clamp for fuel cells," in *Proc. IEEE Power Electron. Spec. Conf.*, Rhodes, Greece, 2008, pp. 1271–1276.

[30] R. L. Andersen and I. Barbi, "A three-phase current-fed push–pull DC–DC converter," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 358–368, Feb. 2009.

[31] R. L. Andersen and I. Barbi, "A ZVS-PWM three-phase current-fed push–pull DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 3, pp. 838–847, Mar. 2013.

[32] S. Lee, J. Park, and S. Choi, "A three-phase current-fed push–pull DC–DC converter with active clamp for fuel cell applications," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2266–2277, Aug. 2011.

[33] Q. Wu, Q. Wang, J. Li, and Z. Wang, "ZVS three-phase current-fed push–pull converter employing a simple active-clamp circuit for voltage step-up applications," *IET Power Electron*., vol. 11, no. 14, pp. 2286–2294, Nov. 27, 2018.

[34] F. Z. Peng, H. Li, G.-J. Su, and J. S. Lawler, "A new ZVS bidirectional DC-DC converter for fuel cell and battery application," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 54–65, Jan. 2004.

[35] H. Li, F. Z. Peng, and J. S. Lawler, "A natural ZVS medium-power bidirectional DC-DC converter with minimum number of devices," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 525–535, Mar./Apr. 2003.

[36] G. Ma, W. Qu, G. Yu, Y. Liu, N. Liang, and W. Li, "A zero-voltage-switching bidirectional DC–DC converter with state analysis and soft-switching-oriented design consideration," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2174–2184, Jun. 2009.

[37] X. Sun, X. Wu, Y. Shen, X. Li, and Z. Lu, "A current-fed isolated bidirectional DC–DC converter," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6882–6895, Sep. 2017.

[38] Z. Wang and H. Li, "A soft switching three-phase current-fed bidirectional DC-DC converter with high efficiency over a wide input voltage range," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 669–684, Feb. 2012.

[39] L. Wang, Z. Wang, and H. Li, "Asymmetrical duty cycle control and decoupled power flow design of a three-port bidirectional DC-DC converter for fuel cell vehicle application," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 891–904, Feb. 2012.

[40] L. Cao, K. H. Loo, and Y. M. Lai, "Output-impedance shaping of bidirectional DAB DC–DC converter using double-proportional-integral feedback for near-ripple-free DC bus voltage regulation in renewable energy systems," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2187–2199, Mar. 2016.

[41] H. Xiao and S. Xie, "A ZVS bidirectional DC-DC converter with phase-shift plus PWM control scheme," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 813–823, Mar. 2008.

[42] D. Sha, X. Wang, and D. Chen, "High efficiency current-fed dual active bridge DC–DC converter with ZVS achievement throughout full range of load using optimized switching patterns," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1347–1357, Feb. 2018.

[43] Z. Guo, K. Sun, T. Wu, and C. Li, "An improved modulation scheme of current-fed bidirectional DC–DC converters for loss reduction," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4441–4457, May 2018.

[44] D. Sha, X. Wang, K. Liu, and C. Chen, "A current-fed dual-active-bridge DC–DC converter using extended duty cycle control and magnetic-integrated inductors with optimized voltage mismatching control," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 462–473, Jan. 2019.

[45] J. Zhang and D. Sha, "A current-fed dual active bridge DC-DC converter using dual PWM plus double phase shifted control with equal duty cycles," in *Proc. Asian Conf. Energy Power Transp. Electrific.*, Singapore, 2016, pp. 1–6.

[46] D. Sha, D. Chen, and J. Zhang, "A bidirectional three-level DC-DC converter with reduced circulating loss and fully ZVS achievement for battery charging/discharging," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 2, pp. 993–1003, Jun. 2018.

[47] D. Sha, Y. Xu, J. Zhang, and Y. Yan, "Current-fed hybrid dual active bridge DC-DC converter for a fuel cell power conditioning system with reduced input current ripple," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6628–6638, Aug. 2017.

[48] Z. Ding, C. Yang, Z. Zhang, C. Wang, and S. Xie, "A novel soft-switching multiport bidirectional DC–DC converter for hybrid energy storage system," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1595–1609, Apr. 2014.

[49] T. Duong, M. Nguyen, Y. Lim, and J. Choi, "An active-clamped current-fed half-bridge DC-DC converter with three switches," in *Proc. Int. Power Electron. Conf.*, Niigata, Japan, 2018, pp. 982–986.

[50] D. Sha, K. Liu, X. Wang, and J. Zhang, "A current-fed DC-DC converter using two transformers with reducing current ripple and wide input range," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, San Antonio, TX, USA, 2018, pp. 2198–2202.

[51] L. Chen, L. Tarisciotti, A. Costabeber, F. Gao, P. Wheeler, and P. Zanchetta, "Advanced modulations for a current-fed isolated DC-DC converter with wide voltage operating ranges," *IEEE J. Emerg. Sel. Topics Power Electron.*, to be published, doi: 10.1109/JESTPE.2018.2870827.

[52] D. Sha, J. Zhang, X. Wang, and W. Yuan, "Dynamic response improvements of parallel-connected bidirectional DC-DC converters for electrical drive powered by low-voltage battery employing optimized feedforward control," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7783–7794, Oct. 2017.

[53] D. Sha, W. Yuan, G. Xu, F. You, and J. Chen, "Parallel-connected bidirectional current-fed dual active bridge DC-DC converters with decentralized control," in *Proc. IEEE Energy Convers. Congr. Expo.*, Milwaukee, WI, USA, 2016, pp. 1–7.

[54] S. Jalbrzykowski and T. Citko, "Current-fed resonant full-bridge boost DC/AC/DC converter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1198–1205, Mar. 2008.

[55] J. Hiltunen, V. Väisänen, and P. Silventoinen, "A bidirectional current-fed resonant push-pull converter for low voltage, high current applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, Denver, CO, USA, 2013, pp. 4770–4774.

[56] S. Jalbrzykowski, A. Bogdan, and T. Citko, "A dual full-bridge resonant class-E bidirectional DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 3879–3883, Sep. 2011.

[57] T. N. Gücin, M. Biberoğlu, and B. Fincan, "A constant-current constant-voltage charging based control and design approach for the parallel resonant converter," in *Proc. Int. Conf. Renewable Energy Res. Appl.*, Palermo, Italy, 2015, pp. 414–419.

[58] S. Samanta and A. K. Rathore, "A new current-fed CLC transmitter and LC receiver topology for inductive wireless power transfer application: Analysis, design, and experimental results," *IEEE Trans. Transp. Electrific.*, vol. 1, no. 4, pp. 357–368, Dec. 2015.

[59] X. Sun, Y. Shen, Y. Zhu, and X. Guo, "Interleaved boost-integrated LLC resonant converter with fixed-frequency PWM control for renewable energy generation applications," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4312–4326, Aug. 2015.

[60] V. R. Vakacharla and A. K. Rathore, "Current-fed isolated LCC-T resonant converter with ZCS and improved transformer utilization," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2735–2745, Apr. 2019.

[61] Y. Zhang, C. Liu, L. Sun, and Y. Zhi, "Novel individual phase current control with self-adaption unbalanced-voltage handling capability for power electronics transformer," in *Proc. IEEE PES Asia-Pacific Power Energy Eng. Conf.*, Xi'an, China, 2016, pp. 315–319.

[62] S. Samanta, A. K. Rathore, and D. J. Thrimawithana, "Bidirectional current-fed half-bridge (C)(LC)-(LC) configuration for inductive wireless power transfer system," *IEEE Trans. Ind. Appl.*, vol. 53, no. 4, pp. 4053–4062, Jul./Aug. 2017.

[63] H. Wu, K. Sun, Y. Li, and Y. Xing, "Fixed-frequency PWM-controlled bidirectional current-fed soft-switching series-resonant converter for energy storage applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6190–6201, Aug. 2017.

[64] Y. Li, Y. Xing, Y. Lu, H. Wu, and P. Xu, "Performance analysis of a current-fed bidirectional LLC resonant converter," in *Proc. 42nd Annu. Conf. IEEE Ind. Electron. Soc.*, Florence, Italy, 2016, pp. 2486–2491.

[65] Y. S. Noh, C. Y. Won, M. S. Oh, J. Y. Jeon, and Y. C. Jung, "Design and analysis of isolated bi-directional DC/DC converter using quasi-resonant ZVS," in *Proc. Int. Power Electron. Conf.*, Hiroshima, Japan, 2014, pp. 166–171.

[66] Y. Noh, S. Choi, E. Ha, B. Kim, and C. Won, "Current-fed two-inductor bi-directional DC/DC converter with wide output voltage range," in *Proc. 18th Int. Conf. Elect. Mach. Syst.*, Pattaya, Thailand, 2015, pp. 2099–2103.

[67] J.-H. Jegal, Y.-S. Noh, and C.-Y. Won, "Control method for increasing efficiency of current-fed isolated bi-directional dual half-bridge converter using resonant switch," in *Proc. IEEE Asia-Pacific Transp. Electrific. Conf. Expo*, Busan, South Korea, 2016, pp. 302–307.

[68] K. R. Sree and A. K. Rathore, "Impulse commutated zero-current switching current-fed push–pull converter: Analysis, design, and experimental results," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 363–370, Jan. 2015.

[69] K. R. Sree and A. K. Rathore, "Impulse commutated high-frequency soft-switching modular current-fed three-phase DC/DC converter for fuel cell applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6618–6627, Aug. 2017.

[70] S. K. Radha and A. K. Rathore, "Comparison and evaluation of three-phase current-fed impulse commutated ZCS DC/DC converter topologies with variable frequency modulation," in *Proc. IEEE Uttar Pradesh Section Int. Conf. Elect. Comput. Electron. Eng.*, Varanasi, India, 2016, pp. 641–646.

[71] L. Zhu, "A novel soft-commutating isolated boost full-bridge ZVS-PWM DC–DC converter for bidirectional high power applications," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 422–429, Mar. 2006.

[72] T. Reimann, S. Szeponik, G. Berger, and J. Petzoldt, "A novel control principle of bi-directional DC-DC power conversion," in *Proc. IEEE Power Electron. Spec. Conf.*, 1997, pp. 978–984.

[73] U. R. Prasanna, A. K. Rathore, and S. K. Mazumder, "Novel zero-current-switching current-fed half-bridge isolated DC/DC converter for fuel-cell-based applications," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1658–1668, Jul./Aug. 2013.

[74] A. K. Rathore and U. R. Prasanna, "Analysis, design, and experimental results of novel snubberless bidirectional naturally clamped ZCS/ZVS current-fed half-bridge DC/DC converter for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4482–4491, Oct. 2013.

[75] P. Xuewei and A. K. Rathore, "Novel bidirectional snubberless naturally commutated soft-switching current-fed full-bridge isolated DC/DC converter for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2307–2315, May 2014.

[76] S. Bal, D. B. Yelaverthi, A. K. Rathore, and D. Srinivasan, "Improved modulation strategy using dual phase shift modulation for active commutated current-fed dual active bridge," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7359–7375, Sep. 2018.

[77] S. Bal, A. K. Rathore, and D. Srinivasan, "Modular snubberless bidirectional soft-switching current-fed dual 6-pack (CFD6P) DC/DC converter," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 519–523, Feb. 2015.

[78] S. Bal, A. K. Rathore, and D. Srinivasan, "Naturally clamped snubberless soft-switching bidirectional current-fed three-phase push-pull DC/DC converter for DC microgrid application," *IEEE Trans. Ind. Appl.*, vol. 52, no. 2, pp. 1577–1587, Mar./Apr. 2016.

[79] T. F. Wu, Y. C. Chen, J. G. Yang, and C. L. Kuo, "Isolated bidirectional full-bridge DC-DC converter with a flyback snubber," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1915–1922, Jul. 2010.

[80] T. F. Wu, Y. C. Chen, J. G. Yang, Y. C. Huang, S. S. Shyu, and C. L. Lee, "1.5 kW isolated bi-directional DC-DC converter with a flyback snubber," in *Proc. Int. Conf. Power Electron. Drive Syst.*, Taipei, Taiwan, 2009, pp. 164–169.

[81] P. Sharon and S. Paul Sathiyan, "Design and simulation of bidirectional converter with flyback and capacitor diode snubbers," in *Proc. Int. Conf. Innov. Inf. Embedded Commun. Syst.*, Coimbatore, India, 2015, pp. 1–5.

[82] A. Averberg, K. R. Meyer, and A. Mertens, "Current-fed full bridge converter for fuel cell systems," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 866–872.

[83] M. Cacciato, A. Consoli, V. Crisafulli, G. Vitale, and N. Abbate, "A new resonant active clamping technique for bi-directional converters in HEVs," in *Proc. IEEE Energy Convers. Congr. Expo.*, Atlanta, GA, USA, 2010, pp. 1436–1441.

[84] G. Vitale, "DC/DC converter for HEVs and resonant active clamping technique," in *Proc. AEIT Annu. Conf.*, Mondello, Italy, 2013, pp. 1–6.

[85] H. Wang, Q. Sun, H. S. H. Chung, S. Tapuchi, and A. Ioinovici, "A ZCS current-fed full-bridge PWM converter with self-adaptable soft-switching snubber energy," *IEEE Trans. Power Electron.*, vol. 24, no. 8, pp. 1977–1991, Aug. 2009.

[86] A. Chub, R. Kosenko, A. Blinov, V. Ivakhno, V. Zamaruiev, and B. Styslo, "Full soft-switching bidirectional current-fed DC-DC converter," in *Proc. 56th Int. Sci. Conf. Power Elect. Eng. Riga Tech. Univ.*, Riga, Latvia, 2015, pp. 1–6.

[87] R. Kosenko, A. Chub, and A. Blinov, "A three-phase full soft-switching current-fed naturally clamped DC-DC converter for high-power fuel cell applications," in *Proc. 2nd Int. Conf. Intell. Energy Power Syst.*, Kiev, Ukraine, 2016, pp. 1–5.

[88] K. R. Sree and A. K. Rathore, "Hybrid modulated extended secondary universal current-fed ZVS converter for wide voltage range: Analysis, design, and experimental results," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4471–4480, Jul. 2015.

[89] S. W. Jwa, J. B. Lee, Y. Jeong, K. Kim, G. W. Moon, and J.-H. Kim, "Active clamped current-fed full-bridge integrating LLC converter with low current and voltage stress," in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf.*, Hefei, China, 2016, pp. 3211–3217.

[90] H.-J. Chiu and L.-W. Lin, "A bidirectional DC-DC converter for fuel cell electric vehicle driving system," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 950–958, Nov. 2006.

[91] Z. Zhang, Z. Ouyang, O. C. Thomsen, and M. A. E. Andersen, "Analysis and design of a bidirectional isolated DC-DC converter for fuel cells and supercapacitors hybrid system," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 848–859, Feb. 2012.

[92] R. Burkart and J. W. Kolar, "Component cost models for multi-objective optimizations of switched-mode power converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Denver, CO, USA, 2013, pp. 2139–2146.

[93] M. Leitner, *Economies of Scale in Semiconductor Manufacturing*. Munich, Germany: Grin Verlag, 2011.

[94] *Semiconductor & System Solutions—Infineon Technologies*, 2018. [Online]. Available: https://www.infineon.com

[95] *Global Leader in High Performance Ferrite—Ferroxcube*, 2018. [Online]. Available: https://www.ferroxcube.com

[96] *Micrometals Arnold Powder Cores*, 2018. [Online]. Available: https://www.micrometalsarnoldpowdercores.com

[97] *KEMET—Electronic Components*, 2018. [Online]. Available: http://www.kemet.com

[98] S. Dusmez, A. Hasanzadeh, and A. Khaligh, "Comparative analysis of bidirectional three-level DC–DC converter for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3305–3315, May 2015.

[99] D. Graovac, M. Purschel, and A. Kiep, "MOSFET power losses calculation using the data-sheet parameters," in Infineon Technol., Dresden, Germany, Jul. 2006, Appl. note.

[100] O. J. Hector, "AC resistance evaluation of foil, round and Litz conductors in magnetic components," Ph.D. dissertation, Dept. Electr. Pow. Eng., Chalmers Univ. Technol., Gothenburg, Sweden, 2013.

[101] *Micrometals Alloy Powder Cores*, 2017. [Online]. Available: https://www.micrometalsarnoldpowdercores.com/downloads/mm_2017cat_web.pdf

[102] F. Krismer, J. Biela, and J. W. Kolar, "A comparative evaluation of isolated bi-directional DC/DC converters with wide input and output voltage range," in *Proc. 14th IAS Annu. Meeting Conf. Rec. Ind. Appl. Conf.*, Kowloon, Hong Kong, vol. 1, 2005, pp. 599–606.
[103] J. Reinert, A. Brockmeyer, and R. W. A. A. De Doncker, "Calculation of losses in ferro- and ferrimagnetic materials based on the modified Steinmetz equation," *IEEE Trans. Ind. Appl.*, vol. 37, no. 4, pp. 1055–1061, Jul./Aug. 2001.
[104] R. Burkart, J. W. Kolar, and G. Griepentrog, "Comprehensive comparative evaluation of single- and multi-stage three-phase power converters for photovoltaic applications," in *Proc. Intelec*, Scottsdale, AZ, USA, 2012, pp. 1–8.
[105] R. Pittini, "High efficiency reversible fuel cell power converter," Ph.D. dissertation, Dept. Electr. Eng., Tech. Univ. Denmark, Kongens Lyngby, Denmark, 2014.
[106] M. Zhao, Z. Wang, and Y. Xue, "An overview on application analysis of power electronic technology in smart grid," in *Proc. Chin. Control Decis. Conf.*, Shenyang, China, 2018, pp. 5186–5189.
[107] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si-evaluation of potentials for performance improvement of inverter and DC–DC converter systems by SiC power semiconductors," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2872–2882, Jul. 2011.

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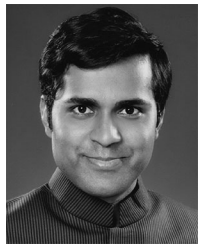

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