

An Improved Three-Phase Buck Rectifier Topology With Reduced Voltage Stress on Transistors

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Abstract—The three-phase buck rectifier (3ph-BR) is suitable for applications where a voltage step-down function is required. In this paper, an improved 3ph-BR topology is proposed to reduce the voltage stress on the transistors. The freewheeling diode in the conventional topology is split into two diodes in series and the input neutral point is connected to the common point of the two diodes. With the proposed topology and the corresponding modified modulation scheme, the transistors only need to withstand the input phase voltage instead of the line-to-line voltage, bringing about the significant reduction of voltage stress. The proposed topology enables a more cost-efficient and flexible selection of the transistors. Experimental results have verified the validity of the modified topology and associated modulation scheme.

Index Terms—Buck rectifier, voltage stress, neutral point connection, freewheeling diode.

I. INTRODUCTION

THE three-phase buck rectifier (3ph-BR), featuring wide control range of output voltage, small input filter, and intrinsic capability to limit the start-up inrush current, is suitable for applications that require a voltage step-down function from an ac source to a dc output [1]–[3]. The topology has attracted a lot of attentions for telecom power supplies and the electric vehicle chargers.

The conventional 3ph-BR topology is shown in Fig. 1, which consists of three legs and one freewheeling diode. Each leg includes two transistors (MOSFETs or IGBTs) and two diodes in series. Alternatively, one transistor and four diodes can be used in each leg, forming the topology of three-switch 3ph-BR [5]. The modulation and control technique of the 3ph-BR is well

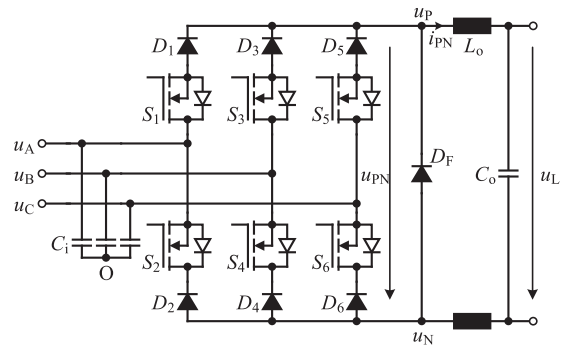


Fig. 1. Conventional topology of the 3ph-BR.

developed [1], [2], [7], [8]. In recent years, researchers have tried to improve the practical performance [4], [5], [9]–[12], especially the efficiency. For example, in [4], a 98.8% efficient 5-kW 3ph-BR was realized by paralleling devices. Accurate expressions for loss calculations are presented in [5], which are useful guidelines for hardware design. In [10], a prototype using silicon carbide (SiC) devices was designed, achieving efficiency higher than 98.5% at 7.5 kW. In [11], different device combinations were considered to improve the efficiency. In [12], a 3ph-BR topology with delta-type input connection was explored to reduce the conduction losses.

The understanding of the efficiency of the 3ph-BR is therefore good, yet less attention has been paid to the voltage stress on devices. It is generally thought that all the devices need to withstand the line-to-line input voltage [5], and the voltage rating must be selected accordingly. For a 380 V utility grid input, the maximum voltage stress is about 540 V. Considering a typical margin (around 50%), voltage rating of devices must be at least 900 V or higher. This leads to a problem of device selection. Silicon (Si) MOSFETs have good performance but their voltage ratings are usually less than 650 V (except the CoolMos [13]). IGBTs can easily achieve higher voltage rating (upwards of 1200 V), but their switching performance is poor and devices cannot be paralleled to improve efficiency. SiC MOSFETs can reach a higher voltage rating with superior switching performance, but they are still expensive compared with the comparable Si devices. This makes the conventional topology less attractive compared with its competitor: the newly developed SWISS rectifier (SR) [14]–[17]. SR could also achieve voltage step-down function, and the devices also withstand the input-to-line voltages.

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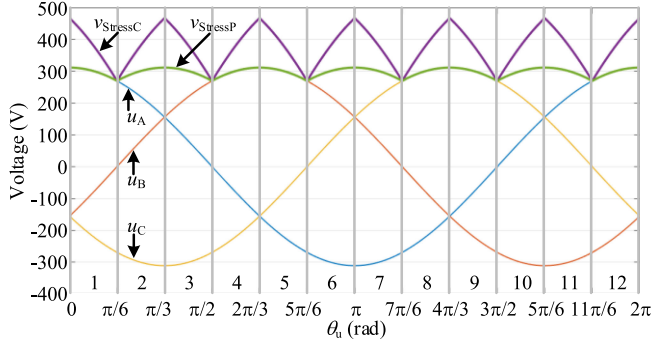


Fig. 2. Sector division of three-phase input voltages (u_A , u_B , and u_C) and the maximum voltage stress on transistors in each sector. $v_{StressC}$ and $v_{StressP}$ are for the conventional topology and the proposed topology, respectively.

However, the switching frequency of the most devices in SR is the input fundamental frequency. Therefore, it is easier and more cost efficient for SR to achieve extremely high efficiency.

In this paper, a circuit improvement is proposed to reduce the voltage stress on transistors in the conventional 3ph-BR topology. The modification splits the freewheeling diode into two diodes in series and connects the input neutral point to the common point of the two diodes. The modulation scheme is modified accordingly, which turns OFF all the transistors at the freewheeling stage. With the proposed topology and its modulation scheme, the transistors only need to withstand the input phase voltage instead of the line-to-line voltage. For the 380 V input applications, the ideal voltage stress on transistors is only 311 V. Transistors of 600 V (e.g., Si MOSFETs) are, therefore, sufficient for the proposed topology, enabling a more cost efficient and flexible selection of devices. Besides, the control performance remains the same under the unity input power factor.

The rest of this paper is organized as follows. Section II reviews the conventional 3ph-BR topology and presents the voltage stress analysis. Section III introduces the principle of the proposed topology. Section IV presents some discussions. Experimental verification is provided in Section V and the conclusion is drawn in Section VI.

II. CONVENTIONAL 3ph-BR TOPOLOGY

A. Modulation Scheme

Several modulation schemes have been developed for the 3ph-BR topology. Among them, the optimized one presented in [7] guarantees minimum switching loss, input and output ripples, and thus is adopted by this paper. In this scheme, the three-phase input voltages are divided into 12 sectors subject to the voltage profile, as shown in Fig. 2. According to the topology symmetry, the following analysis is based on the assumption that input voltages fall into sector 1. For other sectors, the analysis can be carried out similarly.

In sector 1, the three-phase input voltages are in the sequence of $u_A > 0 > u_B > u_C$ and their absolute values are in the sequence of $|u_A| > |u_C| > |u_B|$. Therefore, the duty cycles for

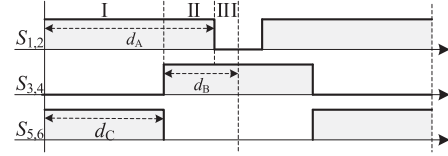


Fig. 3. Switching pattern of the conventional 3ph-BR topology in sector 1.

TABLE I
VOLTAGE STRESS ANALYSIS FOR THE CONVENTIONAL TOPOLOGY IN SECTOR I

	Stage I	Stage II	Stage III
u_P	u_A	u_A	u_B
u_N	u_C	u_B	u_B
v_{S1}	0	0	$u_A - u_B$
v_{S2}	0	0	0
v_{S3}	0	0	0
v_{S4}	0	0	0
v_{S5}	0	0	0
v_{S6}	0	$u_B - u_C$	$u_B - u_C$
v_{D1}	0	0	0
v_{D2}	$u_A - u_C$	$u_A - u_B$	$u_A - u_B$
v_{D3}	$u_A - u_B$	$u_A - u_B$	0
v_{D4}	$u_B - u_C$	0	0
v_{D5}	$u_A - u_C$	$u_A - u_C$	$u_B - u_C$
v_{D6}	0	0	0
v_{DF}	$u_A - u_C$	$u_A - u_B$	0

the three legs are calculated as [7]

$$d_A = K_d |u_A|, \quad d_C = K_d |u_C|, \quad d_B = 1 - d_C \quad (1)$$

where K_d is expressed as

$$K_d = u_L^* / (u_A^2 + u_B^2 + u_C^2) \quad (2)$$

where u_L^* is the reference value of the dc load voltage.

After the duty cycles are obtained, the gate signals can be applied to the transistors according to the switching pattern, as shown in Fig. 3. The two transistors in each leg share the same gate signals for simplifying the drive logic without affecting the control performance.

B. Voltage Stress Analysis

As shown in Fig. 3, the switching pattern is divided into three stages (I, II, and III). At each stage, voltage stresses for devices are illustrated in Table I, where v_{Si} and v_{Di} ($i = 1, 2, \dots, 6$) represent the voltage stresses on the transistors and the diodes of each input phase leg, respectively, and v_{DF} represents the voltage stress on the freewheeling diode. Voltages u_P and u_N on the upper and lower dc buses, which are referenced to the neutral point O of the input filter capacitors, are also listed in Table I to assist the analysis.

Considering the conduction characteristic of all the diodes (including the body diodes of the transistors), the voltage stress analysis is based on the following rules.

- 1) If $u_x > u_P$ ($x = A, B$, and C), the corresponding transistor on the *upper* arm withstands the voltage stress $u_x - u_P$ while the diode withstands the zero-voltage stress. Otherwise, the diode withstands the voltage stress

$u_P - u_x$ and the transistor withstands the zero-voltage stress.

- 2) If $u_x < u_N$ ($x = A, B,$ and C), the corresponding transistor on the lower arm withstands the voltage stress $u_N - u_x$ while the diode withstands the zero-voltage stress. Otherwise, the diode withstands the voltage stress $u_x - u_N$ and the transistor withstands the zero-voltage stress.
- 3) The freewheeling diode always with stands the output voltage u_{PN} , which is equal to $u_P - u_N$.

At stage I: According to Fig. 3, transistors $S_1, S_2, S_5,$ and S_6 are in ON-state but only S_1 and S_6 conduct the output current i_{PN} because $u_A > u_C$. The upper bus voltage u_P is equal to u_A while the lower bus voltage u_N is equal to u_C . According to the analysis rules, no transistors at this stage withstand the voltage stress because of the input voltage sequence $u_A > 0 > u_B > u_C$. Voltage stresses are withstood by the diodes.

At stage II: Similarly, S_1 and S_4 conduct the output current, so u_P is equal to u_A and u_N is equal to u_B . S_6 withstands the voltage stress $u_B - u_C$, which is the minimum value of the absolute line-to-line input voltages. Other transistors still do not withstand the voltage stress.

At stage III: Output current flows through the freewheeling diode D_F . However, because S_3 and S_4 are still in ON-state, the bus is clamped to the input phase B. Therefore, u_P and u_N are both equal to u_B . Transistor S_1 withstands the voltage stress $u_A - u_B$, which is the middle value of the absolute line-to-line input voltages. S_6 still withstands the voltage stress $u_B - u_C$ while other transistors withstand the zero-voltage stress.

It can be seen from Table I that diodes can withstand the maximum line-to-line input voltage. However, transistors only need to withstand the middle value of the absolute line-to-line input voltages, which happens at the freewheeling stage. The maximum voltage stress $v_{StressC}$ on the transistors of the conventional topology in each sector is plotted in Fig. 2. For the general 380 V input, the maximum value of $v_{StressC}$ is about 466 V, less than the amplitude 537 V of the input line-to-line voltages. Nevertheless, this is only true for the optimized switching pattern shown in Fig. 3. If the input phase with minimum voltage (e.g., phase C in sector I) is clamped to the dc bus at stage III, the maximum value of $v_{StressC}$ will be 537 V. That means if the wrong gate signals are applied to transistors or gate signals are missing, they could still withstand the maximum input line-to-line voltage. Therefore, for reliability, the voltage rating of switching devices should be selected based on the amplitude of input line-to-line voltage plus additional margin, considering the worst case. For the 380 V input, 900 or 1200 V transistors are applicable but not those under 650 V.

III. PROPOSED 3ph-BR TOPOLOGY

To reduce the voltage stress on transistors, an improved topology is proposed, as shown in Fig. 4. Compared with the conventional topology, the modification is simple, as only the freewheeling diode is split into two diodes (D_{F1} and D_{F2}) in series and the neutral point O of input filter capacitors is connected to the common point of D_{F1} and D_{F2} .

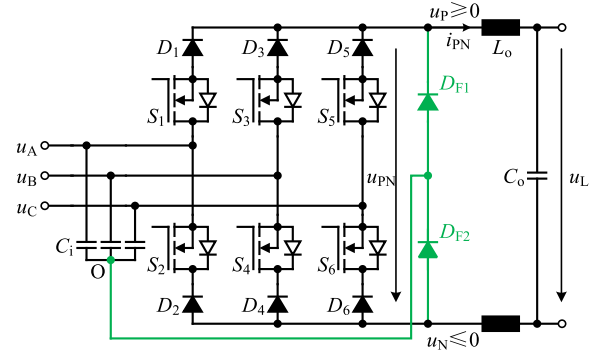


Fig. 4. Proposed topology of the 3ph-BR.

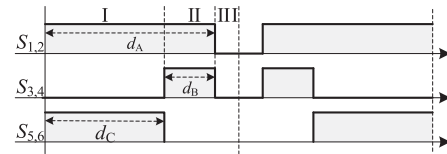


Fig. 5. Switching pattern of the proposed 3ph-BR topology in sector I.

The principle of the proposed topology to reduce the voltage stress on transistors is quite straightforward. According to Fig. 4, the voltage u_P at bus P referenced to point O must be positive, and u_N at bus N must be negative. Therefore, according to the analysis rules 1) and 2) presented in Section II-B, the voltage stress on each transistor must be less than the absolute value of phase voltage. It means that the reduction of the voltage stress is guaranteed by the circuit itself and is not affected by the modulation scheme.

To generate sinusoidal input current and constant output voltage, the proposed topology needs to adopt the modified switching pattern, as shown in Fig. 5, which differs from the conventional topology at the freewheeling stage where all the transistors are turned OFF. The duty cycles for each phase are

$$d_A = K_d |u_A|, \quad d_C = K_d |u_C|, \quad d_B = K_d |u_B|. \quad (3)$$

It can be seen from (1) and (3) that the duty cycle for phase B is changed.

The detailed voltage stress on each device is listed in Table II, where the differences with Table I have been highlighted in bold and green. Comparing Tables I and II, it can be found as follows.

- 1) At stages I and II, voltage stresses on transistors and their serial diodes remain the same. The voltage stress on the freewheeling diode in the conventional topology is distributed on the two diodes in the proposed topology, but the total voltage stress does not change. Each freewheeling diode withstands the voltage stress no larger than the phase voltage.
- 2) At stage II, the voltage stress on S_6 is $u_B - u_C$, which is less than u_A according to the input voltage profile in sector I.
- 3) At stage III, the voltage stress distribution is quite different. For the proposed topology, each leg has one transistor

TABLE II
VOLTAGE STRESS ANALYSIS FOR THE PROPOSED TOPOLOGY IN SECTOR I

	Stage I	Stage II	Stage III
u_P	u_A	u_A	0
u_N	u_C	u_B	0
v_{S1}	0	0	u_A
v_{S2}	0	0	0
v_{S3}	0	0	0
v_{S4}	0	0	$-u_B$
v_{S5}	0	0	0
v_{S6}	0	$u_B - u_C$	$-u_C$
v_{D1}	0	0	0
v_{D2}	$u_A - u_C$	$u_A - u_B$	u_A
v_{D3}	$u_A - u_B$	$u_A - u_B$	$-u_B$
v_{D4}	$u_B - u_C$	0	0
v_{D5}	$u_A - u_C$	$u_A - u_C$	$-u_C$
v_{D6}	0	0	0
v_{DF1}	u_A	u_A	0
v_{DF2}	$-u_C$	$-u_B$	0

and diode withstanding the corresponding input phase voltage. No line-to-line voltage is withstood by any device. In particular, v_{S1} and v_{D2} withstand the voltage stress u_A , which is the maximum input phase voltage.

To sum up, the transistors of the proposed topology only need to withstand the input phase voltage instead of the line-to-line voltage. The maximum voltage stress $v_{StressP}$ on transistors in each sector is also plotted in Fig. 2. For the general 380 V input, the maximum value of $v_{StressP}$ is only the amplitude of phase voltage, which is 311 V and thus is much smaller than $v_{StressP}$. More importantly, there are much more types of low-cost high-performance transistors (e.g., 600 V MOSFETs) that can thereby be selected to construct the hardware.

It can also be found from Tables I and II that the proposed topology does not change the output voltage u_{PN} , which is equal to $u_P - u_N$, and thus the control performance is not affected. Besides, the only function of the additional connection is to clamp the voltage on each transistor to less than the input phase voltage and there is no current D flowing through it to the input filter capacitors. Therefore, no common-mode component will be imposed on the input voltages. Voltages on the input filter capacitors are exactly the same with the conventional topology and are also not affected by the additional connection. For both the conventional and proposed topologies, the input filter capacitors should be selected according to the rated power of the converter so that the voltage ripple on the capacitors would not affect the voltage stress significantly. Anyhow, the proposed topology always reduces the voltage stress on transistors to the input phase voltage, which is the major benefit the additional connection brings.

It should be noted herein that a similar topology, designated as the four-pole rectifier as shown in Fig. 6, was proposed two decades ago [18]. The same version with thyristors was even earlier. In this topology, the neutral point of input filter capacitors is connected to the fourth leg composed of the controlled transistors and diodes. The primary goal of this topology is to reduce the input current harmonics and the output voltage ripple with the multilevel modulation scheme. Although the proposed

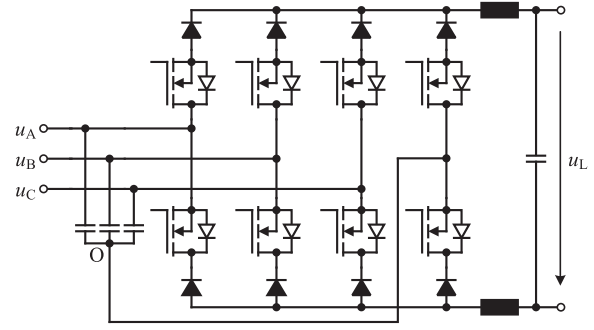


Fig. 6. Topology of the three-phase four-pole buck rectifier [18].

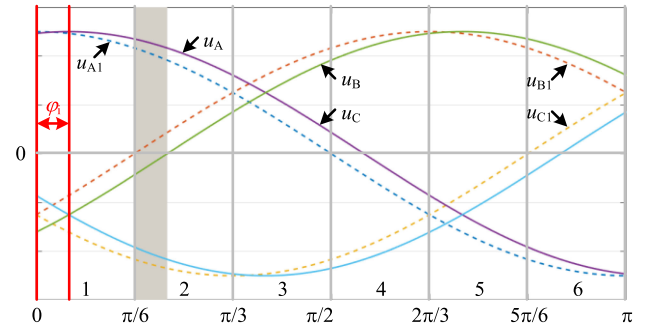


Fig. 7. Modulation signals (u_{A1} , u_{B1} , and u_{C1}) with a displacement angle φ_i . The shadowed part in sector 2 shows the area that the proposed topology loses control.

modulation scheme can also be applied to this topology so as to reduce the voltage stress on transistors, selection of the transistor voltage rating still has to be based on the input line-to-line voltages instead of phase voltages in case of missing gate signals of the fourth leg. On the contrary, the voltage stress reduction in the proposed topology is guaranteed by the hardware connection, not affected by the modulation scheme. In addition, the primary goal of splitting freewheeling diodes is to reduce the voltage stress, not to realize the multilevel operation although it does have the capability.

IV. DISCUSSIONS

A. Influence on the Input Displacement Angle

For a 3ph-BR, the input filter capacitors consume some reactive power, degrading the input power factor. In some cases, the 3ph-BR may need to compensate such reactive power. For traditional topology, this goal can be realized by applying new modulation signals (u_{A1} , u_{B1} , and u_{C1}) with a displacement angle φ_i referenced to the input voltages (u_A , u_B , and u_C), as shown in Fig. 7.

However, this goal cannot be realized by the proposed topology. As shown in Fig. 4, the voltages u_P and u_N on the upper and lower buses of the proposed topology must be positive and negative, respectively, due to the connection of the freewheeling diodes. As a result, the proposed topology must impose positive phase voltages on the upper bus and negative phase voltages on the lower bus. If the new modulation signals are applied to

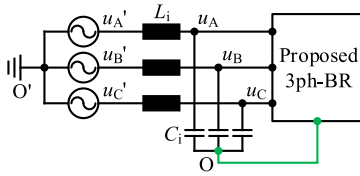


Fig. 8. Connection of the practical supply and the proposed 3ph-BR.

the proposed topology, the converter cannot behave as expected in some phase angle range. For the example shown in Fig. 7, when the phase angle of the new modulation signals falls into the shadowed area in sector 2, the topology will try to impose negative voltage u_B on the upper bus. However, the actual device conducting the dc bus current on the upper bus will be D_{F1} , instead of the expected transistor S_{BP} . Consequently, distortions will present in the input current of phase B . The width of this area is just equal to the displacement angle φ_i .

Therefore, the proposed topology and the modulation scheme can only generate the high-quality input and output currents under zero-input displacement angle. However, this drawback is minor as the displacement angle is always set to zero in practice. According to the study of Prof. Kolar's group from ETH [1], the dc output voltage of the buck rectifier satisfies

$$U_{PN} \leq \sqrt{\frac{3}{2}} U_{N,LL,rms} \cos(\varphi_i) \quad (4)$$

where U_{PN} is the average dc output voltage and $U_{N,LL,rms}$ is the rms value of the input line-to-line voltages. It shows that the maximum voltage utilization ratio of the converter is proportional to the cosine of the displacement angle. To obtain a wide control range of the output voltage, the input displacement angle has to be limited to small values [1]. Actually, the input displacement angle is always set to zero in practice, which is true for both the conventional and proposed topologies. Therefore, the aforementioned drawback is acceptable, especially considering its advantage of reducing the voltage stresses on transistors significantly. In this case, the actual input power factor is not exactly unity resulting from the reactive power consumed by the filter but would be quite close to unity (usually larger than 0.99) as the input filter should be always selected appropriately according to the rated power.

It should be noted that, the additional displacement angle only affects the power quality but not the maximum voltage stress on transistors. It can be seen from Section III that the maximum voltage stress on transistors will not exceed the amplitude of input voltages, which is determined by the hardware connection of the devices and is not affected by any modulation scheme.

B. Performance Under Disturbed Input Voltages

In practice, the three-phase input voltages may be distorted and/or unbalanced due to the nonlinear and unbalanced load in the power grid. The practical connection of the input supply and the proposed 3ph-BR topology is shown in Fig. 8, where u'_A , u'_B , and u'_C are the real supply voltages and O' is their neutral point. In this case, the three-phase voltages u_A , u_B , and u_C on

the input filter capacitor referenced to their neutral point O are not equal to the supply voltages, satisfying

$$\begin{cases} u_A = u'_A - u_{OO'} \\ u_B = u'_B - u_{OO'} \\ u_C = u'_C - u_{OO'} \end{cases} \quad (5)$$

where $u_{OO'}$ is the voltage on the point O referenced to the supply neutral point O' . $u_{OO'}$ represents the common-mode component in the three-phase input voltages

$$u_{OO'} = (u'_A + u'_B + u'_C) / 3. \quad (6)$$

With the substitution of (2) into (3), the actual output voltage u_{PN} on the dc bus when u_A , u_B , and u_C fall into sector I is expressed as follows:

$$u_{PN} = u_P - u_N = d_A u_A - (d_B u_B + d_C u_C) = u_L^*. \quad (7)$$

Therefore, with the proposed modulation scheme, the actual output voltage is always equal to its reference, regardless of the common-mode component or the disturbances of distortions and unbalance in the actual supply voltages. This can also be found from the comparison between the two topologies. The output voltages at three stages of the switching pattern are all the same in the two topologies. It is well acknowledged that the conventional 3ph-BR topology with the appropriate modulation scheme has the immunity to input disturbances. Therefore, the proposed topology also has this capability.

According to the presentation in Section III, the transistors only need to withstand the phase voltages u_A , u_B , and u_C on the filter capacitors rather than the actual supply voltages u'_A , u'_B , and u'_C . This means that the common-mode voltage $u_{OO'}$ does not influence the voltages stresses on devices and thus is omitted in this paper. The distortions and unbalance in input voltages increase the instantaneous value of the capacitor voltages and further increase the voltage stress, which should be considered in the selection of devices, just the same with the conventional topology. Nevertheless, 600 V transistors are still able to tolerate up to 29% increase from the general 380 V ($L-L$ rms) input voltages, with 50% additional margin.

C. Conduction and Switching Losses

1) *Conduction Loss*: It is clear from the proposed topology that the conduction loss is increased since two diodes are on the current path at the freewheeling stage. However, the impact is slight as the conduction loss of the freewheeling diodes usually accounts for a small part of the total losses [5], if the voltage utilization ratio is high. Moreover, the freewheeling diodes only need to withstand the input phase voltages instead of the line-to-line voltages, as illustrated in Table II. Therefore, for the general 380 V input applications, the conventional topology needs to adopt the 1200 V freewheeling diode while the proposed topology only needs to adopt 600 V freewheeling diodes. Moreover, it is possible to use the low-cost MOSFETs in parallel to replace the freewheeling diodes so as to reduce the conduction loss.

TABLE III
TRANSITION FROM STAGE II TO STAGE III IN SECTOR I

Devices	Conventional Topology		Proposed Topology	
	$\bar{v}i$	Δv	$\bar{v}i$	Δv
S_1	$(u_A - u_B)i_{PN}$	$u_A - u_B$	$u_A i_{PN}$	u_A
S_4	0	0	$-u_B i_{PN}$	$-u_B$
S_6	0	0	0	$-u_B$
D_2	0	0	0	$-u_B$
D_3	0	$u_A - u_B$	0	u_A
D_5	0	$u_A - u_B$	0	u_A
D_F	$(u_A - u_B)i_{PN}$	$u_A - u_B$	---	---
D_{F1}	---	---	$u_A i_{PN}$	u_A
D_{F2}	---	---	$-u_B i_{PN}$	$-u_B$
Total	$2(u_A - u_B)i_{PN}$	$4(u_A - u_B)$	$2(u_A - u_B)i_{PN}$	$4(u_A - u_B)$

2) *Switching Loss*: As shown in Fig. 5, the proposed topology with the associated modulation scheme requires more switching actions during the transition from stage II to stage III. However, the total switching loss is actually decreased, benefiting from the reduction of voltage stress.

According to the work presented in [19], the switching loss p_{sw} for one device is mainly composed of two parts. The first part is caused by the crossover of the voltage stress and the current stress. The second part is the loss caused by charging and discharging the output capacitance. Generally, p_{sw} can be expressed as

$$p_{sw} = k_1 \bar{v}i + k_2 (\Delta v)^2 \quad (8)$$

where \bar{v} and i are the average voltage stress and conducted current during the transition; Δv is the absolute change of the voltage stresses between two states.

By comparing Tables I and II, it can be found that the voltage stress and the conducted current during the transition from stage I to stage II are all the same for the topologies, but are different during the transition from stage II to stage III. The differences are listed in Table III. At stage II, the devices S_1 , D_1 , S_4 , and D_4 conduct current. At stage III, the freewheeling diodes conduct current. Therefore, only these devices generate the cross-over switching loss. It can be seen from Table III that the two topologies generate the same total of $\bar{v}i$. As a result, for the first part in (8), the two topologies are the same. It can also be seen that the sum of Δv is the same for the two topologies. However, as the second part in (8) is proportional to the square of Δv , the proposed topology generates smaller loss related to this part, according to the Cauchy-Schwarz inequality. In addition, it can also be known that the switching loss distribution in the proposed topology is more balanced since more devices share the switching loss.

To sum up, the conduction loss in the proposed topology is slightly increased, but it is compromised by the decreased switching loss if the same devices are adopted. However, the proposed topology enables the adoption of the low-cost high-performance devices so as to reduce both the conduction and switching losses. Therefore, it is easier and more cost efficient to achieve higher efficiency, especially for applications requiring high switching frequency.

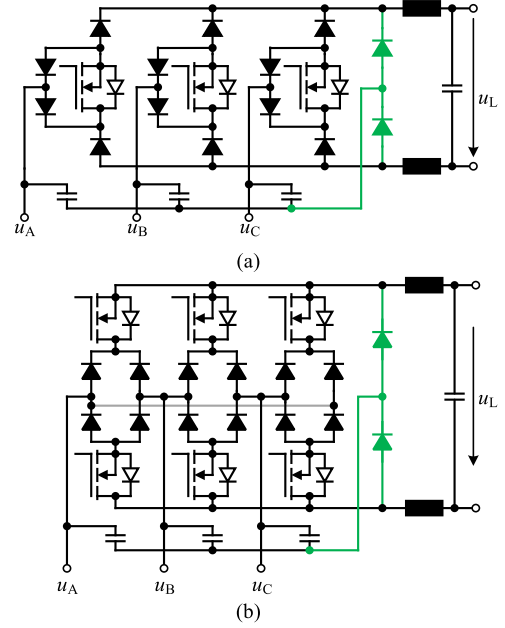


Fig. 9. Extensions of the proposed improvement to other three-phase buck topologies. (a) Improved three-switch 3ph-BR topology. (b) Improved 3ph-BR topology with delta input connection.

D. Extension to Other 3ph-BR Topologies

The proposed modification can be easily extended to the three-switch 3ph-BR topology and the one with delta input connection presented in [12]. The improved topologies are shown in Fig. 9, of which the freewheeling diode is split into two diodes in series and the neutral point of input filter capacitors is connected to the common point of the two diodes. The modulation scheme needs to be modified accordingly. With the modification, transistors in these topologies also withstand the input phase voltages instead of the line-to-line voltages, reducing the voltage stress significantly. Transistors of 600 V are also sufficient for these improved topologies to work under the general 380 V input.

The topologies discussed in this paper are all unidirectional. If bidirectional power flow is required, the diodes in these topologies can be replaced with transistors with the same voltage rating, while the proposed improvement is still applicable to the transistors on the forward current path.

V. EXPERIMENTAL VERIFICATION

A. Experimental Prototype

In order to verify the effectiveness of the proposed topology, a prototype is constructed, which is presented in Fig. 10. The prototype parameters are listed in Table IV. In particular, the transistors used are MOSFETs with the rated voltage of 600 V. The two freewheeling diodes are also rated at 600 V. As all the devices have high switching performance, the sampling frequency is set 60 kHz, and thus a small input filter is adequate to attenuate the high-frequency harmonics. A passive resistor of 41.6 Ω serves as the load.

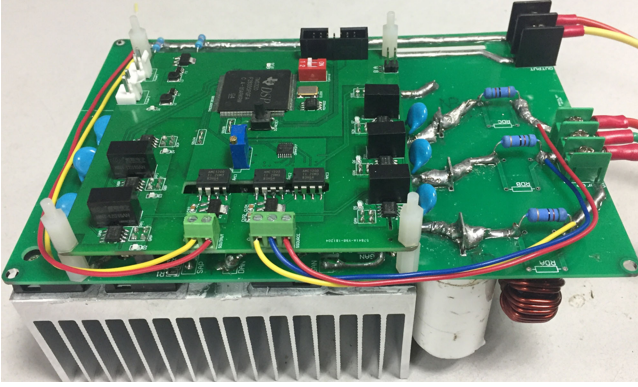


Fig. 10. Experimental prototype of the proposed 3ph-BR.

TABLE IV
PROTOTYPE PARAMETERS

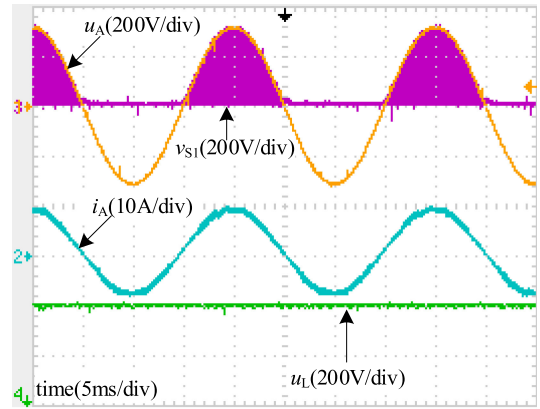
Term	Specification
Diodes D_i	On Semi, RHRG30120, 1200V, 30A
MOSFETs S_i	Rohm, R6030ENZ1C9, 600V, 130m Ω
Diodes D_{F1}, D_{F2}	Vishay, VS-EPU3006-N3, 600V, 30A
Sampling Frequency f_s	60 kHz
Input Filter Inductor L_i	100 μ H
Input Filter Capacitor C_i	5 μ F
Filter Damping Resistor R_d	51 Ω
Output Filter Inductor L_o	330 μ H
Output Filter Capacitor C_o	100 μ F
Load Resistor R_L	41.6 Ω

B. Case I: Comparison With Conventional Topology

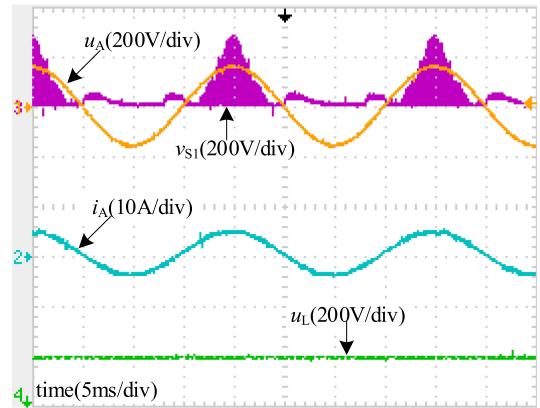
The proposed topology is first evaluated under the sinusoidal and balanced input voltages of 380 V/50 Hz (line-to-line rms). The output voltage reference is 400 V. The experimental result is shown in Fig. 11(a), which proves that the proposed topology can obtain sinusoidal input current and constant output voltage. The waveform of the voltage stress v_{S1} on the transistor S_1 shows that it only needs to withstand the input phase voltage instead of the line-to-line voltage. Even if the nonideal switching behavior of power devices increases the voltage stress a bit, no voltage stress on S_1 larger than 450 V is observed in experiments. Therefore, 600 V transistors are sufficient for the proposed topology to work reliably under the general 380 V/50 Hz input.

On the same prototype, the conventional topology is also evaluated comparatively. In this case, the input neutral point is disconnected from the freewheeling diodes. For safety issue, three-phase input voltages are reduced by half to 190 V and the output voltage reference is reduced to 200 V accordingly. The experimental result is shown in Fig. 11(b). It is found that the maximum value of voltage stress on the transistor S_1 is about 290 V. It can be deduced that the voltage stress will increase to over 580 V with 380 V input. Therefore, 900 V or 1200 V transistors are necessary for the conventional topology with 380 V input and 600 V ones are not applicable.

The efficiencies of the two topologies under different input voltages and output voltages are shown in Fig. 12. For fair comparison, the efficiencies are first measured under 190 V input voltage. It can be seen that the efficiencies of the two topologies



(a)



(b)

Fig. 11. Experimental results in Case I. (a) With the proposed topology, three-phase input voltages are 380 V (line-to-line rms) and output voltage is 400 V. (b) With the conventional topology, input voltages are reduced to 190 V and output voltage is 200 V for safety of the prototype. u_A and i_A are the voltage and current of input phase A, respectively. u_L is the load voltage. v_{S1} is the measured voltage stress on the transistor S_1 .

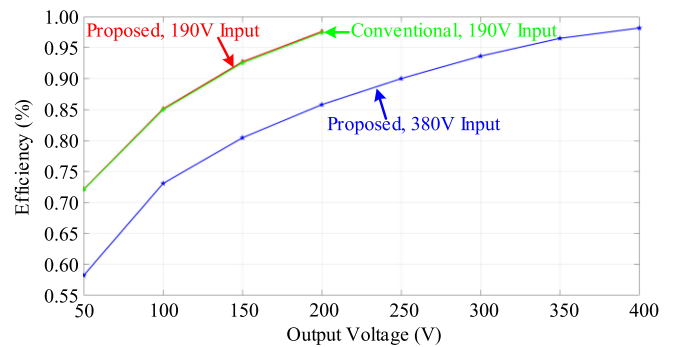


Fig. 12. Efficiency comparison for the conventional and proposed topologies.

are quite close in this case. For the proposed topology working under 380 V input, the converter efficiency is improved when the output voltage increases. The maximum efficiency is about 98.1%. It should be noted that the primary goal of this prototype is to verify the principle of the proposed topology. The converter efficiency can further be improved by the optimized design with high-performance devices.

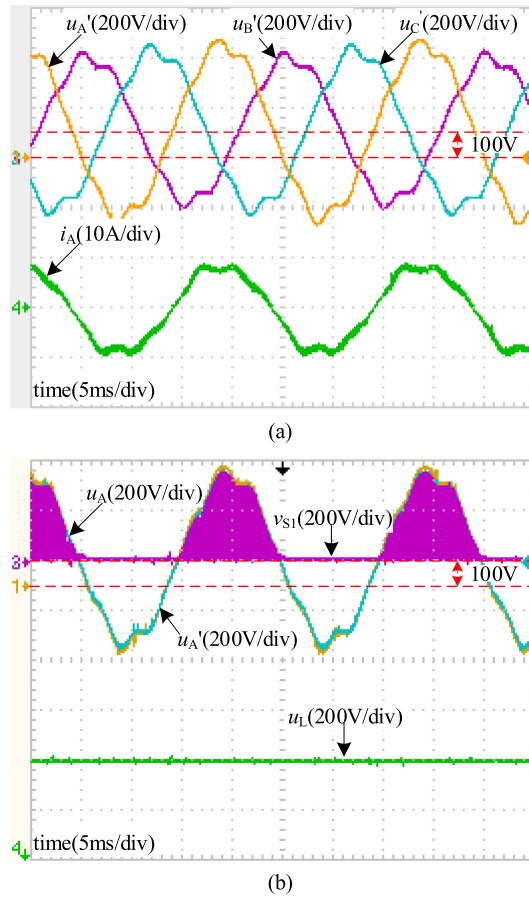


Fig. 13. Experimental results in Case II. (a) Three-phase supply voltages u'_A , u'_B , and u'_C , and the input current i_A . (b) Source voltage u'_A , input capacitor voltage u_A , voltage stress v_{S1} on the transistor S_1 , and the load voltage u_L .

C. Case II: Performance Under Disturbed Supply Voltages

In this case, the proposed topology is evaluated under input voltage disturbances. The three-phase supply voltages are set unbalanced, of which the rms values are 240, 220, and 200 V, respectively. Each phase voltage contains 5% 5th and 5% 7th harmonics. In addition, the common-mode voltage of 100 V is injected to the supply voltages. The waveforms of the three-phase supply voltages are shown in Fig. 13(a). It can be found that the supply voltages are highly disturbed with the large dc bias.

Although the voltage disturbance causes distorted input current as presented in Fig. 13(a), the load voltage remains constant, as shown in Fig. 13(b). Besides, the transistor only needs to withstand the phase voltage on the input filter capacitor, rather than the real supply phase voltage. The common-mode voltage does not affect the voltage stress. Although the voltage distortions and unbalance increase the instantaneous amplitude of the input phase voltages, the adopted 600 V devices could still work reliably in this case.

Figs. 11, 12, and 13 under various working conditions also prove that the prototype works safely without being damaged by any overvoltage transient. Therefore, the additional connection is sufficiently robust to reduce the voltage stress on transistors.

VI. CONCLUSION

It was widely taken for granted that the voltage rating of all the devices in the 3ph-BR should be selected based on the amplitude of input line-to-line voltages. This makes the conventional topology less competitive than other solutions in terms of performance and cost. As demonstrated in this paper, the transistors only need to withstand the input phase voltage, only if the hardware connection is modified slightly. Transistors of 600 V, instead of 900 or 1200 V ones required by conventional topology, are sufficient for the proposed topology to work under the general 380 V (line-to-line rms voltage) input with almost 100% safety margin. Therefore, the proposed topology is a very competitive solution to other topologies.

To generate high-quality input and output power, the proposed topology needs to adopt the modified modulation scheme. A drawback of the proposed topology with this scheme is that it has to work under zero-input displacement angle, otherwise the input currents may be distorted. Nevertheless, such drawback is minor, as zero-input displacement angle is the common operation mode of the 3ph-BR.

In the future, the paralleling low-cost MOSFETs to explore the extreme efficiency of the proposed topology will be an interesting topic.

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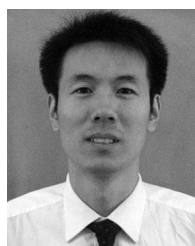
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