A Hybrid Control of a Semidual-Active-Bridge DC–DC Converter With Minimum Current Stress

Ming Lu, Xiaodong Li, *Senior Member, IEEE*, and Guo Chen

***Abstract*—With the conventional secondary phase-shifted (PS) control, a semidual-active-bridge (S-DAB) dc–dc converter suffers from low efficiency at light load in buck mode due to hard switching and high tank current. In order to avoid this phenomenon and extend soft-switching range, a hybrid control including the primary pulsewidth modulation plus secondary phase-shifted (PWM+PS) is proposed in this paper. Under the proposed hybrid control, all steady-state operation modes with distinctive features are identified and analyzed. Based on the operation range, power characteristics and switching behaviors in each mode, a minimum peak current control route is developed, which can enable the converter to work with low tank current and soft switching over the whole load range. A lab-scale S-DAB converter is implemented to validate the theoretical analysis, and experimental results reveal that the higher efficiency can be achieved using the proposed control route.**

***Index Terms*—Phase-shifted (PS) control, pulsewidth modulation (PWM), semidual-active-bridge (S-DAB).**

I. Introduction

PROPOSED two decades ago, the high-frequency (HF) isolated dual-active-bridge (DAB) converter is widely used in bidirectional dc–dc applications such as electric vehicles and renewable energy applications due to high power density, high efficiency, and easy control [1]–[3]. With the single phase-shift between two active bridges as the sole control variable, a DAB converter can keep wide zero-voltage switching (ZVS) range only at unity converter gain and suffers from high circulating current at light load. Therefore, many advanced control strategies for DAB converters are then developed to extend the ZVS range, eliminate circulating current, and depress switch stress. All of them are based on the manipulation of the three phase-shift angles among the four switch legs and the switching frequency [4]–[13].

By using diodes to replace some secondary-side switches in a DAB converter, a semidual-active-bridge (S-DAB) dc–dc converter can be formed [14]–[18]. While saving a few active switches and their driver circuits, it still retains the capability of interbridge phase-shift control through the remaining switches for unidirectional dc–dc applications. It was recommended for medium to high output voltage applications, such as the dc–dc stage of photovoltaic generation [14], [15], [18]. When compared with the conventional phase-shifted full-bridge converter, it has a wider ZVS range and is free of voltage spike of secondary diodes. The type I of semiactive bridge has one active switch leg and one passive diode leg on the secondary side [14]–[16]. The type II of semiactive bridge has two identical hybrid legs, each of which includes one high-side diode and low-side switch [17]–[19]. It is proved that the two types of secondary semiactive bridges show almost same characteristics of power transfer and switching behavior except for the current rating of secondary switches/diode due to different conduction duration [20]. Naturally the S-DAB converter retains many characteristics of a DAB converter, such as buck–boost operation and wide ZVS range. Adopting the conventional secondary phase-shifted (PS) control, the different operation modes with its characteristic in power transfer and soft switching of an S-DAB converter with the first type of semiactive bridge are investigated in detail in [14]. Practical evaluations on the regulations of output power and voltage as well as the effects of various load conditions on the converter efficiencies are discussed in [15]. A modified S-DAB converter is proposed in [16], with a three-phase secondary semiactive bridge including two diode legs and one switch leg. It employs two HF transformers in a primary-series and secondary-parallel configuration to achieve low output voltage ripple and reduced inductor voltage. The work presented in [18] focuses on the steady-state analysis of the main power transfer mode and the comparisons with DAB converter in terms of the ZVS range and output current. The small-signal model of the S-DAB converter is also presented. Targeting at applications with high input voltage, an S-DAB converter with the primary bridge implemented in the three-level structure is explored for high efficiency, low primary switch voltage stress, and wide voltage gain conversion in [17]. To interface both battery storage system and photovoltaic panel, a three-port S-DAB converter with both voltage-feed and current-feed inputs is explored in [19], in which the primary duty cycle is also adopted for voltage regulation. With the series *LC* resonant tank, the resonant-type S-DAB converter is also investigated for distinctive operation modes in [21].

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Despite the different arrangement of the primary-side circuit, all voltage-fed S-DAB converters in the literature have either the first type or second type of semiactive bridge. With the PS control, they would share three main operation modes including two continuous-current modes (CCMs) and one discontinuous-current mode (DCM). At heavy load, the converter works in one CCM with ZVS regardless of the converter gain. Working in boost operation, the converter would enter into the DCM at light load, in which the primary switch can be turned ON/OFF at zero current and secondary switches work with ZVS [14]. However, another CCM, which exists at buck operation with light load only, has two undesired features: hard switching of the secondary switches and high circulation current. As a result, both switching loss and conduction loss will be high and the overall conversion efficiency is degraded. Thus, the particular CCM restricts the wide load range operation of the S-DAB converter, which only attracted limited attentions in previous studies. The work presented in [14] suggested that the magnetizing current and a long-enough dead time of gating signal are helpful to keep ZVS. It was just mentioned in [16] that the secondary-side switching loss in this mode might not be very high due to small turn-OFF current without giving any solution. An improved boundary operation is discussed in [22] for the ZVS achievement and nonactive power reduction. It adopted the type II structure on the secondary side with total three phase-shift angles as control variables. The design for boundary mode compensation is complicated and the control will not be effective at light load. In [23], a multimode control is proposed to improve the light load performance of an S-DAB converter. It adopts three control variables including the conventional secondary PS, the variable switching frequency, and the primary pulsewidth modulation (PWM), and apply one or two of them in three different stages of load level. However, it becomes quite complicated and costly for implementation. Conclusively, in order to achieve full load range operation of an S-DAB converter, it is still meaningful to find solutions to totally avoid the particular CCM in buck operation with undesired characteristics and improve the light load performance. In this paper, the primary PWM control will be combined with the secondary PS control to form a hybrid PWM+PS control strategy for an S-DAB converter. Under such a hybrid control strategy, a specified control route with minimum peak current (MPC) is then developed, along which the S-DAB converter can achieve full soft-switching operation in the whole load range with high efficiency.

This paper is organized as follows. In Section II, a comprehensive steady-state analysis of S-DAB converter with the PWM+PS control in buck operation is presented, which gives the power transfer characteristics and switching behaviors in each operation modes. With the obtained features, a modulation strategy is then developed in Section III, which enables the S-DAB converter to work with full soft-switching and minimal current stress in the whole load range. In Section IV, a series of experiments are performed on a lab prototype S-DAB converter to illustrate the correctness and feasibility of the theoretical analysis. And the final conclusion is drawn in Section V.

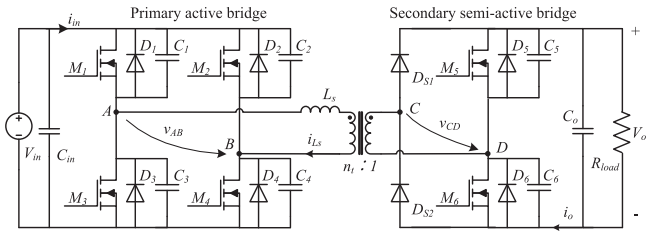

Fig. 1. Typical configuration of an S-DAB dc–dc converter.

II. Steady-State Analysis of an S-DAB Converter With PWM+PS Control

An S-DAB converter is consisted of one active H-bridge and one semiactive H-bridge, as shown in Fig. 1. The semiactive H-bridge has one diode leg and one switch leg. The HF transformer with a turn ratio of $n_t : 1$ not only provides galvanic isolation, but also matches voltage level. The magnetic inductance of the transformer is assumed to be infinity and the leakage inductance would be used as the part of the power transfer inductor L_s. The filter capacitor C_o is assumed to be large enough to keep output voltage almost ripple free.

In this paper, all active switches are operated at 50% duty cycle with a fixed switching frequency f_s. The two switches in each switch leg are turned ON/OFF complementarily. The outer phase shift ϕ is defined as the phase delay between the turn-ON moment of M_1 and that of M_6. And the inner phase shift α is defined as the phase delay between the turn-ON moment of M_1 and that of M_4, which is used to modulate the pulsewidth of the primary HF voltage v_{AB}. While ϕ is the sole control variable under secondary PS control, both α and ϕ will be used to manipulate power under the proposed hybrid PWM+PS control.

Under the hybrid control, an S-DAB converter has five different steady-state operation modes for buck operation ($M < 1$), where the converter voltage gain is defined as $M = n_t V_o / V_{\text{in}}$. The five modes can be categorized into two groups: three CCM A, B, and C as shown in Fig. 2 and two DCMs D and E as shown in Fig. 3. In any mode, there are eight distinctive time intervals in one switching period, in which the ON/OFF state of switches and the polarities of voltages/currents are different.

A. CCM: Modes A, B, and C

As shown in Fig. 2(a), the feature of Mode A can be described as: $\phi > \beta > \alpha > 0$, and the phase angle β is defined as the time delay from the turn-ON moment of M_1 to the zero-crossing point of i_{Ls} in the first half period. The equivalent circuits of the first four time intervals of Mode A are given in Fig. 4. It is assumed that one HF period starts at the positive rising edge of v_{AB}.

Interval I [θ_o, θ_1] [see Fig. 4(a)]: At the beginning of this interval, M_2 is turned OFF forcibly and the negative inductor current is forced to flow through D_4. Then, M_4 can be turned ON with zero voltage. On the secondary side, M_5 and D_{s2} are conducting, i.e., $v_{CD} = -V_o$. Thus, the energy stored in the inductor is transmitted to the load and the input dc source. During this interval, the inductor voltage is maintained at $(V_{\text{in}} + n_t V_o)$, and i_{Ls} increases linearly according to (1) until it reaches zero

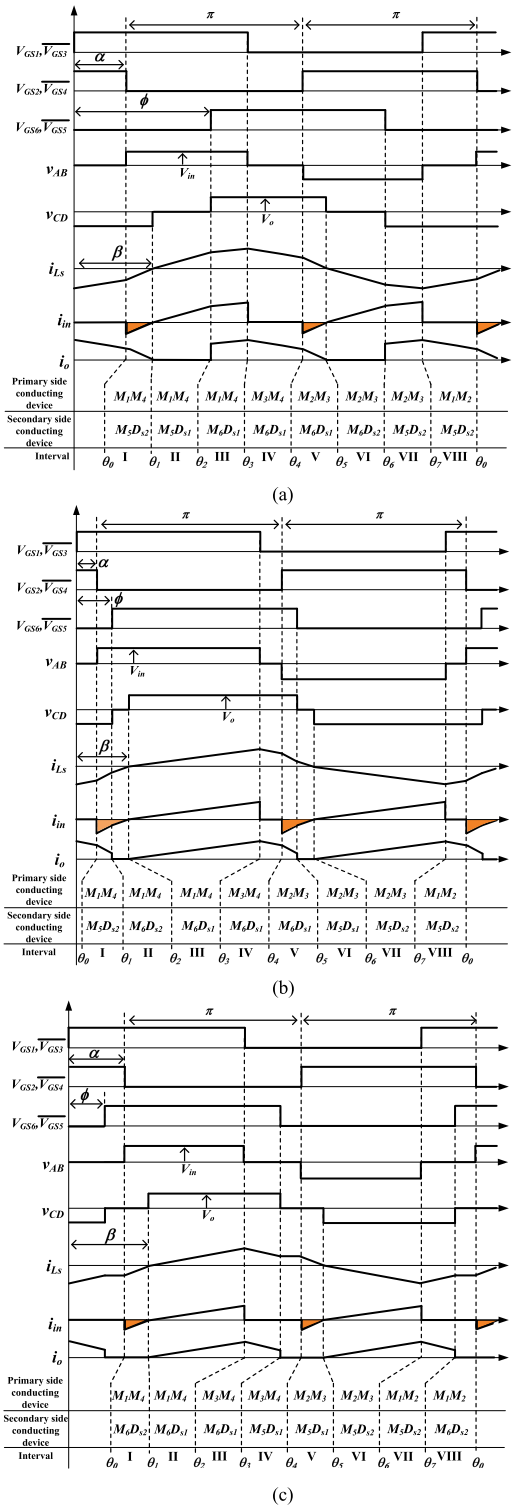

Fig. 2. Steady-state waveforms of three CCMs. (a) Mode A. (b) Mode B. (c) Mode C.

at $\theta = \theta_1$ as follows:

$$i_{Ls}(\theta) = i_{Ls}(\theta_o) + \frac{V_{\text{in}} + n_t V_o}{\omega_s Ls}(\theta - \theta_o) \tag{1}$$

$$i_{Ls}(\theta_1) = i_{Ls}(\beta - \alpha) = 0 \tag{2}$$

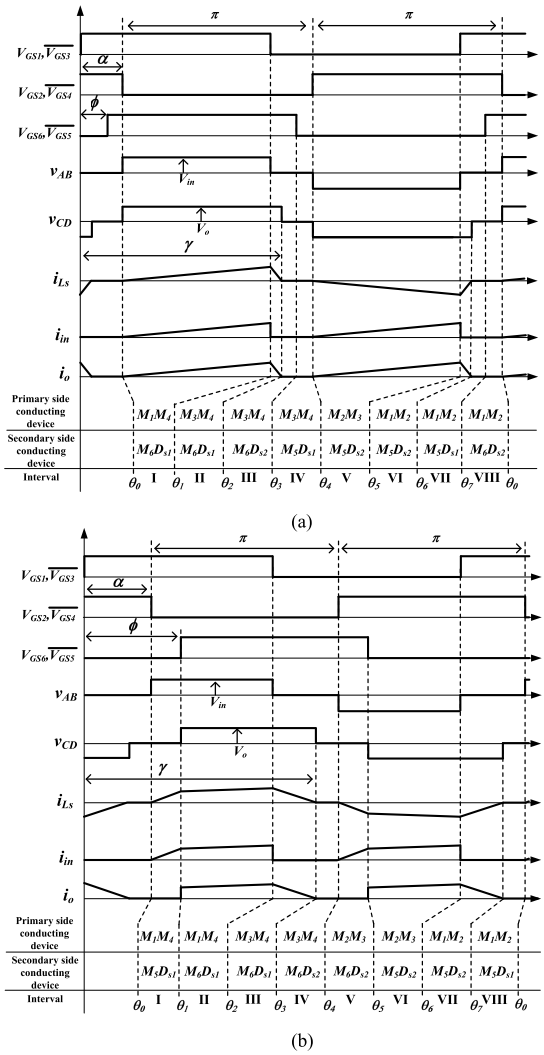

Fig. 3. Steady-state waveforms of two DCMs. (a) Mode D. (b) Mode E.

where ω_s is the switching frequency in radian/second.

Interval II [θ_1, θ_2] [see Fig. 4(b)]: When the polarity of i_{Ls} is changed at θ_1, D_{s2} is turned OFF and D_{s1} is turned ON, both with zero current. Since M_5 is still conducting, the secondary side is shorted and the power is being stored in L_s. Because the inductor voltage is kept at V_{in}, i_{Ls} increases linearly according to (3) in this interval as

$$i_{Ls}(\theta) = i_{Ls}(\theta_1) + \frac{V_{\text{in}}}{\omega_s Ls}(\theta - \theta_1). \tag{3}$$

Interval III [θ_2, θ_3] [see Fig. 4(c)]: At θ_2, M_5 is turned OFF and the secondary current is shifted to D_6, so that M_6 can be turned ON with zero voltage. Thus, the conducting devices on the secondary side are D_{s1} and M_6, i.e., $v_{CD} = V_o$. During this interval, the power is transmitted to the inductor and the load. As the inductor voltage is clamped at $(V_{\text{in}} - n_t V_o)$, i_{Ls} continues to increase linearly according to (4) until it arrives at its maximum as follows:

$$i_{Ls}(\theta) = i_{Ls}(\theta_2) + \frac{V_{\text{in}} - n_t V_o}{\omega_s Ls}(\theta - \theta_2). \tag{4}$$

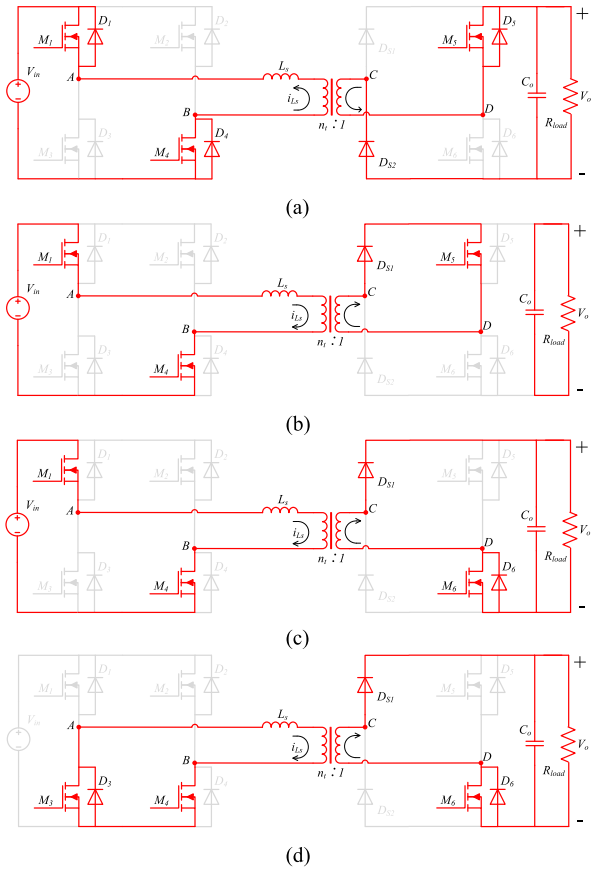

Fig. 4. Equivalent circuits of different intervals in Mode A.

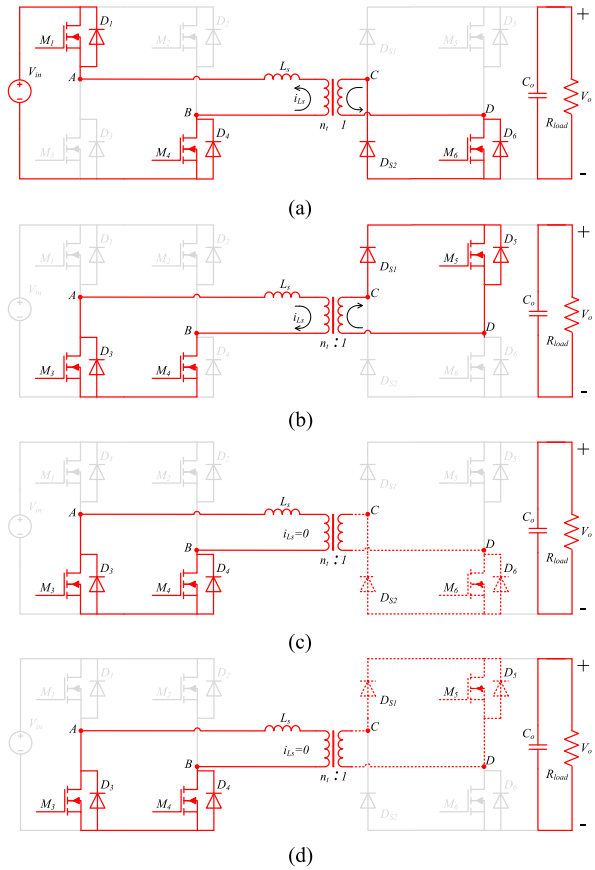

Fig. 5. Equivalent circuits of distinctive intervals in Modes B, C, D, and E.

Interval IV [θ_3, θ_4] [see Fig. 4(d)]: At θ_3, M_1 is turned OFF. The positive inductor current is shifted to D_3, so that M_3 can be turned ON with zero voltage later. The conducting devices on the secondary side are unchanged. Thus, the voltage across inductor is clamped at $-n_t V_o$. During this interval, i_{Ls} starts to decline linearly in terms of (5). At the end of interval IV or the half of a period, i_{Ls} is same as the initial value at θ_o with opposite polarity, and is given by

$$i_{Ls}(\theta) = i_{Ls}(\theta_3) + \frac{-n_t V_o}{\omega_s Ls}(\theta - \theta_3) \tag{5}$$

$$i_{Ls}(\theta_4) = -i_{Ls}(\theta_o). \tag{6}$$

Since the next four intervals in the second half period are same as the first four intervals, except for the directions of voltage/current and involved conducting devices, the analysis detail can be understood easily with the help of Fig. 2. By using the half-wave symmetric characteristics, the instantaneous values of i_{Ls} and the zero-crossing phase angle β can be found by using (1)–(5).

During one HF period, the power is pumped back to the dc source only in interval I and V [the dark shaded area in Fig. 2(a)], which is defined as nonactive power and results in extra unnecessary losses. The nonactive power P_{non} can be evaluated as

$$P_{\text{non}} = \frac{V_{\text{in}}}{\pi} \int_{\theta_0}^{\theta_1} |i_{Ls}(\theta)|\, d\theta. \tag{7}$$

As shown in Fig. 2(b), Mode B is featured with $\beta > \phi > \alpha > 0$. Starting from the positive rising edge of v_{AB} similarly, the first four time intervals in Mode B differs from those in Mode A only at the second interval, whose equivalent circuit is given in Fig. 5(a). This interval begins with the transition from M_5 to M_6 with a negative inductor current, which indicates a hard-switched turn ON for M_6. The inductor voltage is V_{in} and the negative inductor current will increase linearly until zero as in (3). In Mode B, the nonactive power exists in interval I, II,V, and VI.

The steady-state waveforms of Mode C are presented in Fig. 2(c) with $\beta > \alpha > \phi > 0$. Starting from the turn OFF of M_2, the first three time intervals in Mode C are exactly same as the second to the fourth one in Mode B, while the fourth interval of Mode C is unique, whose equivalent circuit is given in Fig. 5(b). This interval begins with the commutation from M_6 to M_5 with a positive inductor current, which indicates a hard-switched turn ON for M_5. The inductor voltage is zero since both sides are short circuited. Therefore, the positive inductor current remains constant until the end of the half period. In Mode C, the nonactive power shows in interval I and V.

In Table I, the calculated characteristics for each CCM including the current phase angle β, average output power, and nonactive power are listed. For the purpose of simplicity, all values have been normalized by the following base values:

$$V_B = V_{\text{in}}, I_B = \frac{V_{\text{in}}}{\omega_s L_s}, P_B = V_B I_B = \frac{V_{\text{in}}^2}{\omega_s L_s}. \tag{8}$$

TABLE I
ELECTRICAL CHARACTERISTICS IN CCM

Mode	β	$P_{o,pu}$	$P_{non,pu}$
A ($\phi > \beta > \alpha$)	$\frac{\pi+\alpha-\pi M+\phi M}{2+M}$	$\frac{M\left(X_1+X_2+4\pi\phi M^2-2\pi\alpha M^2-2\pi^2M^2\right)}{2\pi(2+M)^2}$	$\frac{-M-1}{\pi}\int_{\theta_0}^{\theta_1}\left[\theta+\frac{(\alpha-\pi+\alpha M-\phi M+\pi M)}{M+2}\right]d\theta$
B ($\beta > \phi > \alpha$)	$\frac{\pi+\alpha-\pi M-\phi M}{2-M}$	$\frac{M(X_1-X_2)}{2\pi(2-M)^2}$	$\frac{1}{\pi}\int_{\theta_0}^{\theta_1}\left[\frac{2\phi-\alpha+\pi}{M-2}+\pi+(\phi-\alpha-\theta)(1+M)\right]d\theta$ $+\frac{1}{\pi}\int_{\theta_1}^{\theta_2}\left[\frac{2\phi-\alpha+\pi}{M-2}+\pi+\phi-\alpha-\theta\right]d\theta$
C ($\beta > \alpha > \phi$)	$\frac{\pi+\alpha-\pi M-\phi M}{2-M}$	$\frac{M(X_1-X_2)}{2\pi(2-M)^2}+\frac{M(\alpha-\phi)^2}{2\pi}$	$\frac{1}{\pi}\int_{\theta_0}^{\theta_1}\left(\frac{\alpha-\pi-\alpha M+\phi M+\pi M}{M-2}-\theta\right)d\theta$

Note: $X_1=2\alpha\phi M^2+4\alpha\phi+4\pi\phi+\pi^2-\alpha^2M^2-2\phi^2M^2-3\alpha^2-2\pi\alpha-4\phi^2,\ X_2=4\alpha\phi M+\pi^2M+4\pi\phi M-3\alpha^2M-2\pi\alpha M-4\phi^2M.$

TABLE II
ELECTRICAL CHARACTERISTICS IN DCM

Mode	γ	$P_{o,pu}$	$P_{non,pu}$
D ($\gamma > \alpha > \phi$)	$\frac{\pi-\alpha+\alpha M}{M}$	$\frac{2\pi\alpha M-\alpha^2M+X_3}{2\pi}$	0
E ($\gamma > \phi > \alpha$)	$\frac{\pi-\alpha+\phi M}{M}$	$\frac{2\pi\phi M-\phi^2M+X_3}{2\pi}$	0

Note: $X_3=(\alpha-\pi)^2-\pi^2M.$

TABLE III
SWITCHING BEHAVIOR IN FIVE STEADY-STATE MODES

Mode	M_1,M_3	M_2,M_4	M_5,M_6	D_{S1},D_{S2}
A	ZVS	ZVS	ZVS	ZCS
B	ZVS	ZVS	hard switching	ZCS
C	ZVS	ZVS	hard switching	ZCS
D	ZVS	ZCS	ZCS	ZCS
E	ZVS	ZCS	ZVS	ZCS

B. DCM: Modes D and E

In DCM, there is at least one time interval in each half period, in which the inductor current i_{Ls} remains zero. In Fig. 3(a) and (b), the phase angle γ is defined as the time delay from the turn-ON moment of M_1 to the next positive falling edge of v_{CD}.

As shown in Fig. 3(a), the relationship among the three phase angles in Mode D is $\gamma > \alpha > \phi > 0$. The last two intervals (III and IV) in the first half period starting from the positive rising edge of v_{AB} are all zero-current intervals. Although both sides of the inductor are shorted in those two intervals, they do have different equivalent circuits as shown in Fig. 5(c) and (d), respectively. At the end of Interval III, M_6 is turned OFF, so that the short-circuit route is changed to D_{s2} and M_5. Fig. 5(d) looks exactly same as Fig. 5(b), except that the inductor current is zero in Fig. 5(d) .

As shown in Fig. 3(b), Mode E is featured with $\gamma > \phi > \alpha > 0$. Different from Mode D, there is only one zero-current interval in each half period in Mode E, which is same as the one in Fig. 5(c).

By making use of the zero current features in (9), the instant current values and transferred power in DCM can be evaluated easily

$$i_{Ls}(\theta_0)=0;\ i_{Ls}(\gamma-\alpha)=0. \tag{9}$$

The calculated characteristics for each DCM including the current phase angle γ, average output power, and nonactive power are normalized and concluded in Table II. It is noted that all these characteristics in Mode D can only be determined by α and are independent of ϕ.

C. Switching Behavior

In each mode, the two diodes on the secondary-side H-bridge are always turned ON/OFF at zero current, which is free from reverse recovery. However, the switching behaviors of all active switches vary with the operation modes. According to the polarity of switch current at switching moment, the switching behaviors of all switches in each mode are concluded in Table III. It is seen that Mode A has lowest switching losses due to full ZVS operation of all switches. Because of the existence of zero-current interval, some switches are operated with zero-current switching (ZCS) and the others can work with ZVS in Modes D and E. Generally Modes B and C should be avoided since the secondary-side switches work at hard switching, which will bring up more switching loss and electromagnetic interference problem.

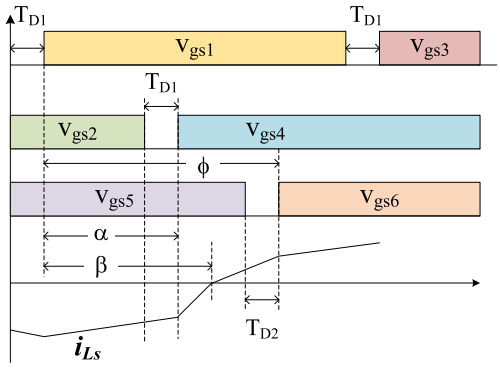

Fig. 6. Effect of dead time on the ZVS commutation of all switches.

The soft-switching conditions mentioned above are theoretically derived by the assumption of a zero dead time of gating signals. In practice, a certain amount of dead time exists, during which the switch parasitic capacitor has to be charged or discharged to complete the commutation process. Fig. 6 shows the switching transient state of the active switches under the ZVS operation. It can be seen that the commutation of switches (M_1, M_3) in the leading leg is easy to achieve since the inductor current is at its maximum, so a small dead time might be enough. When $\alpha < \beta$ is maintained, the switches (M_2, M_4)

in the lagging leg can operate at ZVS too, if T_{D1} is longer than the required commutation period. On the secondary side, the difference $\phi - \beta$ should be large enough to provide an adjustable range for T_{D2}, which should be long enough for commutation process. Conclusively, a long dead time is helpful to keep ZVS for the S-DAB converter. However, it should not be too large otherwise the effective voltage duty cycle will decrease and more circulation current will be generated.

D. Operation Range and Power Characteristic

Through the abovementioned analysis, the power range in each mode and the boundary between those modes can be identified, which is helpful for the development of control strategy based on the proposed hybrid control method.

Also existing under the conventional secondary PS control, Modes A and B have the boundary condition between them at $\beta = \phi$, which leads to the relationship between α and ϕ as

$$\alpha = 2\phi + (M-1)\pi. \tag{10}$$

In Mode A, β tends to decrease with the increase of α. When $\beta = \alpha$, the converter enters into Mode E with $\gamma = \pi + \alpha$. And the critical condition can be solved as

$$\alpha = \frac{M}{1+M}\phi + \frac{1-M}{1+M}\pi. \tag{11}$$

In the operation range of $\alpha > \phi$, the converter may operate in either Modes C or D. The feature of the boundary mode between Modes C and D is that the duration of interval I of Mode C shrinks to zero and the inductor current declines to zero, i.e., $\beta = \alpha, \gamma = \pi + \phi$. Thus, the relationship between ϕ and α at the boundary condition can be expressed as

$$\alpha = \pi - \frac{M}{1-M}\phi. \tag{12}$$

Sharing the common feature of $\beta \le \phi$, Modes B and C has the boundary condition indicated as

$$\alpha = \phi \le \pi(1-M). \tag{13}$$

Similarly, the boundary condition between Modes D and E can be expressed as

$$\alpha = \phi \ge \pi(1-M). \tag{14}$$

Based on these boundary conditions, the ranges of each mode on the $\alpha - \phi$ plane at $M = 0.6$ are shown in Fig. 7. The zero power is indicated by $\alpha = \pi$, below which is the effective power region. The boundary conditions between every two neighboring modes are plotted by the dashed lines, and those boundary lines intersect at the point O_1 ($\alpha = \phi = \pi(1-M)$). The power contours with the same P_A value are plotted by the solid curves for the values of P_A changing from 0.2 to 1 with a step of 0.2. P_A is defined as the normalized percentage load: $P_A = P_{o,pu}/P_{oM,pu}$ and $P_{oM,pu} = \frac{\pi\left(M^2+M\right)}{2(M^2+2M+2)}$. When P_A is equal to 1, the contour shrinks into the point O_2 ($\phi = \frac{1+M+M^2}{M^2+2M+2}\pi$, $\alpha = 0$), representing the maximum load capacity of an S-DAB converter under the hybrid control. Under the conventional PS control, only ϕ can be varied to adjust the output power, whose range is just along the ϕ-axis.

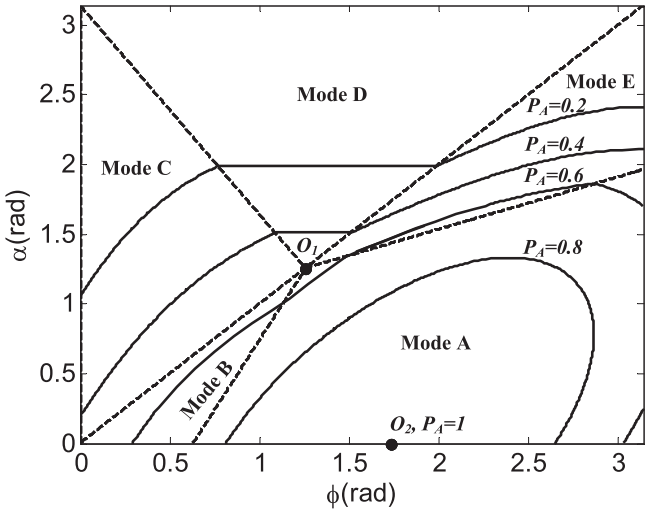

Fig. 7. Operating range of each mode and the normalized power contours with regards to α and ϕ at $M = 0.6$.

TABLE IV
PEAK INDUCTOR CURRENT AND POWER RANGE IN EACH MODE

Mode	$I_{peak,pu}$	P_A
A	$\pi + (\pi-\phi)(1-M) - \frac{\alpha-2\phi+3\pi}{2+M}$	$P_A \in \left[\frac{M^3+2M^2+2M}{M^3+3M^2+3M+1}, 1\right]$
B	$\frac{(1-M)(\pi-\alpha+\phi M)}{2-M}$	$P_A \in \left[\frac{2-M^3-M^2}{M^3-3M^2+4}, \frac{2-M^3-M^2}{2}\right]$
C	$\frac{(1-M)(\pi-\alpha+\phi M)}{2-M}$	$P_A \in \left[0, \frac{2-M^3-M^2}{M^3-2M^2+3}\right]$
D	$\pi - \alpha + \alpha M - \pi M$	$P_A \in \left[0, \frac{2M-M^3-M^4}{M+1}\right]$
E	$\pi - \alpha + \phi M - \pi M$	$P_A \in \left[0, \frac{M^3+2M^2+2M}{M^3+2M^2+2M+1}\right]$

III. MPC CONTROL ROUTE

With the introduction of one more control variable α in the proposed hybrid control, the average output power is a function of two variables now. Therefore, a specified control route needs to be developed to manipulate the power. In this paper, the peak current I_{peak} of the inductor L_s is selected as the optimization objective to find a reasonable control route, since I_{peak} has a significant effect on the life span of switches, conduction loss, and system stability [8], [12], [13]. With the steady-state analysis results, the peak current and the power range in each mode can be calculated and concluded in Table IV. As an example, the variation of I_{peak} with regard to ϕ under different power levels is shown in Fig. 8. It can be seen that for a fixed power level, the peak current is a convex function of ϕ, which has a global minimum. At heavy load, the minimum is located in Mode A, and the minimum becomes a flat line located in Mode D at light load.

By using the Lagrangian multiplier method, the objective function to find the MPC route in each mode can be written as

$$L(\phi, \alpha, \lambda) = I_{\text{peak},pu}(\phi, \alpha) + \lambda\left[P_A(\phi, \alpha) - P_A^*\right] \tag{15}$$

where λ is the Lagrangian multiplier and P_A^* is the specified power. By letting the partial derivatives of L with regard to ϕ, α, and λ be zero, the local MPC routes in each mode with the same P_A^* and M can be obtained. Through comparing the local

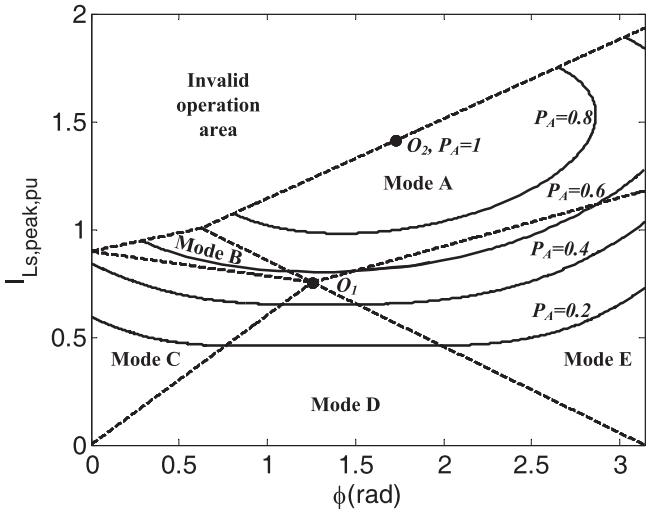

Fig. 8. Variation of peak inductor current under different load level with regards to ϕ at $M = 0.6$.

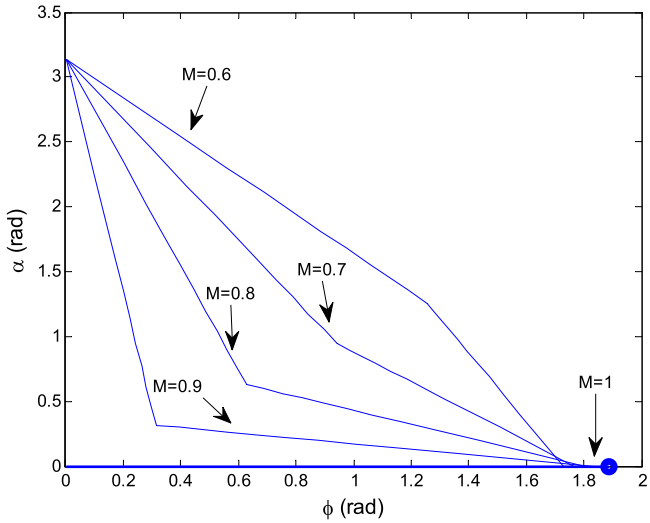

Fig. 9. Proposed MPC route under different converter gains.

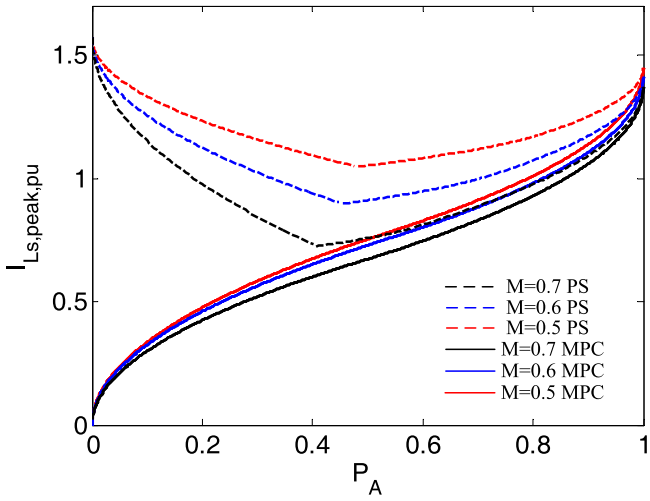

Fig. 10. Variation of peak inductor current with regards to load level under the MPC route and the secondary PS control.

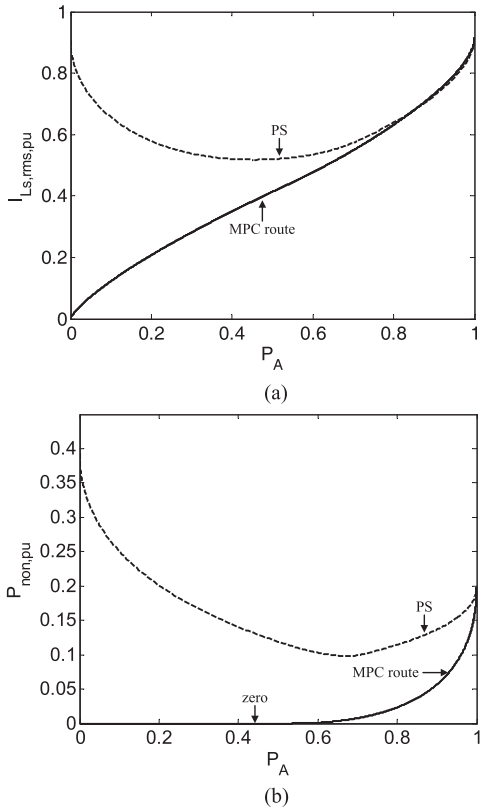

Fig. 11. (a) Variation of rms inductor current with regards to load level under the MPC route and the secondary PS control. (b) Variation of nonactive power with regards to load level under the MPC route and the secondary PS control.

MPC route of five modes, the global MPC route from full power to zero power can be obtained then.

Thus, the closed-form solution across the whole power range with the global MPC is given as follows, which is named as MPC control route.

Stage 1: $P_A \in \left[\frac{2M-M^3-M^4}{M+1}, 1\right]$

$$\begin{cases} \alpha = \dfrac{\pi(1-M)\sqrt{(1-P_A)(M^5+2M^4+M^3-M^2+1)}}{M^4+M^3-M+1} \\ \phi = \dfrac{\pi+\alpha-\alpha M-2\alpha M^2-\alpha M^3-\pi M^3}{2-M^3-M^2} \end{cases} \tag{16}$$

Stage 2: $P_A \in \left[0, \frac{2M-M^3-M^4}{M+1}\right]$

$$\begin{cases} \alpha = \pi - \sqrt{\dfrac{\pi^2 M P_A(1+M)}{2-M^3-M^2}} \\ \phi = \dfrac{(1-M)(\pi-\alpha)}{M}. \end{cases} \tag{17}$$

In stage 1, the converter works in Mode A only with full ZVS operation. In stage 2, the converter is supposed to work in Mode D only. Since both the peak current and the power are dependent on α solely in Mode D, the route can be anywhere in Mode D. In this paper, the boundary of Modes C and D will be selected as the route at low power, which can avoid the voltage

TABLE V
COMPARISONS OF THE PROPOSED MPC WITH PREVIOUS WORKS

	Proposed MPC	S-DAB in [22]	S-DAB in [14]	S-DAB in [23]	S-DAB in [16]
Voltage Gain	$n_t V_o/V_{in}$	$n_t V_o/V_{in}$	$n_t V_o/V_{in}$	$n_t V_o/V_{in}$	$2n_t V_o/V_{in}$
Phase-shift Angles	2	3	1	2	1
Switching Frequency	fixed	fixed	fixed	variable	fixed
Secondary Structure	type I	type II	type I	type II	type I + 1 diode leg
Transformer	1	1	1	1	2
Soft-switching	yes	yes	not at light load	not at light load	not at light load
Efficiency	high	high	low at light load	high	low at light load
Control Complexity	medium	high	low	high	low

ringing of v_{CD} during the zero-current interval and keep $P_{\text{non}} = 0$. The proposed MPC routes at different converter gains are illustrated in Fig. 9, in which the two sections in each route are all linear functions. When $M = 1$, there is no need for two-stage control and the conventional PS control is used with $\alpha = 0$. The converter works in Mode A only from full load ($\phi = 0.6\pi$) to zero load ($\phi = 0$), i.e., its control route is along the x-axis.

A comparison of $I_{\text{peak},pu}$ along the proposed MPC route and under the PS control is given in Fig. 10. It can be seen clearly that $I_{\text{peak},pu}$ along the MPC route decreases with the reduction of power level across the whole power range for different M. Also, the peak current under the MPC route is always lower than that under the PS control for the same power level. In order to illustrate the advantages of the proposed route, more comparisons between the PS control and MPC control route under $M = 0.6$ are carried out and presented in Fig. 11. Compared with the PS control, the rms inductor current at lower power levels is reduced effectively. Meanwhile, the nonactive power across the whole power range is also depressed significantly, which indicates that the converter under the MPC route can achieve lower conduction loss.

In Table V, the comparison of the proposed MPC with the previous works are summarized. In general, the proposed MPC extends the soft-switching range and reduces the circulation current effectively for the whole load range at medium cost. Although solutions given in [22] and [23] are also effective for soft-switching improvement and efficiency enhancement, both of them demand high efforts for design and costly implementation with three control dimensions.

IV. EXPERIMENTAL RESULTS

In order to verify the theoretical steady-state analysis and the proposed MPC route, a laboratory prototype S-DAB converter is built and tested. The specifications of the prototype converter are listed in Table VI. Six power transistors IPP600N25N with $R_{ds(\text{on})} = 0.051\,\Omega$ are used as the active switches. Two fast Schottky diodes DSSK20-015A with 0.61 V forward voltage are used to implement the diode leg. The HF transformer with a turns ratio at 13:13 is made with an ETD39/N97 ferrite core. The power inductance is the sum of leakage inductance of transformer and an external inductor with an RM14/N87 ferrite core. The gating signals of S-DAB are generated by an EP2C8Q208C8N FPGA from Altera. The dead time of gating signals is selected at 200 ns or 7.2°. In the experimental test, an EA 8360-15T bench power supply is used as the input dc source, while the load is provided with a BK 8510 programmable dc electronics load. The layout of experiment setup is given in Fig. 12.

TABLE VI
SPECIFICATIONS OF THE PROTOTYPE S-DAB CONVERTER

Parameters	Values
Input DC voltage V_{in}	$110 \sim 130$ V
Output DC voltage V_o	72 V
Rated power	200 W
Switching frequency	100 kHz
Power inductance L_s	43 μH
Transformer turns ratio	13 : 13, ETD39/N97
Filter Cap. C_o	1x470μF Elec. + 2x1nF CBB
Switch $M_1 \sim M_6$	IPP600N25N
Diode D_{s1}, D_{s2}	DSSK20-015A

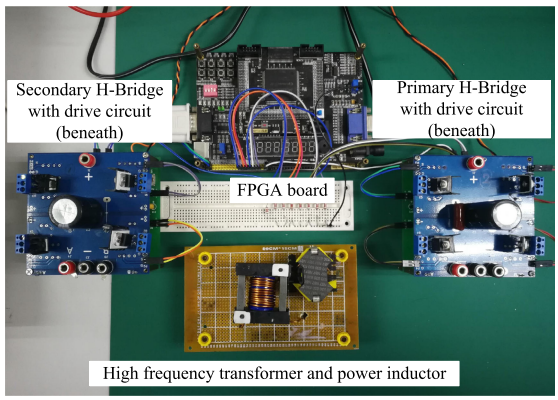

Fig. 12. Experimental setup of an S-DAB dc–dc converter.

A. Verification of Operation Modes

At first, a series of tests on the prototype converter is performed to validate the existence of different operation modes. The input/output voltages are fixed at 120 and 72 V, respectively, for $M = 0.6$. Experimental waveforms corresponding to all the effective modes at different load levels are presented in Fig. 13. In each figure, the steady-state waveforms of the primary voltage v_{AB}, the secondary voltage v_{CD}, the inductor current i_{Ls}, and the gating signal of M_6 are captured and shown from top to bottom. The distinctive relationships between all phase angles in each mode can be verified. It is seen that the inductor

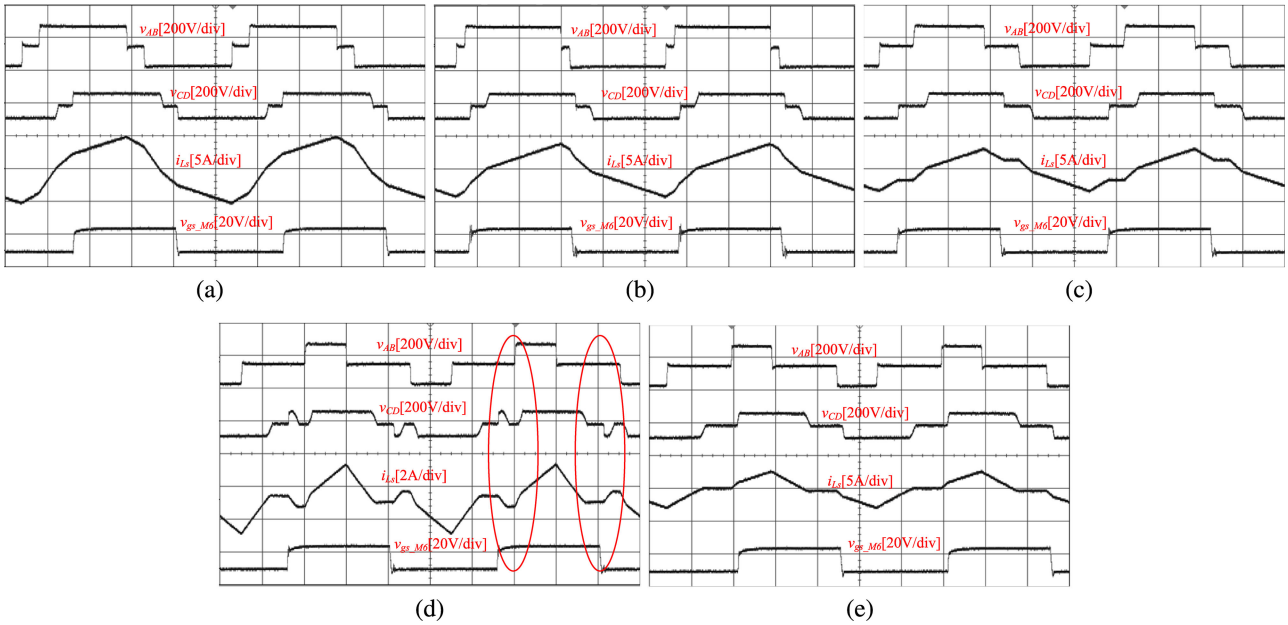

Fig. 13. Experimental waveform of different steady-state modes of an S-DAB converter under the hybrid control with $M = 0.6$ (time scale: $2\,\mu$s/div). (a) Mode A. (b) Mode B. (c) Mode C. (d) Mode D. (e) Mode E.

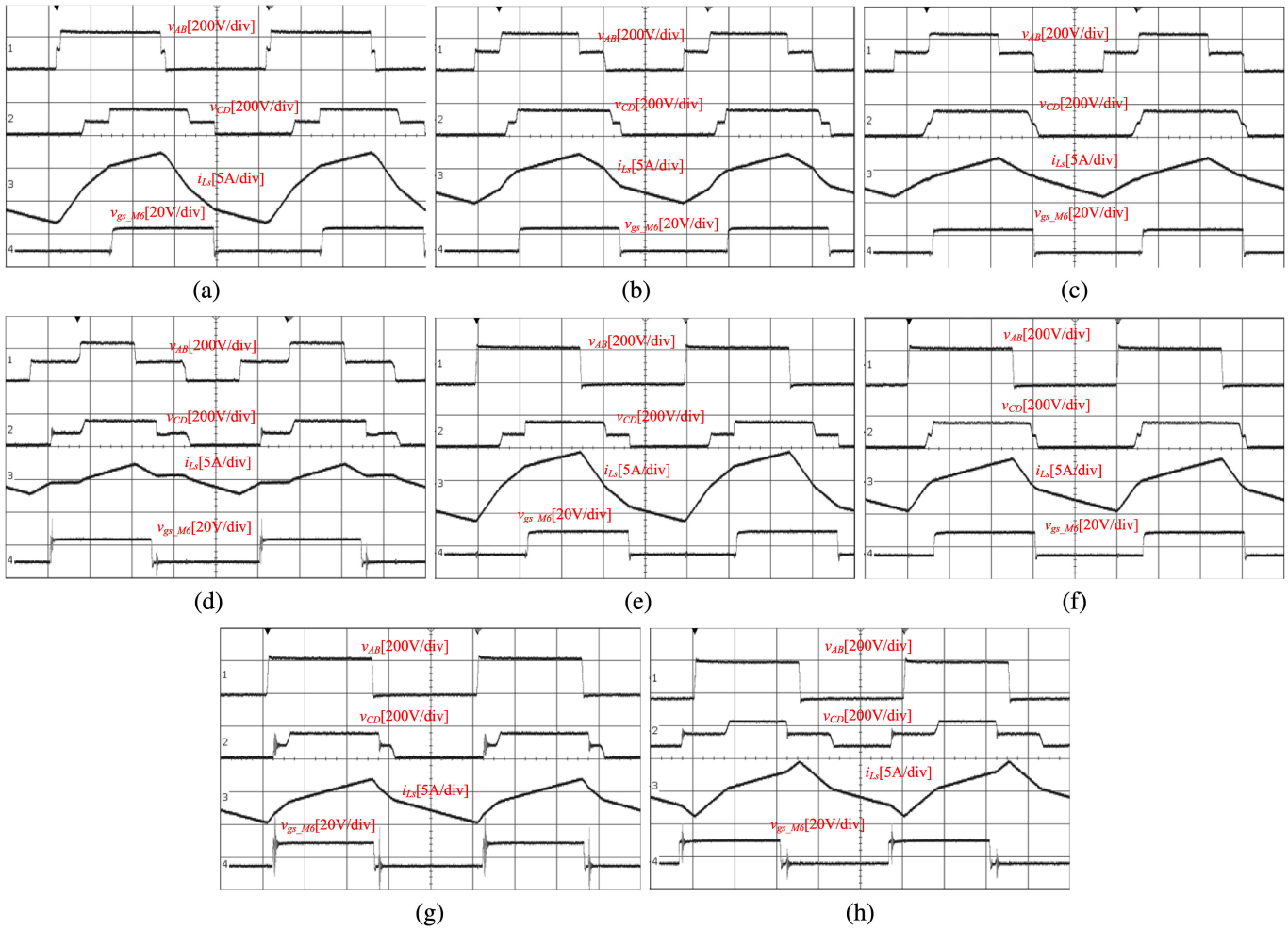

Fig. 14. Experimental waveforms of an S-DAB converter with $M = 0.6$ (time scale: $2\,\mu$s/div) at: (a) 200 W under MPC, (b) 150 W under MPC, (c) 100 W under MPC, (d) 50 W under MPC, (e) 200 W under PS, (f) 150 W under PS, (g) 100 W under PS, and (h) 50 W under PS.

TABLE VII
COMPARISONS OF STEADY-STATE OPERATION AT $V_{IN} = 120$ V AND $V_o = 72$ V

Power		PS control					MPC control route				
		α (°)	ϕ (°)	I_{rms} (A)	I_{peak} (A)	η (%)	α (°)	ϕ (°)	I_{rms} (A)	I_{peak} (A)	η (%)
200W	theor.	0	86.08	3.45	5.25	-	10.89	93.64	3.48	5.18	-
	exp.	0	86.4	3.51	5.43	93.21	8.89	94.86	3.55	5.39	93.16
150W	theor.	0	40.8	2.36	3.94	-	45.5	72.41	2.32	3.64	-
	exp.	0	42.12	2.49	4.21	94.15	44.45	73.06	2.47	3.86	94.64
100W	theor.	0	6.89	1.91	3.37	-	64.25	61.09	1.63	2.84	-
	exp.	0	6.66	1.95	3.5	93.03	60.95	62.94	1.74	3.04	94.21
50W	theor.	0	-21.88	2.05	4.04	-	98.07	43.24	1.23	2.36	-
	exp.	0	-25.02	2.12	4.31	85.66	89.71	47.65	1.21	2.4	93.74

current is continuous in Modes A, B, and C. The turn-ON moment of M_6 lags the zero-crossing point of inductor current in Mode A ($\phi > \beta$), but leads the zero-crossing point of inductor current in both B and C ($\phi < \beta$). Zero-current durations can be identified from waveforms in Fig. 13(d) and (e) for Modes D and E, respectively. Generally, these experimental waveforms match the theoretical ones predicted in Fig. 2 well except for Mode D [see Fig. 13(d)], where there are the voltage ringing of the secondary-side voltage v_{CD} in interval IV. This phenomenon is attributed to the resonance between the parasitic capacitances of switches/diode and the transformer leakage inductance triggered by the switch commutation during zero-current intervals.

B. Verification of the Proposed MPC Route

To validate the proposed MPC route and demonstrate its advantages over the secondary PS control, the prototype converter was tested with the two control methods, respectively, for different load conditions. The input and output voltages are still $V_{\text{in}} = 120$ V and $V_o = 72$ V. At $M = 0.6$, the boundary power level between the two stages under the MPC control is calculated to be 51% or 102 W. Therefore, as predicted, the converter works in stage 1 or Mode A at 200 and 150 W under the MPC control as shown in Fig. 14(a) and (b), respectively, and it is working approximately near the boundary condition when the power is 100 W as shown in Fig. 14(c). For the case of 50 W as shown in Fig. 14(d), the converter under the MPC control is working in stage 2, i.e., along the boundary between Modes C and D as predicted in (17). It is seen that there is no voltage ringing existing during the zero-current interval for light load operation. The measured waveforms under the PS control are presented in Fig. 14(g) and (h) for different load too. At the load level 200 and 150 W, the converter under the PS control is also working in Mode A with full ZVS operation. At light load (100 and 50 W) the converter enters into Mode B as $\phi < \beta$. The loss of ZVS can be identified from the negative rising edge and positive falling edge of v_{CD} in Fig. 14(g) and (h). At 50 W under the PS control as seen in Fig. 14(h), the phase shift ϕ has to be negative, which induces quite high peak and rms inductor current at 4.31 and 2.12 A, while those two values are measured at 2.4 and 1.21 A under the MPC control in Fig. 14(d).

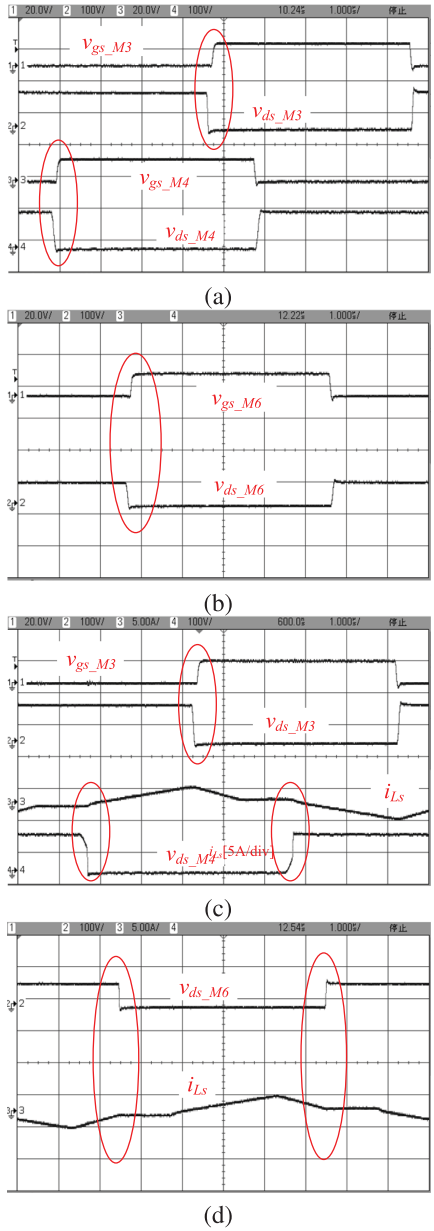

Fig. 15. Switch behavior of all switches and diodes with the MPC control route (time scale: 1μs/div). (a) Primary switches in stage 1. (b) Secondary switches in stage 1. (c) Primary switches in stage 2. (d) Secondary switches in stage 2.

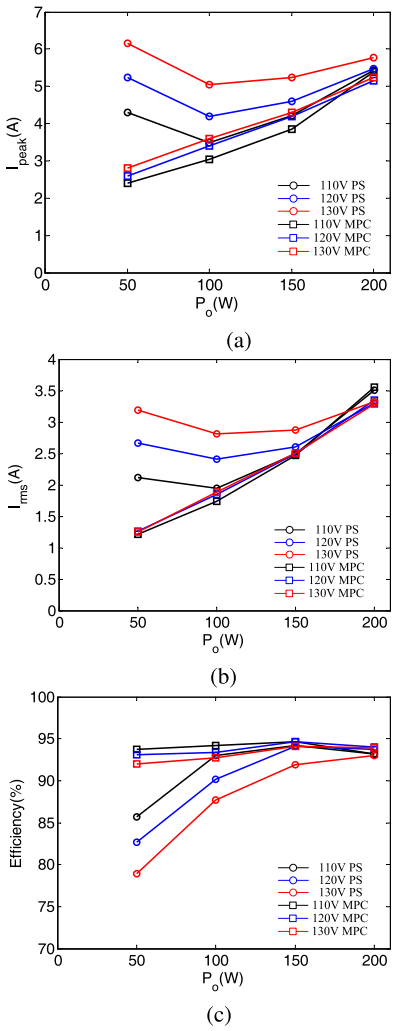

Fig. 16. Performance comparisons for an S-DAB under the PS control and the MPC control route with variation of input voltage. (a) Peak current with regard to power. (b) RMS current with regard to power. (c) Efficiency with regard to power.

Under the MPC control, the switching behavior in the two stages are validated and shown in Fig. 15. In Fig. 15(a), the gating signals of primary switches M_3, M_4 with their drain-to-source voltages in stage 1 are shown together, which indicates the ZVS operation of primary switches. Similarly, the ZVS operation of the secondary switch M_6 in stage 1 can be viewed in Fig. 15(b) in terms of the gating signal V_{GS6} and V_{DS6}. Fig. 15(c) and (d) records the switching behavior in stage 2. On the primary side [see Fig. 15(c)], M_3 is still working with ZVS while M_4 now are turned ON/OFF at zero current. The zero current switching ON and OFF applies for the secondary switch M_6 too, which can be viewed in Fig. 15(d).

Important parameters measured from experimental test are concluded and compared with theoretical calculations for both the PS control and MPC control in Table VII. As the MPC route is optimized for the MPC operation, the rms and peak current of the inductor under the MPC control are lower than those under the PS control, as expected, and the improvement becomes more apparent especially for the partial load. The measured efficiency under the MPC control also show advantageous over that under the PS control, especially at light load condition due to low rms/peak current and soft-switching operation. With the variations of input voltage, extended experimental tests were conducted under the two different control methods. More comparisons based on the measurements are visualized in Fig. 16 for variation of the input voltage V_{in} at 110, 120, and 130 V, respectively. It can be concluded that both the peak/rms current and the conversion efficiency under the proposed MPC route are improved over those under the conventional PS control and the overall improvement is valid for a variation of converter gain.

V. Conclusion

In this paper, an S-DAB dc–dc converter with a hybrid gating scheme is investigated comprehensively for different effective operation modes with distinctive power characteristics and switching behavior. On this basis, an MPC control route across the whole power range is developed and proved to effectively reduce the inductor peak/rms current, depress nonactive power, extend soft-switching range, and enhance conversion efficiency through theoretical calculation and experimental test. Thus, the conventional PS control associated operation mode with hard switching or negative phase-shift angle ϕ are avoided and the working range is extended to zero power in buck operation. Conclusively, the PWM-PS based MPC control improve the overall partial load performance of an S-DAB converter successfully. The control principle proposed in this paper can also be adapted for other existing types of S-DAB converter with modified configuration, which deserve more future efforts.

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