A Fully Soft Switched Point-of-Load Converter for Resource Constraint Drone Applications

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***Abstract*—The power efficiency and weight of present point-of-load (POL) dc–dc converters for drone applications are often compromised because they suffer from large switching losses at continuous conduction mode for heavy loads and excessive hardware overheads at discontinuous conduction mode for light loads. This paper presents a boundary conduction mode (BCM) control scheme for POL converters embodying a single operation mode. This is achieved by means of a hysteresis voltage controller to turn ON/OFF the output power stage when necessary. The proposed BCM control scheme achieves high power efficiency ($\geq$91.2%) over a wide load range (5 mA–1 A) by means of fully soft switching. Specifically, a hysteretic current controller is proposed to realize ZCS, and an adaptive dead time controller is proposed to realize ZVS. Further, the proposed BCM control scheme requires a small output inductor (0.82 μH) by means of designing the customizable peak inductor current. To verify the proposed BCM control scheme, we realize a BCM-based POL converter that features an input voltage range of 5–16 V, output voltage range of 2.5–8 V, switching frequency of 1.5 MHz, peak power efficiency of 96.8%, and $\leq$35 mV output voltage undershoot/overshoot for 1-A load step. When being benchmarked against state-of-the-art counterparts, the proposed design features the lowest voltage undershoot/overshoot, the highest switching frequency, $\sim$5.7$\times$ smaller inductor, and $\sim$11% higher power efficiency at light loads.**

***Index Terms*—Boundary conduction mode (BCM), fully soft switching, high power efficiency, point-of-load (POL) converter, small size.**

I. Introduction

PRESENT-DAY drones are highly resource constraint [1], embodying more functions with more complex hardware, hence leading to compromised flight life. In view of this, the aim of enhancing the flight life is becoming increasingly imperative, and it can be achieved with reduced weight and improved power efficiency.

Inductor-based point-of-load (POL) buck dc–dc converters [2], [3], which are right next to the load and convert the energy from a battery (e.g., 11.4 V) to a voltage (e.g., 5.0 V) appropriate for the load, are ubiquitous in drones with increased numbers (e.g., $\sim$6 POL converters can be found in [1]). In view of this, power efficiency and weight of inductor based POL converters are critical parameters to achieve the above-mentioned aim.

The state-of-the-art POL converter attempts the aim in two means [2]. First, it operates at continuous conduction mode (CCM) for heavy loads and discontinuous conduction mode (DCM) for light loads, a dual-mode operation, hence leading to the improved power efficiency particularly over a wide load range. Second, it operates at a high switching frequency (e.g., $\geq$1 MHz) to reduce the size of output inductor, which is typically $\sim$33% of PCB footprint and $\sim$50% of total weight [4].

However, the present approach has three undesirable consequences. First, as the switching frequency increases to MHz, the switching loss becomes severe for CCM. This is because CCM innately cannot realize fully soft switching, which includes zero-current switching (ZCS) and zero-voltage switching (ZVS). Hence, the power efficiency at heavy loads is compromised. Second, the size reduction of the output inductor is often limited by three factors. The first factor is the small inductor current ripple for the avoidance of DCM at heavy loads [5], hence leading to a relatively large inductor. The second factor is the large dc current at heavy loads, typically requiring a large inductor with current rating two to three times higher than the maximum output load current to avoid the risk of magnetic dc saturation [6]. The last factor is the current overshoot—a large inductor is desirable to suppress it during large load steps [7]. Third, excessive hardware overheads are required to achieve both CCM and DCM.

At the boundary between CCM and DCM, there is a special operating mode called boundary conduction mode (BCM), whose inductor current at the valley is around zero. Compared to CCM and DCM, BCM offers three innate advantages. First, as the valley current of BCM is around zero every cycle, it innately allows ZCS, thereby easing the realization of fully soft switching [8]. Second, as the peak inductor current of BCM is customizable, a substantially small inductor can be achieved by means of designing a large peak inductor current [9]. Third, BCM enables the converter with a single modulation type over the whole load range. It is well recognized that conventional converter designs typically employ hybrid modulations, i.e., pulse frequency modulation (PFM) and pulsewidth modulation (PWM), to improve the conversion efficiency over a wide load range. However, due to the employment of both PFM and PWM, the reliability and the output voltage regulation of the converter often gets compromised because of its ensuing design complexity and potential mode transition issue [10].

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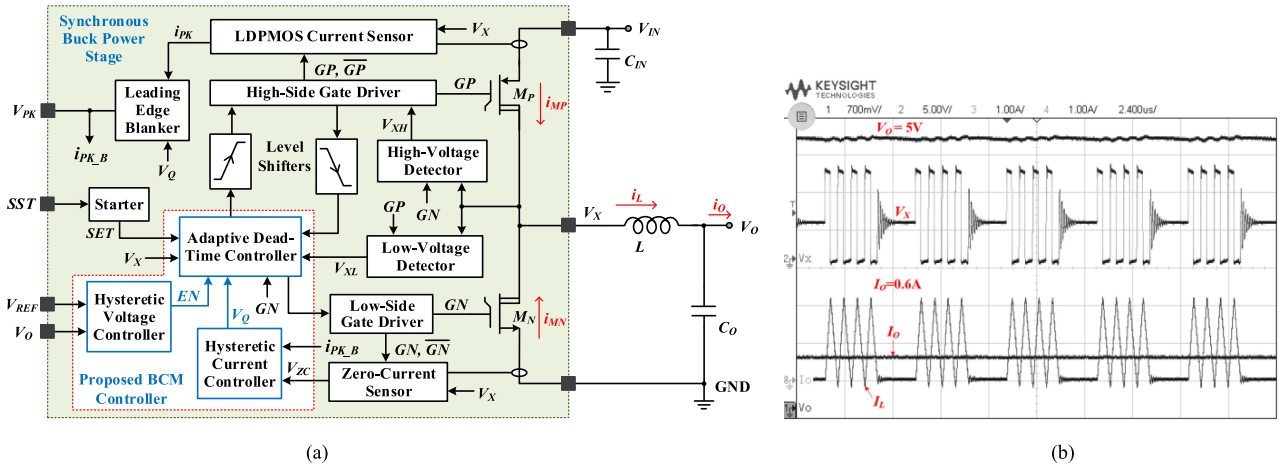

Fig. 1. Proposed BCM-based POL converter. (a) System architecture. (b) Measured waveforms.

Although BCM offers the potential for the combined lighter weight and higher power efficiency over a wide load range, it is rarely adopted for POL converters at this juncture. That is because reported control schemes [11]–[14] for CCM and DCM are inadequate/incompatible for BCM-based POL converters.

In this paper, we propose a novel BCM control scheme for POL converters embodying a single-mode operation. This is achieved by means of a hysteretic voltage controller to turn ON/OFF the synchronous buck power stage when necessary. The proposed BCM control scheme achieves high power efficiency ($\geq$91.2%) over a wide load range (5 mA–1 A) by means of fully soft switching. Specifically, a hysteretic current controller is proposed to realize ZCS, and an adaptive dead time controller is proposed to realize ZVS. Further, the proposed BCM control scheme achieves a small output inductor (0.82 μH) by means of designing the customizable peak inductor current. To verify the proposed BCM control scheme, we realize a BCM-based POL converter that features an input voltage range of 5–16 V, output voltage range of 2.5–8 V, switching frequency of 1.5 MHz, maximum output current of 1 A, and the peak power efficiency of 96.8%. When being benchmarked against state-of-the-art counterparts, the proposed design features the lowest voltage undershoot/overshoot, the highest switching frequency, $\sim$5.7$\times$ smaller inductor, and $\sim$11% higher power efficiency at light loads.

The organization of this paper is as follows. The proposed BCM control scheme and circuitry implementations for a BCM-based POL converter are delineated in Section II. Measurements and benchmarking are presented in Section III, and finally, the conclusions are presented in Section IV.

II. Proposed BCM-Based POL Converter

In this section, we will first delineate the system architecture of the proposed BCM-based POL converter. Thereafter, we will delineate the proposed BCM controller and its circuit implementations of the key functional blocks—hysteretic voltage controller, hysteretic current controller, and adaptive dead time controller.

Fig. 1(a) shows the system architecture of the proposed BCM-based POL converter, wherein the circuit blocks and circuit elements within the left shaded box are monolithically realized in an IC. The power switches (M_P and M_N) are realized by high voltage lateral diffused metal oxide semiconductor (MOS) transistors for low ON-resistance and high switching reliability. The proposed converter features inherent stability and fully soft switching operation, thus rendering no clock signal and no compensation network. The proposed design also features innate input overcurrent protection and output inductor reverse current protection by means of regulating the current and voltage on M_P and M_N.

The proposed BCM controller composes three functional blocks. Specifically, the hysteretic voltage controller is implemented to regulate the output voltage by means of turning the synchronous buck power stage ON/OFF when necessary. The hysteretic current controller is implemented to monitor the inductor current and realize ZCS. The adaptive dead time controller is implemented to modulate the gate driving signals for the high-side and low-side power switches and realize ZVS. Hence, fully soft switching can be obtained.

Fig. 1(b) shows the measured waveforms of the proposed BCM-based POL converter, wherein V_O at the top and V_X at the middle are the output voltage and the voltage at the switching node, respectively. I_L at the bottom is the inductor current. It can be seen that the proposed POL converter performs as a constant current source (the average of I_L is 1 A) and provides a load-demanded current ($I_O = 0.6$ A) by means of turning ON/OFF the synchronous buck power stage. The inductor current features settling within one switching cycle and the power stage is turned OFF only when the inductor current is around zero.

A. Proposed BCM Controller

Fig. 2 shows the operational waveforms of the proposed BCM controller, where V_O is the output voltage and ΔV_O is the predetermined voltage ripple window of V_O. I_O and I_L are the output current and the inductor current, respectively. I_{LPK} and I_{LVY} are the peak and the valley of I_L, respectively. Unlike the

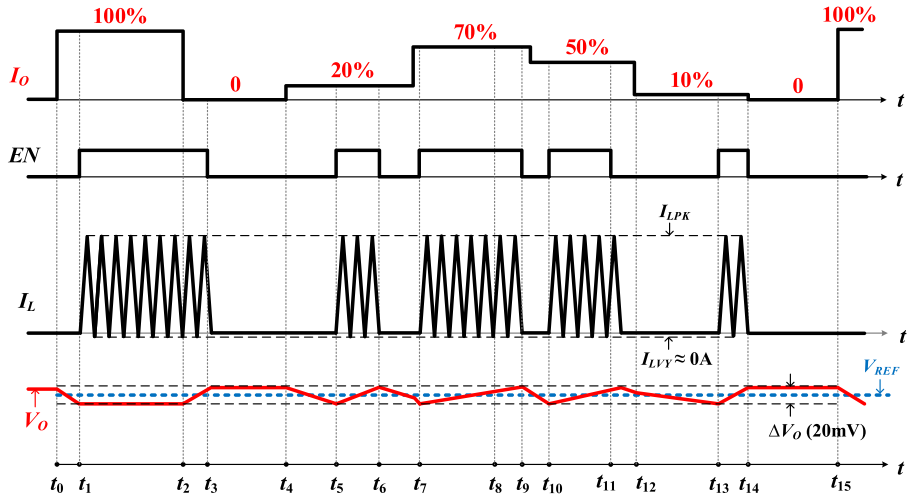

Fig. 2. Operational waveforms of the proposed BCM controller.

dual-mode operations of the state of the art, the proposed BCM controller allows the POL converter to always operate at BCM under all conditions. Hence, I_{LVY} ($\approx$0 A) is close to zero.

The operation principle is as follows: At $t = t_0$, the output current I_O changes from 0 A to full load (i.e., 100%) and subsequently the output voltage V_O commences to decrease due to the discharge of the output capacitor C_O in Fig. 1(a). The synchronous buck power stage in Fig. 1(a) remains OFF until the output voltage V_O reaches the bottom of the predetermined voltage ripple window ΔV_O at $t = t_1$, and an enable signal ($EN = 1$) is generated by the proposed BCM controller. Although the output current I_O becomes 0 A at $t = t_2$, the synchronous buck power stage keeps ON because the output voltage V_O is still low. Once V_O reaches the top of the predetermined voltage ripple window ΔV_O at $t = t_3$, the synchronous buck power stage gets turned OFF and waits for the next switching period (enabled by $EN = 1$).

Consequent to the aforesaid regulation mechanism, the proposed BCM control scheme features the following insightful merits. First, it eases the realization of fully soft switching because of the valley inductor current $I_{LVY} \approx 0$ A (ZCS). Second, it supports single-mode operation, only at BCM, and improves the power efficiency over a wide load range, including light loads and heavy loads. Third, the proposed BCM-based POL converter performs as an ideal voltage source. To meet the variable current demand from the output load, the BCM-based POL converter turns the synchronous buck power stage ON/OFF based on the output voltage. Fourth, the proposed BCM-based POL converter is innately stable and requires no compensation network.

Considering the converter weight, the output passive components, i.e., the output inductor L and output capacitor C_O, are critical and will now be elaborated. The output inductor L can be expressed as

$$L = \frac{1}{I_{LPK}} \cdot \frac{V_O(V_{\rm IN} - V_O)}{f_{\rm SW} \cdot V_{\rm IN}} \tag{1}$$

where $V_{\rm IN}$ and V_O are the input and output voltages, respectively. $f_{\rm SW}$ is the switching frequency. There are two interesting insights from (1). First, it shows that L is customizable and can be controlled by both I_{LPK} and $f_{\rm SW}$; note that, for the same scenario, L in reported designs [2], [15] is only determined by $f_{\rm SW}$. In view of this, it is one of the key advantages of the proposed BCM control scheme to further reduce L by means of increasing I_{LPK}. Second, once the input and output voltages are fixed, the switching frequency of the BCM-based POL converter becomes constant and does not vary with the output load changes. This attributes to the achievement of optimal power efficiency over a wide load range.

The output capacitor C_O can be expressed as

$$C_O = \frac{I_{LPK}}{2\Delta V_O} \cdot nT \quad (n = 2, 3, 4, \ldots) \tag{2}$$

where ΔV_O (e.g., 20 mV) is a regulated voltage ripple of the output voltage V_O. T is one switching cycle and n is the number of switching cycles. In this design, the minimum turn-ON period of the power stage is two switching cycles ($n \geq 2$). Equation (2) shows that a smaller ΔV_O can be achieved by increasing the output capacitance. Note that the size of the output capacitor is typically tens of times smaller than that of the output inductor.

Put simply, the proposed BCM control scheme allows the POL converter to embody high power efficiency over a wide load range by means of fully soft switching, and to employ a small output inductor by means of designing the customizable peak inductor current.

B. Proposed Hysteretic Voltage Controller

The proposed hysteretic voltage controller serves to regulate the output voltage by means of turning ON/OFF the synchronous buck power stage based on the output load demand.

Fig. 3 shows the schematic of the proposed hysteretic voltage controller, where V_O is the output voltage of the proposed POL converter, $VREF$ the voltage reference, and EN is the output regulation signal of the hysteretic voltage controller. The hysteretic comparator features an internal hysteresis ΔV_{TR} (e.g., 0.2 V), and the output voltage window ΔV_O can be determined

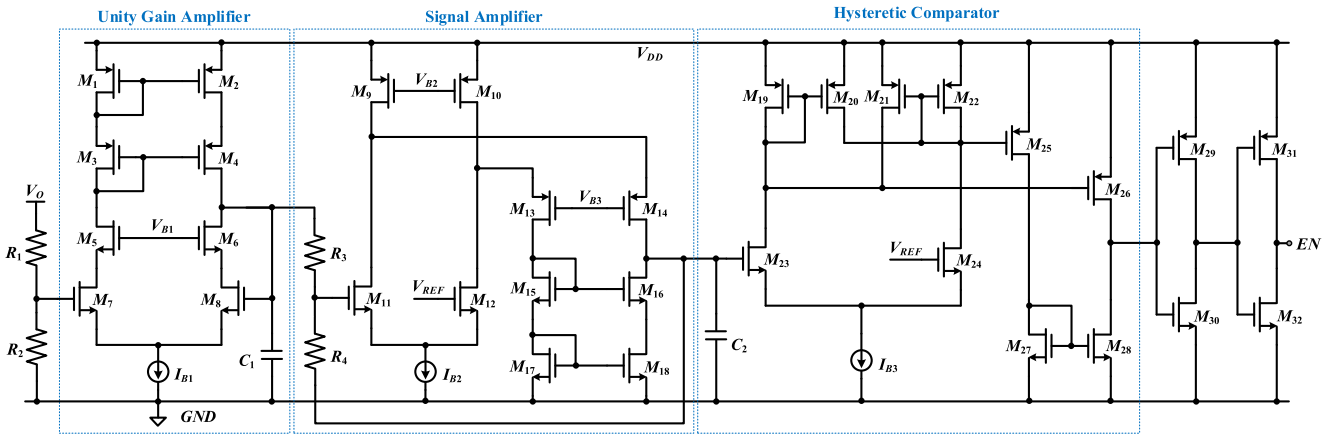

Fig. 3. Schematic of the proposed hysteretic voltage controller.

based on the following:

$$\Delta V_O = \left(1 + \frac{R_1}{R_2}\right) \cdot \frac{R_3}{R_4} \cdot \Delta V_{TR} \tag{3}$$

where $R_1 = R_2 = 10\,\text{k}\Omega$, and $R_4 = 20{\cdot}R_3$ in this design. Equation (3) shows that the proposed design leverages on the ratios of resistors instead of their absolute values. This results in the mitigation of silicon process variations and subsequently higher regulation accuracy.

The proposed hysteretic voltage controller functions as a voltage feedback loop and requires no compensation network, somewhat akin to the pulse frequency modulation [13]. Thus, it features quick transient response and short regulation delay (<50 ns). They are highly advantageous to the mitigation of output voltage undershoot and overshoot caused by large load steps (see Fig. 9).

C. Proposed Hysteretic Current Controller

The proposed hysteretic current controller serves to realize ZCS and regulate the inductor current by means of monitoring the current on power switches and keeping the valley inductor current at the boundary (around zero).

Fig. 4 shows the schematic of the proposed hysteretic current controller, where the lateral diffused p-channel metal oxide semiconductor (LDPMOS) current sensor and zero-current sensor are realized based on the designs in [16] and [17]. The input signals V_{PK} and V_{ZC} are from the LDPMOS current sensor and the zero-current sensor, respectively. The output signal of the proposed hysteretic current controller V_Q is initially set as high. Once the sensed current i_{PK} of the peak inductor current reaches the predetermined value, V_{REF}/R_S, the comparator *CMP* outputs high and resets the RS latch, $V_Q = 0$. When the inductor current drops to zero, the zero-current sensor outputs low $V_{ZC} = 0$, and sets the RS latch $V_Q = 1$. The operation logic of the proposed hysteretic current controller will be further illustrated in Section II-D.

The leading edge blanker is employed to prevent the false trigger by the possible spikes of the replica current from LDPMOS current sensor caused by current switching of M_P in Fig. 1(a).

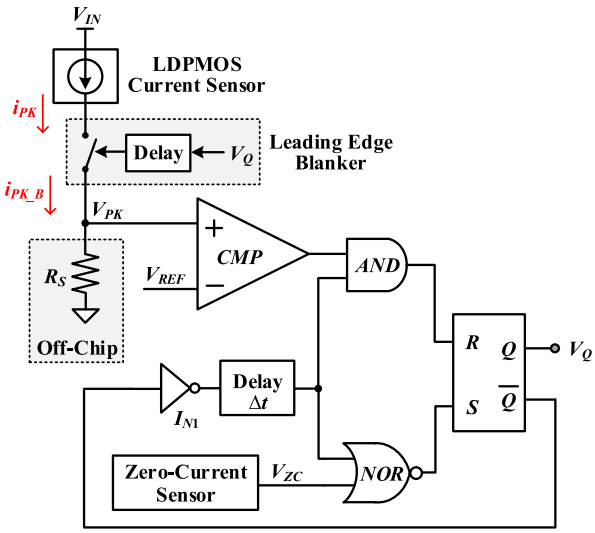

Fig. 4. Schematic of the proposed hysteretic current controller.

As the resistor R_S determines the peak inductor current, R_S is off-chip configured to provide easy customization.

D. Proposed Adaptive Dead Time Controller

The proposed adaptive dead time controller serves to realize ZVS and enable fully soft switching by means of modulating the gate driving signals for power switches and turning ON/OFF the power switches when their drain-to-source voltage/current is around zero.

Fig. 5(a) shows the schematic of the proposed adaptive dead time controller within the shaded box. The input signals *EN*, *SET*, and V_Q are from the hysteretic voltage controller, the converter starter, and the hysteretic current controller, respectively. Two output signals are the gate driving signals for the high-side and low-side power switches.

Fig. 5(b) shows the operational waveforms of the proposed adaptive dead time controller, where *GN* and *GP* are the gate driving signals of power switches M_N and M_P, respectively.

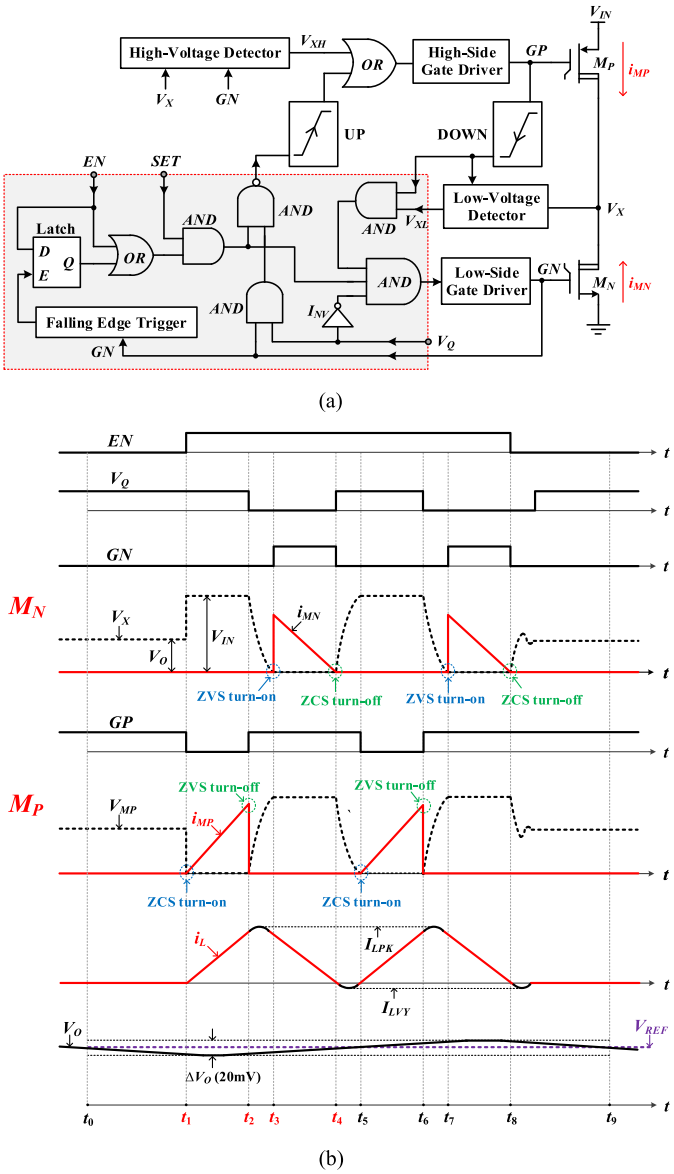

Fig. 5. Proposed adaptive dead time controller: (a) schematic and (b) operational waveforms.

The dashed line V_X and the solid line i_{MN} are the drain-to-source voltage (where the drain is the switching node) and current of M_N, respectively. The dashed line V_{MP} and the solid line i_{MP} are the drain-to-source voltage and current of M_P, respectively. i_L is the inductor current. It can be observed that the power switches, i.e., M_N and M_P, feature soft switching (ZCS or ZVS) in every turn-ON or turn-OFF transition during the period t_1–t_8. Because the switching cycle t_5–t_8 repeats t_1–t_4, for the sake of brevity, only the operation of cycle t_1–t_4 will be described herein.

In Fig. 5(b), at $t = t_0$, the value of the switching node voltage V_X equals to V_O because the synchronous buck power stage remains OFF, $EN = 0$, and the switching node exhibits a high impedance. At $t = t_1$, once the output voltage V_O drops to the bottom $(V_{REF}–\Delta V_O/2)$ of the predetermined voltage-ripple window ΔV_O, an enable signal, $EN = 1$, is generated by the proposed hysteretic voltage controller in Fig. 3 and turns ON the synchronous buck power stage—M_P first gets turned ON with ZCS. Then, the M_P current i_{MP} commences to increase. At $t = t_2$, once i_{MP} reaches the predetermined peak value V_{REF}/R_S (see Fig. 4), the proposed current controller outputs low $V_Q = 0$, and subsequently M_P gets turned OFF with ZVS. Due to the continuation of the inductor current, the switching node voltage V_X thereafter decreases. At $t = t_3$, once the low-voltage detector in Fig. 5(a) detects that V_X reaches zero, the proposed adaptive dead time controller in Fig. 5(a) turns ON M_N (ZVS). Then, the M_N current i_{MN} starts to decrease. At $t = t_4$, once i_{MN} drops near to zero, the proposed current controller in Fig. 4 turns OFF M_N with ZCS. By this mechanism, fully soft switching is achieved.

The realization of fully soft switching enables the proposed POL converter with the adoption of a significant 5.7× smaller output inductor than the state-of-the-art designs (see Table I) because of the high switching frequency and the customizable peak inductor current. Typically, a 5.7× smaller inductance requires 5.7× fewer turns of winding and provides a 5.7× lower dc resistance (DCR). Hence, the dc loss of the inductor gets substantially reduced. Although the ac loss becomes relatively larger, this increment is much smaller than the reduction of the DCR loss.

The realization of fully soft switching results in a relatively large peak-to-peak inductor current, which increases the conduction loss on power switches. This increment of conduction loss is significantly smaller than the saved large switching loss, particularly at high switching frequencies.

Put simply, the proposed hysteretic voltage controller regulates the output voltage and determines the turn ON/OFF of the synchronous buck power stage. To realize fully soft switching, the proposed hysteretic current controller determines the turn OFF of the power switches, and the proposed adaptive dead time controller determines the turn ON of the power switches. The realization of the fully soft switching eliminates the large switching loss, which is significantly larger than the slight compromise of the conduction loss, and thus greatly improves the power efficiency.

III. Measurement Results

Fig. 6 shows the microphotograph of the proposed BCM-based POL converter fabricated in a 130-nm BCDLite process. The prototype is 2.5 × 1.2 mm^2 with 50% of the area occupied by power transistors LDPMOS and lateral diffused n-channel metal oxide semiconductor (LDNMOS), and provides a maximum output current of 1 A. One surface mounted power inductor with 0.82-μH inductance and 7-mΩ DCR, and one 0805-case 100-μF capacitor with ∼10-mΩ equivalent series resistance (ESR) are employed in the setup of the proposed BCM-based POL converter measurement.

Fig. 7(a)–(c) shows the measured voltage and current waveforms of the proposed BCM-based POL converter with the output current of 0.8 A, 0.4 A, and 10 mA, respectively. We note two observations. First, the proposed design regulates the

TABLE I
PERFORMANCE COMPARISONS OF DIFFERENT STATE-OF-THE-ART DC–DC CONVERTERS

		This Work	LMZ12001 [18]	2017 [19]	2019 [20]
Application		POL		PoE	Portable
Fabrication Process		**0.13μm BCDLite**	N.A.	0.5μm BCD	0.35μm CMOS
Soft-Switching Techniques		**ZCS and ZVS**	No	ZVS	No
Operation Mode		**BCM**	CCM, BCM, and DCM	CCM, BCM, and DCM	
Control Scheme		**BCM Control**	COT Control	Dual Mode Control	AOT+PLL
Input Voltage (V)		**5-16**	4.5-20	33-57	3-3.7
Output Voltage (V)		**2.5-8**	0.8-6	12	1.2-1.8
Max. Output Current (A)		**1**	1	2.5	0.7
Switching Frequency (MHz)		**1.5**	1	1	1
Output Passive Components	Capacitor (μF)	**100**	100	122	10
	Inductor (μH)	**0.82**	10	22	4.7
Voltage Regulation for 1A Step	Overshoot (mV)	**28**	50	198	160
	Undershoot (mV)	**35**	50	182	120
Power Efficiency	The Peak	**96.8%**	93%	90.63%	90.04%
	@Max. Load	**96.8%**	92.5%	90.63%	88%
	@5mA Load	**91.2%**	<80%	<60%	<80%

The bold entities are to emphasize the good performance realized in the proposed design.

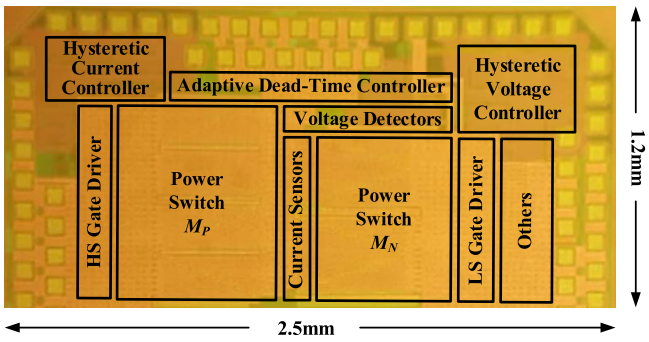

Fig. 6. Microphotograph of the proposed BCM-based POL converter.

output voltage and provides a load-demanded current by means of turning ON/OFF the power stage. The power stages are turned OFF only when the inductor current I_L reaches around zero. This can significantly mitigate the inductor current ringing and reduce the rectification power loss on the body diode of the low-side power switch. Second, the proposed BCM-based POL converter features inductor current settling within one switching cycle. This attribute improves the transient response. Moreover, as mentioned above, the switching cycle n is an integer, i.e., $n \geq 2$.

Fig. 8 shows the measured soft-switching waveforms of the proposed BCM-based POL converter, where it can be seen that fully soft switching is practically realized; as earlier denoted, M_P and M_N are the power switches in Fig. 1(a). ΔI_{L1} and ΔI_{L2} are the practical current errors, and ΔV_1 and ΔV_2 are the practical voltage errors in experimental scenarios. For the sake of being unambiguous, the lower $\Delta I_{L1} - \Delta I_{L2}$ and $\Delta V_1 - \Delta V_2$, the better the soft switching. In this perspective, our design ($\Delta I_{L1} = 10\,\text{mA}$, $\Delta I_{L2} = 8\,\text{mA}$, $\Delta V_1 = 0.1$ V, and $\Delta V_2 = 0.2$ V) is an advantageous attribute. Specifically, ZCS is demonstrated as M_N is turned OFF when its current is (practically) close to zero $\Delta I_{L1} = 10\,\text{mA}$, and subsequently, its voltage is also (practically) close to zero. M_N is turned ON when its voltage is also close to zero $\Delta V_1 = 0.1$ V, thus ZVS is realized. Similarly, ZCS is demonstrated as M_P is turned ON when its current is (practically) close to zero $\Delta I_{L2} = 8\,\text{mA}$, and M_P is turned OFF when its voltage is (practically) close to zero $\Delta V_2 = 0.2$ V.

Fig. 9 shows the measured voltage and current waveforms of the proposed BCM-based POL converter with 1-A load step. It can be seen that the proposed POL converter features a desirably low-voltage undershoot 35 mV, and a low-voltage overshoot 28 mV. This is expectedly because of the fast inductor current slew rate and the adopted large output capacitor. Hence, the proposed POL converter offers meaningfully good output voltage regulation even for large load steps.

Fig. 10 shows the measured power efficiency of the proposed BCM-based POL converter for different output currents over different input voltages. The output voltage is 5 V. As depicted, the switching frequencies for the proposed converter with the input voltages of 6, 12, and 16 V are 0.5, 1.5, and 1.8 MHz, respectively. In general, the configuration with lower input voltage exhibits lower switching frequency and higher power efficiency. This is as expected because of the smaller gate driving loss. In

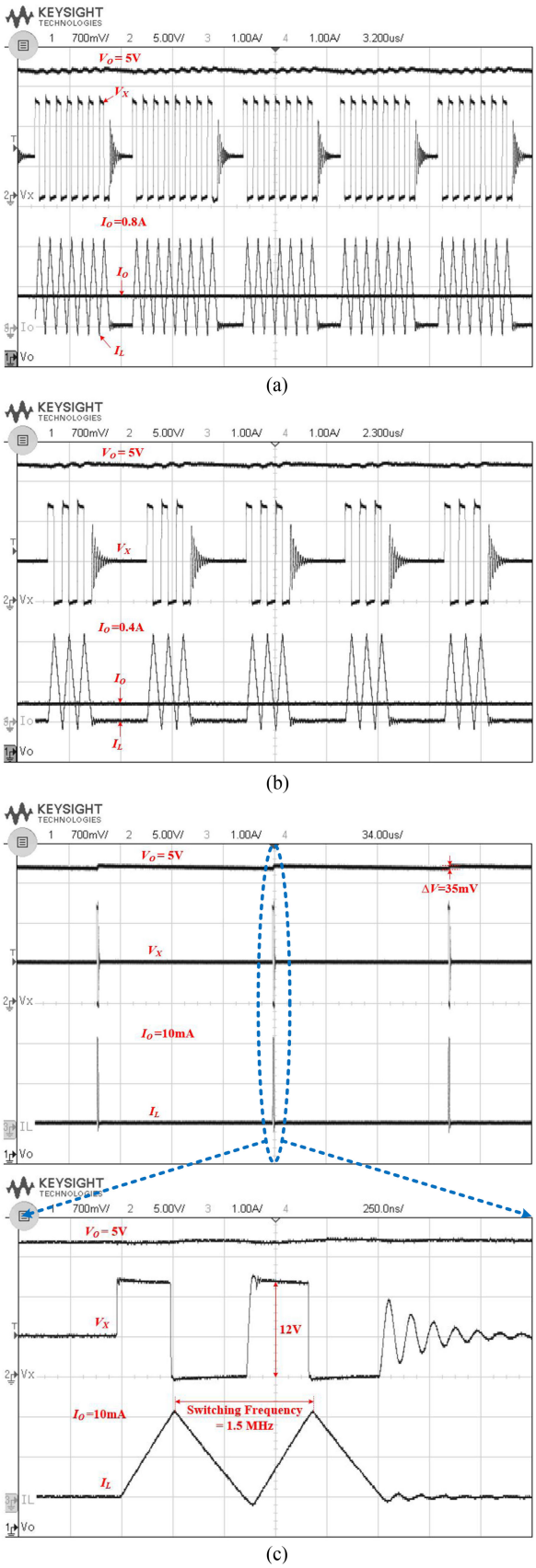

Fig. 7. Measured voltage and current waveforms of the proposed BCM-based POL converter with the output current of (a) 0.8 A, (b) 0.4 A, and (c) 10 mA.

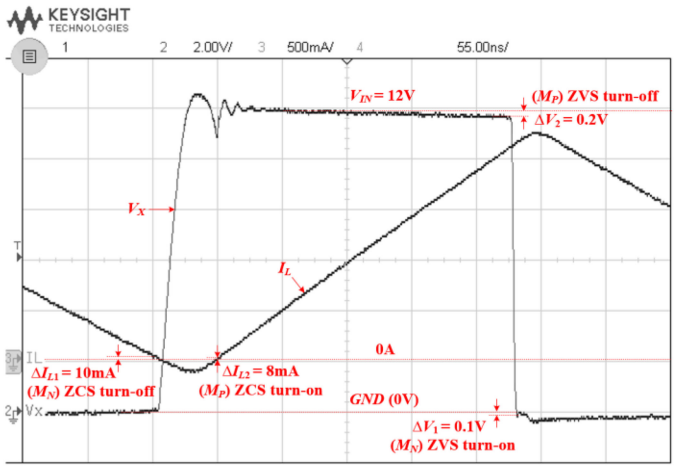

Fig. 8. Measured soft-switching waveforms of the proposed BCM-based POL converter.

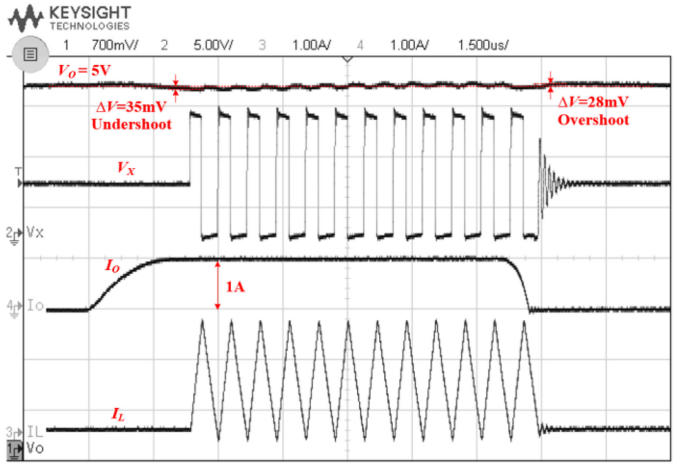

Fig. 9. Measured voltage and current waveforms of the proposed BCM-based POL converter under 1-A load step.

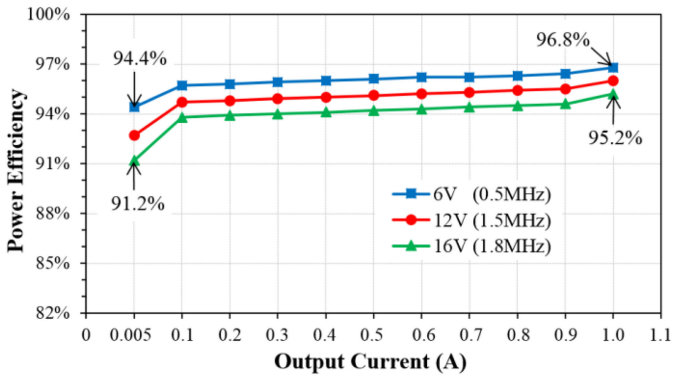

Fig. 10. Measured power efficiency of the proposed BCM-based POL converter for different output currents over different input voltages.

details, the proposed converter achieves a peak power efficiency of 96.8% at the maximum output current, i.e., 1 A and the lowest input voltage, i.e., 6 V. The minimum power efficiency that is obtained under the worst-case scenario, i.e., the lowest output current 5 mA and the highest input voltage 16 V, is still as high as 91.2%. This attribute is achieved because of the proposed BCM controller that features low quiescent current ($\sim$50 μA) and realizes fully soft switching in the whole load range.

Table I summarizes the key parameters of several state-of-the-art dc–dc converters against the proposed POL dc–dc converter. Of particular pertinence, the proposed design is the only design that embodies a single-mode operation, i.e., BCM, and features fully soft switching, including ZCS and ZVS. Consequently, the proposed design is the most power-efficient design over a wide load range.

In the perspective of weight, the proposed design desirably requires a significant 5.7$\times$ smaller inductance than the next most-competitive design. This is largely because of the proposed BCM control scheme and high switching frequency.

In the perspective of the output voltage regulation, it is imperative that the POL converter features low-voltage overshoot and undershoot for various load steps. For a fair comparison, the load steps in designs [18]–[20] are scaled to 1 A based on the same conditions. Obviously, the proposed BCM-based POL converter features the best voltage regulation by means of providing the lowest output voltage undershoot and overshoot.

In summary, by means of a single-mode operation and fully soft switching that substantially eliminate the switching losses, the proposed design features high power efficiency over a wide load range. Attributed to the proposed BCM control scheme, the proposed POL converter features lightweight and good voltage regulation by means of employing a small output inductor.

IV. Conclusion

A BCM-based POL dc–dc converter was proposed to feature both high power efficiency and lightweight by means of the embodiment of a single-mode operation and the realization of fully soft switching. The proposed BCM controller enabled the POL converter with the realization of fully soft switching, including ZVS and ZCS. Consequently, the switching losses were shown to be practically eliminated. The BCM controller also required a small output inductor and subsequently resulted in weight reduction. The prototype BCM-based POL converter featured a high switching frequency (1.5 MHz), good output voltage regulation ($\leq$35 mV for 1-A load step), small output inductor (0.82 μH), and high power efficiency ($\geq$91.2%) over a wide load range (5 mA-1 A). In terms of power efficiency, weight, and output voltage regulation, the proposed BCM-based POL converter was shown to be the most competitive design when benchmarked against the state of the art.

References

[1] *MAVIC PRO User Manual V2.0*, DJI, Shenzhen, China. (2017). [Online]. Available: https://www.dji.com/mavic

[2] F. Lee and Q. Li, "High-frequency integrated point-of-load converters: overview," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4127–4136, Sep. 2013.

[3] W. Zhang, Y. Su, M. Mu, D. Gilham, Q. Li, and F. C. Lee, "High-density integration of high-frequency high-current point-of-load (POL) modules with planar inductors," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1421–1431, Mar. 2015.

[4] Q. Li, Y. Dong, F. C. Lee, and D. J. Gilham, "High-density low-profile coupled inductor design for integrated point-of-load converters," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 547–554, Jan. 2013.

[5] Y. Qu, W. Shu, and J. S. Chang, "An air-core coupled-inductor based dual-phase output stage for point-of-load converters," in *Proc. IEEE Int. Symp. Circuits Syst.*, Florence, Italy, 2018, pp. 1–4.

[6] K. Stoyka, G. Capua, and N. Femia, "A novel AC power loss model for ferrite power inductors," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2680–2692, Mar. 2019.

[7] M. Orabi and A. Shawky, "Proposed switching losses model for integrated point-of-load synchronous buck converters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5136–5150, Sep. 2015.

[8] M. Biglarbegian, N. Kim, and B. Parkhideh, "Boundary conduction mode control of a boost converter with active switch current-mirroring sensing," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 32–36, Jan. 2018.

[9] G. Xu, D. Sha, J. Zhang, and X. Liao, "Unified boundary trapezoidal modulation control utilizing fixed duty cycle compensation and magnetizing current design for dual active bridge DC-DC converter," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2243–2252, Mar. 2017.

[10] M. Du, H. Lee, and J. Liu, "A 5 MHz 91% peak-power-efficiency buck regulator with auto-selectable peak- and valley-current control," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1928–1939, Aug. 2011.

[11] S. J. Kim *et al.*, "High frequency buck converter design using time-based control techniques," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 990–1001, Apr. 2015.

[12] J. Chen, Y. Hwang, C. Jheng, and C. Yu, "A low-electromagnetic-interference buck converter with continuous-time delta-sigma-modulation and burst-mode techniques," *IEEE Trans. Ind. Electron.*, vol. 65, no. 9, pp. 6860–6869, Sep. 2018.

[13] M. G. Jeong, S. H. Kim, and C. Yoo, "Switching battery charger integrated circuit for mobile devices in a 130 nm BCDMOS process," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7943–7952, Nov. 2016.

[14] W. Yan, C. Ho, H. Chung, and K. Au, "Fixed-switching boundary control of buck converter with second-order switching surface," *IEEE Trans. Power Electron.*, vol. 24, no. 9, pp. 2193–2201, Sep. 2009.

[15] Y. Su, Q. Li, and F. C. Lee, "Design and evaluation of a high-frequency LTCC inductor substrate for a three-dimensional integrated DC/DC converter," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4354–4364, Sep. 2013.

[16] Y. Qu, W. Shu, and J. S. Chang, "A low-EMI high-reliability PWM-based dual-phase LED driver for automotive lighting," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1179–1189, Sep. 2018.

[17] Y. Qu, W. Shu, and J. S. Chang, "A 2.8-MHz 96.1%-peak-efficiency 1.4-us-settling-time fully soft-switched LED driver with 0.08-1 dimming range," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10094–10104, Oct. 2019.

[18] Texas Instruments, LMZ12001 1-A simple switcher power module with 20-V maximum input voltage. (2015). [Online]. Available: http://www.ti.com/lit/ds/symlink/lmz12001.pdf

[19] Y. Li and Z. Zhu, "A 30-W 90% efficiency dual-mode controlled DC-DC controller with power over ethernet interface for power device," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 25, no. 6, pp. 1943–1953, Jun. 2017.

[20] J. Chen, Y. Hwang, C. Chang, Y. Ku, and C. Yu, "A sub-1 us fast-response buck converter with adaptive and frequency-locked controlled techniques," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2198–2203, Mar. 2019.

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