A Family of Step-Up Series–Parallel Dual Resonant Switched-Capacitor Converters With Wide Regulation Range

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***Abstract*—In this paper, a family of new step-up series–parallel dual resonant switched-capacitor converters (SP-DRSCs) is proposed to extend the conversion ratio for high step-up applications. The converters feature a wide gain range, continuously adjustable, and enhanced light-load voltage regulation. All flying capacitors operate in resonance, eliminating high transient current spikes and charge sharing losses. Thus, zero-current-switching (ZCS) turn-ON for all transistors and ZCS turn-OFF for all diodes are achieved. A comprehensive analysis of the operation principle, voltage-gain curves, stable regulation range, and voltage and current stress is given. An analytical method to quantify the passive component volume for the group of step-up dual resonance switched-capacitor converters is presented. Further design considerations to optimize the passive component volume of the proposed SP-DRSC and the effect of bulky bypass capacitors on the volume are discussed.**

***Index Terms*—Switched-capacitor converter (SCC), series–parallel (SP), dual resonant, passive component volume.**

I. INTRODUCTION

SWITCHED-CAPACITOR converters (SCCs) are known to have the advantages of light weight, low cost, and high power density [1]. However, SCCs suffer from high transient current spikes, since the capacitors are directly charged/discharged by other capacitors or voltage sources. As a result, the efficiency of the converter may be compromised in some applications [2]–[4]. Step-down resonant switched-capacitor converters (RSCs) with small inductors were presented in [5] and [6], where the charge and discharge current is a half sinusoidal waveform instead of high transient current spikes, which results in none capacitor charge sharing loss and reduced electromagnetic interference noise.

However, the aforementioned SCCs and RSCs have a narrow line regulation range dictated by circuit configurations.

The RSCs typically operate below the resonant frequency to enhance the regulation range [7], while a sneak circuit state appears with hard switching operation [8]. On the contrary, RSCs operating above the resonant frequency has the merit of zero voltage switching (ZVS) for switches [9]. Furthermore, these converters still have poor voltage regulation ability under the light-load condition with frequency modulation [10]. The step-down converter based on Cuk dual resonance core (DRC) performs improved regulation capability for the light load [11].

Multilevel techniques have been implemented in SCCs to extend the conversion ratio, such as the two-switch boosting switched-capacitor converter [12], exponential voltage step-down switched-capacitor converter [13], flying capacitor multilevel dc–dc converter [14], multilevel modular capacitor clamped dc–dc converter [15], and symmetry modular switched-capacitor converter [16]. Typically, multiple resonant inductors in charge/discharge paths of flying capacitors are required to modify the aforementioned multilevel SCCs to multilevel RSCs. In [16]–[18], the distributed stray inductance is carefully designed to ensure zero-current switching (ZCS). Due to the inconsistence of each stray inductance and the tolerance of the capacitance in practice, the variation of resonant frequency could be significant [19]. In [20] and [21], large intermediate bypass capacitors in multilevel RSCs are still required to hold the constant dc voltage. Without voltage regulation, the interleaved RSC performs small current ripple [22]. A switched-capacitor voltage tripler with interleaving operation was proposed to reduce the intermediate capacitors, but has a large number of transistors [23].

A switched-capacitor voltage multiplier based on series–parallel (SP) switched-capacitor cells was introduced with the fault-tolerance ability [24], [25], but numerous resonant inductors are required for the high-voltage conversion ratio as well. A step-up series–parallel resonant switched-capacitor converter based on the Cuk DRC was proposed in [26]. However, only the last cell operates in the resonant mode. So, high current spikes still occur in the previous cells resulting in high power loss

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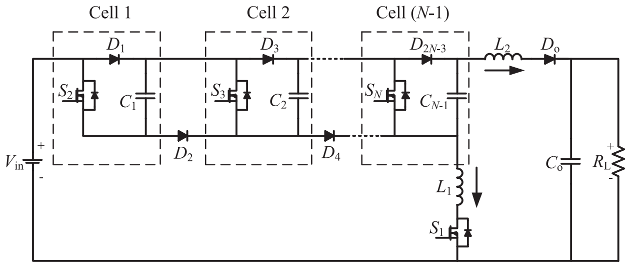


Fig. 1. Circuit oft the *N*X SP-DRSC.

during switching transients. As a result, bulky flying capacitors are required in the previous cells to work as capacitor banks.

In this paper, a family of new step-up series–parallel dual resonant switched-capacitor converters (SP-DRSCs) based on the Cuk DRC is proposed to provide a widely and continuously adjustable conversion ratio. Moreover, inherited from the Cuk DRC, the proposed SP-DRSCs have the distinctive feature of the enhanced light-load voltage regulation ability. Meanwhile, the maximum load limitation to achieve full range and stable close-loop regulation is analyzed. Compared to the converter in [26], all flying capacitors in the proposed converters operate in resonance. As a result, the efficiency is improved by eliminating the charge sharing loss and applying ZCS operation to transistors and diodes. By replacing the bulky capacitor banks with much smaller resonant capacitors, the proposed converters can achieve a smaller size than the converter in [26]. Furthermore, a generalized analytical method to quantify the total passive component volume (TPCV) for the group of step-up dual resonant switched-capacitor converters (DRSCs) is presented. The volume is evaluated according to the energy stored in passive components and the volumetric energy densities of inductors and capacitors. In order to reduce the TPCV of SP-DRSCs, the optimal SP switched-capacitor cell configuration is discussed. Moreover, the effect of bulky bypass capacitors on the TPCV is discussed and verified by comparing SP-DRSCs with the voltage doubler dual resonant switched-capacitor converters (VD-DRSCs).

II. PROPOSED SERIES–PARALLEL CONVERTERS

The circuit of the *N*X SP-DRSC consisting of (*N*−1) SP switched-capacitor cells is shown in Fig. 1. Each SP switched-capacitor cell is composed of a resonant capacitor, a transistor, and one diode connected in a loop with one diode connected in between the two adjacent cells. Moreover, the number of SP switched-capacitor cells can be reduced by cascading SP-DRSCs for high step-up applications. An example of the two-stage cascade SP-DRSC with only two resonant inductors is shown in Fig. 2.

For simplicity, a 3X SP-DRSC shown in Fig. 3 is used as an example for analysis. This converter contains three transistors $S_{1,2,3}$, four diodes $D_{1,2,3,\mathrm{o}}$, two identical resonant capacitors C_1 and C_2, two resonant inductors L_1 and L_2, and one output capacitor C_o. In addition, the input voltage is denoted by V_in, the output voltage is signified by V_o, and the load resistance is represented by R_L.

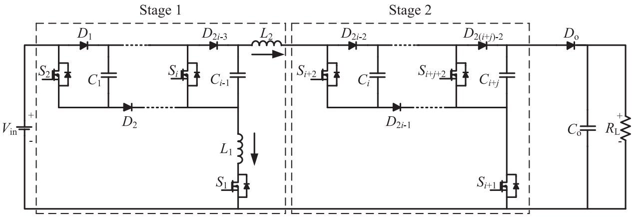


Fig. 2. Circuit of the two-stage cascade SP-DRSC.

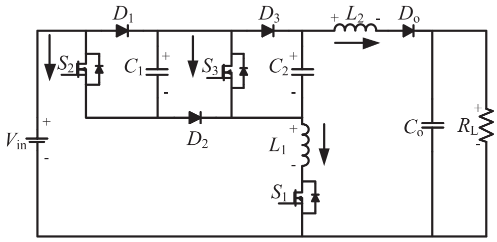


Fig. 3. Circuit of the 3X SP-DRSC.

III. OPERATION PRINCIPLE OF 3X SP-DRSC

In the charging process, the resonant path consists of C_1, C_2, and L_1 with resonant frequency f_{r1}, while the discharge resonant path consists of C_1, C_2, and L_2 with resonant frequency f_{r2}.

The on-time fixed frequency modulation is adopted for the converter with fixed ON-time of S_1 at $t_\mathrm{on} = 1/(2f_{r1})$, while the switching frequency varies to achieve voltage regulation. In order to simplify formula deductions, the capacitance and voltage across C_1 and C_2 are assumed to be identical in all operating states denoted by

$$C_r = C_1 = C_2, \quad v_{Cr}(t) = v_{C1}(t) = v_{C2}(t). \tag{1}$$

In this section, the operation principle of the 3X SP-DRSC is categorized into the normal load mode and the heavy-load mode. The converter operates in the normal load mode when the minimum voltage across flying capacitors is greater than zero. And vice versa, the value drops to zero after the complete discharging process in the heavy-load mode.

A. Mode 1 (Normal Load)

There is a boundary frequency f_b, when the current $i_{\mathrm{L}1}$ and $i_{\mathrm{L}2}$ are two complete half sinusoidal waveforms without overlapping state [26]. If the switching frequency is below f_b, the operation is similar to the traditional RSC with a limited line regulation range. The converter achieves a widely and continuously adjustable conversion ratio when the switching frequency is above f_b

$$f_b = \frac{2f_{r1}f_{r2}}{f_{r1} + f_{r2}} \tag{2}$$

where $f_{r1} = \frac{1}{2\pi\sqrt{2L_1C_r}}$ and $f_{r2} = \frac{1}{2\pi\sqrt{L_2C_r/2}}$.

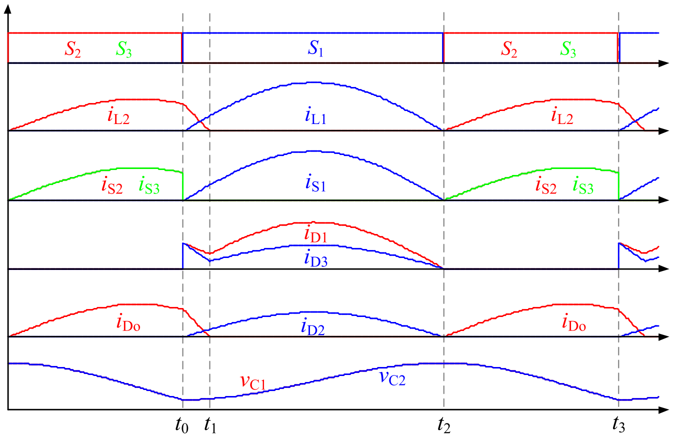
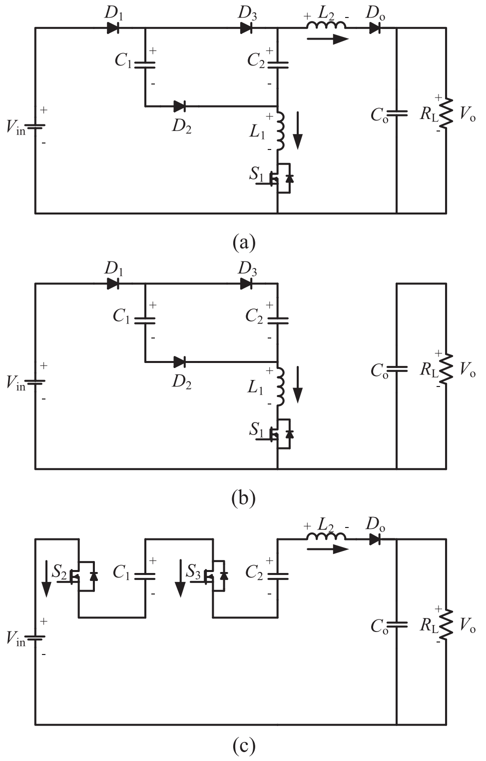


Fig. 4. Key waveforms in the normal load mode.



(a)

(b)

(c)

Fig. 5. Operating states. (a) Stage 1 [t_0, t_1]. (b) Stage 2 [t_1, t_2]. (c) Stage 3 [t_2, t_3].

As a result, there is an overlapping state when L_1 and L_2 conduct simultaneously to regulate the output voltage. The key operating waveforms in the normal load mode are shown in Fig. 4. The corresponding operating states are shown in Fig. 5.

1) Stage 1 [t_0, t_1]: At t_0, switches S_2 and S_3 turn OFF and S_1 turn ON with ZCS operation as shown in Fig. 5(a). During this interval, the two inductor current waveforms overlap, where L_1 operates in the resonant mode and L_2 operates in the linear discharging mode. In this state, the KVL and KCL equations are obtained

$$L_1 \frac{di_{L1}(t)}{dt} = V_{\text{in}} - v_{Cr}(t) \tag{3}$$

$$L_2 \frac{di_{L2}(t)}{dt} = V_{\text{in}} - V_{\text{o}} \tag{4}$$

$$2C_r \frac{dv_{cr}(t)}{dt} = i_{L1}(t). \tag{5}$$

From Fig. 4, the boundary conditions are

$$i_{L1}(t_0) = 0, \quad v_{Cr}(t_0) = V_{Cr\_\text{min}}. \tag{6}$$

Based on (3)–(6), the following expressions are obtained:

$$i_{L1}(t) = (V_{\text{in}} - V_{Cr\_\text{min}}) \sqrt{\frac{2C_r}{L_1}} \sin 2\pi f_{r1}(t - t_0) \tag{7}$$

$$v_{Cr}(t) = V_{\text{in}} - (V_{\text{in}} - V_{Cr\_\text{min}}) \cos 2\pi f_{r1}(t - t_0). \tag{8}$$

2) Stage 2 [t_1, t_2]: At t_1, $i_{L2}(t)$ drops to zero and D_{o} turns OFF with ZCS operation. Switch S_1 and diode $D_{1,2,3}$ continue conducting as Fig. 5(b). The expressions of the resonant current and voltage are the same as (7) and (8). This state ends with $i_{L1}(t)$ resonating to zero, when S_1 and diode $D_{1,2,3}$ turn OFF with ZCS operation.

3) Stage 3 [t_2, t_3]: At t_2, switches S_2 and S_3 turn ON with ZCS operation, while diode D_{o} starts conducting as shown in Fig. 5(c). This stage ends before L_2 is linearly discharged to zero in stage 1 of the next switching cycle. In this state, the KVL and KCL equations are obtained

$$L_2 \frac{di_{L2}(t)}{dt} = V_{\text{in}} + 2v_{Cr}(t) - V_{\text{o}} \tag{9}$$

$$C_r \frac{dv_{Cr}(t)}{dt} = -i_{L2}(t). \tag{10}$$

The boundary conditions are

$$i_{L2}(t_2) = 0, \; v_{Cr}(t_2) = V_{Cr\_\text{max}}. \tag{11}$$

Based on (9)–(11), the following expressions are obtained:

$$i_{L2}(t) = (2V_{Cr\_\text{max}} + V_{\text{in}} - V_{\text{o}}) \sqrt{\frac{C_r}{2L_2}} \sin 2\pi f_{r2}(t - t_2) \tag{12}$$

$$v_{Cr}(t) = \left(V_{Cr\_\text{max}} + \frac{V_{\text{in}} - V_{\text{o}}}{2}\right) \cos 2\pi f_{r2}(t - t_2) - \frac{V_{\text{in}} - V_{\text{o}}}{2}. \tag{13}$$

B. Mode 2 (Heavy Load)

The operating waveforms in the heavy-load mode are shown in Fig. 6. The key operating principle of stage 1 to stage 3 is identical to that in the normal load mode. But there is an extra stage 4 as shown in Fig. 6.

1) Stage 4 [t_3, t_4]: At t_3, $v_{C1,2}(t)$ drop to zero and the L_2 is linearly discharged. In this state, flying capacitors stop discharging until switch S_1 is turned ON at t_4. The expression of the linear discharging current flow through L_2 is the same as (4).

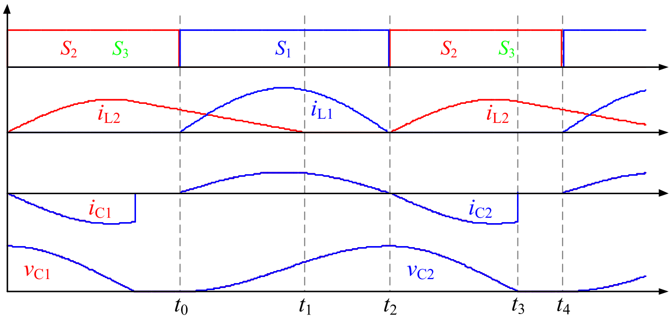


Fig. 6. Key waveforms in the heavy-load mode.

IV. VOLTAGE-GAIN CURVES AND BOUNDARY CONDITIONS

A. Voltage-Gain Curves in Mode 1

During t_0–t_2, the net charge flowing into C_1 and C_2 is

$$q_{t_0\sim t_2} = 2C_r(V_{Cr\_\max} - V_{Cr\_\min}) = \int_{t_0}^{t_2} i_{L1}(t)dt. \tag{14}$$

The ON-time of S_1 is fixed

$$t_{\text{on}} = t_2 - t_0 = \frac{1}{2f_{r1}}. \tag{15}$$

According to (7), (14), and (15), the following expression can be obtained:

$$V_{\text{in}} = (V_{Cr\_\max} + V_{Cr\_\min})/2. \tag{16}$$

In the normal load mode, the period of the stage 3 is obtained from Fig. 4.

$$t_3 - t_2 = \frac{1}{f_s} - \frac{1}{2f_{r1}}. \tag{17}$$

Then, the resonant frequency ratio k is defined as

$$k = \frac{f_{r1}}{f_{r2}} = \frac{1}{2}\sqrt{\frac{L_2}{L_1}}. \tag{18}$$

During t_2–t_3, the net charge flowing out of C_1 and C_2 is

$$q_{t_2\sim t_3} = C_r(V_{Cr\_\max} - V_{Cr\_\min}) = \int_{t_2}^{t_3} i_{L2}(t)dt. \tag{19}$$

By substituting (12), (17), and (18) into (19), the following expression is obtained:

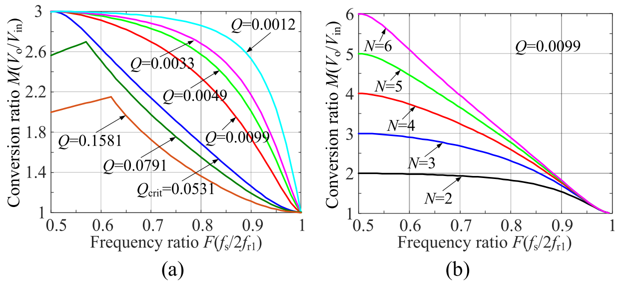
$$h = \cos 2\pi\left(\frac{f_{r1}}{kf_s} - \frac{1}{2k}\right) = \frac{2V_{Cr\_\min} + V_{\text{in}} - V_{\text{o}}}{2V_{Cr\_\max} + V_{\text{in}} - V_{\text{o}}}. \tag{20}$$

According to the KCL equation, the following expression is held in each stage:

$$i_{L2}(t) = i_{\text{Co}}(t) + V_{\text{o}}/R_L. \tag{21}$$

The $i_{\text{Co}}(t)$ is the current flowing through the output capacitor C_{o}. Since the average value of $i_{\text{Co}}(t)$ in one switching cycle equals to zero, the average current of $i_{L2}(t)$ is obtained by applying the charge balance to C_{o}

$$I_{L2} = f_s\int_{t_0}^{t_3} i_{L2}dt = V_{\text{o}}/R_L. \tag{22}$$



(a) (b)

Fig. 7. Conversion ratio curves for the SP-DRSC ($k = 1$). (a) 3X. (b) 2X–6X.

According to (4), (12), (16), (20), and (22), the conversion ratio expression in the normal load mode is derived as

$$M = \frac{V_{\text{o}}}{V_{\text{in}}} = \frac{m(V_{Cr\_\max} - V_{Cr\_\min})(h-1)}{hV_{Cr\_\max} - V_{Cr\_\min}} \tag{23}$$

where $m = C_rR_Lf_s$, f_s is the switching frequency.

Manipulating (16), (20), and (23) yields

$$V_{Cr\_\max} = \frac{-b - \sqrt{b^2 - 4ac}}{2a}V_{\text{in}} \tag{24}$$

$$V_{Cr\_\min} = 2V_{\text{in}} - V_{Cr\_\max} \tag{25}$$

where $a = 2(h+1)^2$, $b = h^2 - 1 - 2m(h-1)^2 - 8(h+1)$, and $c = 2m(h-1)^2 - 2(h-1) + 8$.

For the NX SP-DRSC, the conversion ratio in the normal-load mode holds the same equations as (23)–(25), where $a = (N-1)(h+1)^2$, $b = h^2 - 1 - 2m(h-1)^2 - 4(N-1)(h+1)$, and $c = 2m(h-1)^2 - 2(h-1) + 4(N-1)$.

B. Voltage-Gain Curves in Mode 2

As shown in Fig. 6, the maximum and minimum voltage across flying capacitors in (24) and (25) is clamped to $V_{Cr\_\max} = 2V_{\text{in}}$ and $V_{Cr\_\min} = 0$ in the heavy-load mode. Thus, (20) is rewritten as

$$\cos 2\pi f_{r2}(t_3 - t_2) = \frac{1-M}{5-M}. \tag{26}$$

According to (4), (12), (16), (22), and (26), the conversion ratio expression in the heavy-load mode is derived as

$$M = \frac{V_{\text{o}}}{V_{\text{in}}} = \frac{1 + \sqrt{1 + 8(N-1)m}}{2}. \tag{27}$$

In order to obtain the graphical conversion ratio curve, three parameters are defined as follows:

$$\text{frequency ratio}: F = \frac{t_{\text{on}}}{T_s} = \frac{f_s}{2f_{r1}};$$
$$\text{quality factor}: Q = Z_{r1}/R_L;$$
$$\text{characteristic impedance}: Z_{r1} = \sqrt{\tfrac{L_1}{(N-1)C_r}}.$$

According to (23) and (27), the graphical conversion ratio curves for the 3X SP-DRSC with $k = 1$ are obtained as shown in Fig. 7(a). Conversion ratio curves of four normal load resistances 80, 160, 240, and 640 Ω ($Q = 0.0099$, 0.0049, 0.0033, 0.0012), the critical load resistance 15 Ω ($Q_{\text{cirt}} = 0.0531$) and two heavy-load resistances 5 and 10 Ω ($Q = 0.1581,\ 0.0791$) are compared. The higher Q represents the heavier load. As shown, the conversion ratio can be regulated continuously.

For normal loads and the critical load, the maximum conversion ratio and the minimum voltage gain are $M_{\max} = 3$ at $F = 0.5$ and $M_{\min} = 1$ at $F = 1$. Therefore, the SP-DRSC exhibits improved light-load voltage regulation capability within a finite switching frequency band. In contrast, the maximum conversion ratio $M_{\max}$ for heavy loads is dropped below 3 depending on the value of Q. Thus, the regulation range for heavy loads is reduced.

The graphical conversion ratio curves for the 2X-6X SP-DRSC with $k = 1$ and $Q = 0.0099$ are shown in Fig. 7(b). Thus, the range of the conversion ratio is extended by increasing the number of SP switched-capacitor cells.

C. Boundary Conditions of Stable Regulation Range

As shown in Fig. 7(a), the conversion ratio can be decreased by increasing the switching frequency in the normal load mode. On the contrary, the conversion ratio increases with the switching frequency in the heavy-load mode, which leads to instability of the close-loop regulation. Therefore, the controllable range and boundary conditions between the two modes are discussed in this part.

The power capacity of the DRSC depends on the ability of the charge transferred by the flying capacitors [25] and the power transferred by linear discharging the inductor. In the normal load mode, the input energy is denoted as

$$W_{\text{in}} = W_{\text{in\_ST1,2}} + W_{\text{in\_ST3}}. \tag{28}$$

In stages 1 and 2, the energy taken from the source to charge the flying capacitors and to transfer to the load by linear discharging the inductor is denoted as $W_{\text{in\_ST1,2}}$.

$$W_{\text{in\_ST1,2}} = \sum_{i}^{\text{flying\_Cap}} \frac{1}{2} C_i \left(v_{Ci\_\max}^2 - v_{Ci\_\min}^2 \right) + V_{\text{in}} \int_{\text{linear}} i_{L2}(t)dt. \tag{29}$$

The $v_{Ci\_\max}$ and $v_{Ci\_\min}$ are the maximum and minimum voltage across the flying capacitor C_i.

In the stage 3, the energy taken from the source to discharge the flying capacitor C_1 is denoted as $W_{\text{in\_ST3}}$

$$W_{\text{in\_ST3}} = \frac{1}{2} C_1 \left(v_{Cr\_\max}^2 - v_{Cr\_\min}^2 \right). \tag{30}$$

By neglecting the power loss for the purpose of simplifing the analysis, the input power and output power are equal. Manipulating (16) and (28)–(30) yields

$$P_{\text{in}} = W_{\text{in}} f_s = 2K_m f_s V_{\text{in}} \Delta v_{C1} C_1 = V_{\text{o}}^2 / R_L \tag{31}$$

where Δv_{C1} is the voltage ripple of flying capacitors. The factor K_m for the NX SP-DRSC is

$$K_{m\_\text{SP-DRSC}} = N + \frac{N - M}{M - 1}. \tag{32}$$

As shown in Fig. 7(a), the SP-DRSCs reach the maximum conversion ratio $M_{\max} = 3$ at boundary frequency f_b with both normal load and critical load. Therefore, the corresponding quality factor for the critical load is defined as Q_{crit}. At the boundary frequency f_b, SP-DRSCs operate in the normal load mode when $Q < Q_{\text{crit}}$, and operate in the heavy-load mode when $Q > Q_{\text{crit}}$.

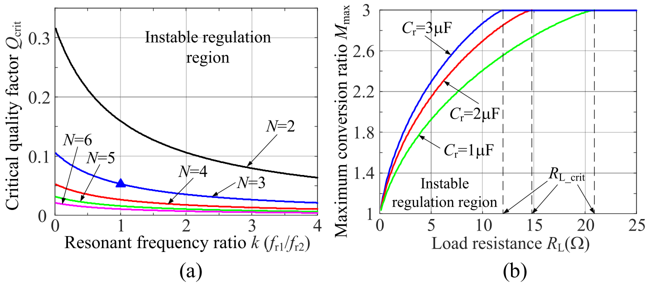


Fig. 8. Boundary conditions of the stable regulation region. (a) Q_{crit} versus k. (b) $M_{\max}$ versus R_{L} at $k = 1$, $N = 3$.

Manipulating (2), (31), and (32) yields

$$Q_{\text{crit}} = \frac{Z_{r1}}{R_{L\_\text{crit}}} = \frac{2}{\pi(1 + k)N(N - 1)} \tag{33}$$

where R_{L_crit} is the critical load resistance.

The Q_{crit} curves for the 2X–6X SP-DRSC are depicted in Fig. 8(a). As shown, the Q_{crit} decreases with the resonant frequency ratio k. It should be noted that Q_{crit} must be designed larger than maximun Q to avoid the instability of the close-loop voltage regulation.

Then, the constraint of resonant capacitance C_r to the converter power capacity is observed. The regulation capability among $C_r = 1$, 2, and 3 μF is compared under the condition $k = 1$, $N = 3$, marked as a triangle in Fig. 8(a). By manipulating (26) and (27), the maximum conversion ratio $M_{\max}$ with respect to load variation can be calculated as shown in Fig. 8(b). As shown, by replacing with larger C_r, the power capacity of converters can be enlarged with smaller R_{L_crit} and greater $M_{\max}$ in the heavy-load mode. Moreover, the converter can even avoid operating in the heavy-load mode as well as regulation instability.

V. PERFORMANCE ANALYSIS OF 3X SP-DRSC

A. Voltage Stress

The voltage stress of devices with $k = 1$ is analyzed in this part.

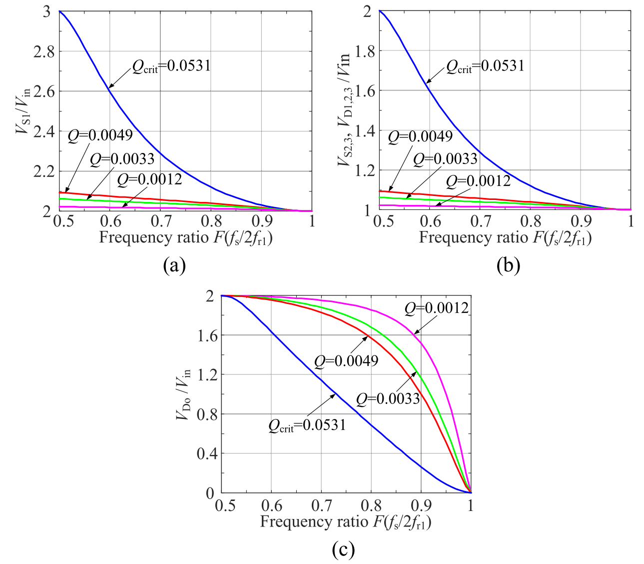
The component parameters and voltage regulation can influence the maximum voltage across the resonant capacitor $V_{Cr\_\max}$ and the output voltage V_{o}, which affect the voltage stress of other components.

The voltage stress of the switch S_1 can be derived by

$$V_{S1} = V_{\text{in}} + V_{Cr\_\max}. \tag{34}$$

The voltage stress of switches S_2 and S_3 and diodes $D_{1,2,3}$ equals to the maximum voltage of the resonant capacitors.

$$V_{S2,3} = V_{D1,2,3} = V_{Cr\_\max}. \tag{35}$$



(a) (b)

(c)

Fig. 9. Voltage stress curves ($k = 1$). (a) Voltage stress of S_1. (b) Voltage stress of $S_{2,3}$ and $D_{1,2,3}$. (c) Voltage stress of D_o.

The voltage stress of the output diode D_o is denoted as

$$V_{Do} = V_o - V_{in}. \tag{36}$$

According to the analyses in (34)–(36), the voltage stress normalized to the input voltage V_{in} is plotted in Fig. 9 with the same specifications as the prototype in Table II. It can be seen that voltage ripple over resonant flying capacitors and the voltage stress on components increases with loads.

B. Current Stress

The current base is defined as the maximum output current under the critical load resistance R_{L_crit} at $M = 3$.

$$I_{o\_max} = 3V_{in}/R_{L\_crit}. \tag{37}$$

Since the fixed ON-time of S_1 is $1/(2f_{r1})$, the current flowing through S_1 is always a half sinusoidal wave. The root-mean-square (rms) current flowing through S_1 is derived

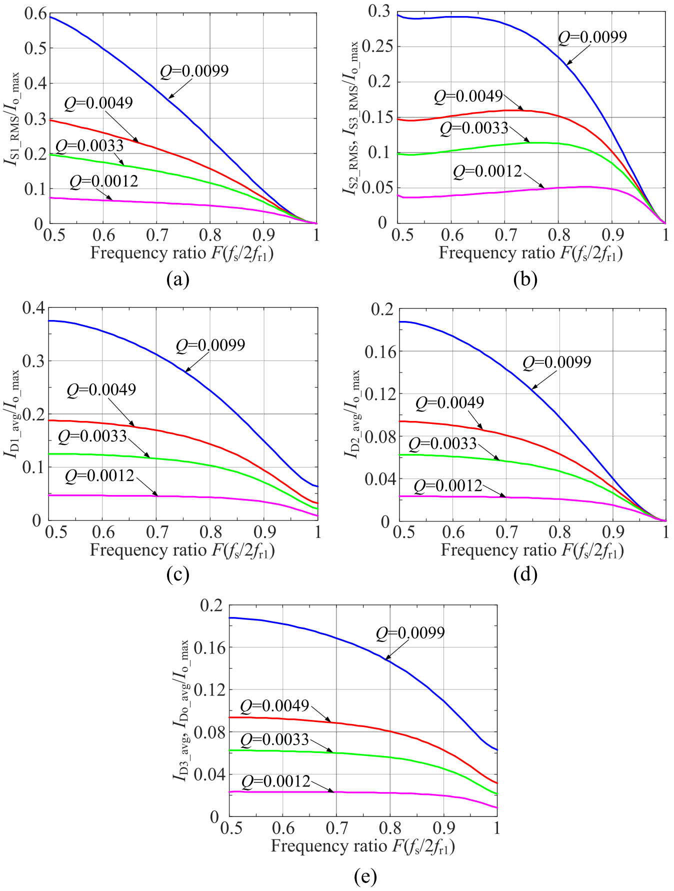
$$I_{S1\_RMS} = \frac{(V_{in} - V_{Cr\_min})}{Z_{r1}}\sqrt{\frac{F}{2}}. \tag{38}$$

The current flowing through S_2 and S_3 is a partial sinusoidal wave with the rms value

$$I_{S2,3\_RMS} = \frac{2V_{Cr\_max} + V_{in} - V_o}{4kZ_{r1}} \times \sqrt{\frac{1-F}{2} - \frac{kF}{4\pi}\sin\pi\left(\frac{2}{kF} - \frac{2}{k}\right)}. \tag{39}$$

The current flowing through D_o, D_1, and D_3 during the overlapping period is a triangle wave with the average value

$$I_{L2\_tri\_avg} = \frac{F(2V_{Cr\_max} + V_{in} - V_o)^2}{8\pi Z_{r1}(V_o - V_{in})}\left(1 - h^2\right). \tag{40}$$



(a) (b)

(c) (d)

(e)

Fig. 10. Current stress curves ($k = 1$). (a) Normalized rms current of S_1. (b) Normalized rms current of S_2 and S_3. (c) Normalized average current of D_1. (d) Normalized average current of D_2. (e) Normalized average current of $D_{3,o}$.

Another part of the current flowing through D_o is a partial sinusoidal wave, which has the equivalent average value to the average current flowing through D_2.

$$I_{L2\_sin\_avg} = I_{D2\_avg} = \frac{F\left(V_{in} - V_{Cr\_min}\right)}{\pi Z_{r1}}. \tag{41}$$

The average current flowing through diodes is given as

$$I_{D3\_avg} = I_{Do\_avg} = I_{D2\_avg} + I_{L2\_tri\_avg} \tag{42}$$

$$I_{D1\_avg} = I_{D2\_avg} + I_{D3\_avg}. \tag{43}$$

According to the analyses in (38)–(43), the current stress normalized to the current base I_{o_max} is depicted in Fig. 10 with the same specifications as the prototype in Table II.

VI. VOLUME EVALUATION FOR DRSCs

In this section, a quantified evaluation method of the TPCV for the group of step-up DRSCs is presented. With the same rated power, input voltage, maximum voltage ripple of flying capacitors, and switching frequency, the TPCV of the 4X SP-DRSC and the 4X VD-DRSC is discussed for comparison.

The schematic drawing of a 4X SP-DRSC is shown in Fig. 11, where symbol $ST_{1,2}$ indicates that the associated switch is ON during the stages 1 and 2. Similarly, symbol $ST_{1,3}$ indicates that the associated switch is ON during the stage 1 and stage 3, while symbol ST_3 indicates that the associated switch is ON during the

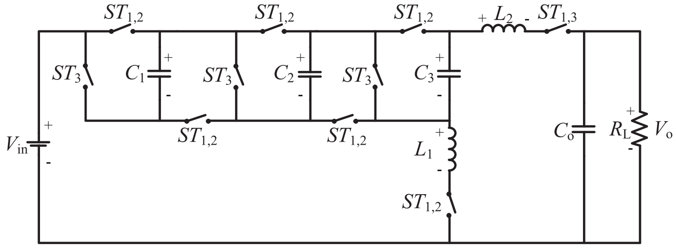


Fig. 11. Schematic drawing of the 4X SP-DRSC.

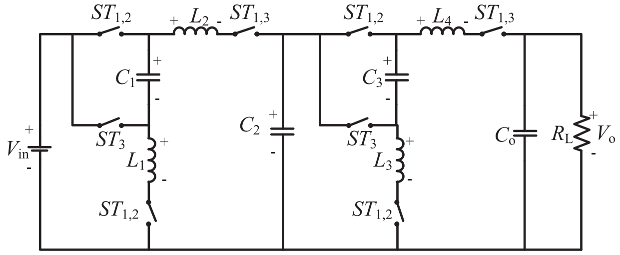


Fig. 12. Schematic drawing of the 4X VD-DRSC.

stage 3. The schematic drawing of a 4X VD-DRSC is shown in Fig. 12.

A. Voltage Ripple on Capacitors

As aforementioned in (31), the voltage ripple on flying capacitors reflects the power capacity of DRSCs. In the Appendix, a detailed deduction is presented to derive the numeric relationship of the voltage ripple and required capacitance among different intermediate capacitors in the group of step-up DRSCs. Here, only the final results are given.

According to the KVL analysis in (73), the orthonormal solution of the capacitor voltage ripple vector for the 4X SP-DRSC is

$$\mathbf{\Delta v_C} = \begin{bmatrix}1 & 1 & 1\end{bmatrix}^T. \tag{44}$$

The charge flow vector is derived from the KCL analysis in (74).

$$\mathbf{q_C} = \begin{bmatrix}1 & 1 & 1\end{bmatrix}^T. \tag{45}$$

Then, the capacitance vector is obtained.

$$\mathbf{C} = \begin{bmatrix}1 & 1 & 1\end{bmatrix}^{\mathbf{T}}. \tag{46}$$

It can be found that the capacitance and the voltage ripple of flying capacitors must be the same in a 4X SP-DRSC to achieve dual resonant operation.

Likewise, the solutions of the capacitor voltage ripple vector and capacitance vector for the 4X VD-DRSC are

$$\mathbf{\Delta v_C} = \begin{bmatrix}1 \; 0 \; \frac{1}{\sqrt{M}}\end{bmatrix}^T \text{and}\, \mathbf{C} = \begin{bmatrix}1 \; \infty \; 1\end{bmatrix}^{\mathbf{T}}. \tag{47}$$

Therefore, the 4X VD-DRSC can achieve dual resonant operation when C_1=C_3 and C_2 is a large enough bypass capacitor compared to C_1 and C_3. The voltage ripple in C_2 is negligible, while the magnitude of the voltage ripple in C_1 is $\sqrt{M}$times of that in C_3.

According to (31), the absolute value of the flying capacitor is obtained

$$C_1 = \frac{P_{\text{in}}}{2K_m f_s V_{\text{in}} \Delta v_{C1}}. \tag{48}$$

Similar to (32), the factor K_{m} for the VD-DRSC is obtained

$$K_{m\_\text{VD-DRSC}} = \frac{\sqrt[r]{M}}{\sqrt[r]{M}-1}, \quad r = \log_2 N. \tag{49}$$

In order to make a quantified evaluation of the TPCV for DRSCs, the input power P_{in}, the input voltage V_{in}, the flying capacitor voltage ripple Δv_{C1}, and switching frequency f_{s} are kept the same. Moreover, the flying capacitor voltage ripple Δv_{C1} is normalized to the input voltage.

$$\Delta v_{C1} = \alpha_V V_{\text{in}}. \tag{50}$$

According to (48), a larger voltage ripple allows for smaller capacitances, but also adds to the maximum voltage rating of capacitors and switches [27]. As aforementioned, the maximum value of α_V is 1 for the group of step-up DRSCs under the critical load condition.

Similarly, the bypass capacitor voltage ripple Δv_{Cb} is defined so as to choose the value of intermediate and output bypass capacitors in VD-DRSCs.

$$\Delta v_{\text{Cb}} = \beta_V V_{\text{o}}. \tag{51}$$

B. Capacitor Energy Storage

For a converter, the energy stored in all flying capacitors, intermediate, and output bypass capacitors can be expressed as

$$E_C = \frac{1}{2} \sum_i^{\text{Capacitors}} C_i V_{\text{C}i\_\max}^2. \tag{52}$$

The C_i is the capacitance and $V_{\text{C}i\_\max}$ is the maximum voltage across the capacitors. It is noted that the analysis here assumes that the flying capacitors of their respective voltage rating are used. In practice, capacitors with a specified voltage rating may be used due to the component availability. In this case, the volume of selected capacitors is expected to be larger and the analysis can be easily modified [27].

C. Inductor Energy Storage

The resonant inductors in DRSCs can be categorized into two classes: high-side inductors connected to the bypass capacitors and low-side inductor connected to the ground. The amplitude of the ac voltage across the high-side inductors and low-side inductors are

$$\Delta v_{L\_\text{high}} = V_{\text{in}} - V_{\text{o}} + \sum_i^{\text{disch\_path}} \Delta v_{\text{C}i} \tag{53}$$

$$\Delta v_{L\_\text{low}} = \Delta v_{\text{C}i}. \tag{54}$$

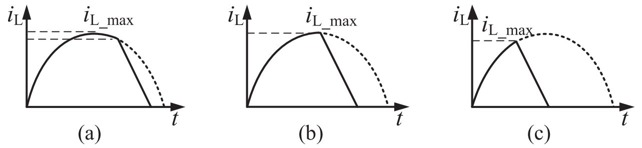


Fig. 13. Conceptual inductor current waveforms with resonant and linear discharging mode. (a) Type I $(M > M_b)$. (b) Type II $(M = M_b)$. (c) Type III $(M < M_b)$.

TABLE I
INDUCTORS STORED ENERGY

	Type I, Type II	Type III
SP-DRSCs E_{L_high}	$\frac{1}{2}C_1\sum\Delta v_{L\_high}^2$	$2C_1V_{in}\Delta v_{C1}(N-M)$
VD-DRSCs E_{L_high}		$2\sum C_1V_{in}\Delta v_{C1}\left(2-\sqrt[r]{M}\right)$
E_{L_low}	$\frac{1}{2}C_1\sum\Delta v_{L\_low}^2$	

As shown in Fig. 13, there are three types of current waveforms for high-side inductors according to the maximum inductor current in the resonant mode and linear discharging mode.

For SP-DRSCs and VD-DRSCs, the type-II operation mode occurs at the boundary conversion ratio M_b.

$$M_{b\_\text{SP-DRSC}} = N - \alpha_V(N-1) \tag{55}$$

$$M_{b\_\text{VD-DRSC}} = f\left(M^{2-\frac{1}{r}} - 2\cdot M^{2-\frac{2}{r}} + \alpha_V = 0\right) \tag{56}$$

where *r* is defined same as (49).

According to (7) and (12), the maximum inductor current under the resonant mode is obtained

$$I_{Lj\_\max} = \Delta v_{Lj}/Z_{rj}. \tag{57}$$

The Z_{rj} is the characteristic impedance of resonant tanks. Similarly, the energy stored in all resonant inductors can be calculated as

$$E_L = \frac{1}{2}\sum_{j}^{\text{Inductors}} L_j I_{Lj\_\max}^2 = E_{L\_\text{high}} + E_{L\_\text{low}} \tag{58}$$

where L_j is the inductance, and E_{L_high} and E_{L_low} are the energy stored in all high-side inductors and all low-side inductors as listed in Table I.

D. Volume Optimization for SP-DRSCs

In order to compare the volume, the stored energy in capacitors and inductors needs to be converted into total volumetric merit, as defined by

$$V_{\text{total}} = \frac{E_C}{\rho_{E,C}} + \frac{E_L}{\rho_{E,L}}. \tag{59}$$

The $\rho_{E,C}$ and $\rho_{E,L}$ are the volumetric energy densities of capacitors and inductors, respectively. It should be noted that $\rho_{E,L}$ also reflects the effect of the magnetic saturation constraint on the inductor size.

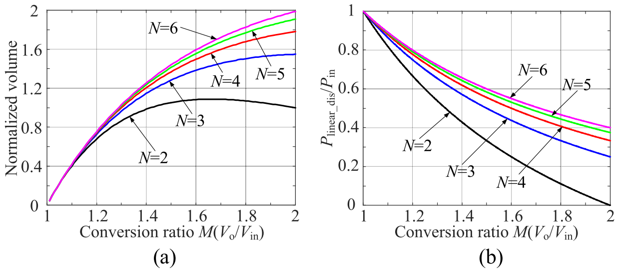


Fig. 14. Comparison of the *N*X SP-DRSC with $\alpha_v = 1$, $\beta_v = 0.05$. (a) Ratio of the TPCV. (b) Ratio of the linear discharging mode transferred power.

Since the circuit and performance are identical in the group of step-up DRSCs when $N = 2$, the TPCV for the 2X DRSC at $M = 2$ is defined as the volume base. Then, the normalized TPCV for the *N*X SP-DRSC is

$$\frac{V(M)_{\text{total,SP-DRSC}}}{V(M=2)_{\text{total,2X-DRSC}}} = \frac{\left(E_C + \frac{\rho_{E,C}}{\rho_{E,L}}E_L\right)_{\text{SP-DRSC}}}{\left(E_C + \frac{\rho_{E,C}}{\rho_{E,L}}E_L\right)_{\text{2X-DRSC}}}. \tag{60}$$

An average value $\rho_{E,C}/\rho_{E,L} = 150$ is obtained from a survey of X7R capacitors from TDK and XAL inductors from Coilcraft [27]. The normalized TPCV for SP-DRSCs of $N = 2$–6 are shown in Fig. 14(a). The TPCV increases with the number of SP switched-capacitor cells ($N-1$) in the conversion ratio range. However, the TPCV is identical for SP-DRSCs at $M = 1$ when the input voltage equals to the output voltage.

The high-side inductor L_2 in the *N*X SP-DRSC operates in the resonant mode, and then, linear discharging mode. In the linear discharging mode, a portion of the power transferred directly from input to output via L_2 without charging/discharging flying capacitors. The ratio of the transferred power in the linear discharging mode $P_{\text{linear\_dis}}$ to the input power is obtained and displayed in Fig. 14(b)

$$\frac{P_{\text{linear\_dis}}}{P_{\text{in}}} = \frac{N-M}{M-1} \Bigg/ \left(N + \frac{N-M}{M-1}\right). \tag{61}$$

As shown in Fig. 14(b), the transferred power in the linear discharging mode increases with the number of SP switched-capacitor cells ($N-1$). Consequently, the utilization of flying capacitors drops due to the increase in $P_{\text{linear\_dis}}$ without charging/discharging the flying capacitors. Therefore, the TPCV of SP-DRSCs can be reduced with minimum SP switched-capacitor cells for a given voltage gain.

E. Generalization to Step-Up DRSCs

The efficiency of the capacitor utilization is defined as

$$\begin{aligned}\lambda &= \frac{C_i}{2}\left(V_{Ci\_\max}^2 - V_{Ci\_\min}^2\right)\Big/\frac{C_i}{2}V_{Ci\_\max}^2 \\ &= \frac{V_{Ci\_\max}^2 - V_{Ci\_\min}^2}{V_{Ci\_\max}^2}\end{aligned} \tag{62}$$

where $V_{Ci\_\min}$ is the minimum voltage across the capacitor.

Solving $P_{\text{in}} = 150$ W, $V_{\text{in}} = 50$ V, $f_s = 50$ kHz, $\alpha_v = 1$, and $\beta_v = 0.05$, the efficiency of the capacitor utilization in SP-DRSCs is 100% for resonant flying capacitors and only 18.14% for the output bypass capacitor.

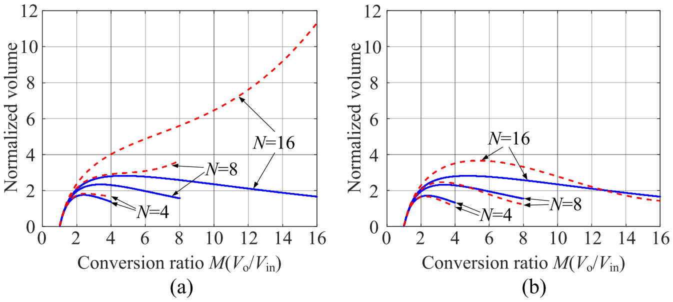


Fig. 15. Passive component volume with $\alpha_v = 1$, $\beta_v = 0.05$. (a) With bypass capacitors. (b) Without bypass capacitors.

TABLE II
SPECIFICATIONS OF 3X SP-DRSC PROTOTYPE

P	<150W	f_s	50~90kHz
V_{in}	50V	L_1	SER1052-252ML
V_o	113.5~145.9V	L_2	SER1360-103KL
$C_{1,2}$	CGA6N3X7R2A2 25K230AB ×4	Diodes	30BQ060 ×3 20CTQ150 ×1
C_o	GRM32EC72A10 6KE05L ×10	Switches	IRFR3518 ×2 IRFR4620 ×1

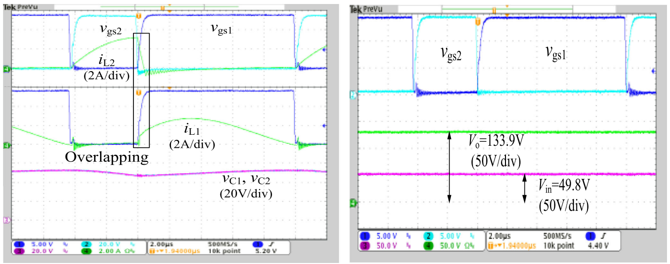


Fig. 16. Experimental waveforms ($Q = 0.0049$, $f_s = 70$ kHz). (a) Waveforms of $i_{L1,2}$ and $v_{C1,2}$. (b) Waveforms of V_{in} and V_{o}.

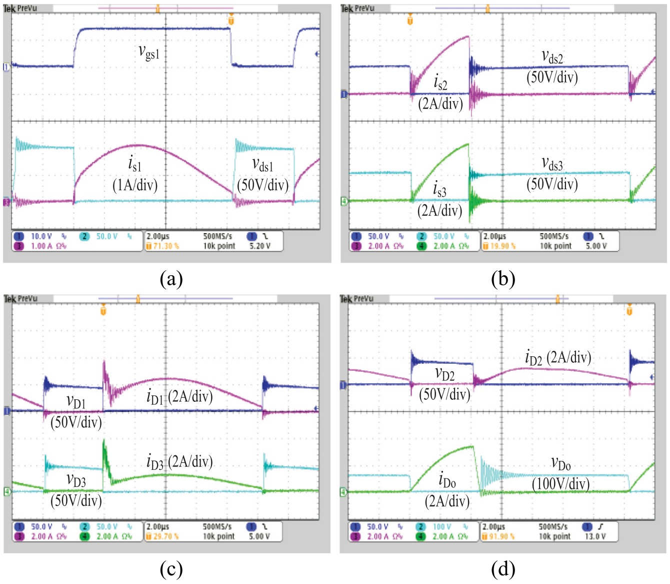


Fig. 17. Waveforms of switches and diodes ($Q = 0.0049$, $f_s = 70$ kHz). (a) Waveforms of switch S_1. (b) Waveforms of switches S_2 and S_3. (c) Waveforms of diodes D_1 and D_3. (d) Waveforms of diodes D_2 and D_o.

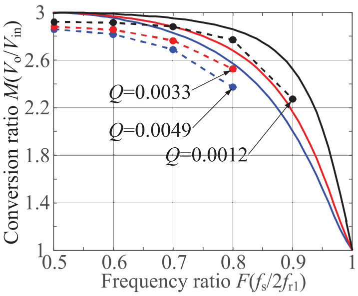


Fig. 18. Gain curves comparison.

The generalized analytical method can be applied to other step-up converters based on the Cuk DRC. In this section, the method is verified by the VD-DRSC as another example to discuss the effect of the bypass capacitor on the TPCV.

A similar definition to (60) is given by normalizing the TPCV of the *N*X SP-DRSC and *N*X VD-DRSC as

$$\frac{V(M)_{\text{total,DRSC}}}{V(M=2)_{\text{total,2X-DRSC}}} = \frac{\left(E_C + \frac{\rho_{E,C}}{\rho_{E,L}} E_L\right)_{\text{DRSC}}}{\left(E_C + \frac{\rho_{E,C}}{\rho_{E,L}} E_L\right)_{\text{2X-DRSC}}}. \quad (63)$$

Substituting the specification into (32), (48)–(59), and (63), the estimated TPCV of the *N*X SP-DRSC and *N*X VD-DRSC of $N = 4$, 8, 16 are shown in Fig. 15. The blue solid lines represent SP-DRSCs, while the red dashed lines represent VD-DRSCs. According to Fig. 15(a) and 15(b), the bypass capacitors take a large portion of the TPCV in high step-up VD-DRSCs, due to the low efficient utilization of intermediate bypass capacitors.

VII. EXPERIMENTAL RESULTS

A 150-W prototype with specifications shown in Table II was built to verify the effectiveness of the 3X SP-DRSC. With rated load $R_L = 160\ \Omega$ ($Q = 0.0049$), the experimental waveforms of $i_{L1,2}$, $v_{C1,2}$, V_{in}, and V_{o} under switching frequency $f_s =$ 70 kHz ($F = 0.7$) are shown in Fig. 16.

In Fig. 16(a), the converter operates at $f_s = 70$ kHz with about 0.4 μs overlapping period between i_{L1} and i_{L2}. With the ON-time fixed at 10 μs for S_1 and half sinusoidal wave of i_{L1}, ZCS turn-ON for S_1 and S_2 is retained. From Fig. 16(b), the conversion ratio is adjusted to 2.68.

The corresponding waveforms of switches and diodes are shown in Fig. 17. The ZCS turn-ON and turn-OFF are achieved for the switch S_1. ZCS turn-ON is achieved for the other switches S_2 and S_3. Thus, the turn-ON loss in switches is reduced. All diodes are turned OFF with ZCS. As a result, the diode reverse recovery current is minimized and so are the associated reverse recovery losses.

Fig. 18 shows the theoretical and the measured voltage gain curves under three different load resistances 160, 240, and 640 Ω ($Q = 0.0049$, 0.0033, 0.0012). The solid lines represent

TABLE III
COMPARISON OF 3X AND 4X MULTILEVEL SOFT-SWITCHING RSC TOPOLOGIES

Topologies	Proposed 3X	Ref. [10] 3X	Ref. [19] 4X	Ref. [20] 3X	Ref. [23] 3X	Ref. [25] 3X
Voltage regulation capability	Full-range	Limited-range	No	No	No	No
Maximum switch voltage stress	$3V_{\text{in}}$	V_{in}	$3V_{\text{in}}$	V_{in}	$2V_{\text{in}}$	$3V_{\text{in}}$
Maximum diode voltage stress	$2V_{\text{in}}$	V_{in}	$3V_{\text{in}}$	V_{in}	-	$2V_{\text{in}}$
No. of switches	3	2	7	2	12	4
No. of diodes	4	4	3	4	0	3
No. of resonant capacitors	2	2	2	2	3	2
No. of bypass capacitors	1	3	1	2	3	1
No. of resonant inductors	2	1	1	2	6	2
Peak Efficiency (V_{in}=50V)	95.7%	98.3%	95.5%	-	96.8%	95%

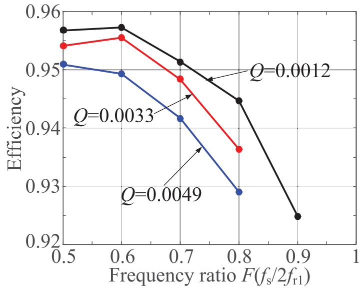
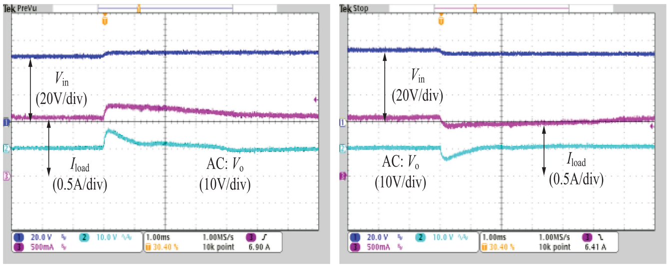
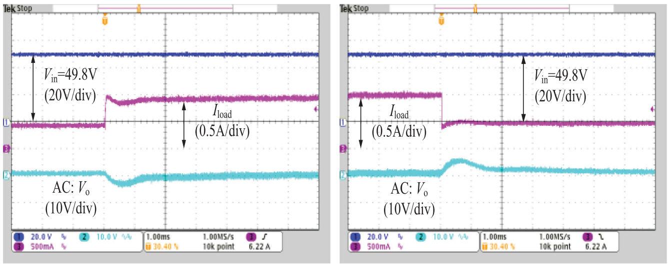


Fig. 19. Efficiency curves.



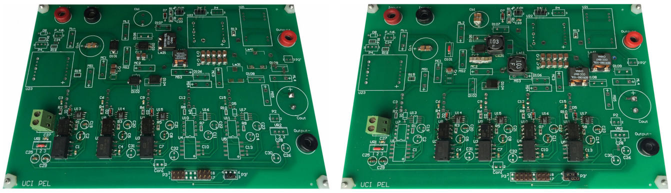
(a) (b)

Fig. 21. Line transient response. (a) Up input voltage. (b) Down input voltage.



(a) (b)

Fig. 20. Load transient response. (a) Uploading. (b) Downloading.



(a) (b)

Fig. 22. Photos of converter prototypes built on a circuit board test bed. (a) 3X SP-DRSC. (b) 4X VD-DRSC.

the theoretical curves, while the dashed lines represent the measured curves. The maximum conversion ratio of the prototype is 2.92 at $f_s = 50$ kHz ($F = 0.5$) with the light-load condition $Q = 0.0012$. The profile of the measured gain curves is close to the theoretical curves, verifying the extended line regulation range of 3X SP-DRSC.

In order to measure the efficiency, two digital power meters (Chroma 66202) were utilized to record the input and output power. The experimental efficiency curves under the three load resistances are given in Fig. 19. The 3X SP-DRSC reaches the experimental peak efficiency of 95.73%, 95.55% and 95.09% with Q = 0.0012, 0.0033, and 0.0049, respectively. However, the efficiency decreases with the switching frequency when the voltage is regulated.

In Fig. 20, the load regulation ability is verified by the load transient response with input voltage constant to 49.8 V. When the load current I_{load} is switched from 0.43 to 0.95 A, the output voltage is regulated back to 140 V after about 1.1-ms transient as shown in Fig. 20(a). Similarly, when I_{load} is switched from 0.95 to 0.43 A, the regulation transient time is about 1.2 ms as shown in Fig. 20(b).

In Fig. 21, the line regulation ability is verified by regulating the output voltage regulated at 140 V over line transient. When the input voltage is switched from 49.8 to 52.9 V, the output voltage is regulated to 140 V after about 1.1-ms transient as shown in Fig. 21(a). Similarly, when the input voltage is switched from 52.9 to 49.8 V, the regulation transient time is about 1 ms as shown in Fig. 21(b).

The photograph of the tested 3X SP-DRSC prototype is shown in Fig. 22(a). In Fig. 22(b), a 4X VD-DRSC prototype was built to verify the calculation. It can be found that fewer inductors and capacitors are applied in the SP-DRSC as analyzed previously.

VIII. COMPARISON WITH PREVIOUS COUNTERPARTS

The proposed SP-DRSCs feature ZCS turn-ON for all switches compared to the earlier counterpart [26]. In order to compare with other multilevel soft-switching RSCs, 3X or 4X step-up configurations presented in the recent literature are tabulated in Table III. The maximum switches and diodes voltage stress is calculated under the critical load resistance with resonant capacitors discharged to zero volts. As shown in Table III, the proposed soft-switching topology achieves the full range and continuously adjustable voltage regulation capability. In addition, compared to other topologies without intermediate bypass capacitors, the proposed topology offers simpler switching sequence than [19] and fewer switch counts than [25]. Efficiency can be increased by replacing diodes with small ON-resistance MOSFETs [23].

IX. CONCLUSION

A family of new step-up SP-DRSCs is proposed to obtain a wide, full-range continuous and enhanced light-load voltage regulation capability. All flying capacitors in the converters operate in resonance to avoid transient current spikes and charge sharing losses. ZCS operation of all transistors and diodes are achieved. In this paper, the critical loads to achieve the full-range regulation capability are provided to assist the design for a stable range of close-loop regulation. Furthermore, an analytical method is presented to quantify the TPCV for the group of step-up DRSCs. By operating at minimum SP switched-capacitor cell configuration, optimal volume for a given voltage gain is achieved due to the improved utilization of flying capacitors. It is found that the converter size can be dramatically reduced for high step-up applications without intermediate bypass capacitors. Finally, the analysis is verified by simulation and experimental results.

APPENDIX

Calculation of Voltage Ripple and Capacitance

The numeric relationship of the voltage ripple and required capacitance between different intermediate capacitors is derived for the group of step-up DRSCs. First, the voltage vector in DRSCs is defined

$$\mathbf{v} = \begin{bmatrix} v_{\text{in}} & \mathbf{v_C^T} & \mathbf{v_L^T} & v_{\text{o}} \end{bmatrix}^{\mathbf{T}} \tag{64}$$

where v_{in} is the input voltage, v_{o} is the output voltage, and $\mathbf{v_C}$ and $\mathbf{v_L}$ are the capacitor and the inductor voltage vectors.

$$\mathbf{v_C} = \begin{bmatrix} v_{C1} & v_{C2} & \cdots & \end{bmatrix}^T \tag{65}$$

$$\mathbf{v_L} = \begin{bmatrix} v_{L1} & v_{L2} & \cdots & \end{bmatrix}^T. \tag{66}$$

The $v_{C1,2}$ are the voltage across capacitors, and $v_{L1,2}$ are the voltage across inductors.

Denoting the voltage vector at the start of stage p as $\mathbf{v}^{\mathrm{p}}$, the matrix-vector-product form of the KVL analysis yields

$$\mathbf{A_p v^p} = \mathbf{0} \tag{67}$$

where $\mathbf{A_p}$ is the reduced loop matrix of the pth stage.

At the end of stage p, the voltage vector becomes $\mathbf{v}^{\mathrm{p}} + \mathbf{\Delta v}^{\mathrm{p}}$, creating a second KVL constrain.

$$\mathbf{A_p} \left(\mathbf{v^p} + \mathbf{\Delta v^p}\right) = \mathbf{0}. \tag{68}$$

The $\mathbf{\Delta v}^{\mathrm{p}}$ represents the change of the voltage in the stage p due to the charge transference, and is in the form of

$$\mathbf{\Delta v^p} = \begin{bmatrix} \Delta v_{\text{in}}^p & \mathbf{\Delta v_C^p}^{\mathbf{T}} & \mathbf{\Delta v_L^p}^{\mathbf{T}} & \Delta v_{\text{o}}^p \end{bmatrix}^T \tag{69}$$

where $\Delta v_{\text{in}}^p = \Delta v_o^p = 0, \mathbf{\Delta v_C^p}$ and $\mathbf{\Delta v_L^p}$ are the vectors of the capacitors voltage change and the inductors voltage change in the stage p

$$\mathbf{\Delta v_C^p} = \begin{bmatrix} \Delta v_{C1}^p & \Delta v_{C2}^p & \cdots \end{bmatrix}^T \tag{70}$$

$$\mathbf{\Delta v_L^p} = \begin{bmatrix} \Delta v_{L1}^p & \Delta v_{L2}^p & \cdots \end{bmatrix}^T. \tag{71}$$

By manipulating (67) and (68), the KVL constrains in the stage p yield

$$\mathbf{A_p \Delta v^p} = \mathbf{0}. \tag{72}$$

Due to the charge balance of capacitors, the vector of capacitors voltage ripple $\Delta \mathbf{v_C}$ is obtained

$$2\mathbf{\Delta v_C} = \left|\mathbf{\Delta v_C^1} + \mathbf{\Delta v_C^2}\right| = \left|\mathbf{\Delta v_C^3}\right|. \tag{73}$$

The charge flow vector of capacitors derived by the KCL analysis is defined as

$$\mathbf{q_C} = \begin{bmatrix} q_{C1} & q_{C2} & \cdots \end{bmatrix}^T. \tag{74}$$

The $q_{C1},_2$ are the net charge flowing into $C_{1,2}$. Then, the capacitance vector is defined as

$$\mathbf{C} = \begin{bmatrix} C_1 & C_2 & \cdots \end{bmatrix}^{\mathbf{T}}. \tag{75}$$

The capacitance of capacitor C_i is calculated by

$$C_i = q_{\mathrm{C}i} / 2\Delta v_{\mathrm{C}i} \tag{76}$$

where $\Delta v_{\mathrm{C}i}$ is the voltage ripple in the capacitor i.

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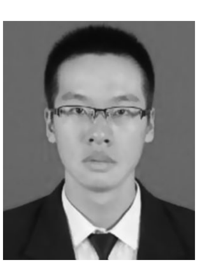

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