A Dual-Active-Bridge-Based Fully ZVS HF-Isolated Inverter With Low Decoupling Capacitance

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***Abstract*—This paper proposes a novel dual active bridge (DAB)-based high-frequency-isolated dc–ac converter topology suitable for photovoltaic microinverter applications. The circuit configuration on the secondary sides of the employed three-winding transformer results in high-frequency current injection into each of the switch nodes, thereby making zero-voltage-switching (ZVS) operation of the devices possible. The topology achieves this functionality while using the same number of devices as conventional two-stage and single-stage high-frequency-link or DAB-based solutions. Furthermore, following a control-oriented power pulsation decoupling strategy involving dynamic variation of phase shift, twice line-frequency energy buffering can be handled on the high-voltage secondary side, thereby resulting in reduction in decoupling capacitance requirement. The working principle of the circuit and the associated control scheme is described followed by a detailed ZVS analysis. Simulation studies and experimental tests on a 310 W prototype verify circuit operation and exhibit efficiency improvements compared to a similar two-stage solution.**

***Index Terms*—Dual active bridge (DAB), microinverter, power decoupling, zero-voltage switching (ZVS).**

I. Introduction

HIGH-FREQUENCY (HF) transformer-isolated single-phase inverter topologies employed in applications such as photovoltaic (PV) and fuel-cell inverters can be broadly classified as single-stage or multistage. The flyback inverter [2], [3] is the simplest single-stage solution with advantages of low device count and cost. However, it has demerits such as output distortion for continuous conduction mode operation, high rms currents and turn-off losses in the discontinuous conduction mode, and hard switching of devices [2].

HF ac-link-based architectures represent another category of single-stage isolated topologies and can be further classified into two types. In the first type [4], [5], an HF square wave or quasi-square wave generated by a primary-side inverter is appropriately modulated by a secondary-side cycloconverter with the objective of rendering a line-frequency sinusoidal profile to the current of an output inductive filter. The major advantages of this approach are its nonreactive power processing and zero-voltage-switching (ZVS) operation of the devices. But a critical concern with this topology is the voltage spike appearing across the secondary-side devices, which necessitates the use of auxiliary voltage clamping circuits. The second category of HF link-isolated topologies [6], [7] is structurally similar to the first type with the exception that the output filter is capacitive and a resonant or inductive network is present in series with the transformer. Operationally, these circuits function like the dc–ac dual-active-bridge (DAB) converter [8], wherein the power flow is regulated by phase-shift control. Advantages of this approach include the absence of turn-off voltage spikes across the switches and natural ZVS operation of the switches.

A major shortcoming of the aforementioned single-stage topologies is that there is no inherent power decoupling arrangement to account for the mismatch between the steady input dc power and the pulsating output ac power. Thus, a prohibitively high value of decoupling capacitance [9] is necessary, entailing the use of low-lifetime electrolytic capacitors. Reduction in decoupling capacitance requirement is possible by introducing additional energy buffer circuitry, as in [10] and [11]; however, this increases circuit complexity.

Multistage topologies perform the task of dc–ac conversion in two or more stages—typically, a front-end isolated dc–dc converter is responsible for voltage boosting, while a cascaded inverter synthesizes the line-frequency output. Depending on the operation of the dc–dc stage, the inverter stage may be line-frequency commutated, as in [12] and [13], or consist of an HF pulsewidth-modulated (PWM) inverter, as in [14] and [15]. Such topologies are easier to control and allow easy power decoupling to be affected via the high-voltage secondary-side dc-bus capacitor [15], allowing the use of low-value long-lifetime film capacitors. However, they suffer from high device count and low efficiency on account of the cascaded power conversion process. Moreover, for the line-frequency inverter-based solution, the dc–dc converter has to be rated for a peak power of twice the nominal power [9], while for the PWM-inverter-based solution, the MOSFETs of the inverter stage do not undergo ZVS over half of the output line cycle. While classical solutions like the resonant dc-link (RDCL) inverter [16] or the auxiliary resonant commutated pole (ARCP) inverter [17] or their modifications

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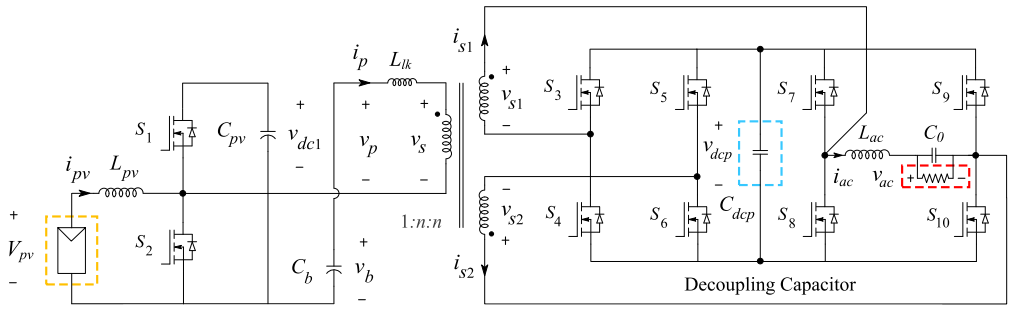

Fig. 1. Proposed inverter topology in a stand-alone configuration. The topological configuration on the secondary side helps in realizing ZVS.

[18]–[21] can be adopted to achieve ZVS operation of the PWM inverter, the auxiliary commutation circuitry used therein increases circuit complexity. Additionally, the RDCL approach increases voltage and current ratings of the main devices, while the ARCP technique has its own challenges, such as voltage imbalance of split capacitors, difficulty in auxiliary gating control, and possible overvoltage across the auxiliary devices [18], [19].

This paper proposes a new HF-isolated PV inverter topology, which combines the aforementioned advantages of conventional HF link and two-stage solutions, viz., ZVS operation of all devices and the presence of an inherent power decoupling arrangement. The topology, depicted in Fig. 1, works according to the DAB principle and requires the same number of devices as comparable HF link and two-stage converters. The topological arrangement of the secondary-side switches ensures that each secondary-side switch node is connected to a terminal of the HF transformer, which helps in realizing ZVS. By dynamically varying the phase shift between transformer primary and secondary voltages, it is possible to completely handle the active power decoupling operation through the high-voltage secondary-side dc-bus capacitor, enabling a film-capacitor-based implementation. In the following sections, the operation of the circuit is explained, followed by its steady-state analysis, a discussion on the closed-loop control scheme, and detailed ZVS analysis. Finally, simulation and experimental results are presented to illustrate circuit operation and highlight the advantages of the topology.

II. Proposed Topology

A. Topology Description and Derivation

As shown in Fig. 1, the PV port is connected to the primary winding of a three-winding HF transformer using an integrated-boost half-bridge interface [22] and an external series inductor $L_{\rm lk}$. This structure offers the benefits of boosting the low input voltage and presenting a current–stiff input interface. The half-bridge $S_1 - S_2$ is operated with a fixed duty ratio D_1 (of the top switch) under the steady state. From the volt–second balance of $L_{\rm pv}$, the average voltage across capacitor $C_{\rm pv}$ is obtained as

$$V_{\rm dc1} = V_{\rm pv}/D_1. \tag{1}$$

Furthermore, from the volt–second balance of the leakage inductor $L_{\rm lk}$, it is evident that the average value of v_b under the steady state is equal to $V_{\rm pv}$. It follows that on switching the half-bridge $S_1 - S_2$, a zero-mean rectangular voltage waveform v_p with positive and negative values of $V_{\rm pv}$ and $-V_{\rm pv}(1 - D_1)/(D_1)$, respectively, is impressed on the primary side of the transformer.

The conceptual evolution of the topological configuration on the secondary side is explained in Fig. 2. Fig. 2(a) depicts a hard-switched PWM full-bridge inverter cell, whose switches miss ZVS over half the line cycle. This is because the direction of the line-frequency current flowing in/out of the switch nodes (A and B) violates the necessary condition for ZVS of each switch for half of the ac line cycle. With the intention of realizing ZVS of one of the legs (S_7 and S_8), it is imagined in Fig. 2(b) that one of the secondary terminals (T_3) of an HF transformer is connected to switch node A. Since the basic function of the inverter cell is to synthesize an HF voltage across terminals A and B, whose average switching period has a low-frequency sinusoidal variation, it is evident that the other switch node B cannot be connected to the remaining secondary terminal (T_4). Hence, in order to obtain ZVS of the second inverter leg ($S_9 - S_{10}$), a third winding is introduced, one of whose terminals (T_5) is connected to switch node B, as shown in Fig. 2(c). To complete the configuration, two auxiliary legs ($S_3 - S_4$, $S_5 - S_6$) are introduced in Fig. 2(d), whose switch nodes are connected to the remaining transformer terminals (T_4 and T_6). The conceptual development is completed by adding an HF ac voltage source v_p in series with an inductor on the primary side, as shown in Fig. 2(e). In the present circuit, v_p is synthesized by the boost half-bridge interface, which leads to the final form of Fig. 1.

B. Generation of Switching Signals

Assuming that the main load bridge on the secondary side ($S_7 - S_{10}$) is operated with unipolar sine-PWM modulation, switching signals for its top devices are given by

$$S_7 = \text{sgn}\left\{\frac{1}{2} + M\sin\omega t - \text{tri}(t)\right\} \tag{2}$$

$$S_9 = \text{sgn}\left\{\frac{1}{2} - M\sin\omega t - \text{tri}(t)\right\} \tag{3}$$

where $\text{sgn}(x) = 1$ for $x \geq 0$ and is 0 otherwise. The amplitude modulation index is denoted by M ($0 < M < 0.5$), ω is the angular grid frequency, and $\text{tri}(t)$ represents the triangular carrier wave (at switching frequency). Generation of switching signals

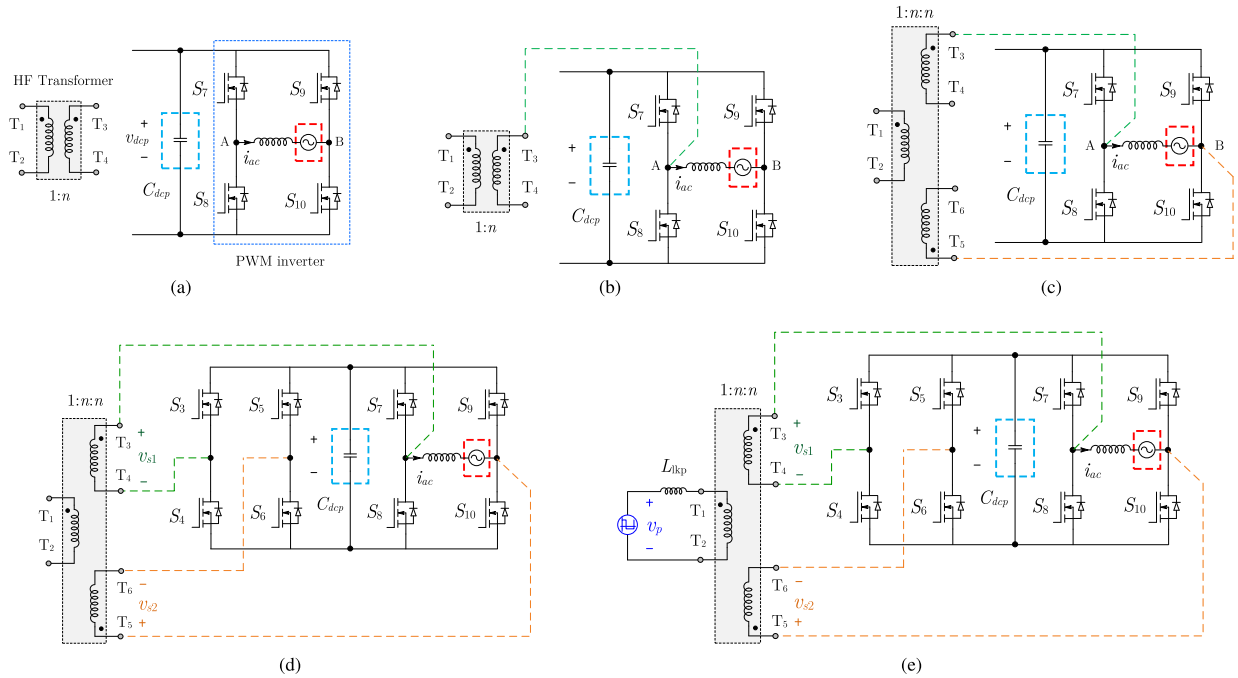

Fig. 2. Explaining conceptual evolution of the proposed topology. (a) PWM inverter cell. (b) Connecting one terminal (T_3) of an HF transformer to one of the switch nodes (A) of the inverter to help with ZVS. Note that the other switch node (B) cannot be connected to the other terminal (T_4), as it would lead to a nonzero switching-period average voltage being impressed across the winding. (c) Inclusion of a third winding, one of whose terminals (T_5) is connected to the other switch node. (d) Inclusion of two auxiliary legs (S_3, S_4 and S_5, S_6), whose switch nodes are connected to the remaining transformer terminals (T_4, T_6). (e) Addition of an HF ac voltage source in series with an inductor on the primary side.

TABLE I
EXPLAINING GENERATION OF THE SWITCHING SIGNALS. HIGH-SIDE SECONDARY SWITCHES CONNECTED TO THE SAME SECONDARY WINDING (S_3, S_7 AND S_5, S_9) HAVE THE SAME MODULATION SIGNAL TO ENSURE ZERO AVERAGE OF VOLTAGES IMPRESSED ACROSS THE SECONDARY WINDINGS

	S_1	S_3	S_5	S_7	S_9
Modulation signal	D_1	1/2 +$M \sin \omega t$	1/2 -$M \sin \omega t$	1/2 +$M \sin \omega t$	1/2 -$M \sin \omega t$
Carrier signal	$tri(t + d_\phi T_s)$	$tri(t + T_s/2)$	$tri(t + T_s/2)$	$tri(t)$	$tri(t)$

for S_3–S_6 (designated as the nonload bridge) is based on ensuring volt–second balance of the transformer over a switching period (T_s). This can be done by simply ensuring that the modulating signals for S_3 and S_7 and that of S_5 and S_9 are same. Though satisfaction of the volt–second balance criterion is independent of the phase relationship among the carrier signals of S_3 and S_7 and that of S_5 and S_9, a phase shift of $T_s/2$ is chosen. It can be shown that any other phase shift would lead to mismatch between the instantaneous values of v_{s1} and v_{s2}, leading to circulating currents. Thus, the switching signals for S_3 and S_5 are given by (4) and (5), respectively:

$$S_3 = \text{sgn}\left\{\frac{1}{2} + M\sin\omega t - \text{tri}\left(t + \frac{T_s}{2}\right)\right\} \tag{4}$$

$$S_5 = \text{sgn}\left\{\frac{1}{2} - M\sin\omega t - \text{tri}\left(t + \frac{T_s}{2}\right)\right\}. \tag{5}$$

A summary of the modulation and carrier signals needed for generating different switching functions is provided in Table I. It may be noted that the carrier signal of the PV half-bridge is phase-advanced by $d_\phi T_s$ relative to the secondary-side carrier signals. This is required for the power flow to occur in the intended direction, as will be explained subsequently.

Switching signals of the secondary-side devices and the synthesized HF voltage waveforms v_{s1} and v_{s2} for $d(t)(= 1/2 + M\sin\omega t) > 0.5$ and $d(t) < 0.5$ are depicted in Fig. 3(a) and (b), respectively, which correspond to the positive and negative portion of the ac line cycle, respectively. It can be observed that in both cases, identical PWM quasi-square wave voltages are impressed across the two secondary windings, with the duration w of the powering (nonzero) states being given by $(1 - d(t))T_s$ and $d(t)T_s$ for $d(t) > 0.5$ and $d(t) < 0.5$, respectively. Thus, in general, w varies as

$$\begin{aligned} w &= \min\{d(t), 1 - d(t)\}.T_s \\ &= \alpha T_s, \text{where} \alpha = (1/2 - M|\sin\omega t|)\,. \end{aligned} \tag{6}$$

C. Steady-State Analysis

As explained in the previous section, a fixed duty-ratio rectangular voltage v_p and a PWM quasi-square-wave voltage v_s' are impressed on either side of the leakage inductor in series with the transformer's primary winding. Hence, following the DAB

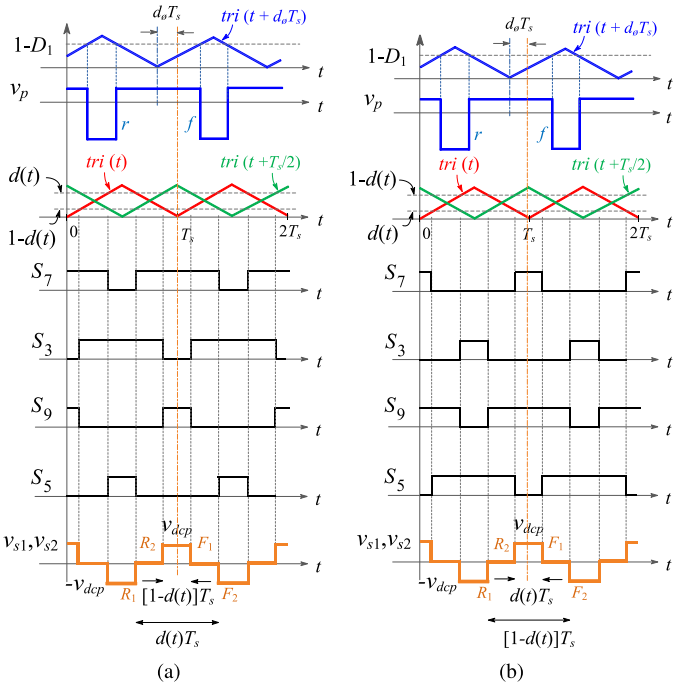

Fig. 3. Key HF waveforms explaining circuit operation. $d(t) = 1/2 + M \sin \omega t$ is the instantaneous duty ratio of the switches S_3 and S_7. The pulsewidth of v_{s1} and v_{s2} varies as $(1/2 - M|\sin \omega t|)T_s$. (a) For positive ac line cycle, $d(t) > 0.5$. (b) For negative ac line cycle, $d(t) < 0.5$.

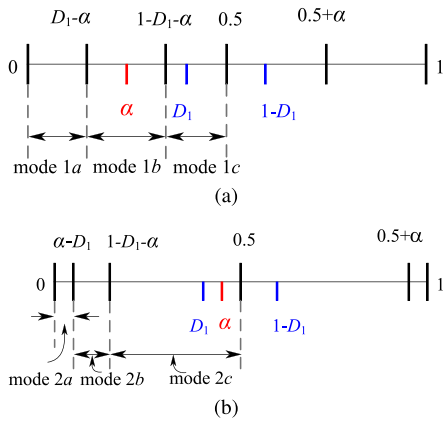

Fig. 4. Range of $2d_\phi$ defining different modes of operation for $D_1 < 0.5$. (a) Modes 1a–1c ($0 < \alpha < D_1 < 0.5 < 1 - D_1 < 0.5 + \alpha$). (b) Modes 2a–2c ($0 < D_1 < \alpha < 0.5 < 1 - D_1 < 0.5 + \alpha$). Similar modes exist for $D_1 > 0.5$. For the simple case of $D_1 = 0.5$, only modes 1a and 1c exist.

principle, the power flow from the primary to the secondary side can be achieved by simply ensuring that v_p is phase-advanced with respect to v_s'.

Depending on the relative values of the phase-shift duty ratio d_ϕ (defined as the angle between the fundamental of v_p and fundamental of v_s', normalized to 2π radians), the duty ratio D_1 of the dc-side half-bridge, and the instantaneous pulsewidth αT_s of v_s', six operating modes are possible for $D_1 < 0.5$. Conditions for operation in each mode are pictorially represented in Fig. 4. Similar modes can be defined for $D_1 > 0.5$; however, these are found to result in high transformer current and also loss of ZVS of the primary-side devices and, hence, ignored. Similarly, it

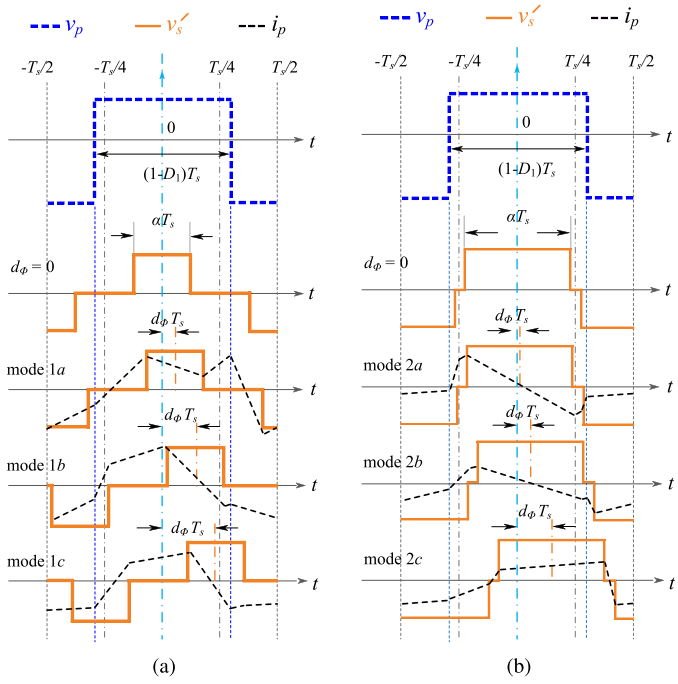

Fig. 5. Representative waveforms of v_p, v_s', and i_p for operation in HF modes 1 and 2. (a) Modes 1a, 1b, and 1c. (b) Modes 2a, 2b, and 2c.

may be noted that the modes are defined such that the maximum value of the phase shift D_ϕ is 0.25. This is because D_ϕ is always limited to be below 0.25, since operation beyond 0.25 results in higher rms currents [23]. Timing diagrams illustrating representative waveforms of v_p, v_s', and i_p for modes 1 and 2 and their submodes are depicted in Fig. 5, where, for ease of representation, the same value of α has been assumed in all three submodes.

It may be observed from Fig. 4 that for the simple case of square-wave operation on the primary side ($D_1 = 0.5$), only modes 1a and 1c exist. However, even in such a simple case, the continuously changing value of α over a line cycle causes circuit operation to periodically move back and forth between these modes. Hence, an exact time-domain steady-state analysis of converter operation presents considerable difficulty. To circumvent this, a fundamental-harmonic-analysis-based approach is adopted. Fig. 6(b) shows the approximate equivalent circuit of a three-winding transformer [24], where X_{lkp}, X_{lks1}, and X_{lks2} are the leakage reactances of the primary and the two secondary windings, respectively. Assuming that $X_{\text{lks1}} = X_{\text{lks2}}$ and since $v_{s1} = v_{s2}$, the circuit can be reduced to its Thevenin equivalent form of Fig. 6(d). The fundamental components of v_p and v_s are given by (7) and (8), respectively [25]:

$$v_{p1} = \frac{2V_{\text{pv}}}{\pi D_1} \sin((1 - D_1)\pi) \cos(\omega_s t) \tag{7}$$

$$v_{s1} = \frac{4v_{\text{dcp}}}{\pi} J_0(\pi M) \cos(\omega_s t - \delta_{\text{av}}) \tag{8}$$

where $\delta_{\text{av}} = 2\pi D_\phi$ is the average phase shift in radians, J denotes the Bessel function of first kind, and M is the amplitude modulation index, as before. The following approximate expressions for average power and rms value of transformer primary

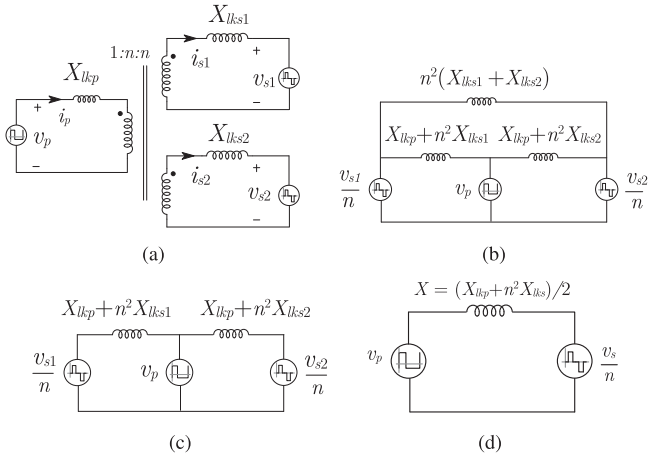

Fig. 6. Steps in the development of the simplified equivalent circuit. (a) Simplified actual circuit. (b) Equivalent circuit. (c) Effective equivalent circuit. (d) Simplified equivalent circuit.

current can then be obtained as

$$P_{\text{av}} \approx v_{p1}\left(\frac{v_{s1}}{n}\right)\left(\frac{1}{X}\right)\sin\delta_{\text{av}} \tag{9}$$

$$i_{p(\text{rms})} \approx \left(\frac{1}{X}\right)\sqrt{{v_{p1}}^2 + \left(\frac{v_{s1}}{n}\right)^2 - 2v_{p1}\frac{v_{s1}}{n}\cos\delta_{\text{av}}} \tag{10}$$

where $X = 2\pi L_{\text{lk}} f_s$, and v_{p1} and v_{s1} are the rms values of the fundamental components of primary and secondary voltages, respectively.

D. Control Scheme

In standard closed-loop implementation in a stand-alone mode, the phase shift is controlled by a PI controller, which regulates the average value of the dc-bus voltage $v_{\text{dc}p}$ at a desired reference $V_{\text{dc}p(\text{ref})}$. Typically, the controller is designed to have a very low gain at 100 Hz ($2f_0$) [26], implying that the resulting phase shift is practically constant. As illustrated in Fig. 7(a), such a control scheme results in variation of power transferred over successive HF switching cycles, on account of the sinusoidal modulation of the pulsewidth of v_s'. This would ultimately result in double-line-frequency power pulsations being transmitted to the primary side.

The key idea behind the adopted control-oriented power-decoupling approach is explained in Fig. 7(b). As the pulsewidth of v_s' diminishes near the ac cycle peaks and, consequently, its fundamental amplitude reduces, the phase shift is correspondingly increased so as to achieve the same average power flow in successive HF switching cycles. The primary side is now completely decoupled from low-frequency power pulsations, and the energy buffering is now affected via the secondary-side dc-bus capacitor. As both the average and the peak–peak ripple values of the voltage across this capacitor is much higher (compared to the case when the decoupling capacitor is placed across the module), it leads to considerable reduction in the required value of decoupling capacitance, implying that low-valued film capacitors can be used.

The implementation strategy for realizing power decoupling control is depicted in Fig. 8. The scheme, which is similar

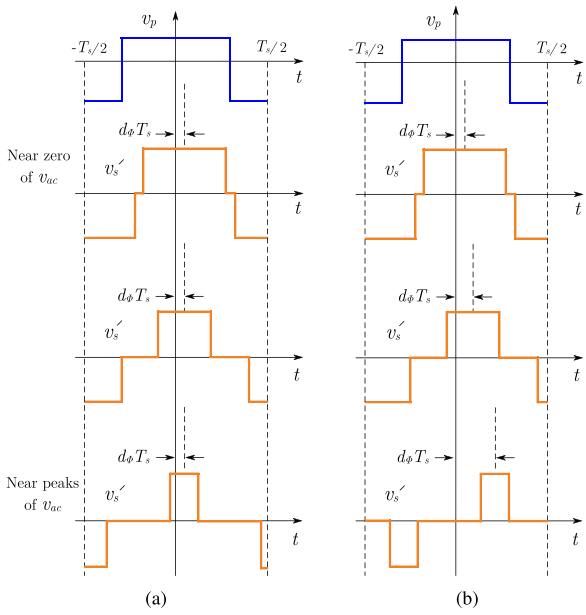

Fig. 7. Principle behind the power decoupling approach. (a) Operation with a constant phase shift d_ϕ leads to variation in power in successive switching cycles. (b) Phase shift d_ϕ is dynamically changed to keep the average power (over T_s) constant. The phase shift is increased near the ac line cycle peaks, where the magnitude of the fundamental of v_s' is reduced.

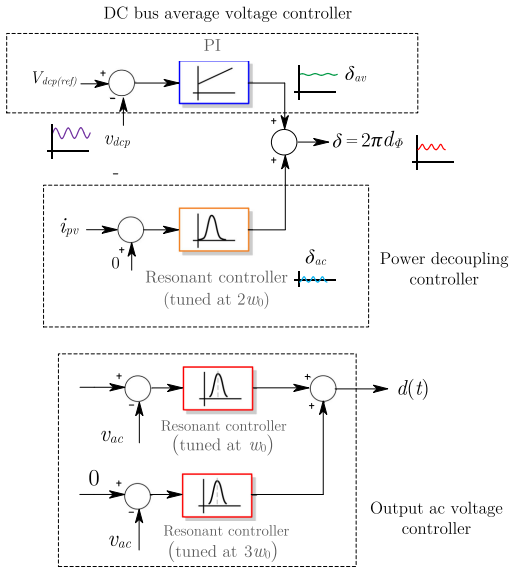

Fig. 8. Overall control architecture including the dc-bus average voltage controller, the power decoupling controller, as in [15], and the output ac voltage controller with a third harmonic rejection block for compensating the effect of a substantial $2\omega_0$ component of the dc-bus voltage.

to the approach outlined in [15], uses two controllers, which contribute different portions of the final phase-shift signal. The almost-constant first part (δ_{av}) is obtained from a PI controller regulating the average dc-bus voltage. A second component (δ_{ac}) of the phase shift comes from a resonant controller, whose goal is to completely eliminate $2f_0$ oscillations in i_{pv}. Since this paper chiefly focuses on the operational and design aspects of the proposed topology, a quantitative control-loop design, as in [28], has not been performed. Instead, a heuristic approach toward the controller design is followed, which is found to result

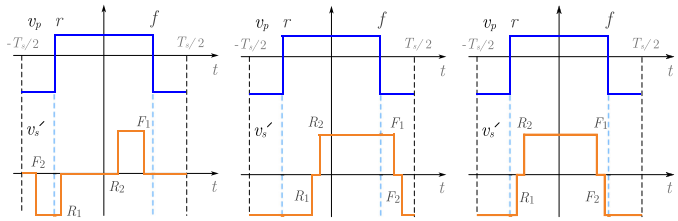

Fig. 9. Different HF modes relevant for ZVS analysis. (a) Mode 1b, which occurs near ac line cycle peaks is used for analyzing ZVS of the secondary-side devices. (b) Mode 2a and (c) mode 2c occur near zero crossings and are used for ZVS analysis of the primary-side devices.

in satisfactory closed-loop performance in extensive simulation studies and experimental tests.

III. ZVS Analysis

In this section, the necessary conditions for ZVS operation of the switches are analytically derived. For ease of analysis, resistive drops of the switches and transformer windings as well as the switching ripple of $v_{\rm dc1}$, $v_{\rm dcp}$, and $i_{\rm ac}$ are ignored. Furthermore, the preliminary analysis presented next considers a unity-power-factor (pf) load.

In general, the circuit can operate in any one of the six HF modes depicted in Fig. 5. However, for the purpose of ZVS analysis, operation in only three modes, depicted in Fig. 9, needs to be considered. For the secondary-side devices, the worst-case condition for ZVS operation occurs near the peaks of $v_{\rm ac}$, where the circuit is found to work in mode 1b. This is intuitively evident from Fig. 5, which shows that operations both near the peaks of $v_{\rm ac}$ and in mode 1b correspond to low values of α. Similarly, the primary-side devices are most likely to miss ZVS operation near the zero crossings of $v_{\rm ac}$, where the circuit operates in mode 2a or 2c with $\alpha \approx 0.5$.

As the next step of the analysis, switches turning ON at different rising and falling edges of v_p and v_s' are identified. The rising and falling edges of v_p, denoted by r and f, respectively, in Fig. 9, correspond to the turn-on of S_2 and S_1, respectively. Secondary switches turning ON at the four transitions of v_s' (R_1, R_2, F_1, F_2) can also be identified by referring to Fig. 3. A summary of these observations for operation in mode 1b is presented in Table II. As can be noted, at each of the R_1 and R_2 transitions, one of the top switches of the load-bridge (S_7/S_9) turns ON simultaneously with one of the bottom switches of the nonload bridge (S_4/S_6). Similarly, at each of the F_1 and F_2 transitions, one of the bottom switches of the load-bridge (S_8/S_{10}) and one of the top switches of the nonload bridge (S_3/S_5) turn ON simultaneously. Furthermore, recognizing that ZVS turn-on of any switch implies a negative initial current through it, necessary conditions for ZVS operation of the switches may be formulated. These conditions are also listed in Table II, where $i_{\rm pv(min)}$ and $i_{\rm pv(max)}$ refer to the minimum and maximum values of $i_{\rm pv}$, respectively, considering its switching ripple, and i_{s1} and i_{s2} denote the two secondary winding currents, which are assumed to be equal and given by

$$i_{s1} = i_{s2} = i_p/(2n). \tag{11}$$

TABLE II
Switches Turning ON at the Different Transitions in Mode 1b and the Corresponding Necessary Conditions for ZVS Turn-on

		$i_{ac} > 0$		$i_{ac} < 0$
Edge	Switch	ZVS condition	Switch	ZVS condition
r	S_2	$-i_p(r) > i_{pv(min)}$	Same as $i_{ac} > 0$	
f	S_1	$-i_p(f) < i_{pv(max)}$	Same as $i_{ac} > 0$	
R_1	S_7	$i_{s1}(R_1) > i_{ac}$	S_9	$i_{s2}(R_1) > -i_{ac}$
	S_6	$i_{s2}(R_1) > 0$	S_4	$i_{s1}(R_1) > 0$
R_2	S_9	$i_{s2}(R_2) > -i_{ac}$	S_7	$i_{s1}(R_2) > i_{ac}$
	S_4	$i_{s1}(R_2) > 0$	S_6	$i_{s2}(R_2) > 0$
F_1	S_{10}	$i_{s2}(F_1) < -i_{ac}$	S_8	$i_{s1}(F_1) < i_{ac}$
	S_3	$i_{s1}(F_1) < 0$	S_5	$i_{s2}(F_1) < 0$
F_2	S_8	$i_{s1}(F_2) < i_{ac}$	S_{10}	$i_{s2}(F_2) < -i_{ac}$
	S_5	$i_{s2}(F_2) < 0$	S_3	$i_{s1}(F_2) < 0$

A. ZVS Condition for Secondary-Side Switches

As can be noted from Table II, at each of the four secondary transitions, two switches turn ON simultaneously. The ZVS condition of one of these two switches is more stringent than the other, e.g., for the R_1 transition for $i_{\rm ac} > 0$, if the ZVS condition of S_7 is satisfied, that of S_6 is evidently satisfied, and hence, S_7 is more critical vis-a-vis ZVS occurrence. Similarly, it may be concluded that for the R_2 transition for $i_{\rm ac} > 0$, S_4 is more critical. Further simplification of the analysis is made possible by observing from Fig. 9 that the slope of the transformer current in the $R_1 - R_2$ duration is positive, and hence, $i_{s1(R_1)} > i_{s1(R_2)}$. This implies that between S_4 and S_7, the ZVS condition of S_7 is more stringent. In summary, for $i_{\rm ac} > 0$, ZVS of S_7 ensures ZVS of S_4, S_6, and S_9, and the simplified ZVS condition is given by $i_{s(R_1)} > i_{\rm ac}$. Similarly, it may be shown that for $i_{\rm ac} < 0$, ZVS of S_9 ensures ZVS of the remaining three devices switching at the R_1 and R_2 transitions, which leads to the same ZVS constraint of $i_{s(R_1)} > |i_{\rm ac}|$. In summary, for the R_1 and R_2 transitions, the top switches of the load-side bridge are most critical for ZVS turn-on, and the simplified condition ensuring ZVS of all commutating devices is given by $i_{s(R_1)} > |i_{\rm ac}|$.

Using similar arguments, it may be concluded that the simplified ZVS conditions for the F_1 and F_2 transitions are given by $i_{s(F_1)} < -|i_{\rm ac}|$ and $i_{s(F_2)} < 0$, respectively. Unlike the R_1 and R_2 transitions, however, it is not possible, in general, to identify a single transition among F_1 and F_2 as more stringent for ZVS occurrence. Hence, recalling that the worst-case condition for ZVS of the secondary devices occurs near the line cycle peaks, the ZVS constraints for the secondary-side devices may be summarized as

$$i_{s(R_1)} > |i_{\rm ac(pk)}|,\ i_{s(F_1)} < -|i_{\rm ac(pk)}|,\quad i_{s(F_2)} < 0. \tag{12}$$

Closed-form expressions of the corner values of the transformer primary current (i_p) are listed in Table III. Using these expressions and (9), the conditions for ZVS occurrence at R_1/R_2,

TABLE III
EXPRESSIONS FOR THE CORNER VALUES OF i_p IN MODE 1b

Current	Expression
$i_p(r)$	$C[(v_{dcp}/n)(D_1-2d_\phi)-V_{pv}D_1']$
$i_p(R_1)$	$C[(v_{dcp}/n)\alpha-V_{pv}(1-\alpha-2d_\phi)]$
$i_p(R_2)$	$C[(v_{dcp}/n)\alpha-V_{pv}(\alpha-2d_\phi)]$
$i_p(F_1)$	$C[-(v_{dcp}/n)\alpha+V_{pv}(\alpha+2d_\phi)]$
$i_p(f)$	$C[-(v_{dcp}/n)\alpha+V_{pv}D_1']$
$i_p(F_2)$	$C[-(v_{dcp}/n)\alpha+V_{pv}(D_1'/D_1)(\alpha-2d_\phi)]$

Expression for $i_p(r)$ in modes 2a and 2c are the same as that in mode 1b. $C=1/(2L_{\rm lk}f_s)$, $D_1'=1-D_1$.

F_1, and F_2 can be, respectively, expressed as

$$n < n_{\text{sec(crit1)}} = \frac{\alpha_{\min}V_{\rm dcp}}{(1-\alpha_{\min}-2D_\phi))V_{\rm pv}+V_K} \tag{13a}$$

$$n < n_{\text{sec(crit2)}} = \frac{\alpha_{\min}V_{\rm dcp}}{(\alpha_{\min}+2D_\phi))V_{\rm pv}+V_K} \tag{13b}$$

$$n < n_{\text{sec(crit3)}} = \frac{\alpha_{\min}D_1V_{\rm dcp}}{(\alpha_{\min}-2D_\phi))(1-D_1)V_{\rm pv}} \tag{13c}$$

where $\alpha_{\min}=(1/2-M)$, and V_K is a constant equal to $(2\sqrt{2}/\pi)v_{p1}v_{s1}\sin(2\pi D_\phi)/v_{\text{ac(rms)}}$. The final value of n, which satisfies all the above conditions and thus ensures ZVS of all the secondary devices across the line cycle, is given by

$$n < \min\left\{n_{\text{sec(crit1)}}, n_{\text{sec(crit2)}}, n_{\text{sec(crit3)}}\right\}. \tag{14}$$

Though the above conditions represent the design guidelines for a generic case, for the specific operating conditions of the converter considered in this paper (provided in the next section), a more simplistic condition can be obtained. Both theoretical analysis and simulation studies can be used to show that for the adopted design specifications, the ZVS conditions for the top switches of the load-bridge are most stringent. Thus, the condition for achieving ZVS of all of the ac-side switches across the line cycle is given by

$$i_{s(R_1)} > |i_{\text{ac(pk)}}| \tag{15}$$

and the corresponding design condition on the turns ratio is simply expressed by (13a).

B. ZVS Condition for Primary-Side Switches

For analyzing ZVS of the primary-side switches, only the bottom switch S_2 is considered, since its ZVS condition is found to be more stringent. Formulation of the ZVS criterion is made simple by the fact that the expression of $i_{p(r)}$ is the same in modes 1b and 2a/2c (which are relevant for analyzing ZVS of the primary devices). Hence, using Tables II and III, the ZVS criterion for the primary-side devices is obtained as

$$n > n_{\text{pri(crit)}} = \frac{(D_1-2D_\phi)V_{\rm dc}+V_K'}{(1-D_1)(1+L_{lk}/L_{\rm pv})V_{\rm pv}} \tag{16}$$

TABLE IV
PARAMETER VALUES FOR THE SIMULATION MODEL

V_{ac}	$P_{av}(max)$	V_{pv}	L_{pv}	C_{pv}	L_{in}	C_{in}
110 V rms	310 W	25-35 V	140 μH	20 μF	40 μH	44 μF
C_b	Turns-ratio	L_{lkp}	f_s	C_{dcp}	L_f	C_f
40 μF	1:2.13:2.13	60 μH	25 kHz	40 μF	3.5 mH	2.2 μF

where $V_k'=(v_{p1}v_{s1}/\pi)\sin(2\pi D_\phi)$. Combining (14) and (16), it may be concluded that for $n_{\text{pri(crit)}} < n < n_{\text{sec(crit)}}$, ZVS turn-on of both primary and secondary devices can be realized.

C. ZVS Analysis for Nonunity-Power-Factor Load

Present-day microinverters are often required to be able to supply reactive power to the grid, if needed [29], [30]. Hence, the ZVS capability of the circuit for operation with a nonunity-pf load also needs to be explored.

As shown in Table II, ZVS conditions of the dc-side switches are not dependent on $i_{\rm ac}$ and are, thus, evidently not affected by the pf load. Conditions for the ac-side switches, on the other hand, are clearly dependent on $i_{\rm ac}$. Furthermore, since the peaks of $v_{\rm ac}$ and $i_{\rm ac}$ do not occur at the same time for nonunity-pf operation, the previously derived ZVS conditions should be re-evaluated. For this analysis, the unity- and nonunity-pf loads are considered to be of the same (rms or peak) current rating.

As with unity-pf operation, even in the nonunity-pf case, the top switches of the load bridge are the most critical for ZVS, and thus, the fundamental condition for satisfying ZVS is given by (15). Neglecting the line-cycle variations of $v_{\rm dcp}$ and d_ϕ for simplicity of analysis, from Table III, it is clear that the value of $i_{s(R_1)}$ depends linearly on α and decreases as α decreases. From (6), it may be seen that α is minimum at the peaks of $v_{\rm ac}$, and correspondingly, $i_{s(R_1)}$ is also minimum there. This explains why the ZVS conditions for S_7 are most stringent at the peaks of $v_{\rm ac}$ for unity-pf operation. For nonunity-pf operation (both capacitive and inductive loads), the instantaneous value of $i_{\rm ac}$ at the peaks of $v_{\rm ac}$ is lower than its peak value. This implies that if the circuit can operate with ZVS of the ac switches for unity-pf load, it is certain to do the same with a nonunity-pf load of the same current rating, since the value of $i_{s(R_1)}$ at the corresponding peak of $i_{\rm ac}$ will definitely satisfy (15).

IV. SIMULATION RESULTS

A simulation model of the proposed topology, with specifications listed in Table IV, has been developed in PLECS. Components $L_{\rm in}$ and $C_{\rm in}$ noted in the table refer to an HF filter added at the input port to attenuate switching ripple in the input current. The results shown correspond to the nominal operating condition of $V_{\rm pv}=30$ V, $P_{\rm av}=200$ W, $D_1=0.2$, and $V_{\rm dcp}=300$ V and for operation with a resistive load, unless otherwise mentioned. The transformer turns ratio of 2.13 is chosen so as to satisfy the ZVS constraints of (14) and (16) under this operating condition. The value of 40 μF for the decoupling capacitor $C_{\rm dcp}$

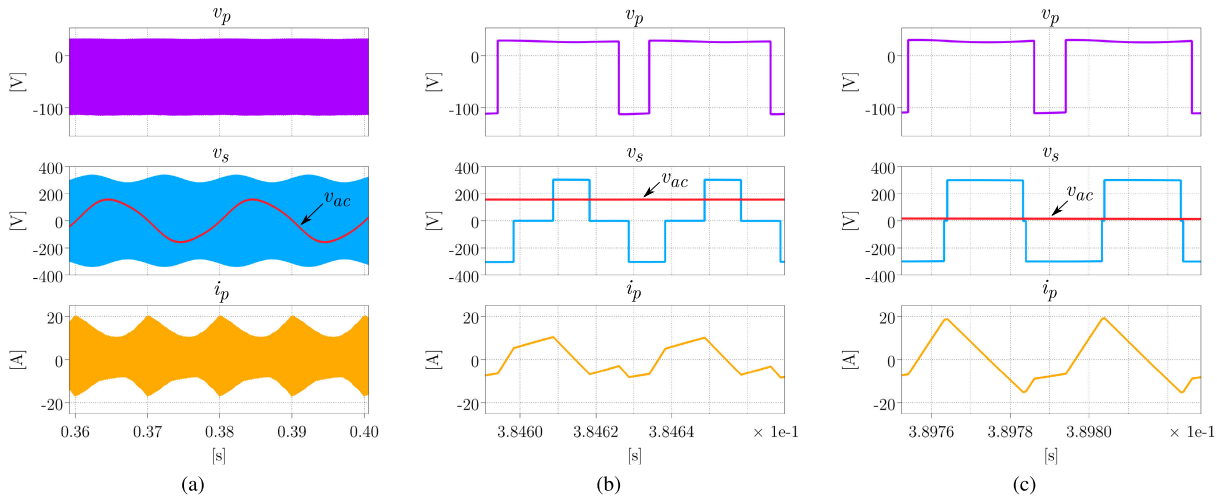

Fig. 10. Transformer voltage and current waveforms (a) over the full line cycle and (b) near peak of output ac line cycle. Operation corresponds to mode 1b and (c) near zero crossing of output ac line cycle. Operation corresponds to mode 2a.

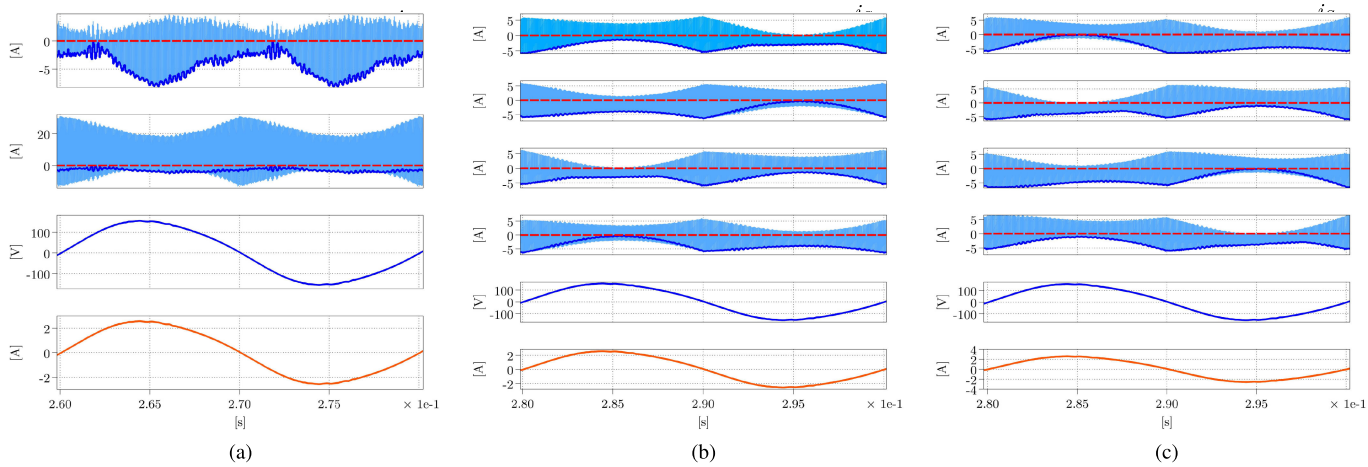

Fig. 11. Occurrence of ZVS for all switches over the full 50-Hz cycle for a unity-pf load. (a) Primary-side and (b) secondary-side switches not directly connected to the load. (c) Secondary-side switches directly connected to the load. The instantaneous current through the switches (light blue) and the current at the turn-on instant (dark blue) are shown. It can be observed that the turn-on currents are negative throughout the line cycle indicating ZVS turn-on. It can also be seen that for the secondary-side devices, it is more difficult to achieve ZVS near the line-cycle peaks, while for the primary-side devices, the same is true near the zero crossings.

is based on a design choice of having a peak–peak voltage ripple ($v_{\mathrm{dc}p}$) of 50 V about the average value of 300 V at the nominal power of 200 W, as predicted by [9]

$$C_{\mathrm{dc}p} = \frac{P_{\mathrm{av}}}{V_{\mathrm{dc}p}.\Delta v_{\mathrm{dc}p}.\omega_0}. \tag{17}$$

Transformer voltage and current waveforms across the line cycle and near the peaks and zero crossings of v_{ac} are depicted in Fig. 10. It may be observed that operations at these two points correspond to the modes discussed in Section II-C. Furthermore, it can be seen that the transformer current has higher peak and rms values near zero crossing.

ZVS turn-on of the primary-side and secondary-side devices across the ac line cycle for unity-pf load is verified from Fig. 11, in which the current through each switch is shown by the light blue trace. The dark blue trace corresponds to the current at the turn-on instant of the switch. It can be observed that the turn-on current of each switch is negative, implying satisfaction of the necessary condition for ZVS. A zoomed view of the waveforms of Fig. 11 at portions of the line cycle corresponding to respective worst-case conditions for ZVS is illustrated in Fig. 12, which confirm the previous observations.

ZVS turn-on of the primary-side and secondary-side devices across the ac line cycle for a nonunity-pf load can be verified from Fig. 13. As stated in the last section, the load is assumed to be of the same current rating as the unity-pf case and can be observed to be an inductive one with a pf angle of 20°. As in the unity-pf case, the turn-on current of each switch is negative over the ac line cycle, implying satisfaction of the necessary condition for ZVS.

Circuit operation with and without power decoupling control is compared in Fig. 14, where the current through the inductor L_{pv} and the hf-filtered PV current are both shown. The results clearly indicate that operation with decoupling control leads to drastic reduction in the low-frequency component of the input PV current. It may be observed that with power decoupling

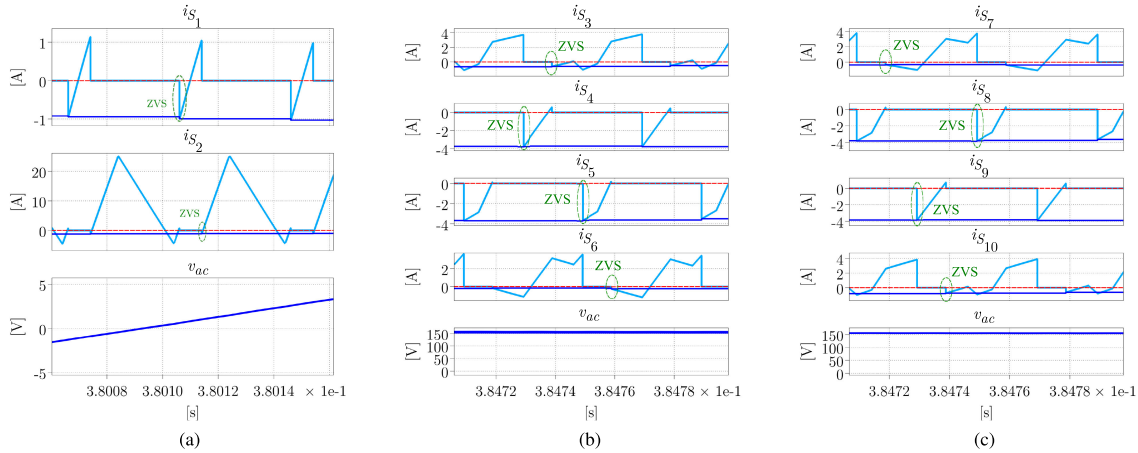

Fig. 12. Zoomed view of switch currents illustrating occurrence of ZVS under respective worst-case conditions for a unity-pf load. (a) Primary-side switches near zero crossing of $v_{\rm ac}$. (b) Secondary-side switches not directly connected to the load near peak of $v_{\rm ac}$. (c) Secondary-side switches directly connected to the load near peak of $v_{\rm ac}$.

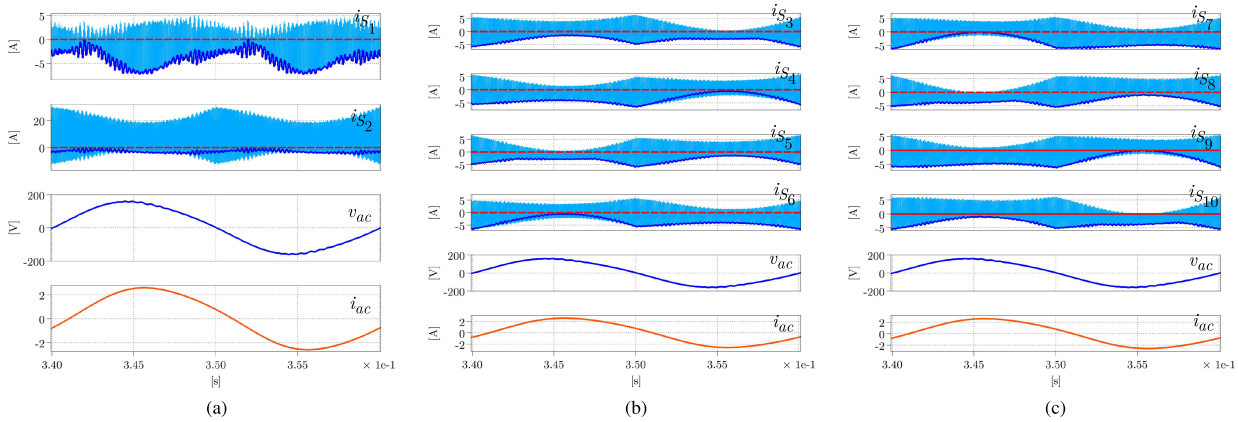

Fig. 13. Occurrence of ZVS for all switches over the full 50-Hz cycle for a nonunity-pf (inductive) load. (a) Primary-side and (b) secondary-side switches not directly connected to the load. (c) Secondary-side switches directly connected to the load. The current rating of the load is the same as that of the unity-pf load of Fig. 11.

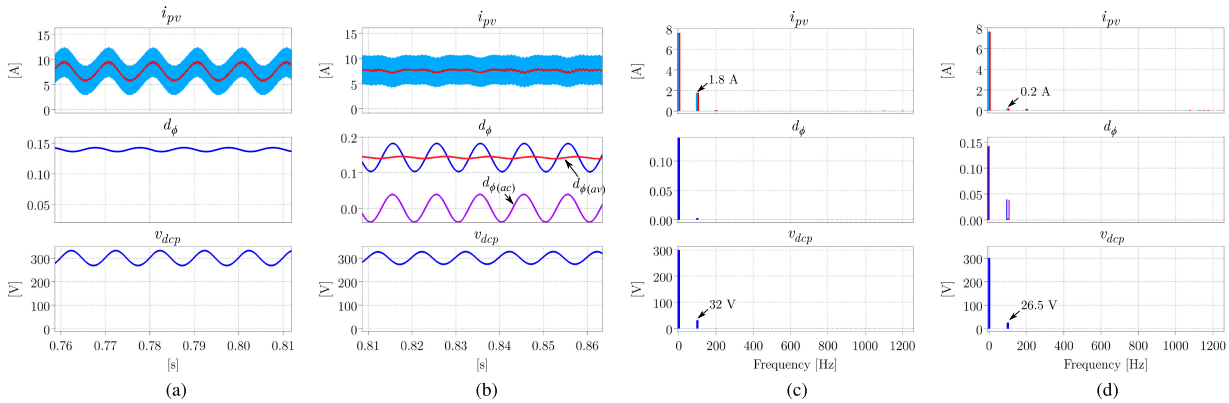

Fig. 14. Substantial reduction of the low-frequency component in the PV current ($i_{\rm pv}$) by employing power decoupling. Also shown are the dc-bus voltages ($v_{\rm dcp}$) and the variation of D_ϕ required to achieve power decoupling. (a) With power decoupling control—waveforms. (b) Without power decoupling control—waveforms. (c) With power decoupling control—FFT results. (d) Without power decoupling control—FFT results.

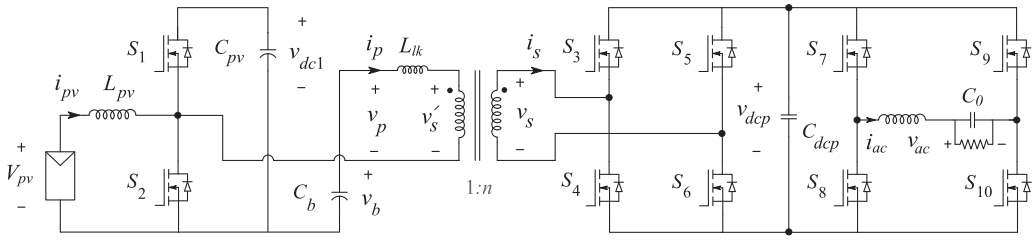

Fig. 15. Schematic of the two-stage topology employing the current-fed DAB as the dc–dc stage.

TABLE V
COMPARISON OF THE RMS CURRENT RATINGS OF THE SWITCHES AND TRANSFORMER OF THE PROPOSED TOPOLOGY WITH AND WITHOUT POWER DECOUPLING AND THE TWO-STAGE CURRENT-FED DAB-BASED TOPOLOGY. ZVS STATUS OF THE SWITCHES IS ALSO INDICATED. $V_g = 30$ V, $v_{\rm ac} = 110$ V (RMS), $P = 200$ W, $V_{\rm dc1} = 150$ V, AND $V_{\rm dcp} = 300$ V IN ALL CASES

	Primary switches	Secondary switches S_3-S_6	Secondary switches S_7-S_{10}	Transformer
Proposed topology (with power decoupling)	S_1-0.92 A, S_2-10.48 A ZVS - Yes	S_3-S_6-1.45 A ZVS - Yes	S_7-S_{10}-1.7 A ZVS - Yes	$i_{p(rms)}$ = 8.2 A
Proposed topology (without power decoupling)	S_1-0.88 A, S_2-10.2 A ZVS - Yes	S_3-S_6-1.42 A ZVS - Yes	S_7-S_{10}-1.667 A ZVS - Yes	$i_{p(rms)}$ = 8.08 A
Two-stage topology (Fig. 15)	S_1-2.78 A, S_2-9.54 A ZVS - Yes	S_3, S_5-1 A; S_4, S_6-0.9 A ZVS - Yes	1.32 A ZVS - 50% of line cycle	$i_{p(rms)}$ = 6.8 A

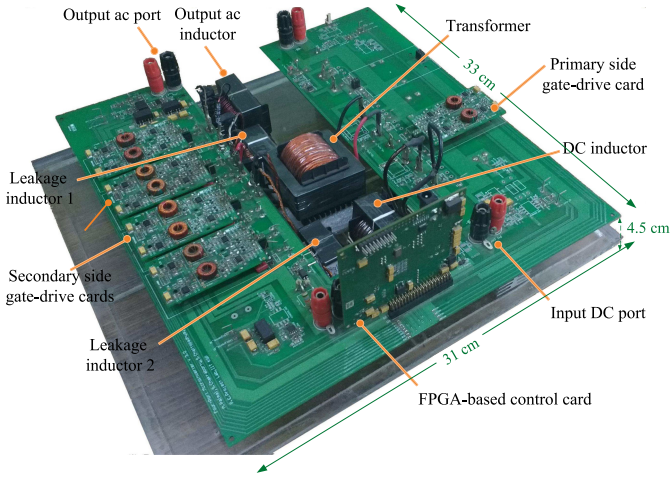

Fig. 16. Photograph of the hardware prototype.

TABLE VI
DETAILS OF COMPONENTS USED IN THE HARDWARE PROTOTYPE

Component	Description
Pri. switches (S_1, S_2)	IPP110N20NA (200 V, 20 mΩ)
Sec. switches ($S_3 - S_{10}$)	IPA50R140CP (500 V, 200 mΩ)
DC inductor (L_{pv})	140 μH, 19 T/ 12 wire gauge on EE 55/28
Pri. capacitors (C_{pv}, C_b)	20 μF, 500 V dc, film
Transformer	Turns-ratio (pr : sec) = 14:30:30, winding made using 40 strands of 32 wire gauge R_{ac}(pr) = 38 mΩ at 25 kHz, Core-EE 65/32/27
L_{lk}	Two inductors, each 545 μH in series with the secondary windings. 60 T/ 22 strands of 32 wire gauge on EE 42/20, R_{ac} = 225 mΩ at 25 kHz
Sec. dc bus capacitor (C_{dcp})	40 μF, 500 V, film
AC inductor (L_{ac})	3.5 mH, 3 A, 140 T/ 18 wire gauge on EE 55/28
Output filter capacitor (C_0)	2.2 μF, 310 V ac, film

control, the phase shift d_ϕ has an appreciable 100-Hz component, which is essentially required to cancel out the effect of the 100-Hz load disturbance.

In order to compare the performance of the proposed topology with an equivalent conventional solution, PLECS simulation of a two-stage topology having a current-fed DAB as the dc–dc stage (see Fig. 15) has been performed. The simulation specifications are same as the nominal values noted before (30 V to 110 V ac, 200 W, $D_1 = 0.2$, and $V_{\rm dcp} = 300$ V). The optimal values of n and $L_{\rm lk}$, which result in least $i_{p(\rm rms)}$ while realizing ZVS of all switches of the dc–dc stage, are iteratively found to be $n = 5$ and $L_{\rm lk} = 35$ μH. Since D_1 and $V_{\rm dcp}$ are same in both simulations, the voltage stress of the switches and the volt–second of the transformer are also same in both cases.

A comparison of the rms current ratings of the switches and the transformer as well as the ZVS status of the switches for the proposed topology with and without power decoupling enabled and the two-stage solution is presented in Table V. The results reveal almost no practical change in the current ratings or ZVS status with or without power decoupling, though, strictly speaking, the current ratings are a bit less when power decoupling is absent. As regards to comparison with the two-stage topology, it is observed that apart from S_1, the rms current ratings in the

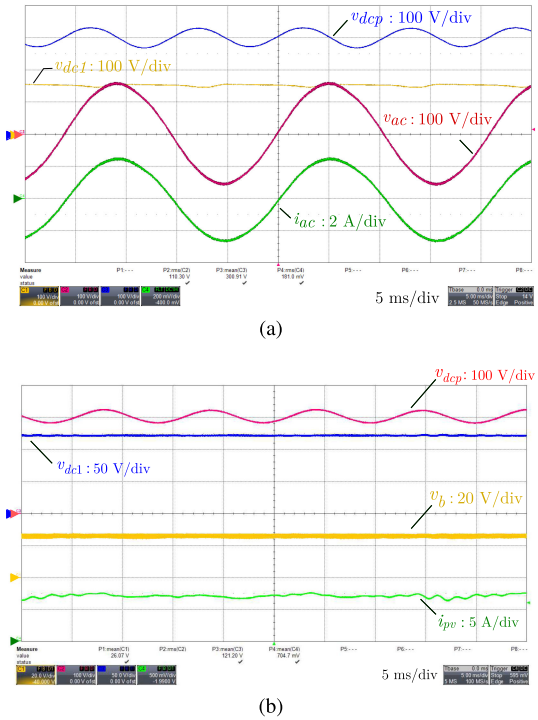

Fig. 17. Key low-frequency waveforms. (a) DC capacitor voltages and output voltage and current. (b) DC capacitor voltages and input current.

proposed topology are slightly higher, which can be attributed to the additional HF current necessary to achieve ZVS of the secondary switches across the ac line cycle. While this imposes some conduction loss penalty, the benefit of achieving ZVS for all secondary switches in the proposed topology as opposed to partial ZVS of the inverter-stage MOSFETs (S_7–S_{10}) in the two-stage solution could be a greater advantage in high-voltage high-switching-frequency applications. This claim is validated through experimental results.

V. Experimental Results

A 310 W max, 25–35 V in, 110 V, 50 Hz ac out laboratory prototype of the converter (see Fig. 16) has been built and tested. The developed prototype is a multipurpose one, reconfigurable as the battery-integrated topologies of [1] and [31] as well as the two-stage topology of Fig. 15, and hence, the printed circuit board area is considerably larger than ideally required.

Details of the components used in the hardware are presented in Table VI. Logic signals for the switches, generated using a Xilinx XC3S400 field-programmable gate array (FPGA)-based control board, are fed to individual gate-driver cards, each of which produces the gate signals for a half-bridge leg.

Since the objective of this paper was to demonstrate the advantages of the proposed solution, the focus was on converter design and operation. Hence, a real PV module or a solar array simulator or an emulated PV source (as is done in [27] by using a resistor in series with a dc source) was not employed. Instead a DC power supply (70 V, 25 A, Aplab make) was used as the dc source. Relevant experimental results illustrating circuit operation are depicted in Figs. 17–21.

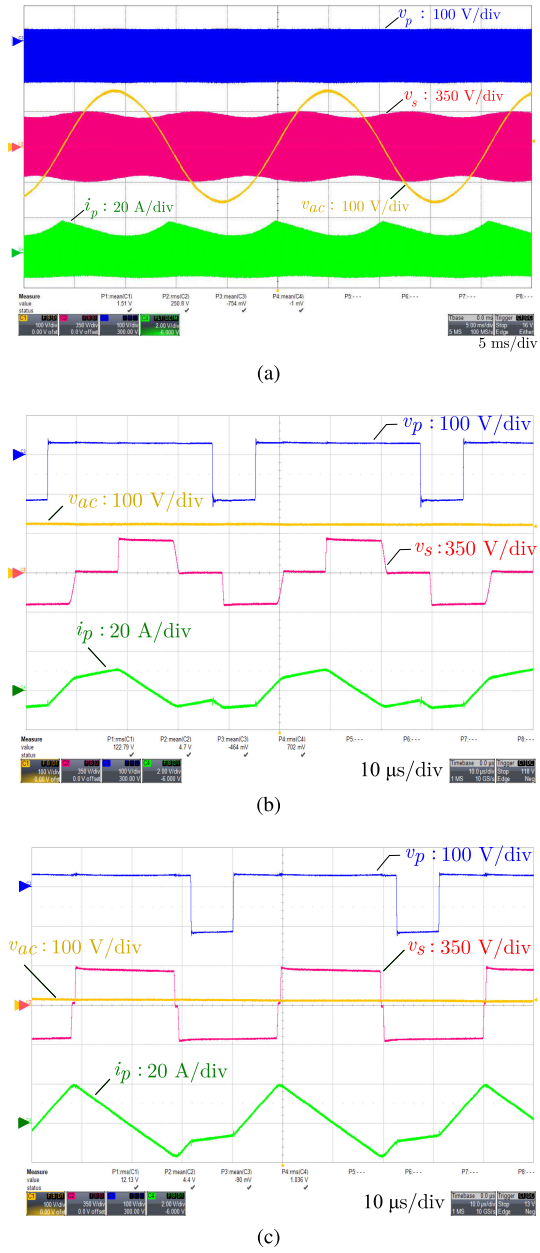

Fig. 18. (a) Transformer voltages and primary current over a full ac line cycle. (b) Transformer voltages and primary current near peaks of ac line cycle. (c) Transformer voltages and primary current near zero crossing of ac line cycle.

Key low-frequency waveforms of the circuit including, the dc capacitor voltages, the output voltage, current, and input current, are shown in Fig. 17. As can be observed from Fig. 17(b), the voltages v_b and $v_{\rm dc1}$ across the dc-side capacitors C_b and $C_{\rm pv}$, respectively, as well as the input dc current are free from low-frequency ripple, indicating that the energy buffering action is performed by the ac-side capacitor $C_{\rm dcp}$. Transformer voltage and current waveforms at two different points of the ac line cycle are shown in Fig. 18(b) and (c), which show excellent qualitative and quantitative match with the simulation results of Fig. 10.

Fig. 19 illustrates ZVS turn-on of the bottom switch on the primary side (S_2) and one of the secondary-side switches

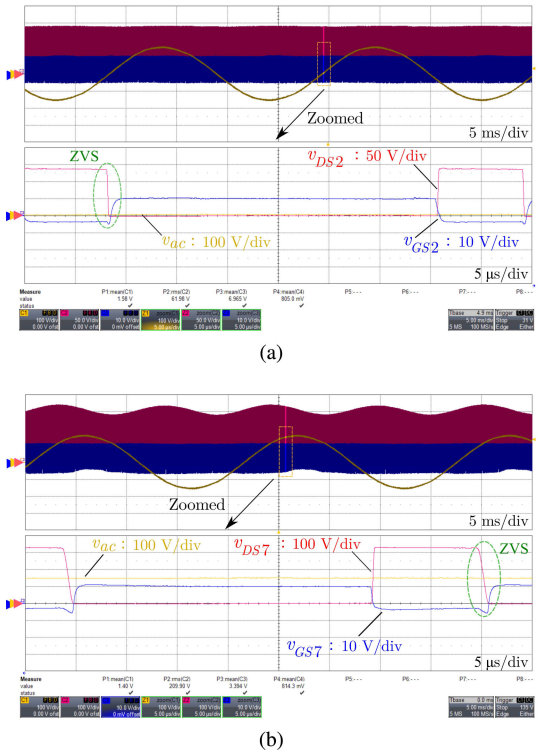

Fig. 19. ZVS turn-on of switches under respective worst-case conditions. (a) Primary switch S_2 near zero crossing of line cycle. (b) Secondary switch S_7 near peak of line cycle.

(S_7) directly connected to the load under respective worst-case conditions of the ac line cycle.

Closed-loop experimental results illustrating the effectiveness of power decoupling control in mitigating the low-frequency component of $i_{\rm pv}$ are depicted in Fig. 20. As can be seen from the fast Fourier transform (FFT) results, compared to the case of operation without power decoupling control, which results in a 100-Hz component of about 20% of the average value, operation with power decoupling limits the low-frequency components to less than 4% of the average value.

Transient response of the converter for a step change in load and input voltage is presented in Fig. 21. Dynamic behavior for an increase in load from 75 to 150 W at an input voltage of $V_{\rm pv} = 22$ V is illustrated in Fig. 21(a). The response shows stable behavior with a settling time of 60–70 ms for the dc-bus voltage control loop (corresponding to a design bandwidth of about 10–20 Hz). A similar stable response can be observed in Fig. 21(b), which shows the dynamic response of the converter for a step drop in input dc voltage from 23 to 16 V at a fixed load power of 125 W.

A comparison of the efficiency of the proposed converter and the two-stage DAB-based topology of Fig. 15 under different load conditions for switching frequencies of 25 and 50 kHz[1] at $V_{\rm pv} = 30$ V is shown in Fig. 22(a) and (b), respectively. The peak and CEC efficiencies of the proposed topology are 93% and 90.7%, respectively, at 25 kHz and 91% and 88.4%,

[1]For the 50-kHz operation, suitably designed smaller magnetic components were used.

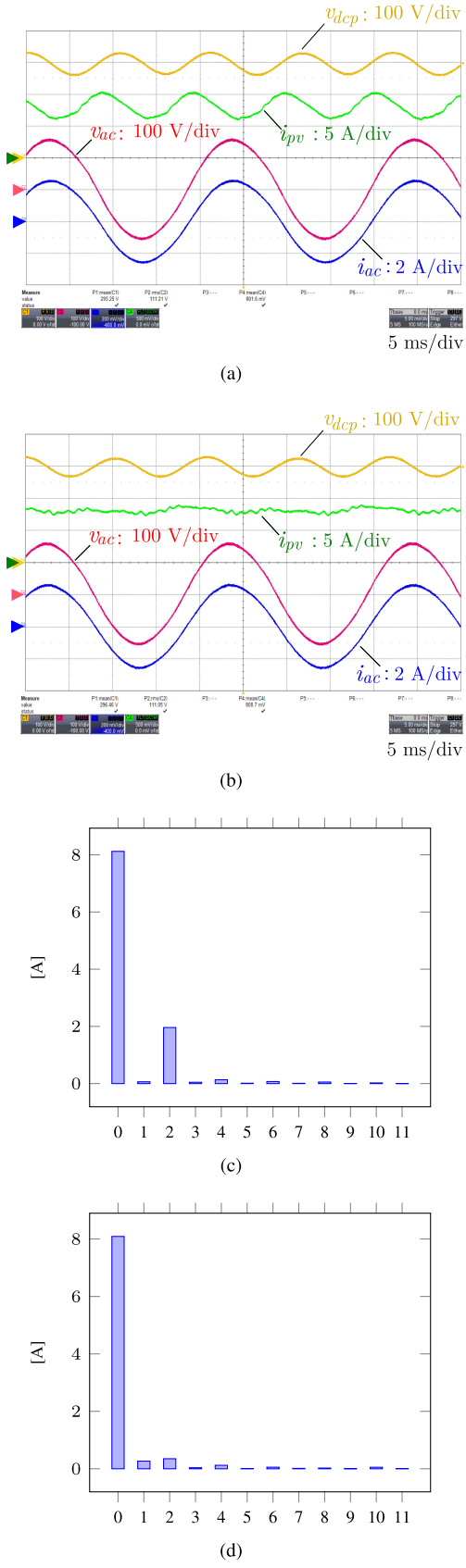

Fig. 20. Closed-loop experimental results illustrating elimination of the low-frequency component in the input current. (a) Without power decoupling control. (b) With power decoupling control. (c) FFT of the input current ($i_{\rm pv}$) without power decoupling. (d) FFT of the input current with power decoupling.

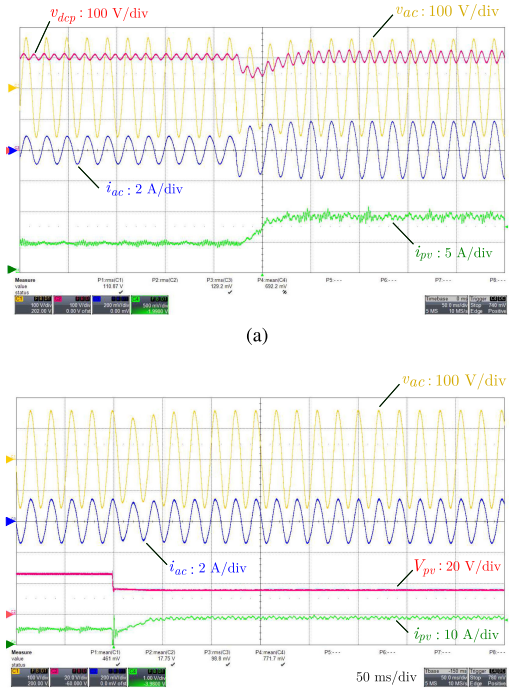

Fig. 21. Dynamic response of the converter (a) for a step change in load from 75 to 150 W (at $V_{\rm pv} = 22$ V) and (b) for a step change in input dc voltage from 23 to 16 V (at $P_{\rm out} = 125$ W).

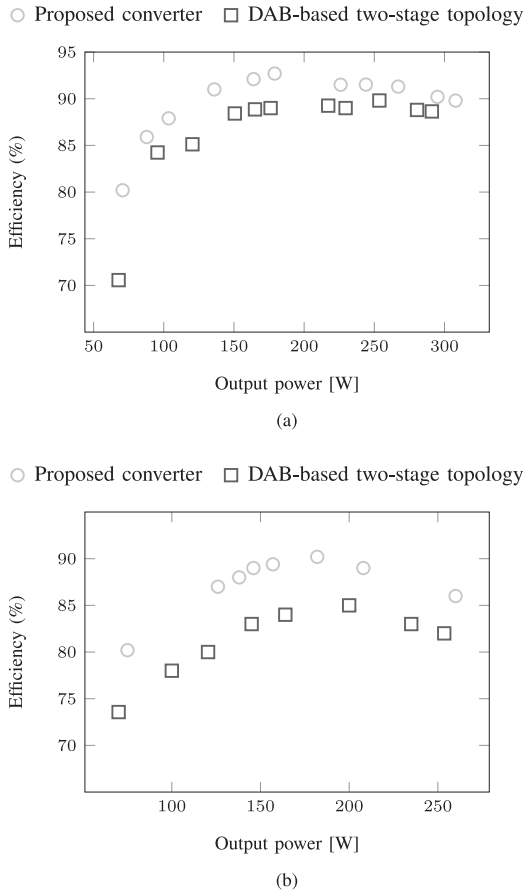

Fig. 22. Comparison of experimental efficiency of the proposed converter with the current-fed DAB-based two-stage topology at $V_{\rm pv} = 30$ V (a) for 25-kHz switching frequency and (b) for 50-kHz switching frequency.

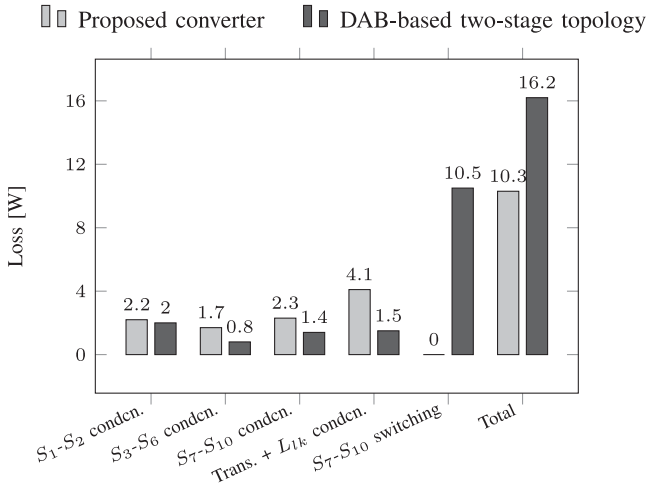

Fig. 23. Comparison of conduction and switching losses (at 25 kHz) of the proposed topology and the DAB-based two-stage topology at 200 W.

respectively, at 50 kHz. The comparison results indicate clear efficiency improvements for the proposed topology, with the margin of improvement higher at 50 kHz. To understand this, a comparative breakdown of the losses for 25-kHz switching frequency is presented in Fig. 23, in which losses in $L_{\rm dc}$ (1.4 W) and $L_{\rm ac}$ (3.5 W) and core losses of the transformer and $L_{\rm lk}$ (2.5 W), common in both topologies, have been omitted. It can be seen that the switching loss of 10.5 W incurred in the two-stage topology due to hard switching of S_7–S_{10} outweigh the increased conduction losses in the proposed solution, ultimately resulting in more net losses in the two-stage topology.

VI. Conclusion

A novel DAB-based isolated microinverter topology with a current–stiff interface for the PV port is proposed. The key advantage of the proposed solution is its ability to realize ZVS turn-on of all switches across the ac line cycle, unlike conventional two-stage solutions, which miss ZVS over half the ac line cycle. The topology achieves this functionality without using additional circuitry, as is required with ZVT-based solutions. Though the proposed circuit introduces additional conduction losses compared to two-stage topologies, ZVS operation can lead to better efficiency in cases where switching losses are significant, as is experimentally demonstrated. Furthermore, by employing a control strategy involving dynamic variation of phase shift over an ac line cycle, low-frequency power decoupling can be handled by the high-voltage secondary dc-bus capacitor. This results in substantial reduction in decoupling capacitance requirement, allowing a film-capacitor-based implementation, which is not possible in standard single-stage topologies.

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