Three Phase Current-Fed Semi Dual Active Bridge DC–DC Converter With Hybrid Operating Mode Control

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***Abstract*—A high-frequency isolated unidirectional three phase (3p) current-fed (CF) semi-dual active bridge (SDAB) dc–dc converter is proposed for unidirectional power-flow applications suitable for wide input and load variations with small input current ripple, such as for fuel stacks and photovoltaic (PV) array. A hybrid operating mode control was proposed to handle the operating stability throughout full load range especially the light load conditions by which, dual-pulsewidth modulation (PWM) and phase shifted control with fixed clamping voltage was implemented over certain kind of load while varying clamping voltage using only dual-PWM (D-PWM) control was used under light-load conditions. The ideal power transferred expressions are derived based on the analysis of power transmission characteristics. The ideal rms expressions of the leakage inductor current are ideally derived for leakage inductance value optimization or minimizing the loss; and the ideal soft-switching conditions based on charges have been given. A 2-kW 3p-CF-SDAB prototype using SiC MOSFETs has been built to verify the validity the proposed control strategy. With the proposed control, the steady-state performance throughout full load of range is pretty well. Seamless transition can be obtained between the two operating modes and the dynamic performance is good. The conversion efficiency is high and the loss distribution is given.**

***Index Terms*—High voltage interface, small current ripple, three phase current-fed semi dual active bridge (3p-CF-SDAB) dc–dc converter, wide input range.**

I. Introduction

As FUEL cells or photovoltaic (PV) panels working as distributed input source for dc–dc converters, their output voltage is wide. Besides, their output current ripples are preferred to be as small as possible [1], [2]. Otherwise, the life time of the input voltage sources, such as the fuel cell may be shortened [3] or the maximum power point tracking efficiency for PV is not accurate [4]. Besides, their output power range is also very wide. Even in facing the wide input voltage range and power range, for the dc–dc converter, high conversion efficiency is a perpetual requirement. The voltage-fed (VF) isolated dc–dc converters are common options for these applications. The most widely used topologies is phase shifted (PS) full bridge (FB) and *LLC* resonant dc-dc converter for their zero voltage switching (ZVS) and even zero current switching (ZCS) achievement [5], [6]. However, they are still some challenges, for instance, duty cycle loss, etc. A hybrid converter, dual active bridge (DAB), composed of two H-bridge connected through a high-frequency ac transformer for power flow and isolation was proposed in [7]. Thanks to the several advantages, such as natural ZVS, galvanic isolation, and bidirectional power flow, DAB dc–dc converter has attracted a great deal of attention over the past few decades [8]–[11]. DAB has been widely and successfully used in the fields of energy storage, auxiliary power supply in hybrid electric vehicles, micro grids, aerospace applications, and so on [11]–[14]. However, these VF converters have a disadvantage that the current ripple is comparatively high and the life time of the input voltage sources such as the fuel cell may be affected [3]. So the aforementioned VF converters are thus unsuitable for battery charging/discharging applications directly.

The current-fed (CF) isolated dc–dc converter is attractive because it significantly reduces the current ripple on the battery side [15], [16]. An integrated boost resonant converter consisting of an extremely simple structure was proposed in [17], but its peak current is very high. A CF push–pull dc–dc converter was proposed in [18] to achieve ZCS and ZVS for primary- and secondary-side switches, respectively. However, the current stress is also high. A novel modulation based on naturally clamped soft-switching bidirectional snubberless CF-DAB dc–dc converter was proposed in [19], but large circulating losses results in lower conversion efficiency. A buck/boost configuration is proposed in [20] to further reduce the current ripple. Many optimization control strategies have been raised to improve its operating performance, such as voltage matching control [21], optimized pulsewidth modulation (PWM) plus dual phase shift (PDPS) control [22], fixed duty cycle compensation [23], and so on.

Handling high power and achieving small current ripple is a big challenge for single-phase (1p) CF-DAB due to the high current stress on the devices. Multiphase converters came into being [24]–[26]. A novel interleaved bidirectional snubberless soft-switching CF FB voltage doubler was proposed in [27], and

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TABLE I
COMPARISON BETWEEN DIFFERENT TOPOLOGIES

	Single Phase Converters	Multiphase Converters	Series or Parallel Connection of Modules	Parallel Connection of Switches
Power Rating	LOW	HIGH	HIGH	HIGH
Reliability	HIGH	HIGH	LOW	LOW
Current Stress	HIGH	LOW	LOW	LOW
Cost	LOW	MID	HIGH	MID

its capacity of power handling is greatly enhanced. However, it has the same disadvantages [19] because both have the same basic structure. A multiphase dc–dc converter using a boost half-bridge cell unit for high voltage and high-power applications was proposed in [28] to increase the output voltage and/or output power. However, the voltage stress across their input switches was high. A three phase (3p) ac-link CF dc–dc converter raised in [29] is preferred for high-current application owing to current sharing, lower current stress, and lower transformer power rating. However, its efficiency will be seriously affected by the use of diode rectifier bridges. A 3p-CF-DAB is introduced in [30], and high dc inductor current ripple is used to maintain ZVS with a wide voltage variation.

The distinctive characteristics of DAB are also very attractive to be used in applications that only need unidirectional power flow, such as PV panels and fuel cells. While taking into account the conversion efficiency, the reliability of the converter is greatly improved, and the system structure is simplified. The risk of shoot through can be completely avoided and the system configuration can be significantly simplified. A new concept of 1p-VF semi-DAB (SDAB) is proposed in [31], whose output side top switches are replaced by diodes. Nevertheless, there is still room for further reduction of non-active power. A CF-SDAB converter introduced in [32] can significantly reduce the non-active power by applying dual-PWM and phase shift control (DPPS), but the current stress on the input-side bottom switches is comparatively high. As aforementioned, 1p configuration is not suitable for high-power applications. 1p-SDAB is therefore generalized to multiphase, 3p for example, to minimize current stress and output capacitor size. The multiphase converter has a simpler circuit and higher reliability than a simple series and parallel combination of multiple 1p converters. The comparison with other topology is summarized in Table I. However, the discussion on SDAB is not extensive, and the demonstration of multiphase SDAB lacks standards. Moreover, in the existing literature, the light-load conditions of the VF-SDAB and CF-SDAB are rarely discussed, except [33], [34]. Their stability under light-load conditions is also unknown.

In this paper, a hybrid operating mode control is proposed to meet wide voltage variations and full load range operation capability requirement. Its light load operation conditions have been envisaged. Dual-PWM control strategy has been proposed to completely deal with the issue of light load stable operation. This paper is organized as follows. Mode analysis of the proposed control strategy is given in Section II. Performance analysis

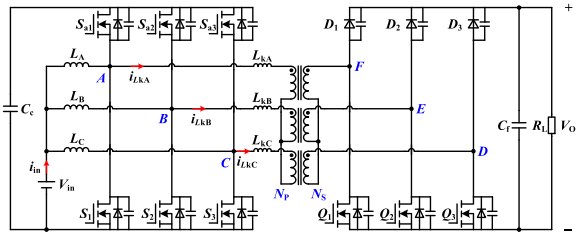


Fig. 1. Topology of 3p-CF-SDAB dc–dc converter.

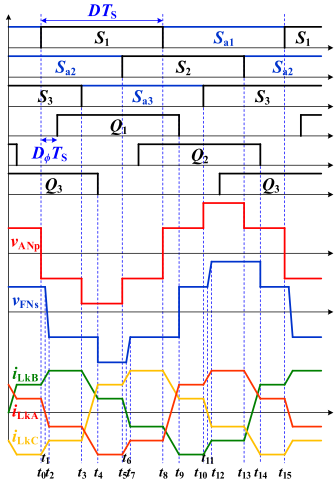


Fig. 2. Steady-state waveforms of the proposed dc–dc converter with DPPS control.

and discussion is made in Section III. Experimental results are illustrated in Section IV. Section V gives the conclusion.

II. MODE ANALYSIS WITH PROPOSED CONTROL STRATEGY

The proposed topology is shown in Fig. 1. For the primary side, L_A, L_B, and L_C are dc inductors. $S_{a1}\sim S_{a3}$ and $S_1\sim S_3$ are the power switches with body diodes and parasitic capacitors. C_c is the clamping capacitor. The ac inductors L_{kA}, L_{kB}, and L_{kC} represent the sum of the secondary-side referred transformer leakage inductance and the external ac inductance for each phase, respectively. In the secondary side, $Q_1\sim Q_3$ are the power switches. $D_1\sim D_3$ are the power diodes. The transformer is Y-Y connected. The current flow direction has been highlighted in Fig. 1. The ratio of the ON-time of primary-side bottom switch to the entire period is defined as the duty cycle D. The phase different between the driving signal of the secondary side switch and the primary-side bottom switch in each phase is the phase shift angle. The ratio between the phase shift angle and 2π is defined as D_ϕ.

One of the main steady-state waveforms of the proposed dc–dc converter during one complete switching period is shown in Fig. 2. Each phase is 120 degrees PS with each other. The driving signals of each leg are complementary and each phase is PS by 120 degrees. i_{LkA}, i_{LkB}, i_{LkC} represent the phase-to-neutral current, namely the leakage inductor current of each phase. v_{ANp} is the primary-side phase-to-neutral voltage of phase A and it is depends on the primary-side driving signals. v_{FNs} is the secondary-side phase-to-neutral voltage of phase A who is

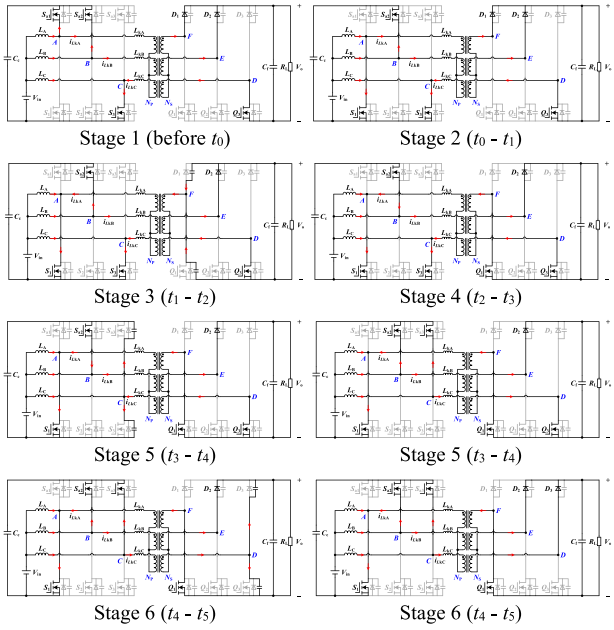


Fig. 3. Modes of the proposed topology during the third time.

not only determined by secondary-side driving signals but also current zero-crossing moment in diodes. T_S is the switching period.

The typical operation modes are shown in Fig. 3. The detailed mode analysis is described as follows.

Stage 1 (before t_0): S_{a1}, S_{a2}, S_3, Q_3, D_1, and D_2 conduct, and v_{ANp}, v_{FNs}, i_{LkA}, i_{LkB} are positive, and i_{LkC} is negative. $v_{ANp} = V_{Cc}/3$ and $v_{FNs} = V_O/3$, where V_{Cc} is the clamping voltage of C_c and V_O is the output voltage. During this stage, the power flows from the primary side (V_{in}) to the secondary side (V_O).

Stage 2 (t_0–t_1): At t_0, S_{a1} is turned OFF and S_1 is turned ON. v_{ANp} becomes $-V_{Cc}/3$ and v_{FNs} does not change. i_{LkB}, i_{LkC} increase positively and i_{LkA} decreases negatively until i_{LkA} falls to zero.

Stage 3 (t_1–t_2): When i_{LkA} falls to zero, D_1 is reverse biased, and v_{FNs} starts to gradually change from $V_O/3$ to $-V_O/3$. i_{LkA} will continue to decrease negatively and eventually become negative. At this time, the current on the secondary side of transformer phase-A simultaneously charges the junction capacitor of D_1 and discharges the junction capacitor of Q_1, waiting for Q_1 to turn ON with ZVS.

Stage 4 (t_2–t_3): Since the voltages of the primary and secondary sides match each other, v_{ANp}, v_{FNs}, i_{LkA}, i_{LkB} and i_{LkC} are all maintained at the previous values until the time instant of t_3.

Stage 5 (t_3–t_4): At t_3, S_3 is turned OFF. The difference between i_{LC} and i_{LkC} begins to charge/discharge the junction capacitors of S_{a3} and S_3 simultaneously. Then S_{a3} is turned ON with ZVS. v_{ANp} becomes $-2V_{Cc}/3$, and i_{LkC} increases positively while i_{LkA} and i_{LkB} decrease negatively.

Stage 6 (t_4–t_5): At t_4, Q_3 is turned OFF, and the current on the secondary side of the transformer phase-C simultaneously charges the junction capacitance of Q_3 and discharges the junction capacitance of D_3. Then D_3 conducts and v_{FNs} becomes $-2V_O/3$ consequently. After that, v_{ANp}, v_{FNs}, i_{LkA}, i_{LkB} and i_{LkC} remain unchanged. At t_5, S_{a2} is turned OFF while S_2 is turned ON. The corresponding voltages and currents of phase A, B, and C change alternately, and the first one-third of the period is reproduced until the end of the entire period. Thus they are omitted herein for the sake of brevity.

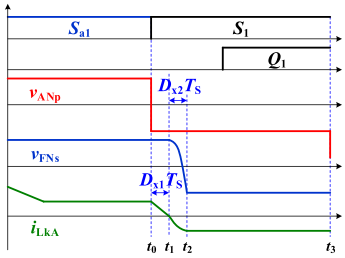


Fig. 4. Partial interval waveform enlargement.

III. Performance Analysis and Discussion

A. Leakage Inductor Current and Output Power

As previously analyzed, v_{ANp} varies negatively once S_{a1} is turned OFF and S_1 is turned ON since the leakage inductor suffers from reverse voltage. v_{FNs} begins to change its polarity when the polarity of the leakage inductor current changes completely. At this time, the junction capacitors of D_1 and Q_1 are charged and discharged by the leakage inductor current. Fully parsing this resonance process is complicated. Thence, this process can be approximated by a quadratic equation. Partial enlargement of it is shown in Fig. 4. The leakage inductor current expressions can be derived as follows:

$$i_{Lk}(t) = \begin{cases} -k \cdot k_1 \cdot (t - t_0) + i_{Lk}(t_0) & [t_0\ ,\ t_1) \\ i_{Lk2}(t) & [t_1\ ,\ t_2) \\ -k \cdot k_2 \cdot (t - t_2) + i_{Lk}(t_2) & [t_2\ ,\ t_3) \\ k \cdot k_3 \cdot (t - t_3) + i_{Lk}(t_3) & [t_3\ ,\ t_4) \\ -2k \cdot k_2 \cdot (t - t_4) + i_{Lk}(t_4) & [t_4\ ,\ t_5) \\ -k \cdot k_4 (t - t_5) + i_{Lk}(t_5) & [t_5\ ,\ t_6) \\ i_{Lk7}(t) & [t_6\ ,\ t_7) \\ -k \cdot k_2 \cdot (t - t_7) + i_{Lk}(t_7) & [t_7\ ,\ t_8) \\ k \cdot k_1 \cdot (t - t_8) + i_{Lk}(t_8) & [t_8\ ,\ t_9) \\ k \cdot k_2 \cdot (t - t_9) + i_{Lk}(t_9) & [t_9\ ,\ t_{10}) \\ -k \cdot k_3 \cdot (t - t_{10}) + i_{Lk}(t_{10}) & [t_{10}\ ,\ t_{11}) \\ i_{Lk12}(t) & [t_{11}\ ,\ t_{12}) \\ 2k \cdot k_2 \cdot (t - t_{12}) + i_{Lk}(t_{12}) & [t_{12}\ ,\ t_{13}) \\ k \cdot k_4 \cdot (t - t_{13}) + i_{Lk}(t_{13}) & [t_{13}\ ,\ t_{14}) \\ k \cdot k_2 \cdot (t - t_{14}) + i_{Lk}(t_{14}) & [t_{14}\ ,\ t_{15}] \end{cases} \quad (1)$$

where n is the turn ratio of the transformer, $D_E = 1/3$, $k = D_E/L_{kA}$, $k_1 = V_{Cc} + nV_O$, $k_2 = V_{Cc} - nV_O$, $k_3 = nV_O - 2V_{Cc}$, and $k_4 = V_{Cc} - 2nV_O$.

Suppose the expression of v_{FNs} within $t \in [t_1, t_2)$ (marking $\Delta_2 = t_2 - t_1$) is expressed as

$$v_{FNs}(t) = D_E V_O \left[1 - \frac{2}{\Delta_2^2}(t - t_1)^2\right]. \tag{2}$$

And then the corresponding leakage inductor current can be deduced as the following:

$$-D_E V_{Cc} - n v_{FNs}(t) = L\frac{di_{Lk2}(t)}{dt}. \tag{3}$$

Integrating the (3) and substituting the initial conditions yields the following:

$$i_{Lk2}(t) = \frac{2knV_O}{3D_{X2}^2 T_S^2}(t - t_1)^3 - k \cdot k_1 \cdot (t - t_1). \tag{4}$$

Similarly, the expressions of $i_{Lk7}(t)$ and $i_{Lk12}(t)$ also can be obtained accordingly, which are shown below

$$i_{Lk7}(t) = -\frac{knV_O}{3D_{X2}^2 T_S^2}(t - t_6)^3 - k \cdot k_4 \cdot (t - t_6) + i_{Lk}(t_6) \tag{5}$$

$$i_{Lk12}(t) = -\frac{knV_O}{3D_{X2}^2 T_S^2}(t - t_{11})^3 - k \cdot k_3 \cdot (t - t_{11}) + i_{Lk}(t_{11}). \tag{6}$$

Theoretically, there is no dc component in the leakage inductor current. Namely, the average value of the leakage inductor current during a switching period is zero. D_{x1} can be obtained accordingly which is as follows:

$$D_{X1} = D_E - \frac{1 - 2D_{X2}}{3V_{Cc}} V_O n. \tag{7}$$

Meanwhile, the junction capacitors of D_1 and Q_1 are simultaneously charged and discharged, respectively. According to the principle of conservation of charge, the following formula stands. Here C_D, C_Q are the junction capacitance value of D_1 and Q_1, respectively

$$n\int_{t_1}^{t_2} i_{Lk}(t)\, dt = (C_D + C_Q) V_O. \tag{8}$$

Simplifying and rearranging (8) yields

$$D_{X2} = f_S \sqrt{\frac{6V_O(C_D + C_Q)}{nk(3V_{Cc} + 2nV_O)}}. \tag{9}$$

The power expression can be obtained consequently which is written below

$$\begin{aligned} P_O &= 3f_S \int_{t_0}^{t_{15}} i_{Lk}(t)\, v_{ANp}(t) dt \\ &= kT_S V_{Cc} V_O n \begin{bmatrix} (D_\phi + D_{X1}) + 2D_{X2}(D_E - D_{X1}) \\ -1.5\left(D_\phi^2 + D_{X1}^2\right) - 0.75D_{X2}^2 \end{bmatrix}. \end{aligned} \tag{10}$$

The output power P_O versus the phase shift angle ratio D_ϕ is plotted in Fig. 5. The specific parameters are listed in Table II. The dark-blue solid line is the calculation results based on (10), and the red-dashed line with red dots is the simulation results

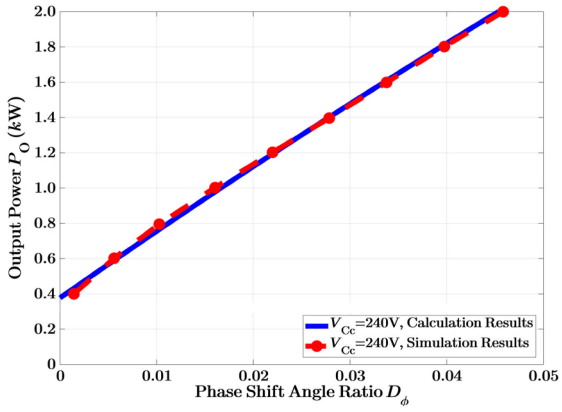


Fig. 5. Output power P_O versus phase shift angle ratio D_ϕ.

TABLE II
SYSTEM SPECIFICATIONS

Components	Parameters
Output Voltage (V_O)	400 V
Input Voltage (V_{in})	100-160 V
Clamping Voltage (V_{Cc})	240 V
Output Power (P_{omax})	2 kW
Switching Frequency (f_S)	100 kHz
Turn ratio (n)	9:15
DC Inductance (L)	40 μH
Leakage Inductance (L_k)	5 μH

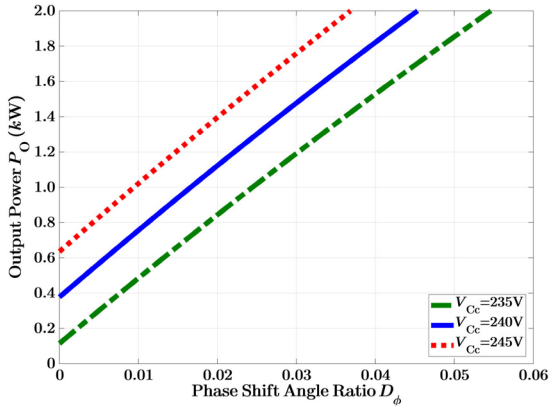


Fig. 6. P_O versus D_ϕ with different clamp voltages.

(based on PSIM). These two curves fit perfectly, with some deviations only at very light load conditions. Therefore, (10) has theoretical guiding significance for output power.

Meanwhile, it must be noted that the output power is not zero when D_ϕ is diminished to zero, which indicates that the output voltage is uncontrollable under light load or even no-load conditions only using DPPS control. Therefore, it is imperative to search an effective method to handle the light load issue.

Fig. 6 shows P_O versus D_ϕ with different clamping voltages based on (10). As shown, the required D_ϕ is inversely related to the clamping voltage at the same power rating. Therefore, it is possible to suppress the slop of the leakage inductor current by lowering the clamping voltage, thereby achieving the

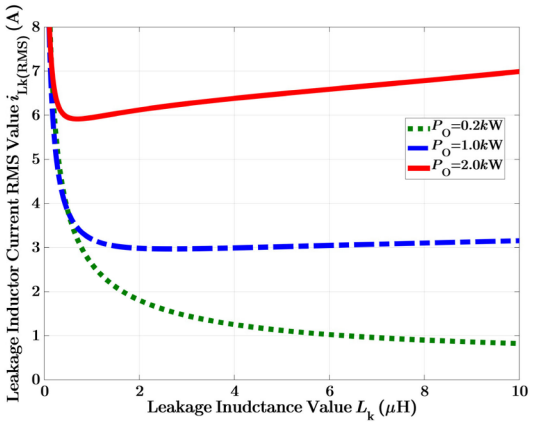


Fig. 7. L_k versus the leakage inductor current rms value $i_{Lk(\mathrm{RMS})}$.

condition of regulating the light load operation of the converter. This is a pure and extremely effective method that can completely solve the problem of uncontrollable light-load conditions. This method is referred to herein as a dual-PWM (D-PWM) control. An exhaustive control block diagram will be explained later in detail.

B. Leakage Inductor Current Stress Analysis

The magnitude of the leakage inductance limits the power transferred capability and affects the rms value of i_{Lk}. It is feasible to discuss the current stress of i_{Lk} to reduce the converter losses. The leakage inductor current equation in the whole period is given by (1) and the phase shift angle ratio can be obtained from (10). Then the leakage inductor current rms value expression $i_{Lk(\mathrm{RMS})}$ can be expressed as follows:

$$i_{Lk(\mathrm{RMS})} = \sqrt{f_S \int_{t_0}^{t_{15}} i_{Lk}^2(t)dt} = kT_S V_C \sqrt{\left[\begin{array}{l} \frac{2}{3}D_\phi\left(D_\phi + 2D_{X1}\right) - D_\phi^3 \\ -D_{X1}^2\left(\frac{302}{35}D_{X1} - \frac{8}{3}\right) \end{array}\right]}. \quad (11)$$

The $i_{Lk(\mathrm{RMS})}$ versus L_k can be plotted in Fig. 7. The specific parameters used for plotting are listed in Table II. There is a pole point in each of the $i_{Lk(\mathrm{RMS})}$ curves shown in Fig. 7. Each power rating has a different pole point coordinate. And $i_{Lk(\mathrm{RMS})}$ gets the minimum at these pole points.

Proverbially, larger leakage inductor requires larger phase shift angle at the same power rating. Meanwhile, the larger leakage inductance can alleviate the light load uncontrollable issue of SDAB dc–dc converter to a certain extent and broaden its stable working range. However, an excessive inductance will result in a large inductor size. In view of this, the effective total leakage inductance is designed around 5 μH in this paper.

C. Soft Switching Conditions

Since the other two phases entirely chime with phase A, only the phase A is taken as an example for analysis. Fig. 8 indicates

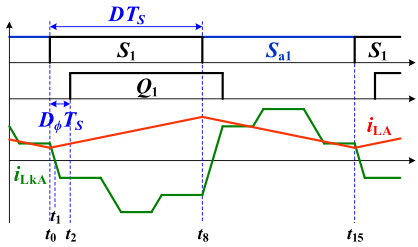


Fig. 8. Key waveforms of ZVS.

the phase-to-neutral current of phase A. Furthermore, the impact of the dead time is also taken into account. The implementation of ZVS requires a large enough current to draw the charge on the MOSFETs before it is turned ON. The exhaustive analysis will be developed below.

1) Primary-Side Switches: The maximum and minimum values of the dc inductor current of phase A are $I_{LA\max} = I_{LA} + 0.5\Delta i_{LA}$ and $I_{LA\min} = I_{LA} - 0.5\Delta i_{LA}$, respectively. I_{LA} is the average current of dc inductor of phase A and $I_{LA} = P_O/(3V_{\mathrm{in}})$. Δi_{LA} is the current ripple of dc inductor of phase A and $\Delta i_{LA} = V_{\mathrm{in}}DT_S/L_A$.

Thereafter, the expression of the dc inductor current in a switching period can be expressed as follows:

$$i_{LA}(t) = \begin{cases} I_{LA\min} + \frac{V_{\mathrm{in}}}{L_A}(t - t_0) & t \in [t_0\ , t_8) \\ I_{LA\max} + \frac{V_{\mathrm{in}} - V_{Cc}}{L_A}(t - t_8) & t \in [t_8, t_{15}]. \end{cases} \quad (12)$$

Before S_{a1} is turned ON, the difference between i_{LA} and i_{LkA} must thoroughly charge/discharge the junction capacitors of S_1 and S_{a1} within the dead time. The ZVS condition of S_{a1} can be formed consequently as the following:

$$\int_{t_8}^{t_8+T_{dP}} \left[i_{LA}(t) - i_{LkA}(t)\right] dt \geq 2C_{oss\cdot P}V_{Cc} \quad (13)$$

where T_{dP} is the primary side dead time, $C_{oss\cdot P}$ is the junction capacitance of the primary side MOSFETs. Analogously, the ZVS condition of S_1 can be established as follows:

$$\int_{t_0}^{t_0+T_{dP}} \left[i_{LkA}(t) - i_{LA}(t)\right] dt \geq 2C_{oss\cdot P}V_{Cc}. \quad (14)$$

Actually, Fig. 8 intuitively indicates that the ZVS condition of S_{a1} is more easily satisfied than that of S_1. It can be proved that (13) is always satisfied regardless of the input voltage and the output power discussed in this paper in the case of $L < 160$ μH. Therefore, (14) is the main consideration. After reorganization and simplification (14), the ZVS condition of the primary side, namely the selection of the dc inductance, can be obtained. The result is as follows:

$$L \leq \frac{3L_kT_{dP}V_{\mathrm{in}}^2\left(DT_S - T_{dP}\right)}{2\left[L_kP_OT_d + \left(6C_{oss\cdot P}L_k + T_{dP}^2 - 2D_{X1}T_ST_{dP}\right)V_{\mathrm{in}}V_{Cc}\right]}. \quad (15)$$

Substituting the necessary parameters listed in Table II and (10) into (15), the relationship between the ratio of $M = L/L_k$ and D_ϕ can be obtained and the corresponding picture with different D is plotted in Fig. 9.

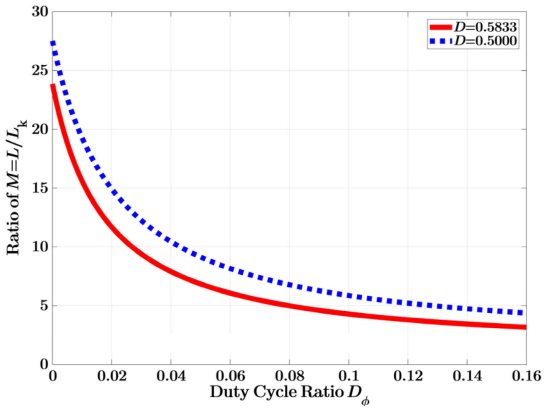


Fig. 9. ZVS range of primary-side bottom switches with different duty cycles.

Fig. 9 illustrates that the higher the input voltage, the wider the selection range of dc inductance values at the same power rating. And the ZVS range of S_1 becomes narrower as the power rating increases. This indicates that it requires more current ripple. In order to achieve the ZVS of primary-side bottom switches in heavy load, $M = 8$ is taken in this paper.

2) Secondary-Side Switches: As described above, the leakage inductor reflected to the secondary side resonates with the junction capacitors of secondary side MOSFETs and diodes. Obviously, ZVS of Q_1 can be fully guaranteed only if $D_{X2} < D_\phi$. Thus the ZVS condition of Q_1 is summarized as follows:

$$P_O \geq T_S V_{Cc}^2 k \left(D_{X1} + 5 D_E D_{X2} - \frac{3}{2} D_{X1}^2 - \frac{9}{4} D_{X2}^2 - 2 D_{X1} D_{X2} \right). \quad (16)$$

The right side of the inequality is a constant value. Substituting the parameters listed in Table II into (16) and calculating, this constant value is approximately equal to 660 W. That is to say, when the converter discussed in this paper operates above 660 W, the ZVS of Q_1 can be guaranteed.

It should be emphasized here that the ZVS conditions discussed above were made with $D_\phi > 0$. The case where $D_\phi = 0$ and the reference value of V_{Cc} is regulated has not been discussed. As can be seen from Fig. 5, the proportion of the second case is very small and it can only occur under very light-load conditions. Therefore, ZVS of that situation is not discussed herein.

D. Control Strategy

As aforementioned that the transferred power is not zero when D_ϕ is zero if DPPS control is implemented by using the phase shift angle ratio defined in this paper. This means that if the minimum of D_ϕ is designed to be zero then the output voltage will be out of control at light-load conditions when using DPPS control. Of course, this issue can be alleviated rather than thoroughly solved by extending the D_ϕ to be negative. However, the monotonic interval of the output power with respect to D_ϕ is not fixed, and it varies with the loads and input voltages.

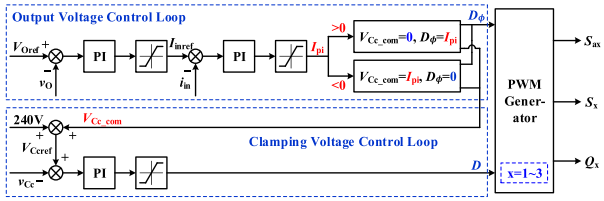
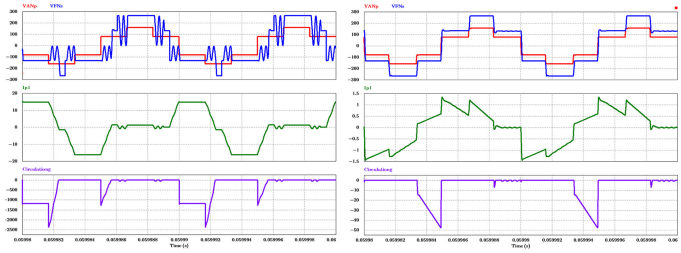


Fig. 10. Control block diagram.



(a) (b)

Fig. 11. Steady state waveforms when $V_{\rm in} = 120$ V and $P_O = 0.2$ kW. (a) DPPS control with minus D_ϕ. (b) D-PWM control.

Its turning point is hard to find. Therefore, the output of the limiter needs to be adjusted with the input and load variations. It is troublesome and uncertain. Especially at no-load conditions, the output voltage will increase sharply, posing a hazard. Moreover, the circulating current or reverse power is very high if $D_\phi < 0$. It must cause very low conversion efficiency. Therefore, it is not suitable to regulate the output voltage only using DPPS by allowing minus D_ϕ at light load conditions. Fig. 6 has already illustrated that when D_ϕ is diminished to zero; the output power can be suppressed by lowering the clamping voltage. A varying control strategy is consequently proposed in this paper based on this pure idea to thoroughly handle this issue. The control block diagram of the proposed method is shown in Fig. 10.

As seen in Fig. 10, v_O, v_{Cc} are the feedback information of the output and the clamping voltage, respectively. $V_{O\rm ref}$, $V_{C\rm cref}$ are their corresponding reference. The input of the proportion integration (PI) compensator is the difference between $V_{O\rm ref}$ and v_O, and its output is restricted by the limiter and used as the reference $I_{\rm inref}$ for the dc inductor current inner loop. The difference between $I_{\rm inref}$ and $i_{\rm in}$ serve as the input of another PI compensator, and the output of this PI compensator is also limited by the limiter. When the output of the second limiter is positive, the $V_{C\rm cref}$ is set to 240 V and remains constant, and the output power is only controlled by D_ϕ. In comparison, when its output is negative, D_ϕ is set to zero and the $V_{C\rm cref}$ is regulated negatively to restrict the output power. The clamping voltage control loop has a similar working process. What's more, D is always regulated automatically.

Fig. 11 illustrates the simulation results by using different control strategies when $V_{\rm in} = 120$ V and $P_O = 0.2$ kW. Fig. 11(a) is under the DPPS control by allowing the minus D_ϕ while Fig. 11(b) is applied by D-PWM control. The top of each figure are phase to neutral voltage v_{ANp} and v_{FNs} of phase A. The phase-to-neutral current of phase A is shown in the middle of each figure. And the bottom one shows the instantaneous reverse power calculated by v_{ANp} times i_{LkA} and only shows the minus

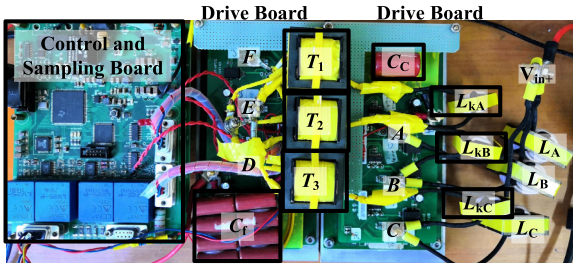


Fig. 12. Photograph of the test prototype.

TABLE III
ALL DEVICES MODELS

Devices	Patterns
Control Chip	TMS320F28335
Drive Chip	Si8233
SiC MOSFETs	C3M0065090J
Diodes	C3D10060G
Transformer Core	DMR95 EE42A
DC Inductor Core	DMR95 EE42A
Leakage Inductor Core	DMR95 EI30

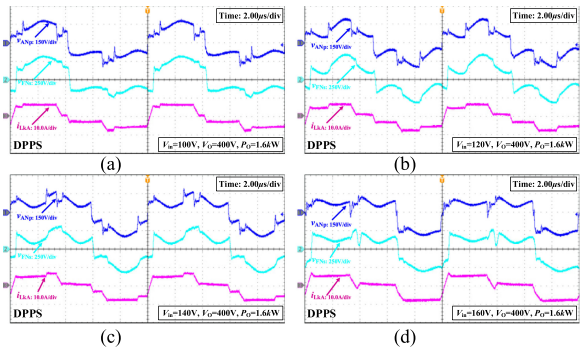


Fig. 13. Steady-state experimental waveforms in 1.6 kW with different input voltages. (a) V_{in} = 100 V, P_O = 1.6 kW. (b) V_{in} = 120 V, P_O = 1.6 kW. (c) V_{in} = 140 V, P_O = 1.6 kW. (d) V_{in} = 160 V, P_O = 1.6 kW.

value. Obviously, the peak current in Fig. 11(a) is much higher than that in Fig. 11(b). So is the reverse power. The average reverse power in Fig. 11(a) is about 319.33 W while only 4.68 W in Fig. 11(b). They are vastly different.

Consequently, the efficiency by using DPPS control with minus D_ϕ at light-load condition is much lower than that of D-PWM control.

IV. Experimental Results

A. Prototype

A 2-kW experimental prototype has been built to verify the effectiveness of the 3p-CF-SDAB dc–dc converter utilizing the proposed control. The prototype photograph is shown in Fig. 12. The parameters of the converter system are listed in Table II and all device patterns are summarized in Table III.

B. Steady-State Experimental Results

Figs. 13–14 show the experimental waveforms of the proposed converter under different input voltages and different

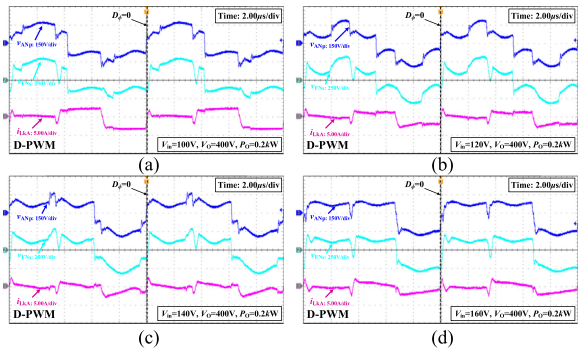


Fig. 14. Steady-state experimental waveforms in 0.2 kW with different input voltages. (a) V_{in} = 100 V, P_O = 0.2 kW. (b) V_{in} = 120 V, P_O = 0.2 kW. (c) V_{in} = 140 V, P_O = 0.2 kW. (d) V_{in} = 160 V, P_O = 0.2 kW.

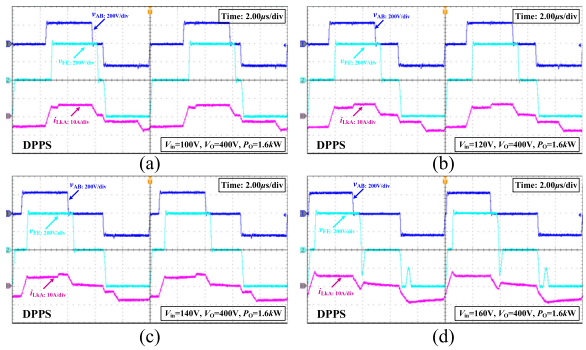


Fig. 15. Primary- and secondary-side line-to-line voltage and phase-to-neutral current waveforms. (a) V_{in} = 100 V, P_O = 1.6 kW. (b) V_{in} = 120 V, P_O = 1.6 kW. (c) V_{in} = 140 V, P_O = 1.6 kW. (d) V_{in} = 160 V, P_O = 1.6 kW.

loads with the proposed control strategy. It can be seen that the phase-to-neutral voltage waveforms (v_{ANp} and v_{FNs}) in Figs. 13 and 14 are not so regular, which are different from the ideal analysis. This is due to the fact that the neutral point of the primary and secondary side is floating. The asymmetry of each phase parameters results in a very irregular neutral point voltage waveform. This affects the phase-to-neutral voltage waveforms. Meanwhile, the constituent components, such as the transformers, inductors, and power devices are not ideal, and the effect of dead time is also taken into account. In comparison, the experimental current waveforms are relatively regular and pretty similar to their theoretical waveforms. Moreover, D_ϕ is positive as the output power is 1.6 kW (Fig. 13) while the D_ϕ is zero when the output power is 0.2 kW (Fig. 14).

Fig. 15 shows the primary and secondary-side line-to-line voltage ($v_{AB} = v_{ANp} - v_{BNp}$, $v_{FE} = v_{FNs} - v_{ENs}$) and phase-to-neutral current waveforms. It can be seen that the primary side line-to-line voltage is very regular and smooth. This is because the primary-side line-to line-voltages are only determined by switching logic of the primary-side switches rather than the leakage inductor current. Moreover, the effect of the neutral point waveform is eliminated on the line-to-line voltage waveforms. The secondary-side line-to-line voltage waveforms in Fig. 15 are also very clean except Fig. 15(d). The spikes appearing in Fig. 15(d) happens exactly at the natural zero crossing of the phase-to-neutral or line-to-line current.

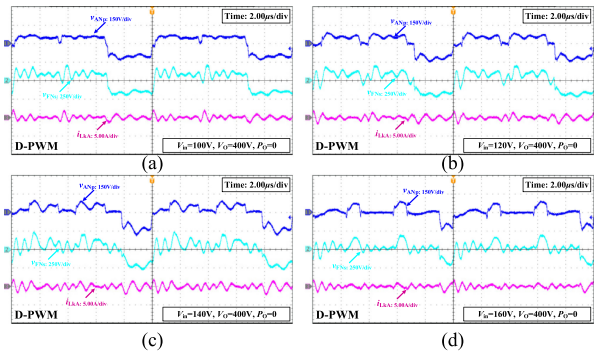


Fig. 16. Steady-state experimental waveforms in 0.0 kW with different input voltages. (a) V_{in} = 100 V, P_O = 0. (b) V_{in} = 120 V, P_O = 0. (c) V_{in} = 140 V, P_O = 0. (d) V_{in} = 160 V, P_O = 0.

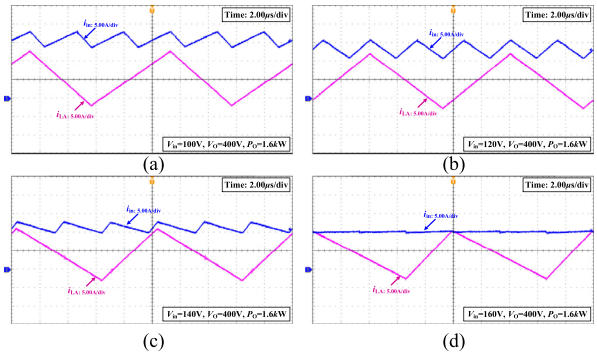


Fig. 17. Input current ripple waveforms in 1.6 kW with different input voltages. (a) V_{in} = 100 V, P_O = 1.6 kW. (b) V_{in} = 120 V, P_O = 1.6 kW. (c) V_{in} = 140 V, P_O = 1.6 kW. (d) V_{in} = 160 V, P_O = 1.6 kW.

At this time, the diode is reverse biased and the leakage inductor resonates with the junction capacitors of the power devices.

Fig. 16 shows the no-load condition experimental waveforms. The proposed converter can work very stably at no-load conditions by utilizing the proposed control strategy, which is enough to prove the effectiveness of this method.

Fig. 17 shows the total input current and input current of phase-A of the proposed converter. It illustrates that the current ripple of each phase is large even the dc inductance value is large enough due to the high input voltage level. However, the ripple of the total input current is quite small thanks to the 3p interleaving structure. The smaller current ripple is beneficial to extend the lifetime of input source, such as fuel cell stack and the PV array. Fig. 18 illustrates the ZVS achievements of S_{a1}, S_1 and Q_1 which are consistent with the theoretical analysis.

C. Dynamic Response Experimental Results

Fig. 19 shows the dynamic response using only DPPS control without minus D_ϕ. The load switching back and forth between 0.8 and 0.2 kW when V_{in} = 120 V. When the converter is working normally, $D_\phi > 0$ under 0.8 kW condition and $D_\phi = 0$ under 0.2 kW condition. It can be seen from the experimental results that the output voltage is uncontrollable when the load is very light. At this moment the regulator fails and the converter operates in an open loop. The output voltage will rise to 432 V

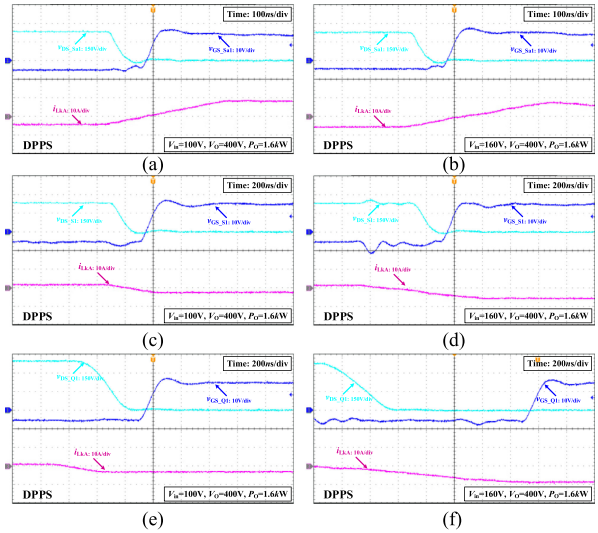


Fig. 18. ZVS operating conditions of active switches when P_O = 1.6 kW. (a) S_{a1}, V_{in} = 100 V, P_O = 1.6 kW. (b) S_{a1}, V_{in} = 160 V, P_O = 1.6 kW. (c) S_1, V_{in} = 100 V, P_O = 1.6 kW. (d) S_1, V_{in} = 160 V, P_O = 1.6 kW. (e) Q_1, V_{in} = 100 V, P_O = 1.6 kW. (f) Q_1, V_{in} = 160 V, P_O = 1.6 kW.

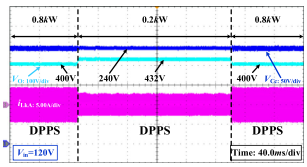


Fig. 19. Dynamic response only using DPPS control without minus D_ϕ.

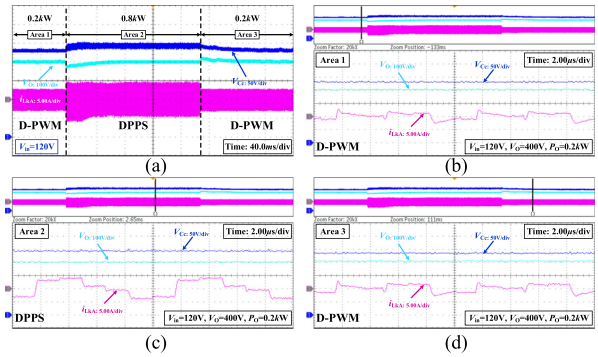


Fig. 20. Dynamic response under different loads. (a) Macro view. (b) Detail of area 1. (c) Detail of area 2. (d) Detail of area 3.

under the operating conditions as shown in Fig. 19. When the load is further reduced, the output voltage will increase rapidly, which is very dangerous. As aforementioned, the stable operating range of the converter can be broadened to some extent by allowing the minus D_ϕ theoretically. But this issue cannot be completely solved. The reason has been described above in detail.

Load-switching experiments between 0.2 (D-PWM control) and 0.8 kW (DPPS control) were implemented to demonstrate the smoothness of the control strategies switching between D-PWM control and DPPS control. Fig. 20 illustrates the dynamic responses experimental results when V_{in} = 120 V. Fig. 20(a) shows the macro view, and it was divided into three areas.

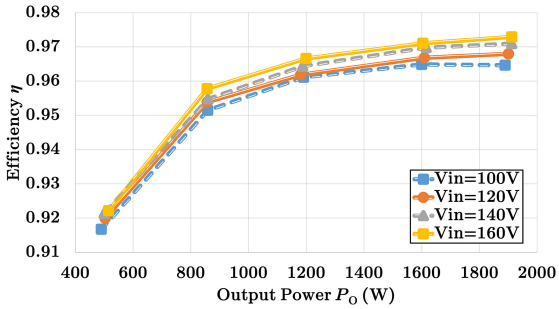


Fig. 21. Power conversion efficiency.

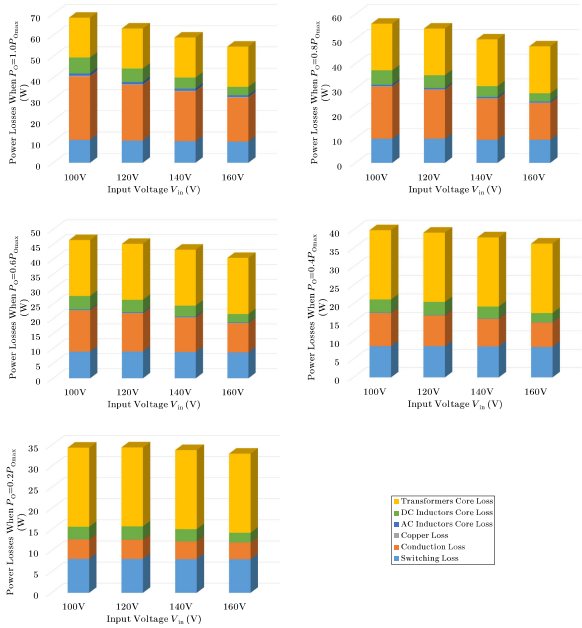


Fig. 22. Loss distribution.

Fig. 20(b) to (d) shows the detail of areas 1–3, respectively. Although there is a small drop or bulge in the output voltage at the transient of load switching, it quickly returns to the ideal value. Switching between these two modes does not cause a large transient of voltage or current. It indicates that the proposed method enables the converter to have a fast dynamic response speed and a smooth modal transition. Load switching experiments at other input voltages were also implemented, and the experimental results have the same conclusion. For brevity, it is omitted herein.

D. Conversion Efficiency and Loss Breakdown

Fig. 21 illustrates the measured efficiency curves under different input voltages and different loads. The high conversion efficiency is guaranteed over a wide variation of input voltage and load conditions. Peak efficiency always occurs around $P_O = 2.0$ kW regardless of the input voltage.

Moreover, the efficiency is positively correlated with the input voltage due to the reduction of core loss of the magnetic components. The maximum efficiency is about 97.29%.

Fig. 22 illustrates the loss distribution. As can be seen from Fig. 22, the core loss of the leakage (ac) inductors and the copper loss of each magnetic element are very small and can be ignored. According to the operating mode of the topology, the volt-second area of the transformers is independent of the input voltage and load, so the core loss of the transformer does not change. And it occupies a considerable proportion. Due to the voltage clamping of the clamp capacitor, the duty cycle does not change with load at the same input voltage. In the D-PWM mode, the duty cycle changes a little because the clamping voltage changes less. Therefore, the core loss of the dc inductor can also be regarded as a fixed loss under different loads. The achievement of ZVS of primary-side bottom switches (S_1, S_2, and S_3) requires large dc current ripple. The difference between the dc inductor current and the leakage inductor current flows into each switch on the primary side. Therefore, the current rms value and the turn OFF current in the switches, especially the primary-side bottom switches, increases as the load increases. The switching losses of primary-side bottom switches account for more than half of the total switching losses. But this proportion has decreased at light loads. The sum of the conduction losses of the primary-side bottom switches and secondary-side diodes occupies 90% of the total conduction loss.

V. Conclusion

A high-frequency isolated 3p-CF-SDAB dc–dc converter is proposed for unidirectional power-flow applications with wide input voltage range. The ideal power transferred expressions have been obtained for analyzing power transmission characteristics. The ideal rms expressions of the leakage inductor current are ideally derived for the optimal leakage inductance value design. The ideal soft-switching conditions based on charges have been given. In order to deal with the issue of that the 3p-CF-SDAB is uncontrollable when it operates under light-load or even no-load condition, a hybrid operating mode was proposed. Over medium- or heavy-load conditions, only DPPS is implemented. In comparison, under light-load conditions, the uncontrollable issue for CF-SDAB brought by using DPPS control can be solved with DPWM control by regulating the clamp voltage instantaneously. The validity of the proposed converter and the proposed control strategy has been verified by simulation and experimental results of a 2-kW prototype. The converter system has good steady state and dynamic performance even between operating mode transition. The converter with the proposed control has high conversion efficiency and work stably throughout the full load range. The loss distribution analysis is given.

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