Resonant Inductance Design and Loss Analysis of a Novel Resonant DC Link Inverter

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***Abstract*—To realize a soft-switching inverter with the advantages of a simple structure, high efficiency, low-voltage stress, and easy to control, a novel parallel resonant dc-link inverter with the function of pulse current regeneration is proposed in this paper. All switches in the inverter main circuit can achieve zero-voltage switching (ZVS) turn-ON and ZVS turn-OFF. In addition, all switches in the auxiliary commutation circuit (ACC) can achieve soft switching. The power in the ACC is small. Freewheeling diodes in the inverter turn OFF under zero current condition, which can reduce the reverse recovery loss of freewheeling diodes. In addition, the bulk capacitors are avoided in the circuit and there is no neutral point potential variation problem. At the same time, the zero-voltage duration is independent of the load current, and the time of transition can be selected freely. According to the equivalent circuits in different operation modes under the proposed modulation strategy, the operation principle, soft-switching implementation condition, and parameter design procedure of the proposed inverter are analyzed successively in this paper. Finally, a 10 kW, 10 kHz soft-switching inverter prototype with insulated gate bipolar transistor based switches is built. Experimental results are given to demonstrate the validity and features of the soft-switching inverter.**

***Index Terms*—Parallel resonant, resonant dc-link inverter, reverse recovery, zero-current switching (ZCS), zero-voltage switching (ZVS).**

I. Introduction

In THE field of power converter applications, such as motor drive, uninterruptible power supply, and new energy grid connected, continuous improvement in the performance and efficiency of inverters is required [1]–[3]. With the use of a soft-switching inverter technology, the switching loss of power device is obviously reduced and the switching frequency can be further increased while ensuring high efficiency. So the soft-switching technology has become a focus of research.

Among many soft-switching inverters, an auxiliary resonant commutated inverter is an important type. It can be divided into auxiliary resonant commutated pole (ARCP) inverters [2]–[12] and resonant dc-link (RDCL) inverters [13]–[29]. The ARCP soft-switching inverter topologies [6]–[9] have the following features: the control of auxiliary circuit and inverter are completely independent; the main switches and the auxiliary switches can realize soft switching; the soft-switching operation of main switches is not affected by the load condition; resonant inductor and main power channel are separated. These topologies are very suitable for high-power inverter applications. However, when applied to ARCP three-phase inverters, there are as many as 6 or 12 auxiliary switches, so the control is complex and the hardware cost is relatively high, especially in medium and small power applications.

Because RDCL inverters are simple and easy to control, they are widely concerned by experts in related fields and have been the key research direction of soft-switching inverters.

The work in [13] is the famous RDCL inverter topology proposed by Divan originally, which initiates the research on an RDCL inverter. But the inverter has following problems: the resonant peak value of dc bus voltage is too high, which increases the voltage stress of main switches; the voltage zero-crossing points are difficult to synchronize with the modulation strategy, so the inverter output contains a large number of harmonics; the resonant inductor locates in the main power channel, so the efficiency of the inverter is reduced.

In order to overcome the drawback of high-voltage stress on main switches, actively clamped RDCL (ACRDCL) inverters were proposed in [14]–[18]. However, the inductor power loss is still large because the resonant inductor is in the main power channel.

Later several parallel RDCL (PRDCL) inverters were proposed in [19]–[29]. These inverters not only limit the peak-voltage stress of the inverter's switches to the input dc voltage, but also avoid the resonant inductor being connected in series on the dc link, which greatly reduces the circuit loss. However, the PRDCL inverter topologies proposed so far also have some limitations. In [19]–[21], the PRDCL inverters require setting threshold of inductor's current or capacitor's voltage, and this will cause complex control. The PRDCL inverters proposed in [22]–[24] need not set threshold of inductor's current or capacitor's voltage, but they need to use two bulk capacitors, which not only has the problem of the neutral point potential variation but also increases the volume and weight of the inverter. The topology proposed in [25]–[27] avoids the use of two bulk capacitors, but these circuits need coupled inductors or transformers, which increases the complexity and cost of the circuit system design and reduces the practicability of the

Manuscript received November 1, 2018; revised February 19, 2019 and April 12, 2019; accepted June 16, 2019. Date of publication June 20, 2019; date of current version November 12, 2019. This work was supported in part by the National Natural Science Foundation of China under Grant 51977028. Recommended for publication by Associate Editor V. Agarwal. *(Corresponding author: Enhui Chu.)*

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Digital Object Identifier 10.1109/TPEL.2019.2924252

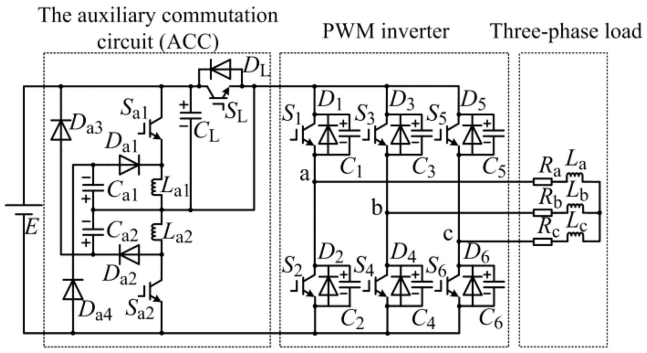

Fig. 1. Novel parallel resonant dc-link inverter.

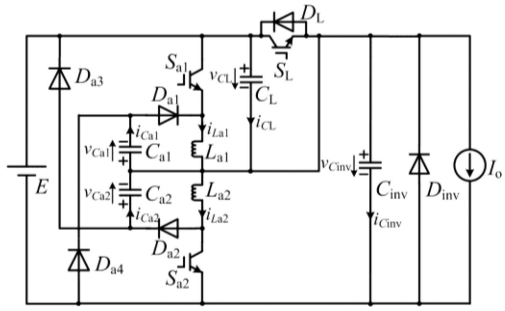

Fig. 2. Equivalent circuit of proposed inverter.

abovementioned circuit. Furthermore, auxiliary switches in the inverters proposed in [28] and [29] cannot achieve soft turn-ON, which will lead to the increase of switching loss.

In order to overcome the problems mentioned above, this paper puts forward a novel PRDCL inverter. The main advantages of the proposed topology are as follows.

1) The inverter avoids using two bulk capacitors, which eliminates the neutral point potential variation.
2) No resonance threshold limitation for auxiliary resonance circuit.
3) The main switches achieve zero-voltage switching (ZVS) turn-ON and ZVS turn-OFF. The bus switch achieves ZVS turn-ON and pseudo ZVS turn-OFF. The auxiliary switches achieve pseudozero-current switching (ZCS) turn-ON and pseudo ZVS turn-OFF.
4) The peak-voltage stress on the inverter's switches is limited to the dc supply voltage.
5) Freewheeling diodes turn OFF under zero current condition, which can restrict the production of electromagnetic interference (EMI) and reduce the reverse recovery loss of freewheeling diodes.
6) The proposed inverter can generate voltage notches of the dc link at controllable instants and keep the dc-link voltage at zero for arbitrary period whenever the main switches in the inverter need to change their status.

Therefore, various modulation strategies can be used for controlling the inverter instead of the DPM technique, which causes undesirable subharmonics. According to the equivalent circuits in different operation modes, the operation principle, soft-switching implementation condition, and parameter design procedure of the proposed inverter are analyzed successively in this paper. Finally, experimental results are given to demonstrate the validity of the proposed inverter.

II. Circuit Topology and Operation Principle

A. Circuit Topology

Fig. 1 shows the novel PRDCL inverter topology. The system includes the dc voltage source, auxiliary commutation circuit (ACC), and conventional pulsewidth modulation (PWM) inverter. The ACC consists of the bus switch (S_L) and its antiparallel diode (D_L), auxiliary switches $(S_{a1},\ S_{a2})$, main resonant capacitor (C_L), auxiliary resonant capacitors $(C_{a1},\ C_{a2})$, auxiliary resonant inductors $(L_{a1},\ L_{a2})$, auxiliary diodes $(D_{a1},\ D_{a2})$, and energy regeneration feedback diodes $(D_{a3},\ D_{a4})$. In the PWM inverter, main switches S_1–S_6 are paralleled with snubber capacitors C_1–C_6, whose values are equal to C_s, respectively. The inverter system shown in Fig. 1 can be simplified to that shown in Fig. 2. The load current I_o represents the PWM inverter in the period of each switching cycle. In order to facilitate the analysis, several assumptions are employed as follows.

1) All switches, diodes, capacitors, and inductors are ideal devices.
2) The load current I_o is approximately constant during one switching cycle, because the inverter's load inductance is much larger than the resonant inductance. In addition, the value and direction of the load current I_o depend on the individual phase currents and the states of the six inverter's main switches.
3) The diode $D_{\rm inv}$ represents the freewheeling diodes antiparalleled with the inverter's main switches. In addition, the equivalent capacitance $C_{\rm inv}$, whose value is $3C_s$, represents the snubber capacitors antiparalleled with the inverter's main switches.
4) The values of main resonant capacitor C_L and equivalent capacitor $C_{\rm inv}$ are $C_L = C_{\rm inv} = C_a = 3C_s$. The values of auxiliary resonant capacitors C_{a1} and C_{a2} are $C_{a1} = C_{a2} = C_b$. The values of auxiliary resonant inductors L_{a1} and L_{a2} are $L_{a1} = L_{a2} = L$.
5) The referential positive directions of physical quantities in the ACC are consistent with the directions of arrowheads in Fig. 2.

B. Operation Principle

The control of the novel PRDCL inverter mainly includes two parts: the control of the ACC and the control of the PWM inverter main circuit. The control of the PWM inverter main circuit is similar to the hard-switching inverter. The main power switches operate in the mode of sinusoidal PWM. Meanwhile the upper and lower main power switches of one bridge conduct complementarily with a phase difference of π. The ACC provides ZVS condition for the main switches of the PWM inverter.

Fig. 3 shows the modulation strategy of the novel PRDCL inverter. $t_{\rm dead}$ is the dead time in conventional hard-switching PWM inverters. The operation sequence of each switch under the modulation strategy is that to achieve ZVS turn-OFF and ZVS turn-ON for all switches in the inverter main circuit, the moment of turning OFF the bus switch S_L is advanced for δ_1 compared

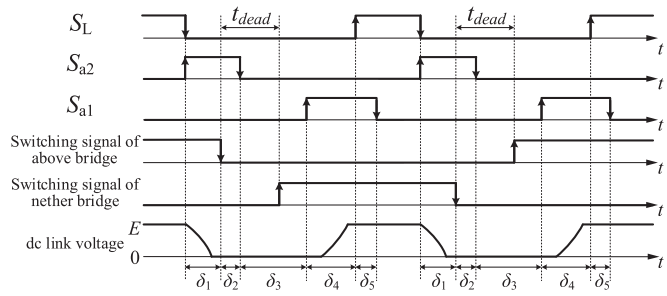

Fig. 3. Modulation strategy.

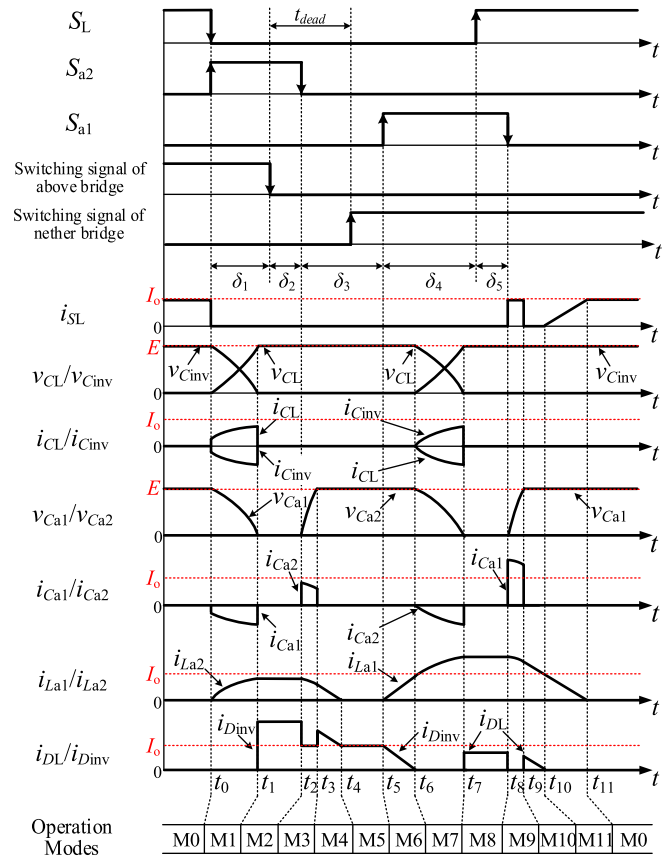

Fig. 4. Key theoretical waveforms of the circuit.

with that of turning OFF the main switch. At the moment of turning OFF the bus switch S_L, the auxiliary switches S_{a2} is turned ON immediately. In order to achieve ZVS turn-OFF for the auxiliary switch S_{a2} reliably, the moment of turning OFF the auxiliary switch S_{a2} is prolonged for δ_2 compared with that of turning OFF the main switch. The moment of turning ON the auxiliary switch S_{a1} is prolonged for δ_3 compared with that of turning OFF the auxiliary switch S_{a2} (the zero-voltage duration can be changed by adjusting δ_3). In order to achieve ZVS turn-ON for the bus switch S_L, the moment of turning ON the bus switch S_L is prolonged for δ_4 compared with that of turning ON auxiliary switch S_{a1}. In addition, the moment of turning OFF the auxiliary switch S_{a1} is prolonged for δ_5 compared with that of turning ON the bus switch S_L.

The key theoretical waveforms are shown in Fig. 4 and the equivalent circuits of different operation modes are shown in Fig. 5. In the following, the operation modes of the circuit are analyzed in detail.

Mode 0 [~t_0]: Before t_0, S_L is in the turn-ON state and S_{a1} and S_{a2} are in the turn-OFF state. The dc voltage source E supplies energy to the load via S_L and the circuit works in the steady state. $v_{CL}(t_0) = v_{Ca2}(t_0) = 0, v_{Ca1}(t_0) = v_{C\mathrm{inv}}(t_0) = E$, $i_{SL}(t_0) = I_o$.

Mode 1 [t_0, t_1]: At instant t_0, S_L is turned OFF meanwhile S_{a2} is turned ON and D_{a4} conducts. C_L, C_{a1}, and C_{inv} resonate with L_{a2} while supplying the load current I_o. C_L is charged and C_{a1} and C_{inv} are discharged. Under the restriction of C_L, C_{a1}, and C_{inv}, the voltage of S_L cannot be changed abruptly, so S_L achieves pseudo ZVS turn-OFF. Due to the effect of series inductor L_{a2}, the current of S_{a2} rises from zero, so S_{a2} achieves pseudo ZCS turn-ON. In this mode, the current and voltage expressions of C_L, C_{a1}, C_{inv}, and L_{a2} are

$$i_{C_L}(t) = -i_{C\mathrm{inv}}(t) = \frac{C_a}{2C_a + C_b} \cdot \left(\frac{E}{\omega_1 L} \sin \omega_1 t + I_o \cos \omega_1 t \right) \tag{1}$$

$$i_{Ca1}(t) = -\frac{C_b}{2C_a + C_b} \cdot \left(\frac{E}{\omega_1 L} \sin \omega_1 t + I_o \cos \omega_1 t \right) \tag{2}$$

$$i_{La2}(t) = \frac{E}{\omega_1 L} \sin \omega_1 t + I_o \left(\cos \omega_1 t - 1 \right) \tag{3}$$

$$v_{C_L}(t) = E \left(1 - \cos \omega_1 t \right) + \omega_1 L I_o \sin \omega_1 t \tag{4}$$

$$v_{C\mathrm{inv}}(t) = v_{Ca1}(t) = v_{La2}(t) = E \cos \omega_1 t - \omega_1 L I_o \sin \omega_1 t \tag{5}$$

where $\omega_1 = \frac{1}{\sqrt{L \cdot (2C_a + C_b)}}$.

At instant t_1, the voltages of C_{a1} and C_{inv} fall to zero and the voltage of C_L rises to E. D_{a4} turns OFF and D_{inv} conducts and mode 1 ends. The operation time t_{0-1} of this mode is obtained by (5)

$$t_{0-1} = \frac{1}{\omega_1} \cdot \arctan \left(\frac{E}{\omega_1 L I_o} \right). \tag{6}$$

Mode 2 [t_1, t_2]: At instant t_1, D_{a4} turns OFF and D_{inv} conducts. The current of L_{a2} reaches the maximum value $i_{La2\,\max}$. The load current I_o freewheels via D_{inv}, and the current of L_{a2} circulates in the loop formed by L_{a2}, S_{a2}, and D_{inv} at a constant value $i_{La2\,\max}$. When S_{a2} is turned OFF, mode 2 ends. In this mode, the current expressions of L_{a2} and D_{inv} are

$$i_{La2\max} = \sqrt{\left(\frac{E}{\omega_1 L} \right)^2 + I_o^2} - I_o \tag{7}$$

$$i_{D\mathrm{inv}}(t) = \sqrt{\left(\frac{E}{\omega_1 L} \right)^2 + I_o^2}. \tag{8}$$

The operation time t_{1-2} of this mode is

$$t_{1-2} = \delta_1 + \delta_2 - \frac{1}{\omega_1} \cdot \arctan \left(\frac{E}{\omega_1 L I_o} \right). \tag{9}$$

Mode 3 [t_2, t_3]: At instant t_2, S_{a2} is turned OFF and D_{a2} conducts. L_{a2} starts to resonate with C_{a2}. Under the restriction of C_{a2}, the voltage of S_{a2} cannot be changed abruptly, so S_{a2}

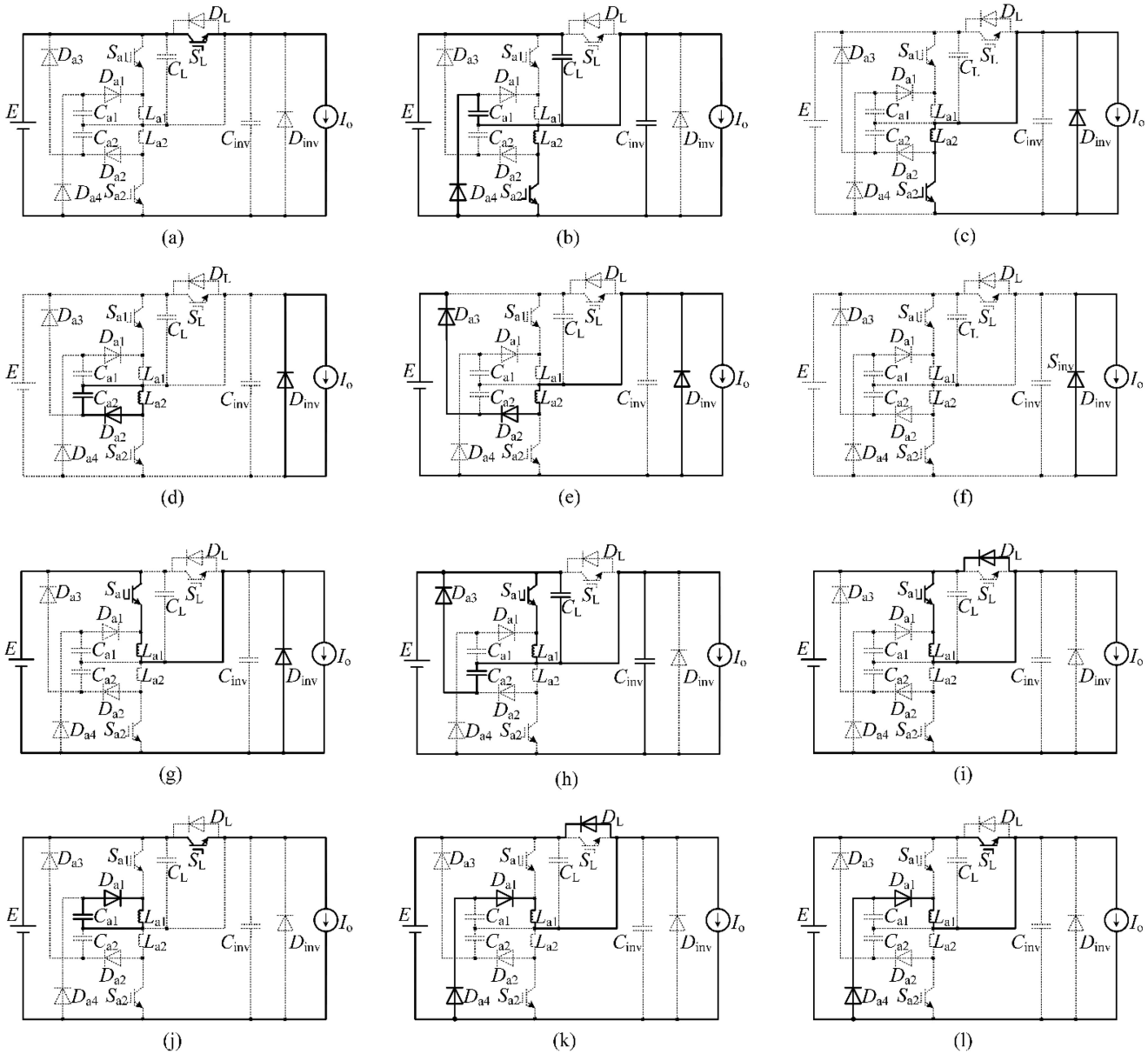

Fig. 5. Equivalent circuits of different operation modes. (a) Mode 0. (b) Mode 1. (c) Mode 2. (d) Mode 3. (e) Mode 4. (f) Mode 5. (g) Mode 6. (h) Mode 7. (i) Mode 8. (j) Mode 9. (k) Mode 10. (l) Mode 11.

achieves pseudo ZVS turn-OFF. In this mode, the voltage and current expressions of L_{a2} and C_{a2} are

$$v_{Ca2}(t) = -v_{La2}(t) = \omega_2 L i_{La2\max} \sin \omega_2 t \tag{10}$$

$$i_{Ca2}(t) = i_{La2}(t) = i_{La2\max} \cos \omega_2 t \tag{11}$$

where $\omega_2 = \frac{1}{\sqrt{LC_b}}$.

At instant t_3, the voltage of C_{a2} is charged to E. D_{a3} turns ON and mode 3 ends. The operation time $t_{2\text{–}3}$ of this mode is obtained by (10)

$$t_{2\text{–}3} = \frac{1}{\omega_2} \cdot \arcsin\left(\frac{E}{\omega_2 L i_{La2\max}}\right). \tag{12}$$

Mode 4 [t_3, t_4]: At instant t_3, D_{a3} turns ON. L_{a2} feeds back energy to dc voltage source E via D_{a2}, D_{a3}, and D_{inv}. In this mode, the current expressions of L_{a2} and D_{inv} are

$$i_{La2}(t) = i_{La2}(t_3) - \frac{E}{L}t \tag{13}$$

$$i_{D\text{inv}}(t) = i_{La2}(t_3) - \frac{E}{L}t + I_o. \tag{14}$$

At instant t_4, the current of L_{a2} falls to zero. D_{a2} and D_{a3} turn OFF and mode 4 ends. The operation time $t_{3\text{–}4}$ of this mode is obtained by (13)

$$t_{3\text{–}4} = \frac{L i_{La2}(t_3)}{E}. \tag{15}$$

Mode 5 [t_4, t_5]: At instant t_4, D_{a2} and D_{a3} turn OFF. The load current I_o freewheels via $D_{\rm inv}$, which is the same as the freewheeling operation mode of a conventional hard-switching inverter.

The operation time t_{4-5} of this mode is

$$t_{4-5} = \delta_3 - \frac{1}{\omega_2} \cdot \arcsin\left(\frac{E}{\omega_2 L i_{La2\max}}\right) - \frac{L i_{La2}(t_3)}{E}. \quad (16)$$

At instant t_5, S_{a1} is turned ON and mode 5 ends. From t_1 to t_5, the dc-link voltage is zero, which creates ZVS condition for the main switches. The dc-link zero-voltage duration can be easily adjusted by changing the turn-ON point of S_{a1}.

Mode 6 [t_5, t_6]: At instant t_5, S_{a1} is turned ON. The load current I_o starts to linearly shift from $D_{\rm inv}$ to L_{a1}. Due to the effect of series inductor L_{a1}, the current of S_{a1} linearly rises from zero, so S_{a1} achieves pseudo ZCS turn-ON. In this mode, the current expressions of L_{a1} and $D_{\rm inv}$ are

$$i_{La1}(t) = \frac{E}{L} \cdot t \quad (17)$$

$$i_{D\rm inv}(t) = I_o - \frac{E}{L} \cdot t. \quad (18)$$

At instant t_6, the current of L_{a1} linearly rises to I_o meanwhile the current of $D_{\rm inv}$ linearly falls to zero and $D_{\rm inv}$ naturally turns OFF. D_{a3} conducts and mode 6 ends. The operation time t_{5-6} of this mode is obtained by (17)

$$t_{5-6} = \frac{L}{E} \cdot I_o. \quad (19)$$

Mode 7 [t_6, t_7]: At instant t_6, $D_{\rm inv}$ turns OFF and D_{a3} conducts. L_{a1} resonates with C_L, C_{a2}, and $C_{\rm inv}$. $C_{\rm inv}$ is charged, C_L and C_{a2} are discharged. The voltage and current expressions of C_L, C_{a2}, $C_{\rm inv}$, and L_{a1} are

$$i_{C_L}(t) = -i_{C\rm inv}(t) = -\frac{C_a}{2C_a + C_b} \cdot \frac{E}{\omega_1 L} \sin \omega_1 t \quad (20)$$

$$i_{Ca2}(t) = -\frac{C_b}{2C_a + C_b} \cdot \frac{E}{\omega_1 L} \sin \omega_1 t \quad (21)$$

$$i_{La1}(t) = \frac{E}{\omega_1 L} \sin \omega_1 t + I_o \quad (22)$$

$$v_{C_L}(t) = v_{Ca2}(t) = v_{La1}(t) = E \cos \omega_1 t \quad (23)$$

$$v_{C\rm inv}(t) = E\left(1 - \cos \omega_1 t\right). \quad (24)$$

At instant t_7, the voltage of $C_{\rm inv}$ rises to E and the voltages of C_L and C_{a2} fall to zero. D_{a3} turns OFF and D_L conducts and mode 7 ends. The operation time t_{6-7} of this mode is obtained by (24)

$$t_{6-7} = \frac{\pi}{2} \cdot \sqrt{(2C_a + C_b)\, L}. \quad (25)$$

At the moment, the current of L_{a1} reaches the maximum value $i_{La1\max}$ as

$$i_{La1\max} = \frac{E}{\omega_1 L} + I_o = E \cdot \sqrt{\frac{2C_a + C_b}{L}} + I_o. \quad (26)$$

Mode 8 [t_7, t_8]: At instant t_7, D_{a3} turns OFF and D_L conducts. The current of L_{a1} reaches the maximum value $i_{La1\max}$. At the moment, the current of L_{a1} consists of two parts. One part balances with the load current I_o and the other part of the resonance current circulates in the loop formed by L_{a1}, D_L, and S_{a1}. The conduction of D_L creates ZVS turn-ON condition for S_L. When S_{a1} is turned OFF, mode 8 ends. In this mode, the current expressions of L_{a1} and $D_{\rm inv}$ are

$$i_{La1}(t) = \frac{E}{\omega_1 L} + I_o = E \cdot \sqrt{\frac{2C_a + C_b}{L}} + I_o \quad (27)$$

$$i_{D_L}(t) = \frac{E}{\omega_1 L} = E \cdot \sqrt{\frac{2C_a + C_b}{L}}. \quad (28)$$

The operation time t_{7-8} of this mode is

$$t_{7-8} = \delta_4 + \delta_5 - \frac{L}{E} \cdot I_o - \frac{\pi}{2} \cdot \sqrt{(2C_a + C_b)\, L}. \quad (29)$$

Mode 9 [t_8, t_9]: At instant t_8, S_{a1} is turned OFF and D_L turns OFF. The load current I_o flows through S_L. L_{a1} starts to resonate with C_{a1}. Under the restriction of C_{a1}, the voltage of S_{a1} cannot be changed abruptly, so S_{a1} achieves pseudo ZVS turn-OFF. In this mode, the voltage and current expressions of L_{a1} and C_{a1} are

$$v_{Ca1}(t) = -v_{La1}(t) = \omega_2 L i_{La1\max} \sin \omega_2 t \quad (30)$$

$$i_{Ca1}(t) = i_{La1}(t) = i_{La1\max} \cos \omega_2 t. \quad (31)$$

At instant t_9, the voltage of C_{a1} rises to E. D_{a4} and D_L conduct and mode 9 ends. The operation time t_{8-9} of this mode is obtained by (30)

$$t_{8-9} = \frac{1}{\omega_2} \cdot \arcsin\left(\frac{E}{\omega_2 L i_{La1\max}}\right). \quad (32)$$

Mode 10 [t_9, t_{10}]: At instant t_9, D_{a4} and D_L conduct. L_{a1} feeds back energy to dc voltage source E via D_{a1}, D_{a4}, and D_L. In this mode, the current expressions of L_{a1} and D_L are

$$i_{La1}(t) = i_{La1}(t_9) - \frac{E}{L} t \quad (33)$$

$$i_{D_L}(t) = i_{La1}(t_9) - \frac{E}{L} t - I_o. \quad (34)$$

At instant t_{10}, the current of L_{a1} linearly falls to I_o. D_L naturally turns OFF and mode 10 ends. The operation time t_{9-10} of this mode is obtained by (33)

$$t_{9-10} = \frac{L\left[i_{La1}(t_9) - I_o\right]}{E}. \quad (35)$$

Mode 11 [t_{10}, t_{11}]: At instant t_{10}, D_L turns OFF. The load current I_o starts to linearly shift from L_{a1} to S_L. In this mode, the current expression of L_{a1} is

$$i_{La1}(t) = I_o - \frac{E}{L} t. \quad (36)$$

At instant t_{11}, the current of L_{a1} falls to zero. The load current I_o is completely shifted to S_L and the mode 11 ends. The operation time t_{10-11} of this mode is obtained by (36)

$$t_{10-11} = \frac{L I_o}{E}. \quad (37)$$

TABLE I
VOLTAGE AND CURRENT STRESSES OF COMPONENTS

	The RCDL inverter
Voltage stress	
Main switches (S_1~S_6)	E
The bus switch (S_L)	E
Auxiliary switches (S_{a1}, S_{a2})	E
Diodes(D_1~D_6, D_{a1}~D_{a4}, D_L)	E
Current stress	
Main switches (S_1~S_6)	$E\cdot\frac{C_s}{\sqrt{(6C_s+C_b)L}}+I_{\text{omax}}$
The bus switch (S_L)	I_{omax}
The auxiliary switch (S_{a1})	$E\cdot\sqrt{\frac{2C_a+C_b}{L}}+I_{\text{omax}}$
The auxiliary switch (S_{a2})	$E\cdot\sqrt{\frac{2C_a+C_b}{L}}$

After this mode, the circuit returns to the initial steady-state Mode 0 and the commutation process ends.

III. STEADY-STATE CHARACTERISTICS

A. Maximum Current and Voltage Stresses of Components

The voltage and current stresses of each component in the circuit are shown in Table I. The voltage stresses of main switches, the bus switch, auxiliary switches, and diodes are equal to dc voltage source E. The current stress of main switches equals the summation of the maximum resonance current through snubber capacitor and the maximum load current. The current stress of the bus switch S_L equals the maximum load current. The current stress of an auxiliary switch S_{a1} equals the summation of the maximum resonance current and the maximum load current, which shows that the current through an auxiliary switch S_{a1} is the summation of resonance current and the load current at the commutation moment. In addition, the current stress of an auxiliary switch S_{a2} equals the maximum resonance current. (Note: $I_{o\max}$ indicates the maximum load current).

B. di/dt of Auxiliary Switches and Freewheeling Diodes

According to (17) and (18), during turn-ON transient of an auxiliary switch, the current change rates of both auxiliary switch and freewheeling diode are

$$di/dt = \frac{E}{L}. \tag{38}$$

According to (38), during turn-ON transient of the auxiliary switch, the current change rates of both auxiliary switch and freewheeling diode are constant. It means the currents of both auxiliary switch and freewheeling diode vary linearly and these change rates can be set arbitrarily in the parameter design.

C. Soft-Switching Implementation Condition

1) ZVS Implementation Condition of Main Switch: According to the analysis of operation principle, in order to achieve ZVS turn-OFF and ZVS turn-ON for main switches, the commutation time δ_1 should meet $\delta_1 \geq t_{0\text{–}1}$. According to (6), the relationship is

$$\delta_1 \geq \frac{\pi}{2}\cdot\sqrt{(2C_a+C_b)L}. \tag{39}$$

2) ZVS Implementation Condition of Bus Switch: On the basis of the analysis mentioned above, in order to achieve ZVS turn-ON for the bus switch S_L, the commutation time δ_4 should meet $\delta_4 \geq t_{5\text{–}6} + t_{6\text{–}7}$. According to (19) and (25), the relationship is

$$\delta_4 \geq \frac{L_{I_{o\max}}}{E} + \frac{\pi}{2}\cdot\sqrt{(2C_a+C_b)L}. \tag{40}$$

3) ZCS Implementation Condition of Auxiliary Switch: In order to enable the current through the auxiliary resonant inductor to drop to zero when the auxiliary switch is turned ON, the commutation time δ_3 should meet $\delta_3 \geq t_{2\text{–}3} + t_{3\text{–}4}$. According to (12) and (15), the relationship is

$$\delta_3 \geq \sqrt{LC_b}\arcsin\left(\frac{E}{i_{La2\max}}\sqrt{\frac{C_b}{L}}\right) + L\cdot\sqrt{\left(\frac{i_{La2\max}}{E}\right)^2 - \frac{C_b}{L}}. \tag{41}$$

IV. PARAMETER DESIGN

A. Design Methodology

1) Assume the dc voltage source is E and the output maximum load current is $I_{o\max}$.
2) The delay time δ_1, δ_4, and δ_3 should meet (39)–(41).
3) According to (19) and (25), the equations are transformed to

$$L = \frac{E}{I_{o\max}}t_{5\text{–}6} \tag{42}$$

$$2C_a + C_b = \frac{4}{\pi^2 L}t_{6\text{–}7}^2. \tag{43}$$

The parameter design of the ACC in the novel PRDCL inverter should follow (39)–(43).

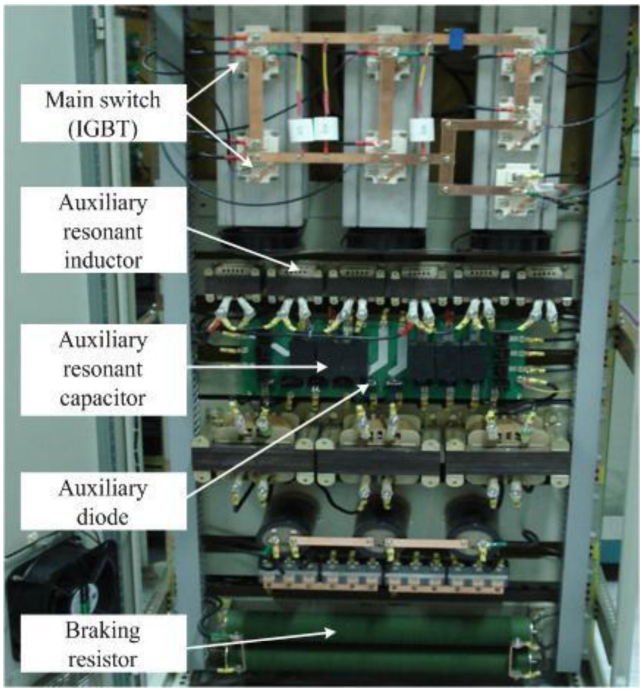

Fig. 6. Photo of the 10-kW three-phase soft-switching PWM inverter prototype.

B. Design Example

In the following, a design example is explained. The dc voltage source E is 400 V and the output maximum load current $I_{o\max}$ is 50 A.

Assume the commutation time ($t_{5-6}+t_{6-7}$) is 1.5 μs, and during t_{6-7} the current change rate of the auxiliary resonant inductor is $di/dt = 100$ A/μs. According to (38) and (42), $L = 4$ μH, $t_{5-6} = 0.5$ μs. So, $t_{6-7} = 1$ μs. According to (43), <ieqn>$2C_a + C_b =$ 100 nF. Take $C_a = 45$ nF, then $C_b = 10$ nF. As is known from the analysis mentioned above, δ_1 δ_3 and δ_4 should meet $\delta_1 \geq t_{0-1} = 1$ μs, $\delta_3 \geq t_{2-3} + t_{3-4} = 0.66$ μs, $\delta_4 \geq t_{5-6} + t_{6-7} = 1.5$ μs.

V. Experimental Results

In order to demonstrate the validity of the aforementioned analysis, a 10-kW PRDCL three-phase PWM soft-switching inverter prototype is built. The parameters of the modulation strategy are $\delta_1 = 1$ μs, $\delta_4 = 2$ μs, and $t_{\text{dead}} = 3$ μs. Fig. 6 shows the photo of the three-phase soft-switching inverter prototype. The parameters of components in the circuit are described in Table II. (Note: The dc voltage source E must be able to regenerate pulse power when the inverter works without large capacity capacitor.)

A. Operation Confirmation and Waveforms Evaluation

Fig. 7 shows the voltage waveform of the dc-link voltage $v_{C\text{inv}}$ and the current waveforms of the commutation inductor current i_{La1} and i_{La2}. It is known that the dc-link voltage falls from E to zero, and then rises again to E, a zero-voltage notch appears.

TABLE II
Components and Parameters of the Prototype

Components	Parameters
Control board	DSP TMS320F2812
Driver board	SKHI23/17
DC voltage source (E)	400 V
Output maximum load current ($I_{o\max}$)	50 A
Switching frequency (f_s)	10 kHz
Output frequency (f_o)	50 Hz
S_L and S_1~S_6	SKM75GB063D(600 V,100 A)
S_{a1} and S_{a2}	IRG4PC50K (600 V, 52 A)
D_{a1}~D_{a4}	RHRG5060 (600 V, 50 A)
C_1~C_6	15 nF
C_L	47 nF
C_{a1} and C_{a2}	10 nF
L_{a1} and L_{a2}	Self-made winding air core inductor L=4 μH, R_L=15 mΩ

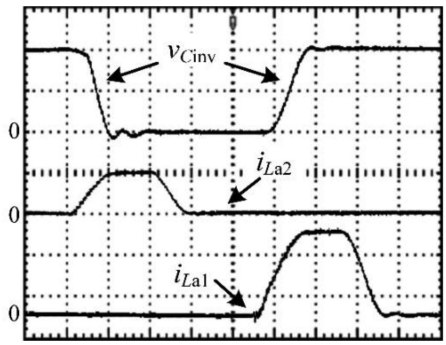

Fig. 7. Waveforms of the dc-link voltage $v_{C\text{inv}}$ and the commutation inductor currents i_{La1}, i_{La2} (scales: 200 V/div, 40 A/div, 1 μs/div).

So the switching devices of the proposed inverter can achieve ZVS turn-ON and ZVS turn-OFF when the dc-link voltage is zero and the dc-link voltage changes through the resonance between the resonant inductor and resonant capacitor. Thus, the circuit can operate at a higher frequency independent of current. Moreover, the duration of the zero-voltage can be selected according to the requirements of the soft switching, and it can occur at any time according to the requirements of the proposed inverter PWM modulation.

Fig. 8 shows waveforms of voltages and currents of bus switch S_L and commutation switch S_{a1} during turn-ON and turn-OFF transition. Fig. 8(a) shows the voltage and current waveforms of S_L during turn-ON transition. Fig. 8(b) shows the voltage and

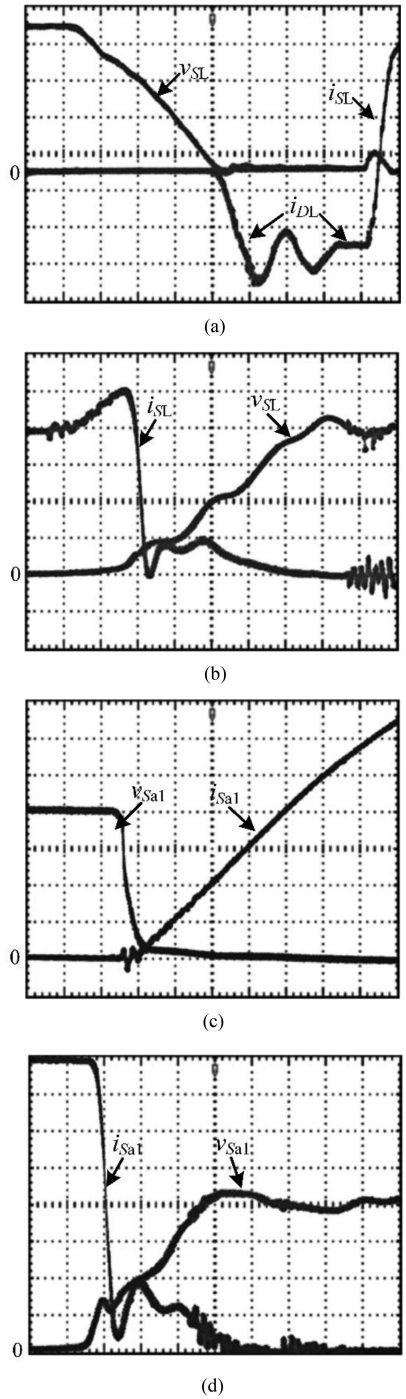

Fig. 8. Waveforms of S_L and S_{a1} during turn-ON and turn-OFF transition. (a) Bus switch S_L turn-ON (scales: 100 V/div, 10 A/div, 200 ns/div). (b) Bus switch S_L turn-OFF (scales: 100 V/div, 10 A/div, 100 ns/div). (c) Commutation switch S_{a1} turn-ON (scales: 100 V/div, 10 A/div, 100 ns/div). (d) Commutation switch S_{a1} turn-OFF (scales: 100 V/div, 10 A/div, 100 ns/div).

current waveforms of S_L during turn-OFF transition. Fig. 8(c) shows the voltage and current waveforms of S_{a1} during turn-ON transition. Fig. 8(d) shows the voltage and current waveforms of S_{a1} during turn-OFF transition. As is shown from Fig. 8, the bus switch S_L achieves ZVS turn-ON and pseudo ZVS turn-OFF, and the auxiliary switch S_{a1} achieves pseudo ZCS turn-ON and pseudo ZVS turn-OFF.

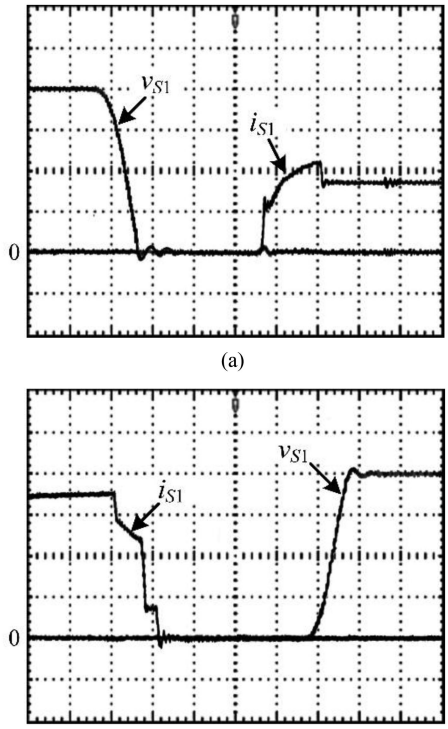

Fig. 9. Waveforms of S_1 during turn-ON and turn-OFF transition. (a) Main switch S_1 turn-ON (scales: 100 V/div, 20 A/div, 1 μs/div). (b) Main switch S_1 turn-OFF (scales: 100 V/div, 10 A/div, 1 μs/div).

Fig. 9 shows waveforms of voltages and currents of main switch S_1 of the proposed inverter during turn-ON and turn-OFF transition. Fig. 9(a) shows the voltage and current waveforms of S_1 during turn-ON transition. Fig. 9(b) shows the voltage and current waveforms of S_1 during turn-OFF transition. As is shown from Fig. 9, the main switch S_1 achieves ZVS turn-ON and ZVS turn-OFF.

Fig. 10 shows the output phase current waveforms and harmonic analysis of the proposed inverter under the resistive and inductive load. Fig. 10(a) shows the output phase current waveforms of the proposed inverter. Fig. 10(b) shows the harmonic analysis of A-phase output current i_a of the proposed inverter. As can be seen from Fig. 10, the output phase current waveform of the inverter is smooth, and the total harmonic distortion (THD) of the output phase current i_a is 0.68%, and the distortion is very small.

Fig. 11 shows the common mode conducted electromagnetic noise EMI characteristic curves of the proposed inverter and the conventional hard-switching inverter (with output filter). From Fig. 11, it can be known that the spectrum peak of the common mode conducted electromagnetic noise EMI of the proposed inverter is lower than that of the hard-switching inverter in the frequency range of 10 kHz–30 MHz. So the proposed inverter can effectively reduce the common mode conducted electromagnetic noise EMI.

B. Efficiency Evaluation

Fig. 12 shows the theoretical loss distribution of the proposed inverter and the hard-switching inverter when the output power

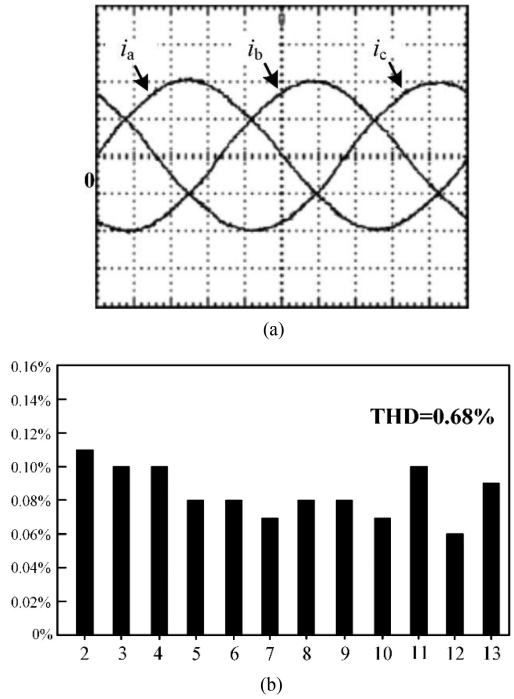

Fig. 10. Inverter output phase current waveforms and harmonic analysis under the resistive and inductive load. (a) Output phase current (scales: 20 A/div, 2 ms/div). (b) Harmonic analysis of A-phase output current i_a.

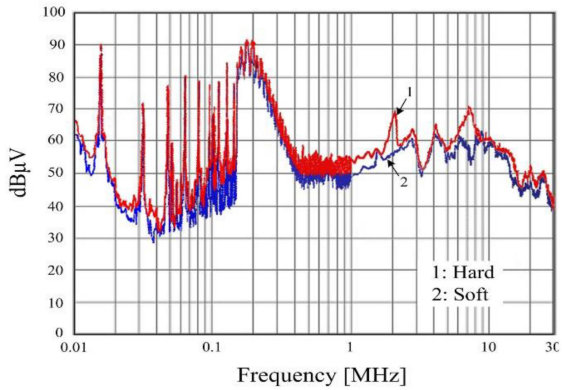

Fig. 11. Measured electromagnetic noise characteristic (output power is 5 kW).

P_o is 10 kW. The theoretical loss analysis is carried out under the same condition as the experiment. In the theoretical loss analysis of the proposed inverter, it is assumed that the switching loss of the main switch is zero, and only the conduction loss of main switch and its antiparallel diode is considered. As shown in Fig. 12, compared with the hard-switching inverter, although the proposed inverter has added the loss of ACC 91 W, which includes the loss of the bus switch $S_L(D_L)$ 35 W (the conduction loss of S_L 25 W and the turn-OFF loss of S_L 4 W and the conduction loss of D_L 6 W) and the loss of auxiliary switch S_{a1} and S_{a2} 38 W and the loss of auxiliary diodes D_{a1}–D_{a4} 10 W, and the loss of auxiliary resonant inductors L_{a1}, L_{a2} 17 W, and resonant capacitor C_L, C_{a1}, and C_{a2} 2 W. The main switch IGBT loss is reduced by 236 W, so the total loss of the proposed inverter is 65.38% of that in the hard-switching inverter. The theoretical

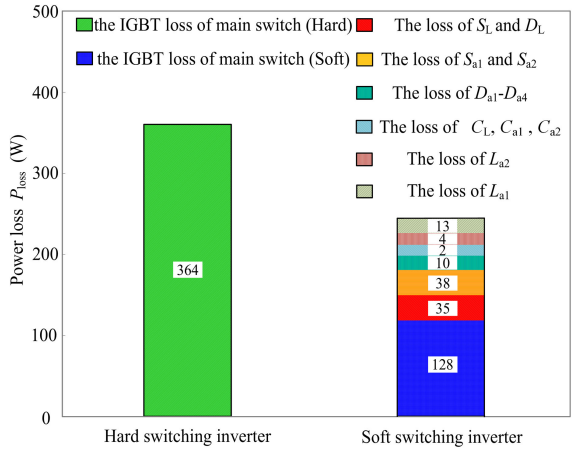

Fig. 12. Power loss distribution.

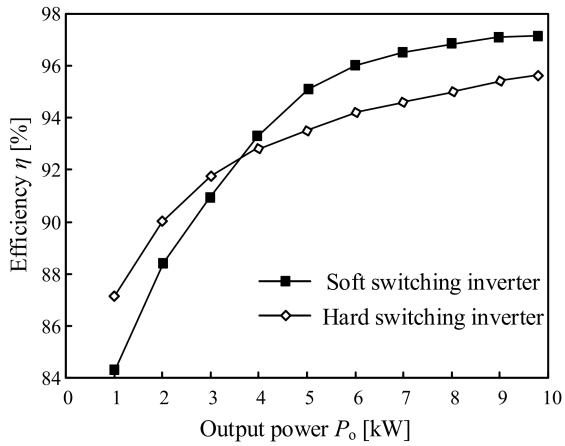

Fig. 13. Experimental efficiency curves.

loss analysis shows that the total loss of the proposed inverter is 230 W (conversion efficiency is 97.75%), and the total loss of the hard-switching inverter is 364 W (conversion efficiency is 96.48%). So the theoretical loss of the proposed inverter is reduced by 126 W, and the efficiency is improved by 1.27%.

Fig. 13 shows the experimental efficiency curves of the proposed inverter and the hard-switching inverter (without output transformer). As shown in Fig. 13, when the output power is less than 40% of rated power (4 kW), the efficiency of the proposed inverter is unsatisfactory, even lower than the hard-switching inverter, especially at light load. Because there will also be some resonance current through the ACC at light or no load. Thus, the loss of ACC is higher than the hard-switching inverter. However, when the output power is more than 40% of rated power (4 kW), the efficiency of the proposed inverter is obviously improved. Near the rated load 10 kW, the proposed inverter can achieve a high efficiency 97.14%. Compared with the efficiency of the hard-switching inverter 95.52%, it improved about by 1.62%.

The efficiency improvement results of theoretical analysis and experimental measurement are 1.38% and 1.62%, respectively. It can be considered that the efficiency improvement of theoretical analysis is approximately consistent with experimental measurement.

From the abovementioned analysis, it can be seen that the theoretical calculation efficiency is higher than the actual power efficiency. This is because the circuit stray parameter losses, such as line resistor, internal resistor of power devices, and equivalent ESL of resonant capacitors during commutation process, are not included in the theoretical loss calculation model.

VI. Conclusion

A novel PRDCL inverter circuit is proposed in this paper. By theoretical analysis and experiment on the 10-kW PRDCL inverter prototype, the soft-switching inverter has the following features.

1) The inverter avoids using two bulk capacitors, which eliminates the neutral point potential variation.
2) The inverter need not set threshold of inductor's current or capacitor's voltage.
3) The peak-voltage stress on the inverter's switches is limited to the dc supply voltage.
4) The main switches achieve ZVS turn-ON and ZVS turn-OFF. The bus switch achieves ZVS turn-ON and pseudo ZVS turn-OFF. The auxiliary switches achieve pseudo ZCS turn-ON and pseudo ZVS turn-OFF. It is beneficial to reduce the switching loss and further improve the switching frequency.
5) Freewheeling diodes turn OFF under zero current condition, which can restrict the production of EMI and reduce the reverse recovery loss of freewheeling diodes.
6) Due to the loss caused by resonant current is relatively large below the half rated load, the efficiency is not improved obviously, even lower than the hard-switching inverter efficiency (this problem needs to be solved in the future). However, the efficiency advantage of the proposed inverter is obviously over the half rated load, and a high efficiency of 97.14% can be obtained near the rated load 10 kW. Compared with the efficiency of the hard-switching inverter 95.52%, it is improved by 1.62%.
7) The THD of the output current is 0.68%, and the distortion is very small.
8) The proposed inverter can generate voltage notches of the dc link at controllable instants and keep the dc-link voltage at zero for arbitrary period whenever the main switches in the inverter need to change their status. Control of resonance is based on time sequence without detecting any current or voltage, so it is more convenient for engineering implementation.

Appendix
Loss Analysis of ACC

In comparison with the conventional hard-switching inverter, there is no switching loss of main switches in the proposed inverter. But the inverter increases the loss of ACC. The loss of ACC can be calculated based on the current analysis of circuits, and it consists of eight parts.

1) Switching Loss of Bus Switch S_L. $P_{sw(bus)}$: The bus switch S_L is ZVS turn-ON and pseudo ZVS turn-OFF. So the switching loss of the bus switch S_L only includes turn-OFF loss as

$$P_{\mathrm{sw(bus)}} = f_o \cdot \sum_{n=1}^{N} E_{\mathrm{off(bus)}}(n). \tag{A1}$$

where f_o is the output current/voltage frequency. N is the switching number of the bus switch during a period of output current/voltage. $E_{\mathrm{off(bus)}}$ (n) is the turn-OFF loss when the bus switch, paralleled with a 47 nF capacitor, is turned OFF during the nth switching period of the bus switch S_L. It is measured through experiment and related to the value of $i_{SL}(n)$, which is the current through the bus switch S_L when the bus switch is turned OFF in the nth time.

2) Conduction Loss of Bus Switch Component S_L/D_L. $P_{con(bus)}$: The conduction loss of a bus switch component S_L/D_L consists of the loss $P_{\mathrm{con1(bus)}}$ caused by the load current flowing through the bus switch S_L and the loss $P_{\mathrm{con2(bus)}}$ caused by the resonance current flowing through the antiparallel diode of bus switch D_L.

The conduction loss $P_{\mathrm{con1(bus)}}$ caused by the load current flowing through S_L is

$$P_{\mathrm{con1(bus)}} = f_o \cdot \sum_{n=1}^{N} \left\{ V_{S(\mathrm{bus})} \cdot i_{S_L}(n) \cdot [T_L - t_{0-11}(n) + t_{8-9}(n)] + \int_0^{t_{10-11}(n)} V_{S(\mathrm{bus})} \cdot [i_{S_L}(n) - i_{La1}(t)]dt \right\} \tag{A2}$$

where T_L is the switching period of the bus switch S_L. $V_{S(\mathrm{bus})}$ is the collector–emitter saturation voltage of bus switch S_L. $t_{0-11}(n)$ is the duration from mode 1 to mode 11, which is the total commutation time of ACC during the nth switching period of the bus switch. $t_{8-9}(n)$ and $t_{10-11}(n)$ are the duration of mode 9 and mode 11, respectively, during the nth switching period of the bus switch, and they can be calculated by (32) and (37). i_{La1} (t) is the current through auxiliary resonant inductor L_{a1} of mode 11 during the nth switching period of the bus switch, which can be calculated by (36).

The second part $P_{\mathrm{con2(bus)}}$ is caused by the resonance current flowing through the antiparallel diode of bus switch as

$$P_{\mathrm{con2(bus)}} = f_o \cdot \sum_{n=1}^{N} \left\{ V_{D(\mathrm{bus})} \cdot i_{\mathrm{resmax}}(n) \cdot t_{7-8}(n) + \int_0^{t_{9-10}(n)} [V_{D(\mathrm{bus})} \cdot i_{\mathrm{res}}(t)]dt \right\} \tag{A3}$$

where $V_{DL(\mathrm{bus})}$ is the forward voltage of antiparallel diode of bus switch. $t_{7-8}(n)$ and $t_{9-10}(n)$ are the duration of mode 8 and mode 10, respectively, during the nth switching period of the bus switch, which can be calculated by (29) and (35). $i_{\mathrm{resmax}}(n)$ is the resonance peak current through the auxiliary resonant inductor L_{a1} during the nth switching period of the bus switch and can be calculated by (26). $i_{\mathrm{res}}(t)$ is the resonance current through the auxiliary resonant inductor L_{a1} of mode 10 during the nth switching period of the bus switch, which can be calculated by (33).

3) Switching Loss of Auxiliary Switch S_{a1}. $P_{sw(aux1)}$: The auxiliary switch S_{a1} is pseudo ZCS turn-ON and pseudo ZVS turn-OFF. Due to auxiliary switch S_{a1} adopt IGBT, the turn-ON loss of auxiliary switch S_{a1} can be ignored. So the switching loss of auxiliary switch S_{a1} only includes turn-OFF loss as

$$P_{\mathrm{sw(aux1)}} = f_o \cdot \sum_{n=1}^{N} E_{\mathrm{off(aux1)}}(n) \tag{A4}$$

where $E_{\mathrm{off(aux1)}}(n)$ is the turn-OFF loss when the auxiliary switch S_{a1}, paralleled a 10 nF capacitor, is turned OFF during the nth switching period of the bus switch. It is measured through experiment and related to the value of $i_{La1\,\max}(n)$, which is the peak current through auxiliary resonant inductor L_{a1} during the nth switching period of the bus switch and can be calculated by (26).

4) Conduction Loss of Auxiliary Switch S_{a1}. $P_{con(aux1)}$: The conduction loss of auxiliary switch S_{a1} consists of two parts. The first part $P_{\mathrm{con1(aux1)}}$ is caused by the load current flowing through auxiliary switch S_{a1} as

$$P_{\mathrm{con1(aux1)}} = f_o \cdot \sum_{n=1}^{N} \left\{ \int_0^{t_{5-6}(n)} [V_{S(\mathrm{aux})} \cdot i_{La1}(t)]dt + V_{S(\mathrm{aux})} \cdot i_{S_L}(n) \cdot [t_{6-7}(n) + t_{7-8}(n)] \right\} \tag{A5}$$

where $V_{S(\mathrm{aux})}$ is the collector–emitter saturation voltage of auxiliary switch S_{a1}. $t_{5-6}(n)$, $t_{6-7}(n)$, and $t_{7-8}(n)$ are the duration of mode 6, mode 7, and mode 8, respectively, during the nth switching period of the bus switch and they can be calculated by (19), (25), and (29). $i_{La1}(t)$ is the current through auxiliary resonant inductor L_{a1} of mode 6 during the nth switching period of the bus switch, which can be calculated by (17).

The second part $P_{\mathrm{con2(aux1)}}$ is caused by the resonance current flowing through auxiliary switch S_{a1} as

$$P_{\mathrm{con2(aux1)}} = f_o \cdot \sum_{n=1}^{N} \left\{ \int_0^{t_{6-7}(n)} [V_{S(\mathrm{aux})} \cdot i_{\mathrm{res}}(t)]dt + V_{S(\mathrm{aux})} \cdot i_{\mathrm{resmax}}(n) \cdot t_{7-8}(n) \right\} \tag{A6}$$

where $V_{S(\mathrm{aux})}$ is the collector–emitter saturation voltage of auxiliary switch S_{a1}. $t_{6-7}(n)$ and $t_{7-8}(n)$ are the duration of mode 6 and mode 7, respectively, during the nth switching period of the bus switch and they can be calculated by (25) and (29). $i_{\mathrm{res}}(t)$ is the resonance current through auxiliary resonant inductor L_{a1} of mode 7 during the nth switching period of the bus switch, which can be calculated by (22). i_{resmax} is the resonance peak current through auxiliary resonant inductor L_{a1} of mode 8 during the nth switching period of the bus switch and can be calculated by (26).

5) Switching Loss of Auxiliary Switch S_{a2}: $P_{sw(aux2)}$: The auxiliary switch S_{a2} is pseudo ZCS turn-ON and pseudo ZVS turn-OFF. Due to auxiliary switch S_{a2} adopt IGBT, the turn-ON loss of auxiliary switch S_{a2} can be ignored. So the switching loss of auxiliary switch S_{a2} only includes turn-OFF loss as

$$P_{\mathrm{sw(aux2)}} = f_o \cdot \sum_{n=1}^{N} E_{\mathrm{off(aux2)}}(n) \tag{A7}$$

where $E_{\mathrm{off(aux2)}}$ (n) is the turn-OFF loss when the auxiliary switch S_{a2}, paralleled a 10 nF capacitor, is turned OFF during the nth switching period of the bus switch. It is measured through experiment and related to the value of $i_{La2\,\max}(n)$, which is the peak current through auxiliary resonant inductor L_{a2} during the nth switching period of the bus switch and can be calculated by (7).

6) Conduction Loss of Auxiliary Switch S_{a2}. $P_{con(aux2)}$:

$$P_{\mathrm{con(aux2)}} = f_o \cdot \sum_{n=1}^{N} \left\{ \int_0^{t_{0-1}(n)} [V_{S(\mathrm{aux})} \cdot i_{\mathrm{res}}(t)]dt + V_{S(\mathrm{aux})} \cdot i_{\mathrm{resmax}}(n) \cdot t_{1-2}(n) \right\} \tag{A8}$$

where $V_{S(\mathrm{aux})}$ is the collector–emitter saturation voltage of auxiliary switch S_{a2}, $t_{0-1}(n)$ and $t_{1-2}(n)$ are the duration of mode 1 and mode 2, respectively, during the nth switching period of the bus switch and they can be calculated by (6) and (9). $i_{\mathrm{res}}(t)$ is the resonance current through auxiliary resonant inductor L_{a2} of mode 1 during the nth switching period of the bus switch, which can be calculated by (3). i_{resmax} is the resonance peak current through auxiliary inductor L_{a2} of mode 2 during the nth switching period of the bus switch and can be calculated by (7).

7) Conduction Loss of Auxiliary Diodes D_{a1}–D_{a4}. $P_{con(diode)}$:

$$\begin{aligned} P_{\mathrm{con(diode)}} = f_o \cdot \sum_{n=1}^{N} \Bigg\{ & \int_0^{t_{0-1}(n)} [V_{D(\mathrm{aux})} \cdot i_{Ca1}(t)]dt \\ & + \int_0^{t_{2-3}(n)} [V_{D(\mathrm{aux})} \cdot i_{La2}(t)]dt \\ & + \int_0^{t_{3-4}(n)} [2V_{D(\mathrm{aux})} \cdot i'_{La2}(t)]dt \\ & + \int_0^{t_{6-7}(n)} [V_{D(\mathrm{aux})} \cdot i_{Ca2}(t)]dt \\ & + \int_0^{t_{8-9}(n)} [V_{D(\mathrm{aux})} \cdot i_{La1}(t)]dt \\ & + \int_0^{t_{9-10}(n)} [2V_{D(\mathrm{aux})} \cdot i'_{La1}(t)]dt \\ & + \int_0^{t_{10-11}(n)} [2V_{D(\mathrm{aux})} \cdot i''_{La1}(t)]dt \Bigg\} \end{aligned} \tag{A9}$$

where $V_{D(\mathrm{aux})}$ is the forward voltage of auxiliary diodes. $i_{Ca1}(t)$ is the current through auxiliary capacitor C_{a1} of mode 1 during the nth switching period of the bus switch, which can be calculated by (2), $i_{Ca2}(t)$ is the current through auxiliary capacitor C_{a2} of mode 7 during the nth switching period of the bus switch, which can be calculated by (21). $t_{0-1}(n)$, $t_{2-3}(n)$, $t_{3-4}(n)$, $t_{6-7}(n)$,

$t_{8-9}(n)$, $t_{9-10}(n)$, and $t_{10-11}(n)$ are the duration of mode 1, mode 3, mode 4, mode 7, mode 9, mode 10, and mode 11, respectively, during the *n*th switching period of the bus switch and they can be calculated by (6), (12), (15), (25), (32), (35), and (37). $i_{La1}(t)$, $i'_{La1}(t)$, and $i''_{La1}(t)$ are the current through auxiliary inductor L_{a1} of mode 9, mode 10, and mode 11, respectively, during the *n*th switching period of the bus switch and they can be calculated by (31), (33), and (36), $i_{La2}(t)$ and $i'_{La2}(t)$ are the current through auxiliary inductor L_{a2} of mode 3 and mode 4, respectively, during the *n*th switching period of the bus switch and they can be calculated by (11) and (13).

8) Loss of Resonant Capacitor C_L, C_{a1}, and C_{a2}. P_C:

$$P_C = f_o \cdot \sum_{n=1}^{N} \left\{ \int_0^{t_{0-1}(n)} [i^2_{C_L-1}(t) \cdot R_{Ca} + i^2_{Ca1}(t) \cdot R_{Cb}]dt + \int_0^{t_{2-3}(n)} [i^2_{La2}(t) \cdot R_{Cb}]dt + \int_0^{t_{6-7}(n)} [i^2_{C_L-2}(t) \cdot R_{Ca} + i^2_{Ca2}(t) \cdot R_{Cb}]dt + \int_0^{t_{8-9}(n)} [i^2_{La1}(t) \cdot R_{Cb}]dt \right\} \quad \text{(A10)}$$

where R_{Cb} is the internal resistor of auxiliary resonant capacitors C_{a1} and C_{a2}. R_{Ca} is the internal resistor of main resonant capacitor C_L. $i_{Ca1}(t)$ is the current through auxiliary resonant capacitor C_{a1} of mode 1 during the *n*th switching period of the bus switch, and it can be calculated by (2). $i_{Ca2}(t)$ is the current through auxiliary resonant capacitor C_{a2} of mode 7 during the *n*th switching period of the bus switch, and it can be calculated by (21). $i_{CL-1}(t)$ and $i_{CL-2}(t)$ are the current through main resonant capacitor C_L of mode 1 and mode 7, respectively, during the *n*th switching period of the bus switch and they can be calculated by (1) and (20).

9) Loss of Auxiliary Resonant Inductors L_{a1}, L_{a2}. P_L: The resonant inductors L_{a1} and L_{a2} in the experimental platform are self-made winding air core inductors, so there is no core loss and the loss mainly exists in copper wire. The loss of L_{a1} and L_{a2} is

$$P_L = P_{La1} + P_{La2} = f_o \cdot \sum_{n=1}^{N} [P_{La1}(n) + P_{La2}(n)] \quad \text{(A11)}$$

where f_o is the output current/voltage frequency. *N* is the switching number of the bus switch during a period of output current/voltage. P_{La1}(n) and P_{La2}(n) are the losses of L_{a1} and L_{a2}, respectively, during the *n*th turn-OFF of the bus switch.

Because the current through L_{a1} and L_{a2} is high-frequency dc pulse current, the winding loss includes dc loss and ac loss (ac loss caused by skin effect and ac loss caused by proximity effect).

The current through the resonant inductors L_{a1} and L_{a2} during the nth turn-OFF of the bus switch is equivalent to the high-frequency dc pulse current, respectively, and the current rms and ac resistors at different frequencies can be obtained by using the Fourier decomposition. The method of calculating ac resistors at different frequencies is showed in [30]

$$i_{La1}(t) = D_{La1} i_{La1\max} + \frac{2 i_{La1\max}}{\pi} \sum_{k=1}^{\infty} \frac{\sin(D_{La1} k\pi)}{k} \cos(k\omega t) \quad \text{(A11-1)}$$

$$i_{La2}(t) = D_{La2} i_{La2\max} + \frac{2 i_{La2\max}}{\pi} \sum_{k=1}^{\infty} \frac{\sin(D_{La2} k\pi)}{k} \cos(k\omega t) \quad \text{(A11-2)}$$

where $i_{La1\max}$ and $i_{La2\max}$ are the peak currents through the auxiliary resonant inductors L_{a1} and L_{a2} during the *n*th switching period of the bus switch, respectively. D_{La1} and D_{La2} are duty cycles of auxiliary resonant inductors L_{a1} and L_{a2} during the *n*th switching period of the bus switch, respectively, ($D_{La2} = t_{0-4}/T_{SL}$, $D_{La1} = t_{5-11}/T_{SL}$), T_{SL} is the switching period of the bus switch, $T_{SL} = T_S/6$. t_{0-4} is the summation of the duration of mode 1, mode 2, mode 3, and mode 4, and they can be calculated by (6), (9), (12), and (15), t_{5-11} is the summation of the duration of mode 6, mode 7, mode 8, mode 9, mode 10, and mode 11, and they can be calculated by (19), (25), (29), (32), (35), and (37). ω is the fundamental angular frequency ($\omega = 2\pi/T_{SL}$), *k* is the harmonic number.

According to (A11-1) and (A11-2), the rms of dc current through L_{a1} and L_{a2} during the *n*th switching period of the bus switch are, respectively,

$$I_{La1} = D_{La1} i_{La1\max} \quad \text{(A11-3)}$$

$$I_{La2} = D_{La2} i_{La2\max}. \quad \text{(A11-4)}$$

The rms of ac current through L_{a1} and L_{a2} at different frequencies during the *n*th switching period of the bus switch are, respectively,

$$I_{La1}(k\omega) = \frac{\sqrt{2} i_{La1\max}}{k\pi} \sin(D_{La1} k\pi) \quad \text{(A11-5)}$$

$$I_{La2}(k\omega) = \frac{\sqrt{2} i_{La2\max}}{k\pi} \sin(D_{La2} k\pi). \quad \text{(A11-6)}$$

According to (A11-3)–(A11-6), the loss of L_{a1} and L_{a2} during the *n*th switching period of the bus switch is

$$P_{La1}(n) = \left[I^2_{La1} R_L + \sum_{k=1}^{\infty} I^2_{La1}(k\omega) R_{\mathrm{ac}}(k\omega) \right] T_{S_L} \quad \text{(A11-7)}$$

$$P_{La2}(n) = \left[I^2_{La2} R_L + \sum_{k=1}^{\infty} I^2_{La2}(k\omega) R_{\mathrm{ac}}(k\omega) \right] T_{S_L} \quad \text{(A11-8)}$$

where R_L is the equivalent dc resistor of auxiliary resonant inductors L_{a1} and L_{a2}, $R_{\mathrm{ac}}(k\omega)$ is the equivalent ac resistor of auxiliary resonant inductors L_{a1} and L_{a2} at different frequencies.

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