Plug-and-Play Control of the Virtual Infinite Capacitor

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***Abstract*—The virtual infinite capacitor (VIC) is a nonlinear active capacitor for dc voltage filtering (ripple elimination). It can replace large and unreliable electrolytic capacitors, and it is intended for dc systems where random fluctuations of the dc bus voltage may occur. We propose a plug-and-play (PnP) realization of the VIC, which can be connected directly to the dc bus like a passive capacitor without any extra connections. The proposed control algorithm automatically adjusts the reference voltage of the VIC so that it will be equal to the equilibrium voltage of the dc bus. For the stability of complex interconnected systems, it is recommended that the impedance of the components should be strictly positive real. By studying the output impedance of PnP VIC, we discuss how to achieve the strictly positive-real property of the overall dc bus by a careful choice of controllers and filters. The results were tested by simulations and experiments on a circuit comprising a commercial power factor compensator with an average of 390 V output and a variable resistive load (up to 345 W).**

***Index Terms*—Active capacitor, active power filter, charge control, digital filter, output impedance, plug-and-play (PnP), ripple elimination, strictly positive real, virtual infinite capacitor (VIC).**

I. Introduction

THE common way to suppress voltage fluctuations on the dc bus of an energy conversion/supply system is to connect large capacitors to this bus. Filtering capacitors are common on the dc bus in various renewable energy sources, electric vehicles, in submodules of modular multilevel converters (MMC), uninterruptible power supplies, and power supplies for LED lighting. Unfortunately, large electrolytic capacitors are bulky, expensive, and break down easily, see [1]–[3].

Many experts have noted that the energy fluctuations in a filtering capacitor are very small in comparison with the average stored energy, so that much of the storage is in fact idle, see for instance [4]. The small fluctuating energy can also be stored in an auxiliary buffering capacitor not directly tied to the dc bus, with large voltage swings, and this buffering capacitor could be a much more reliable film or ceramic capacitor. This idea led to various circuits known as "active power filters" and also as "ripple eliminators," or "active capacitance reduction circuits," see for instance [1], [2], [5]–[14]. These circuits use small buffering capacitors and an electronic circuit (bidirectional converter) to transfer energy from the dc bus to a buffering capacitor and back.

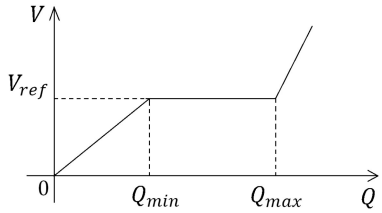

Fig. 1. $Q - V$ characteristics of a VIC. The normal operating range is where $Q \in [Q_{\min}, Q_{\max}]$. V_{ref} is chosen by the user.

There are many possible hardware realizations of the ripple eliminators, such as the bidirectional buck, boost, or buck–boost converter, the H-bridge with inductive or capacitive storage [15], [16], the stacked switched capacitor [1], series-stacked architecture [8], [9], [17], and the symmetrical half-bridge circuit [7], [14]. There are also other novel topologies for power supplies with integrated power decoupling capability, such as the integrated double buck–boost converter [18], the quasi-Z-source converter [19], the differential converter [20], and the θ converter [21].

Most ripple eliminators only target the voltage ripple at certain known frequencies (for instance, in a power factor compensator (PFC), the second and a few other even multiples of the line frequency). In [10], [13], and [14], the voltage loop comprises internal models (proportional–resonant blocks). There is only a current loop in [2] and [8], and a resonant filter is used to extract the ripple component at a selected frequency as the current reference. The controllers used in [6] and [9] are based on high-pass filters (instead of resonant filters) applied to the dc bus voltage. In [7], the buffering capacitor voltage has to track a predetermined waveform, which is calculated based on the instantaneous power balance. To the authors' knowledge, except for [3], [12], [22], and [23], the scenario where the dc bus voltage contains arbitrary low-frequency variations has not yet been fully investigated.

The *virtual infinite capacitor* (VIC) is an abstract device in nonlinear circuit theory. Its voltage V depends on the accumulated charge Q in such a way that V is constant in a certain range (see Fig. 1). Thus, if the charge is maintained in this region by a *charge controller*, then the VIC acts like an infinite capacitor. This abstract device was defined in [3], with ideas for

Manuscript received October 31, 2018; revised January 12, 2019 and March 20, 2019; accepted May 6, 2019. Date of publication May 13, 2019; date of current version November 12, 2019. This work was supported by a Grant from the Momentum Fund managed by Ramot, the Technology Transfer Arm of Tel Aviv University. Recommended for publication by Associate Editor R.-L. Lin. *(Corresponding author: Jun Lin.)*

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Digital Object Identifier 10.1109/TPEL.2019.2916928

its possible realization as an electronic circuit, and its control. The VIC makes no *a priori* assumptions about the spectrum of the incoming current, and hence in theory it can handle random current fluctuations (in practice this holds only in a finite frequency band). Applications of the VIC in circuits comprising MMCs, wind turbine systems, and PFCs have been investigated in [22]–[24], respectively.

A major drawback of the earlier control methods for the VIC is that the reference voltage V_{ref} (see Fig. 1) is fixed. To ensure that the dc bus voltage reaches an equilibrium exactly at this voltage, the charge controller of the VIC has to be integrated with the host system, to be able to influence the voltage regulator of the power source. For this, the power source converter needs to be modified (see [3] and [24]), requiring a specialist to do the installation.

To overcome these difficulties, we propose in this paper a *plug-and-play* (PnP) realization of the VIC, which enables the VIC to be connected directly to the dc bus like a passive capacitor, without extra connections with the host systems nor auxiliary power supplies. Hence, the VIC can work as a stand-alone two-terminal module. Instead of trying to force the dc bus to follow the predetermined reference voltage V_{ref}, the new control algorithm automatically adjusts the reference voltage of the VIC so that it will be equal to the equilibrium voltage of the dc bus. The technician installing the PnP VIC does not have to know in advance the stabilized terminal voltage. The adjustment of V_{ref} takes place on a slow time scale, compared with the bandwidth of the ripple current. A major difficulty is to effectively separate the slow time scale from the fast one—we use high-order digital filters for this.

Another PnP ripple eliminator (not based on the VIC concept) can be found in the interesting papers [9], [11], [17] and related work. We mention that the impedance analysis in [17] does not take into account the inherent time delay of the converter [due to sampling and pulsewidth modulation (PWM)]; therefore, the resulting expression for the impedance is not trustworthy at high frequency. It seems that our capacitance reduction ratio is higher, and compared to other solutions, we achieve much smaller ripple on the dc bus.

Various PnP (or decentralized) control algorithms can also be found in smart grids applications, where grid-tied converters are distributed in different geographic locations, for instance the virtual impedance approach, the decentralized linear quadratic Gaussian control [25], the robust control [26], and the passivity-based PnP controller [27]. The role of the VIC in a dc power supply system is similar to the role of a supercapacitor in a dc grid. Hence, the PnP control strategies developed for smart grids can be applied to the control of the VIC. To compensate the inherent losses within the interface converter of a supercapacitor, a charge recovery mechanism is needed, see for instance [28]. A virtual resistance, which is in parallel with the virtual capacitance, is used for state-of-charge (SOC) recovery in [29]. Our SOC-based charge control for the PnP VIC is more challenging than for a supercapacitor, due to the much smaller energy storage available.

For obvious reasons, the efficiency of the bidirectional converter within the VIC should be as high as possible. A soft-switching topology is highly desired, especially for high-power applications. We shall explore such issues in a different paper. In this paper, the emphasis is on the adaptive control of the PnP VIC, not on the soft switching. The converter in our experimental VIC circuit is a simple half-bridge (as in Fig. 2), working in discontinuous conduction mode (DCM). No current sensor for the inductor current i_S is needed. This simple circuit is suitable for relatively low-power applications (hundreds of Watts consumed from the dc bus).

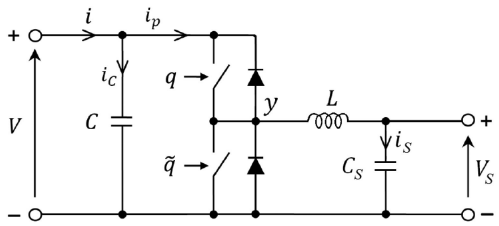


Fig. 2. Approximate realization of the VIC, showing only the main circuit elements and not showing the sensing and control circuits. The terminals for V_S are only for sensing. q and $\tilde{q}$ are binary signals coming from the controller, which determine the ON or OFF status of the switches.

A preliminary and short version of this material is contained in our conference paper [30]. The main contributions of this paper are as follows.

1) An active device, the VIC, is proposed to absorb *arbitrary* harmonics on a dc bus, achieving ripple elimination in a wide range of voltages and frequencies.
2) The PnP realization of the VIC with only two terminals, which enables the end user to deploy it just like a conventional capacitor.
3) Our proposed advanced control method will reduce the dc bus ripple to a very low level.

The structure of this paper is as follows. In Section II, we recall the working principle of the VIC. The PnP control is described in Section III, with particular attention to the resulting output impedance, and some techniques are proposed to improve its performance under load variations. In Section IV, we discuss the stability of a dc bus with a PnP VIC. Simulation and experimental results are discussed in Section V. Finally, Section VI concludes this paper.

II. Brief Introduction to the VIC Circuit

As already discussed in Section I, an electronic circuit that behaves like a nonlinear capacitor with the characteristic curve containing a horizontal segment, as shown in Fig. 1, is called a VIC (see [3]). By the charge Q, we mean of course the integral of the current. One realization of the VIC proposed in [3] uses a bidirectional buck/boost converter, as shown in the simplified circuit in Fig. 2. We see from this figure that there are three regions of operation of a VIC. The *first region*, where $Q \in [0, Q_{\min}]$, is mostly used for the power-up process, see Section V for more details.

We denote by $Q_{\min}$ the charge needed in the power-up process for the capacitor C_S to reach the minimum voltage $V_{S,\min}$ at which the converter can operate in a satisfactory way. The maximum allowed value of V_S, denoted by $V_{S,\max}$, must be less

than V_{ref} for the converter to work. The charge Q that causes V_S to reach $V_{S,\max}$ is denoted by $Q_{\max}$. The *second region*, where $Q \in [Q_{\min}, Q_{\max}]$ (and hence $V_S \in [V_{S,\min}, V_{S,\max}]$), is the *normal operating range* of the VIC. In this region, the charge Q will vary, whereas the voltage on V will remain constant at V_{ref}. Here, the dynamic capacitance dQ/dV is infinite. The *third region* (where $Q > Q_{\max}$) is where the VIC is overcharged. To protect the circuit, both switches are OFF and hence only the capacitor C is connected to the terminals of the VIC. The capacitor C_S is now disconnected and maintains the constant voltage $V_S = V_{S,\max}$.

There must be a *state machine* in the control processor of any VIC that regulates the transitions between the three regions of operation described above. The state machine is sometimes tricky to realize, using hysteresis to avoid spurious oscillations at the boundary between two regions. However, in this paper we do not detail this state machine, we concentrate instead on the most delicate issue, which is the control of the PnP VIC in the second region. The PnP VIC needs also an additional control mechanism to maintain the VIC in the normal operating range described above, called a *charge controller*, see Section III.

To control the terminal voltage of the VIC in the normal operating range, two sliding mode controllers were presented in [3], with the converter operating in continuous conduction mode. Using very high switching frequencies (over 500 kHz), excellent performance was achieved, but operating at such high frequencies is not easy. A complex soft-switching implementation of the algorithms from [3] was proposed in [31]. Another version with a more complex circuit, working in DCM mode, at a much lower constant switching frequency, was proposed in [23].

To avoid misunderstanding, the behavior shown in Fig. 1 is ideal and defines the abstract concept of VIC. Due to various imperfections of the converter and its control (e.g., delays), the behavior of the real circuit is only an approximation of Fig. 1, so that we have some ripples in V.

III. PnP Control

A. General Structure

The greatest challenge in designing a PnP VIC is that the properties of the dc bus (especially the characteristics of the main power source) are not known to the designer. The only communication between the VIC and other devices connected to the dc bus is via the voltage V. This is similar to the dc bus signaling technique in dc microgrids. As the dc bus voltage is regulated both by the power source and the PnP VIC, to avoid control conflicts, we must ensure that the frequency band of the voltage control loop of the PnP VIC is in the higher frequencies (compared to the bandwidth of the power source) so that they practically do not overlap. In other words, the instantaneous value of dc bus voltage is determined by the VIC, whereas the long-term average is determined by the power source (and other devices that may be connected to the dc bus, such as loads). We achieve this by adding a new outer control loop that changes the reference voltage V_{ref} (see Fig. 1 for the meaning of V_{ref}) based on the SOC of the VIC, represented by V_S^2. We refer to this loop as the *charge control loop*, because indirectly it controls the SOC, as we explain in the following section. The overall block diagram is in Fig. 3. (The charge controller in [3] was entirely different and based on influencing the power source via an extra terminal.)

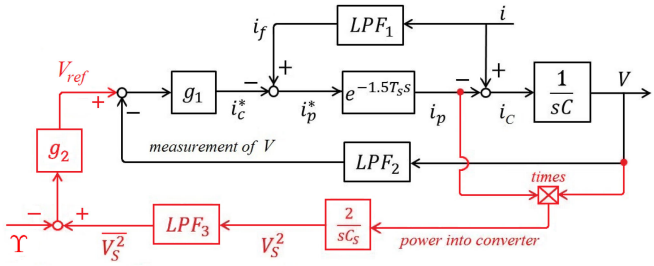


Fig. 3. Block diagram of the PnP VIC, when working in the normal operating range. The charge control part is highlighted in red. The low-pass filters LPF_1 and LPF_2 represent current and voltage sensors. The red part remains unchanged when the VIC leaves the normal range.

From Fig. 2, the output filtering capacitor voltage is governed by

$$\frac{d}{dt}V = \frac{i_C}{C} = \frac{1}{C}(i - i_p). \tag{1}$$

A voltage controller g_1 [see (9)] generates the reference signal for i_C, denoted by i_C^*, and then current feedforward compensation, as shown in black lines in Fig. 3, is used to create the reference signal i_p^* for the converter current i_p. The current feedforward is realized with the filtered disturbance i_f, obtained by a current sensor represented by a low-pass filter (LPF) denoted by LPF_1.

The dc bus voltage V is obtained from i_p in accordance with (1). This *voltage control loop* remains similar to our previous work [24]. Here, LPF_2 represents the voltage sensor. The duty cycle of the active switch can be derived from i_p^* by calculating the area of the triangle under the current waveforms within each PWM period (see [24]). Given the computational and PWM delay, the DCM converter with its fast current control loop is represented approximately by a delay block of delay time 1.5 T_S, where T_S is the sampling period (in our application example $T_S = 20\ \mu\text{s}$).

The proposed charge control loop is highlighted in red in Fig. 3, and the charge controller is g_2. Here, LPF_3 has a much more narrow bandwidth than the sensors LPF_1 and LPF_2, and the sensor for V_S is considered to be a part of LPF_3.

Intuitively, the charge control loop works as follows—the voltage control loop of the VIC has a large bandwidth (in comparison to the power source) and hence V will closely track V_{ref}. If the VIC keeps V smaller than the equilibrium voltage V_0 of the dc bus, more current i will keep flowing toward the VIC, thus increasing V_S. Then, the charge control loop would increase V_{ref}. This process will continue until the local average of V_S^2, denoted $\overline{V_S^2}$ (which equals $\overline{V}_S{}^2 + \frac{\Delta V_S^2}{4}$ for sinusoidal ripple, where ΔV_S is the peak-to-peak value of V_S), is stabilized to its reference value Υ, and then $V = V_{\text{ref}} = V_0$. The reason for working with the squared signal V_S^2 will become clear in the following section. We will use a proportional–integral controller

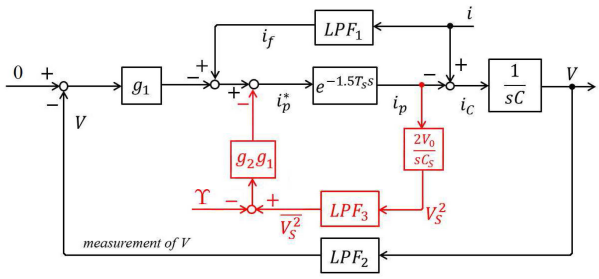


Fig. 4. Equivalent small signal block diagram for the system from Fig. 3, where V_0 is the equilibrium voltage of the dc bus.

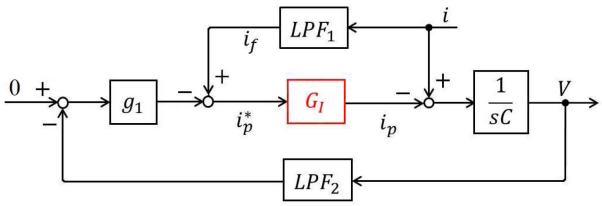


Fig. 5. Simplified small signal block diagram.

for $g_2(s)$

$$g_2(s) = K_p + \frac{K_I}{s} \tag{2}$$

so that it can generate a constant even if its input is zero. The initial value of the integrator in $g_2(s)$ should be set to an initial guess for the dc bus equilibrium voltage V_0.

B. Closed-Loop Model and the Role of the Digital Filter

From Fig. 2, V_S is obtained by integrating i_S/C_S. At frequencies below the switching frequency, the bidirectional buck converter may be regarded as a power conserving circuit, meaning that $i_p V = i_S V_S$. Therefore (similarly as in [3, Sec. 3])

$$\frac{d}{dt}V_S^2 = 2V_S\dot{V}_S = 2V_S\frac{i_S}{C_S} = \frac{2}{C_S}Vi_p$$

and this can be seen in the lower part of Fig. 3. Since there is a lot of ripple in V_S, a narrow-band LPF$_3$ is used to extract the dc part of V_S^2, which is used to compute V_{ref}. The block diagram in Fig. 3 can be transformed as shown in Fig. 4, which shows an equivalent small signal block diagram, valid when V is close to the equilibrium voltage V_0 of the dc bus.

The block diagram in Fig. 4 can be simplified to the one shown in Fig. 5, where the internal loop from Fig. 4 has been replaced by a single block with transfer function

$$G_I(s) = \frac{e^{-1.5T_S s}}{1 + 2V_0 e^{-1.5T_S s} g_1(s) g_2(s) \text{LPF}_3(s)/sC_S}. \tag{3}$$

If the input signal i is at very low frequency (in the frequency band of LPF$_3$), $g_1(0)$ is finite and $g_2(s)$ is as in (2), then for very small $|s|$, we get from (3)

$$G_I(s) \approx s^2\kappa, \quad \text{where } \kappa = \frac{C_S}{2V_0 g_1(0) K_I}. \tag{4}$$

The main difference between the "simple" VIC from Fig. 1 and the PnP VIC is in the very low frequency band.

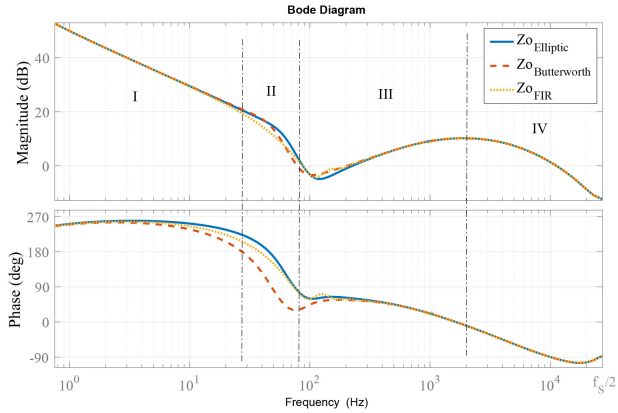


Fig. 6. Bode plots of the output impedance $Z_o(s)$ of the specific PnP VIC from Section V, with different choices for LPF$_3$, described in Section IV. None of the filters ensures that Z_o is strictly positive real.

Indeed, if a dc current i flows to a "simple" VIC, the VIC will act as a voltage source with constant voltage V_{ref} until it gets fully charged (i.e., until V_S reaches the maximum $V_{S,\max}$), and then it moves into the third region, where it is just the capacitor C (see Section II). This is not a desirable behavior, because the capacitor C alone will not attenuate the ripple sufficiently. By contrast, if a dc current flows into a PnP VIC, then V_S will rise, causing V_{ref} to rise, causing V to rise, causing i to decrease, until the average i becomes zero.

The choice of LPF$_3$ is very delicate, since we want to stop the ripple in V_S^2 from reaching V_{ref} (see Fig. 3). At the same time, we would like the impedance of the PnP VIC to be approximately positive real, i.e., $Z_o(j\omega)$ should be in the right half-plane, or at least very close to it, for all frequencies. This is needed to ensure that the uncertain dc bus system should be stable (assuming that all the other devices connected to it are also more or less positive real), see Section IV. To meet all these requirements, we use for LPF$_3$ a high-order digital filter with a sharp decrease of $|\text{LPF}_3|$ around its cutoff frequency, region Ⓘ in Fig. 6, see also Section IV. Our analysis is done in continuous time, but the control algorithm is implemented digitally after a suitable Tustin discretization. While most of the control algorithm is executed at the switching frequency f_S, we recommend to use a lower sampling frequency f_F for LPF$_3$, to avoid numerical problems.

C. Output Impedance

Since the PnP VIC will be connected to a dc bus, to analyze its interaction (e.g., resonance) with other devices, its output impedance Z_o needs to be computed. This impedance is the transfer function from i to V in Fig. 5. Assuming first-order transfer functions with time constants $\tau_1 > 0$ and $\tau_2 > 0$ for LPF$_1$ and LPF$_2$, respectively, we get

$$\begin{aligned} Z_o(s) &= \frac{\frac{1}{sC}}{1 + g_1(s)G_I(s)\frac{1}{sC}\frac{1}{1+\tau_2 s}} - \frac{G_I(s)\frac{1}{sC(1+\tau_1 s)}}{1 + g_1(s)G_I(s)\frac{1}{sC}\frac{1}{1+\tau_2 s}} \\ &= \left(1 - \frac{G_I(s)}{1+\tau_1 s}\right)\frac{1}{sC + g_1(s)G_I(s)/(1+\tau_2 s)}. \end{aligned} \tag{5}$$

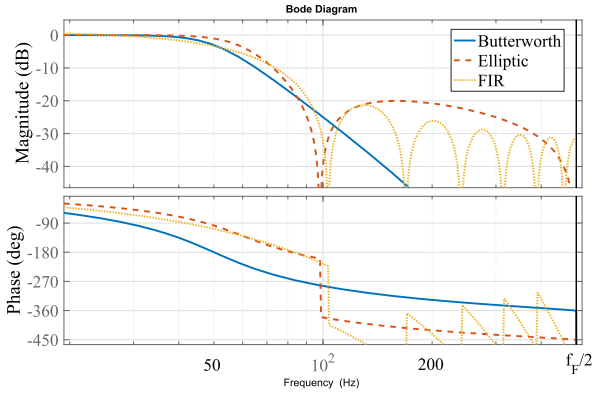


Fig. 7. Bode plots of three digital LPFs under investigation, discretized at $f_F = 1000$ Hz, the plots show the frequencies up to $f_F/2$.

The Bode diagram of $Z_o(s)$ for our specific realization of a PnP VIC is shown in Fig. 6, using the parameters listed in Table II. In the *low-frequency band*, region ① indicated in Fig. 6, $\text{LPF}_3 \approx 1$. By a simple computation using (4) and (5), from the Taylor expansion of $sZ_o(s)$ at 0, neglecting the quadratic and higher order terms, the output impedance at low frequencies is

$$Z_o(s) \approx -\frac{g_1(0)\kappa}{C^2} + \frac{1}{sC} \tag{6}$$

which is like a negative resistor in series with a capacitor. At very low frequencies, the capacitance part dominates $Z_o(s)$, but the real part of $Z_o(s)$ is determined by the resistance part.

Region ② in Fig. 6 corresponds to the range where LPF_3 does its steep descent from values close to 1 (to the left) to values close to 0 (to the right), see also Fig. 7 in Section IV. This region is characterized by sharp changes of $Z_o(s)$ (both in amplitude and in phase).

In the *intermediate range of frequencies*, regions ③ and ④ in Fig. 6, where we expect most of the current ripples to be, we would like $Z_o(s)$ to be very small. In this range, for our application example, we have $|\text{LPF}_3(s)| \approx 0.1$, $e^{-1.5T_S s} \approx 1$ and hence $|2V_0 e^{-1.5T_S s} g_1(s) g_2(s) \text{LPF}_3(s)/sC_S| \leq 0.025$. Looking at (3), we conclude that $G_I(s) \approx 1$. It is reasonable to assume that this would hold also for other application examples in this frequency range. Hence, the expression (5) of $Z_o(s)$ can be simplified as follows:

$$Z_o(s) \approx \frac{\tau_1 s}{1+\tau_1 s} \cdot \frac{1}{sC + \frac{g_1(s)}{1+\tau_2 s}}. \tag{7}$$

Since LPF_2 is meant to filter out the high-frequency switching noise on the dc bus, $1 + \tau_2 s \approx 1$ in the intermediate range. Then, the expression (7) becomes

$$Z_o(s) \approx \frac{1}{sC + \frac{g_1(s)}{\tau_1 s} + g_1(s) + \frac{C}{\tau_1}}. \tag{8}$$

This formula describes Z_o in the intermediate frequency range, which is the most important for ripple suppression. For a proportional or for a lead–lag type controller g_1, $Z_o(s)$ is like an RLC-type output impedance, with inductive or capacitive characteristics dominant in regions ③ and ④, respectively. There is normally a "bump" in $|Z_o|$ in the transition zone from inductive to capacitive behavior (see Fig. 6).

For high frequencies above $f_S/2$, where f_S is the switching frequency of the converter in the VIC, the delay block in Fig. 3 should be replaced with zero, hence $G_I(s) = 0$ and the PnP VIC reduces to the capacitor C acting alone.

In our application example, the peak of the impedance at several kHz is almost 3 Ω, as shown in Fig. 6. This VIC can deal very well with ripple harmonics within the range [60,1000] Hz, but it works quite well also up to $f_S/2 = 25$ kHz. To further improve the performance, one can reduce the delay by using fast switching wide bandgap based switches and increase f_S, or over-sampling techniques. If the delay in Figs. 3–5 is made smaller, then the feedforward term can compensate the disturbance i more effectively at high frequency, reducing the bump in the plot of $Z_o(s)$ in the intermediate range.

D. Controller Choice and the Tuning of Its Parameters

Ideally only currents in the intermediate frequency range should flow into the VIC. For very low frequency harmonics, due to its limited energy storage capability, V_S could get dangerously close to its boundary values. To prevent this, $g_1(s)$ is chosen with a lead–lag transfer function

$$g_1(s) = \frac{K}{a}\frac{1+a\tau s}{1+\tau s} \tag{9}$$

to reduce its gain at low frequency by a factor $1/a$. At the same time, to keep the loop gain of the charge control intact, the gain in $g_2(s)$ in (2) should be increased accordingly.

Ideally, the VIC should have a large working range (the intermediate frequency range discussed earlier) and a small impedance in this range. The peak in the plot of the impedance in the intermediate range can be reduced either by decreasing τ_1 and/or increasing C and g_1. However, the output capacitor C should be small, as this is the motivation for using a VIC (to replace large capacitors with small ones). We cannot choose arbitrarily large g_1, because it would increase the bandwidth of the voltage loop too much, resulting in noise in this loop, including at V.

Similarly as in Section III-B, the loop gain of the charge control loop (see Fig. 4) at very low frequencies is approximately $\frac{2V_0}{sC_S} g_1(s) g_2(s)$, which has been obtained by approximating $\text{LPF}_3(s) \approx 1$ and $e^{-1.5T_S s} \approx 1$. As a rule of thumb, $g_2(s)$ should be chosen such that the bandwidth of the charge control loop is much smaller than that of the voltage control loop of the VIC, and inverse proportional to the bandwidth of the voltage control loop of the main power source. Since $\overline{V_S^2}$ coming from LPF_3 cannot be 100% ripple free, small $g_2(s)$ is needed for high-quality dc bus voltage, whereas large $g_2(s)$ can introduce faster dynamics.

The reference value Υ may be set as a constant. In more clever and flexible implementations, there should be an online monitoring mechanism to update Υ based on past experience. For instance, after some period of stable operation, we may reset $V_{S,\max} = 0.9\, V_{\text{ref}}$, and then reset $\Upsilon = \frac{1}{2}[V_{S,\min}^2 + V_{S,\max}^2]$.

E. Load Variation Processing and Protection

The proposed charge controller works fine for small or slow variations of the dc bus equilibrium voltage V_0, but problems may arise under large and sudden changes of V_0, which may be caused by a sudden change of the load. This is because LPF_3 introduces a large delay into the response of the charge control loop and this may cause larger oscillations of V while V_S oscillates close to its upper or lower bound. To avoid this, we propose the following: recall that LPF_3 works at a lower frequency f_F (see Section IV) than the rest of the algorithm. When there is a large enough difference between the values of $\overline{V_S^2}$, obtained from LPF_3 at two consecutive sampling times of this filter, the VIC enters an emergency mode of operation. In this mode, we increase the proportional gain of $g_2(s)$, K_p in (2), to force the charge control to respond faster, and we also decrease the feedforward current i_f by multiplying it with a gain $\gamma \in (0, 1]$, whose nominal value is 1. After such an increase of K_p and a decrease of γ, they will slowly recover back to their nominal values. In our application example (see Section V), K_p is increased two times and γ is decreased to 0.25. Their recovery time is about 160 ms.

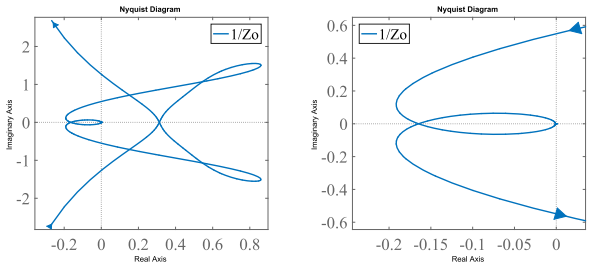
To guarantee smooth running without triggering changes in the state machine mentioned in Section II, another protection mechanism is employed. If V_S is too small (large), the current is only allowed to flow into (out of) C_S. This is achieved as follows: instead of sending the signal i_p^* as a reference input to the current controller, we compute the following modified current reference j:

$$j = \begin{cases} \text{pos}(i_p^*), & \text{when } V_S < (V_{S,\min} + \delta) \\ \text{neg}(i_p^*), & \text{when } V_S > (V_{S,\max} - \delta) \\ i_p^*, & \text{else} \end{cases}$$

where $\text{pos}(x) = \frac{1}{2}(x + |x|)$, $\text{neg}(x) = \frac{1}{2}(x - |x|)$, for any $x \in \mathbb{R}$, and δ is a small positive constant (to avoid triggering mode changes as would follow from Fig. 1). This reference signal j is then applied to the DCM current controller (which in turn operates the PWM generator). This idea is similar to the saturating integrator employed in the control of the reactive power of a synchronverter in [32].

IV. Stability Analysis

Recall that an analytic function Z defined on a domain containing the right half-plane is called *positive real* if the conditions $Z(\overline{s}) = \overline{Z(s)}$ and $\text{Re}Z(s) \geq 0$ hold for all $s \in \mathbb{C}$ with $\text{Re}s > 0$. It is called *strictly positive real* if the above properties remain true on a slightly larger half-plane determined by $\text{Re}s > -\varepsilon$, where $\varepsilon > 0$ (see for instance [33, Definition 4.1]). Positive realness is linked to impedance passivity and the stability of systems, see for instance the recent papers [33], [34] and the many references therein. We need the easily verified facts that if Z is strictly positive real, with ε as above, then also $1/Z$ has this property, and all the poles and zeros of Z are in the left half-plane determined by $\text{Re}s \leq -\varepsilon$. In particular, it follows that if Z is strictly positive real and it has a finite limit at ∞ (as $s \to \infty$ with $\text{Re}s > 0$), then Z is a stable transfer function.



(a) (b)

Fig. 8. (a) Nyquist plot of the output admittance $1/Z_o(s)$ when LPF_3 is an elliptic filter, and the parameters and controllers are as described in Section V. The time delay has been approximated by a first-order Padé approximation to plot the admittance. (b) Zoom of the small region at low frequencies where a positive-realness violation occurs—we see that the violation is small.

Since the VIC is intended to work on an *a priori* unknown dc bus, the passivity-based stability criterion from [35] will be employed here. Reformulated in our terminology, the whole system is stable if its total impedance Z is strictly positive real. This follows from the last sentence of the previous paragraph, since $Z(\infty) = 0$ due to the capacitors on the dc bus. The total admittance $1/Z$ is the sum of the admittances of all the devices connected to the dc bus. If the VIC output admittance is close to being positive real (even if it is not positive real), then the total admittance $1/Z$, and hence also Z, has a good chance of being strictly positive real, because most devices connected to the dc bus have a strictly positive-real admittance.

For our PnP VIC, due to the negative real part of Z_o in the low-frequency band, as seen in (6), we have a violation of the positive-real condition in this range. We prevent this from happening also in the intermediate range of frequencies by a careful choice of LPF_3. For our specific application example, we have investigated the following three options for LPF_3 [36]:

1) a 4th-order Butterworth filter with cutoff frequency $f_3 = 50$ Hz;
2) a 3rd-order elliptic filter with cutoff frequency $f_3 = 25$ Hz;
3) a 12th-order finite impulse response (FIR) filter with cutoff frequency $f_3 = 25$ Hz.

The parameters of these digital filters are tuned on the MATLAB toolbox `FDAtool`, with stopband 100 Hz, attenuation 20 dB, and sampling frequency $f_F = 1000$ Hz. For typical applications with 100-Hz harmonics ripple, we need get the dc component with the least possible phase delay. Hence, a cutoff frequency around 30 Hz would be a good choice. From Fig. 7, the FIR and the elliptic filters have similar phase at low frequency, faster than the Butterworth filter; the notches on the FIR filter can be used to filter selected harmonics. In Fig. 6, the output impedances using these filters are compared. The differences are mainly in region ⑪. They are almost identical in the other frequency regions. We found that the Butterworth filter leads to the widest positive-real region; however, the elliptic filter is much faster to extract the dc component of V_S^2. Hence, the elliptic filter is implemented as LPF_3.

Fig. 8 shows the Nyquist plot of the admittance $1/Z_o(j\omega)$. The PnP VIC is not strictly positive real. The low-frequency

TABLE I
MAIN COMPONENT LIST

DSP	TI F28M35H52C Concerto
Switches	Fairchild UniFET™ FDPF15N65
Driver	International Rectifier IR2113
C	KEMET C4AEGBU5200A12J 20μF
C_S	KEMET C4AEGBU5200A12J 2x20μF
L	Bourns 1140-121K-RC 120μH

TABLE II
SYSTEM PARAMETERS

u_g	$310\sin(2\pi f_g t)$	C_0	10 μF
R_{L1}	880Ω	f_S	50 kHz
R_{L2}	880Ω	f_F	1 kHz
$V_{S,min}$	$0.2V_{ref}$	$V_{S,max}$	$0.9V_{ref}$
f_d	251 Hz	Υ	$(275V)^2$
a	2	τ	$1/(2\pi 140)$
K	0.08	g_2	$0.0001(1+2/s)$
τ_1	$1/(2\pi 6K)$	τ_2	$1/(2\pi 10K)$

local minimum of its real part is around -0.18, as seen in the zoomed subfigure. As shown in Figs. 6 and 8, there is a slight positive-realness violation also at some high frequencies, due to the 1.5 T_S time delay. Notice that the above analysis is based on a lossless model for the VIC. The negative real part at low frequency is smaller in practice, due to the parasitic resistances of the switches and the equivalent series resistance of the inductor. Normally, there are other devices tied on the dc bus, whose impedance at low frequencies is much smaller than that of the VIC. The total impedance at low frequencies is dominated by them. Hence, the low-frequency positive-realness violation has little effect on the overall stability of the system.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation and Experimental Setup

We have built a 400-V rated PnP VIC as in Fig. 2, with the main components listed in Table I. Both C and C_S are film capacitors. The switches are Fairchild UniFET FDPF15N65, which is cost competitive and more efficient than superjunction technology device [37].

The control parameters are listed in the bottom half of Table II. The experiments were conducted using an off-the-shelf boost-type PFC (UCC28180EVM-573 Evaluation Board) from Texas Instruments, whose Simulink model was used as part of our simulation system, connected as shown in Fig. 9.

The voltage controller of this commercial PFC is complex. The 10-Hz low bandwidth voltage controller (designed to work with a 270 μF dc capacitor) is active only when V is within $\pm 5\%$ of its nominal value. If the output voltage is outside this range, then the enhanced dynamic response mechanism will act to speed up the response of the voltage loop. The PFC will stop operating its MOSFET switch if the dc bus voltage is higher than 1.1 times the nominal voltage [38]. This explains why, before the VIC is enabled, V is not sinusoidal, see the first half of Fig. 15.

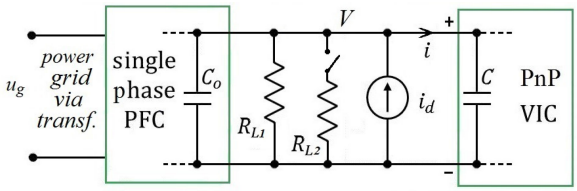


Fig. 9. Simulation and experiment setup, showing the PFC and VIC connected to a dc bus with a split load R_L. The current source i_d injects a low-frequency disturbance (in addition to the ripple current coming from the PFC, and at a different frequency). The VIC is trying to keep V constant.

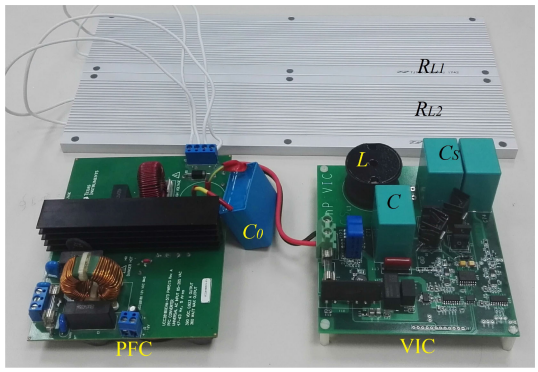


Fig. 10. Lab setup, with the PFC on the left, the load resistors in the back, and the PnP VIC on the right.

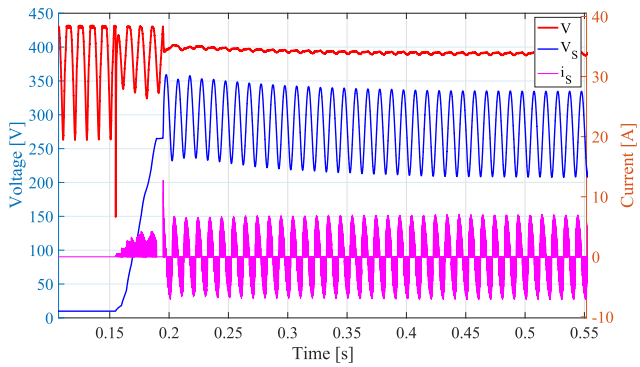


Fig. 11. PnP start-up simulation results showing V, V_S, and i_S. To speed up the convergence, K_p from (2) starts from a large value 0.0004 and decreases exponentially, reaching the 0.0001 at $t = 1$ s.

The PFC has been connected to a 50-Hz power grid with voltage u_g. The original 270 μF bulky electrolytic capacitor of the PFC has been replaced with a small film capacitor $C_0 = 10$ μF, such that in the absence of any further ripple attenuation, a strong second harmonic would appear on the output voltage. The PFC works under its rated power of 350 W, with the average dc bus voltage 390 V, with resistive loads $R_{L1} = R_{L2} = 880$ Ω. A current source i_d that injects a sinusoidal disturbance at $f_d = 251$ Hz, with amplitude 0.3 A, is used to mimic a nonlinear load.

B. Simulation Results

Fig. 11 shows the simulation of the start-up process of our PnP VIC, which is connected to the dc bus at $t = 0.15$ s, so that we can also observe the situation before it is connected. (It is

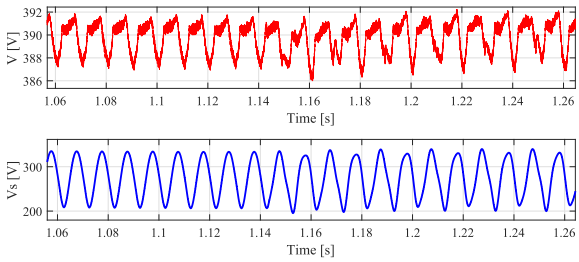


Fig. 12. Simulated steady-state waveform of the voltages V and V_S for our PnP VIC connected to a PFC. At $t = 1.15$ s, a disturbance current $i_d = 0.3\cos(251 \cdot 2\pi t)$ is injected to the dc bus.

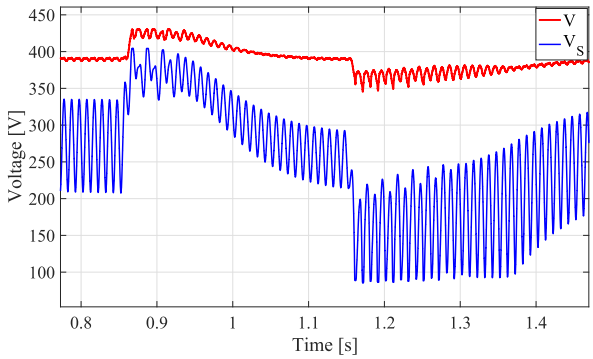


Fig. 13. Simulated waveforms of PnP VIC connected to a PFC under load variations with the load variation processing algorithm and protection enabled. At $t = 0.86$ s, the load changed from 345 W(440 Ω) to 173 W(880 Ω); and at $t = 1.15$ s, the load changed back.

assumed that the PFC has been working long before the PnP VIC.) Before connecting the VIC, the strong second harmonic ripple on V is not symmetric due to the nonlinear behavior of the PFC. The ripple is suppressed by the VIC quickly in two stages. Up to 0.18 s, the VIC operates in the first range of operation (see Fig. 1). The ripple in V is now reduced since the total dc bus capacitance is $C + C_0$. To limit the inrush current i_S, a soft start procedure is used—only the upper switch is active to charge C_S, and its duty cycle grows from 0 to 0.3. The level $V_S^2 = \Upsilon$ is reached at $t = 0.18$ s. For a smooth transition to the normal operating range, the state machine governing the operating ranges waits until $\overline{V_S^2}$ (obtained via LPF_3) grows to reach $\Upsilon - \alpha$, where α is a small constant. During this waiting, both switches are OFF. The VIC enters the normal operating range at $t = 0.19$ s. After this, V_S starts oscillating and the ripple in V becomes very small.

In the zoomed plot, see Fig. 12, we can see that the ripple in V is within 4 V peak-to-peak. The additional disturbance i_d starting at $t = 1.15$ s does not deteriorate the quality of V.

Fig. 13 shows the simulation of sudden changes of the load (up and down) occurring in steady-state operation. Thanks to the proposed load variation processing algorithm (see Section III-E), the charge controller responds fast. Some variation of V is unavoidable, but the ripple is sufficiently suppressed.

C. Experimental Results

The key waveforms of the PFC with original 270 μF were demonstrated in Fig. 14(a) as a benchmark. Due to the second

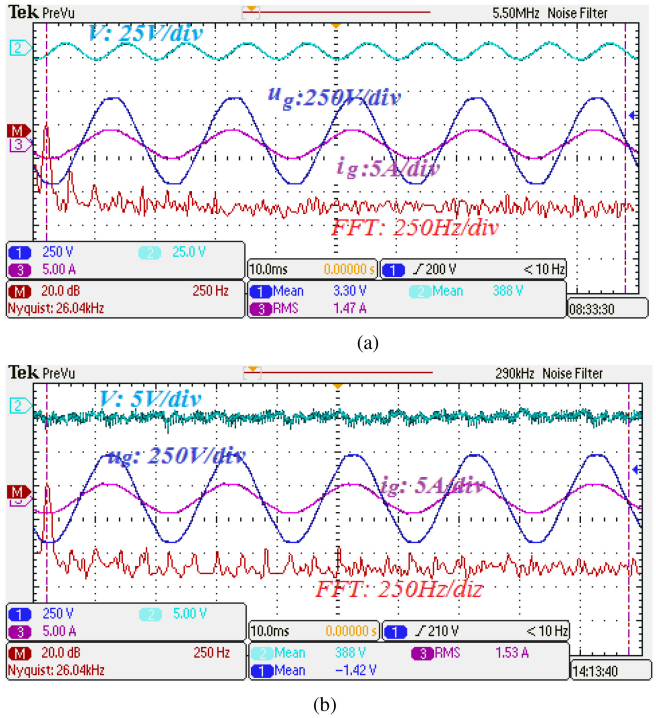


Fig. 14. Experimental results of steady-state input and output waveforms of a PFC. (a) PFC with its original capacitor of 270 μF. (b) PFC with a small capacitor C_0 and with the VIC enabled. From top to bottom, the plots of the dc bus voltage V with 390 V offset, the grid voltage u_g, the grid current i_g, and the fast Fourier transform (FFT) analysis of i_g.

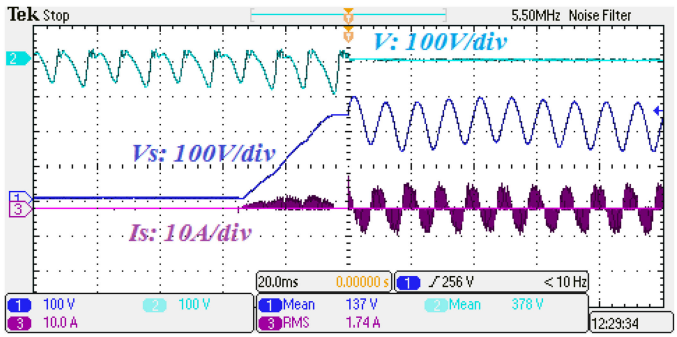


Fig. 15. Experiment showing the moment the PnP VIC is enabled. We see the plots of the dc bus voltage V with 390 V offset, V_S, and i_S. Before the VIC is enabled, there is only C_0 from the PFC and the VIC output capacitor C on the dc bus, resulting in a strong second harmonic. After the VIC is enabled, the ripples are transferred to the VIC, leaving an almost constant dc bus voltage.

harmonics on the dc bus, 12 V peak-to-peak, the grid current contains amount of third and fifth harmonics, etc.

The waveforms at the moment when PnP VIC is enabled are shown in Fig. 15. The VIC can quickly stabilize the dc bus voltage, with the low-order harmonics stored in C_S. The zoomed figure of steady state is shown in Fig. 16. The peak-to-peak ripple on the dc bus is around 2 V out of 388 V. Fig. 14(b) shows the grid voltage and current waveforms. From the FFT analysis, we can notice that the quality of input current improved a lot without the third harmonic.

Figs. 17 and 18 show the transients when there is a 50% load variation on the dc bus, between 345 W(440 Ω) and

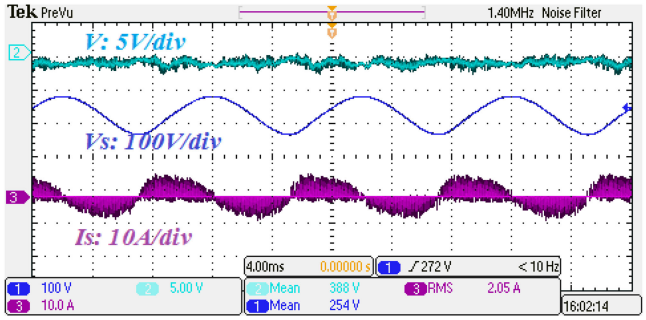
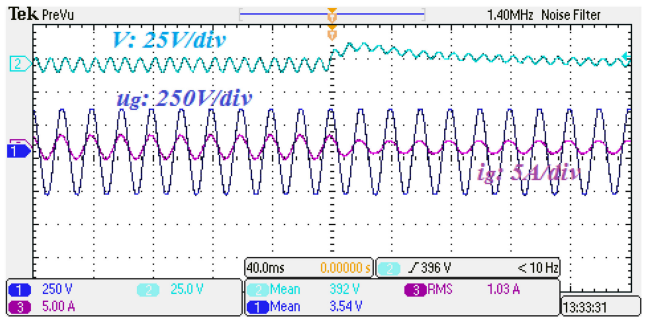
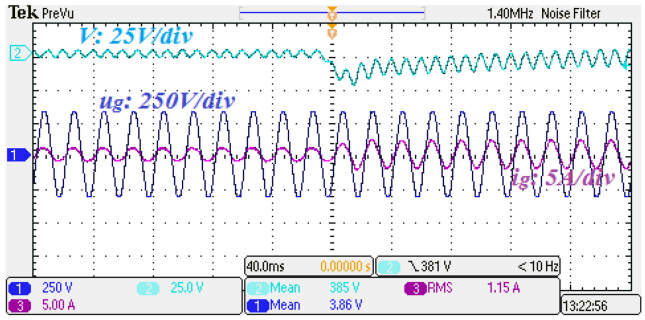


Fig. 16. Experimental results with a PFC, a load, and our VIC in place of the dc bus filtering capacitor—the plots of V, V_S, and i_S, arranged from top to bottom. The peak-to-peak ripple of V is within 2 V out of 388 V.



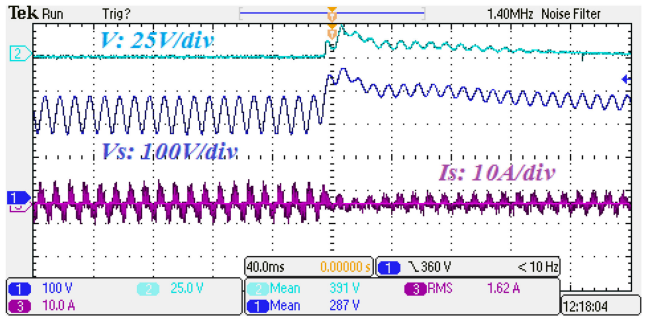
(a)



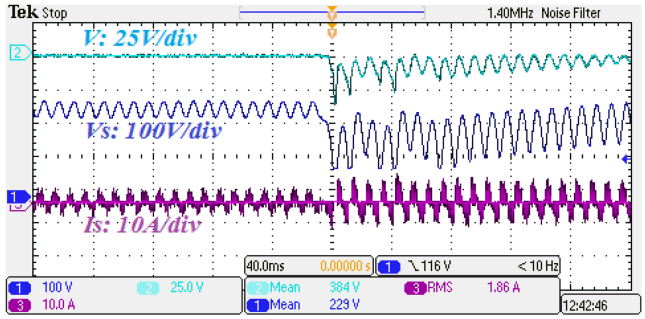
(b)

Fig. 17. Load variation experiment results for the PFC with its original filter capacitor of 270 μF, without VIC. (a) Load changed from 345 W$(440\ \Omega)$ to 173 W$(880\ \Omega)$. (b) Load changed back.

173 W$(880\ \Omega)$. Whenever there is a sudden load change, the instantaneous unbalanced power between the sources and the loads has to be processed by the dc-link capacitors (and the VIC). For the PFC with the original 270 μF capacitor without VIC in Fig. 17, the overshoot and undershoot are 10 and 25 V, respectively. It takes about 120ms for V to get back to its nominal value. For the VIC case as in Fig. 9, the experimental results are shown in Fig. 18. This shows that the setting times are very similar, since the dc part of V is determined by the PFC, and the VIC only processes harmonics. However, the overshoot and undershoot are 25 and 35 V, respectively, which are larger than in Fig. 17. This is because it always takes time for the LPF-based load variation detection algorithm to detect the load changes. During this short interval, the VIC tries to maintain a constant dc bus voltage. Therefore, V_S is quickly pushed toward its upper or lower limit. Depending on the load change point (e.g., the valley or the peak of V_S), under certain circumstances, the



(a)



(b)

Fig. 18. Load variation experiment with a PFC connected to the VIC. (a) Load changed from 345 W$(440\ \Omega)$ to 173 W$(880\ \Omega)$. (b) Load changed back.

charge within C_S might be completely depleted, leaving only C and C_0 on the dc bus to filter out the ripple. In the experiments, the undershoot sometimes is larger than in Fig. 18.

VI. Conclusion

We have proposed a PnP realization of the VIC, with a simple half-bridge bidirectional converter working in DCM as the hardware. It can process a wide range of frequencies just like a passive capacitor, without *a priori* assumptions about the spectrum of the current. The PnP VIC adjusts its reference voltage based on the average value of the SOC of the buffering capacitor C_S until equilibrium is reached on the dc bus. This should greatly simplify the use of the VIC circuit. To improve its performance under load variations, a load variation processing algorithm is proposed. The output impedance of the PnP VIC is evaluated. Due to the charge control loop, the output impedance of the VIC is capacitive at very low frequency. To minimize the influence of the charge control on the dc bus voltage control, we have tested various high-order digital filters LPF_3 to extract the dc component of the buffering capacitor voltage (squared). Due to the phase delay, the output impedance at very low frequencies has a negative real part, but we have argued that this should be acceptable for most dc buses.

One clear drawback of the proposed PnP algorithm is that the optimal tuning of the charge controller $g_2(s)$ depends on the bandwidth of the dc bus voltage controller of the main power source, which may be unknown in advance. Hence, an adaptive $g_2(s)$ may be better for applications where the bandwidth information is missing. More sophisticated adaptive voltage reference generation mechanisms, e.g., a complete PnP solution with a self-parameterizing controller, better load variation

processing algorithm, and soft-switching hardware topology are left for future research.

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