Input-Independent and Output-Series Connected Modular DC–DC Converter With Intermodule Power Balancing Units for MVdc Integration of Distributed PV

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***Abstract*—In this paper, a novel topology of modular dc–dc converter has been proposed for medium voltage dc (MVdc) integration of high-penetration distributed PV. The proposed topology is featured with input-independent and output-series connected configuration and intermodule power balancing units (PBUs). A high voltage gain could be achieved with series-connected submodules (SMs), while each SM's input port is connected with PV array to realize the independent maximum power point tracking (MPPT) control function. PBUs with bidirectional power conversion ability are installed between adjacent SMs for the elimination of intermodule power mismatch. The operation principles of the proposed converter have been explained in detail along with the corresponding control strategies. The design principles of major passive components have been investigated on the basis of boundary operation conditions, while a quantitative analysis of steady-state power losses has been performed. Moreover, a comparative study is conducted from the aspects of operation range, topology complexity, component stress, and power efficiency. The theoretical results have been validated by both simulations and down-scaled experiments.**

***Index Terms*—Distributed PV, modular dc–dc converter, MVdc integration, power balancing unit (PBU), power mismatch.**

I. Introduction

With the rapid expansion of distributed energy resource (DER), the traditional ac power system has been faced with several challenges related to high penetration of distributed PV. These are as follows.

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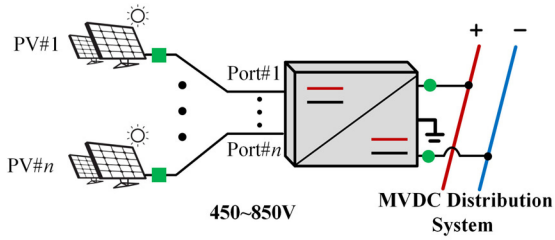

Fig. 1. DC integration of distributed PV via multiport dc–dc converter.

1) Protection under bidirectional power flow.
2) Overload of transformers and distribution lines/cables.
3) Power quality issue caused by inverter harmonics.

Thus, the multiport MVdc integration of distributed PV could be introduced as a new approach. As the typical scenario shown in Fig. 1, n PV arrays are connected to a bipolar MVdc distribution grid via a specially designed multiport dc–dc converter.

As the key equipment of dc integration system, the multiport dc–dc converter should satisfy several following requirements.

1) High voltage conversion ratio and high efficiency.
2) Independent MPPT control on different input ports.
3) Capability to operate under power-mismatch condition.
4) Fault isolation among different input branches.

Nowadays, the research on medium voltage dc (MVdc)/low voltage dc (LVdc) integration of PV systems is becoming a hotspot in the area of renewable energy [1]–[8]. Based on the different application scenarios, several topologies have been investigated from various aspects [9]–[15].

The input-independent and output-series (IIOS) connected modular configuration with isolated submodules (SMs), as shown in Fig. 2(a), could be considered as a feasible way to obtain a high voltage conversion ratio while guaranteeing a high power conversion efficiency.

It should be noted that all PV arrays in the proposed system [see Figs. 1 and 2(a)] should be grounded to limit the potential of PV strings because the maximum permissible voltage of commercially available PV modules is usually 1/1.5 kV, which is much lower than MVdc level. Thus, an isolated dc–dc conversion is needed in each SM to ensure the voltage stacking on MVdc side, as shown in Fig. 2(a).

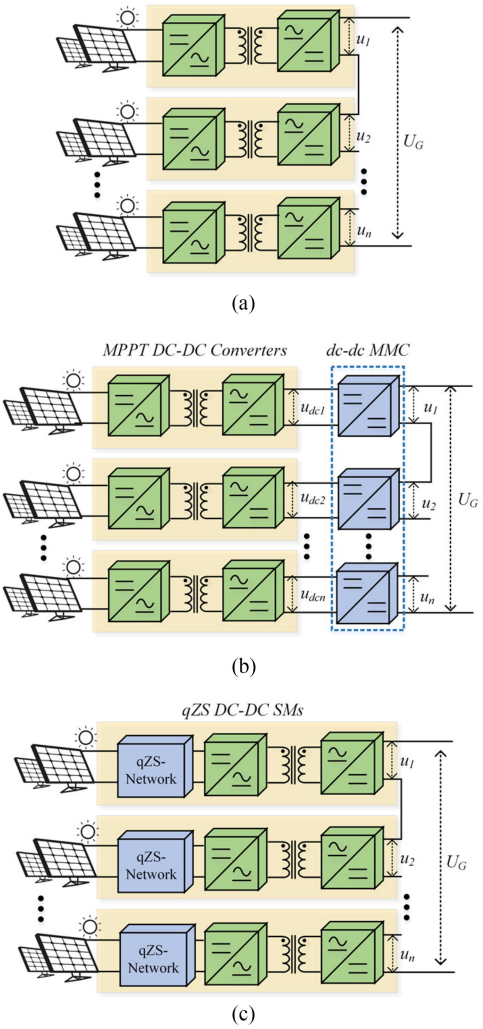

Fig. 2. Elementary topologies: IIOS configuration with isolated SMs. (a) With single-stage isolated SMs. (b) With two-stage isolated SMs. (c) With single-stage isolated qZS SMs.

Due to different irradiance, the output power of PV arrays fluctuates in a wide range, which results in an inevitable power-mismatch issue among the SMs in IIOS converter. A brief analysis of the power-mismatch phenomena in IIOS converter with single-stage SMs, as shown in Fig. 2(a), could be conducted with the assumption that all the PV arrays have the same capacity and physical characteristics.

If m of n PV arrays were shaded, their maximum output power would drop to $1/k$ ($k > 1$) of the rated value. For those unshaded PV arrays, the voltage conversion ratio g would rise from the rated value G_n to a higher value G'. Ignoring the variation of maximum power point (MPP) voltage, we can have following equation:

$$G' = \frac{kn}{(n-m)\,k+m} G_n = \frac{kU_G}{[(n-m)\,k+m]\,U_{pv-mpp}} \quad (1)$$

where U_G is the MVdc grid voltage, which is also the output voltage of IIOS converter; $U_{pv\text{-}mpp}$ is the MPP voltage of PV

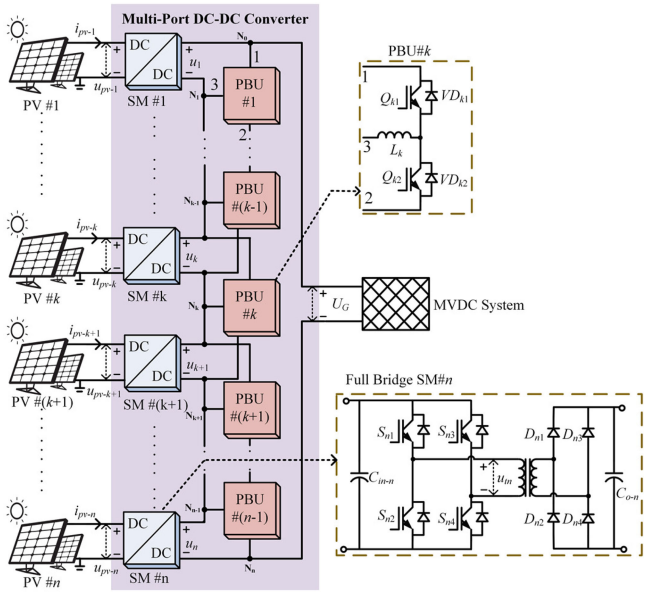

Fig. 3. Proposed topology of IIOS dc–dc converter with PBUs.

arrays. If k is very large, (1) could be simplified to

$$G' = \frac{n}{n-m} G_n. \quad (2)$$

Unfortunately, for isolated SMs, the voltage conversion ratio g is seriously restricted by the turning ratio of high-frequency (HF) transformer. Thus, it is usually impossible for the SMs to reach the voltage conversion ratio G' due to the limited voltage step-up capability. Thus, the output voltage of corresponding PV arrays will deviate from their MPP voltage and the total generated power will decrease.

In order to solve the power-mismatch problem, several alternative topologies have been proposed in [16]–[19]. The configurations of IIOS converter with two-stage SMs or quasi-Z-source network (qZSN) have been presented in Fig. 2(b) and (c), respectively. With the assistance of additional dc–dc MMC stage [16] or qZSN [17]–[19], the voltage-regulation capability of isolated SMs is enhanced to reduce the negative effects of power mismatch. However, both the cost and power losses will be increased with more complicated topologies and more conversion stages, while the voltage conversion ratio is still a key concern.

From the above analysis, it is clearly seen that the power mismatch caused by a wide-range variation of input power could be identified as the main challenge for IIOS converter, which should be taken into consideration in the topology design.

Thus, the concept of intermodule power balancing has been integrated into modular converter, and consequently, a novel topology of IIOS-connected modular dc–dc converter with intermodule power balancing units (PBUs) has been proposed in this paper (see Fig. 3).

The rest of this paper is organized as follows. The topology and working principles of the proposed IIOS converter are described in Section II. The design principles of major passive components are discussed in Section III along with the specifications of defined SMs and PBUs. A detailed analysis of power

efficiency is performed in Section IV. In Section V, different IIOS topologies for dc integration of PV are compared from the aspects of operation range, topology complexity, component stress, and power efficiency. In Section VI, the results of system simulations and down-scaled experiments are analyzed. Finally, the conclusions and future directions are presented in Section VII.

II. Topology and Working Principles

Several PBU technologies have been used for the balancing control of bipolar dc grids, energy storage system (ESS), and the PV distributed maximum power point tracking (DMPPT) [20]–[24]. In [25]–[27], the PBU concept is further applied to the multistage converter system to balance the power from multiple front-end sources. In this paper, the concept of PBU is developed and extended to the single-stage IIOS modular dc–dc converter with multiple power inputs to form a novel topology, which has been proposed in Fig. 3.

As the basis for further analysis, the working principles of the proposed topology are explored in this section.

A. Topology Description

As shown in Fig. 3, the proposed topology consists of n single-stage isolated dc–dc SMs (SM#1–SM#n) with independent MPPT function and $(n-1)$ intermodule PBUs for the elimination of mismatched power. The PBU is a two-port circuit that contains one inductor and two active switches. The H-bridge dc–dc conversion topology with HF isolation and unidirectional power flow is adopted in SMs.

B. Operation Principles of PBUs

As shown in Fig. 3, PBU#k is connected with both SM #k and SM# $(k+1)$ for intermodule power exchange. According to the power flow directions, the operation of PBU#k can be divided into two modes, and each operation mode contains two working substates defined by switching states of Q_{k1} or Q_{k2}.

As a result, there are four basic working substates under two operation modes, which are, respectively, illustrated in Fig. 4. For the convenience of analysis, C_{o-k} and C_{o-k+1} are used to represent the output capacitor in SM#k and SM#$(k+1)$, respectively. P_k and P_{k+1} are the average output power of SM#k and #$(k+1)$. $\Delta I_k'$ is the average current drawn from SM#k and $\Delta I_k''$ is the average current injected into SM#$(k+1)$. I_{o-k} is the average output current of SM#k.

Mode 1: In this mode, Q_{k2} is kept OFF while the duty ratio of Q_{k1} is controlled to transfer energy from SM#k to SM#$(k+1)$.

When Q_{k1} is ON [i.e., substate I as shown in Fig. 4(a)], L_k is charged by C_{o-k} through $Q_{k1}-L_k-C_{o-k}$. When Q_{k1} is OFF [i.e., substate II as shown in Fig. 4(b)], VD_{k2} conducts to form $L_k-C_{o-k+1}-VD_{k2}$ and the energy stored in L_k will be transferred to C_{o-k+1}.

Mode 2 : In this mode, Q_{k1} is kept OFF while the duty ratio of Q_{k2} is controlled to transfer energy from SM#$(k+1)$ to SM#k.

When Q_{k2} is ON [i.e., substate III as shown in Fig. 4(c)], L_k is charged by C_{o-k+1} through $C_{o-k+1}-L_k-Q_{k2}$. When Q_{k2} is OFF [i.e., substate IV as shown in Fig. 4(d)], VD_{k1} conducts to form $L_k-VD_{k1}-C_{o-k}$ and the energy stored in L_k will be transferred to C_{o-k}.

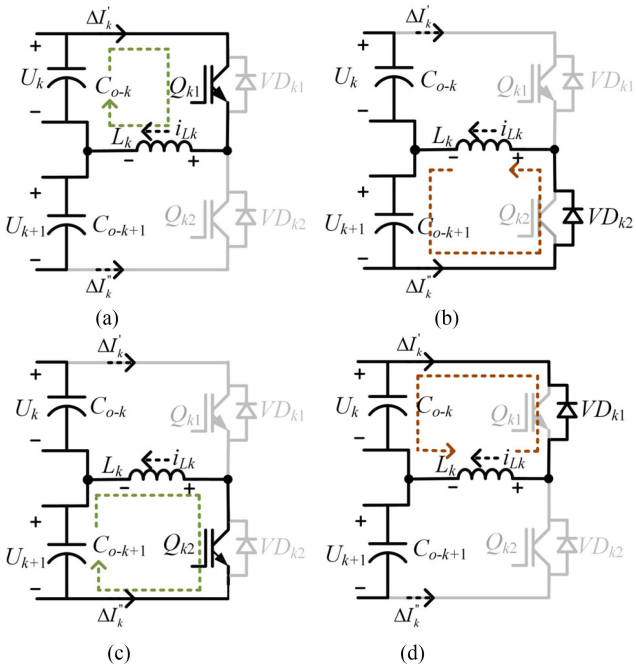

Fig. 4. Equivalent circuit of PBU#k under different working substates. (a) Substate I (Q_{k1} ON, Q_{k2} OFF). (b) Substate II (Q_{k1} Q_{k2} OFF, VD_{k2} ON). (c) Substate III (Q_{k1} OFF, Q_{k2} ON). (d) Substate IV (Q_{k1} Q_{k2} OFF, VD_{k1} ON).

The change of capacitor voltage is regarded as a slow process relative to the switching of Q_{k2} and Q_{k2}. Therefore, the average output voltage of SM#k and SM#$(k+1)$, U_k, and U_{k+1} can be considered as constant values in circuit analysis of PBU#k.

In *Mode* 1, with voltage-second balance is applied to inductor L_k in the steady state, it can be derived that

$$U_k D_{k1} T_s - U_{k+1}(1-D_{k1})T_s = 0 \tag{3}$$

where T_s is the switching cycle of PBU, D_{k1} is the steady-state duty ratio of Q_{k1}.

The similar derivation can also be performed in *Mode* 2, which results in

$$-U_{k+1} D_{k2} T_s + U_k(1-D_{k2})T_s = 0 \tag{4}$$

where D_{k2} is the steady-state duty ratio of Q_{k2}.

From (3) and (4), the steady-state duty ratio D_{k1} (or D_{k2}) of Q_{k1} (or Q_{k2}) in *Mode* 1 (or 2) can be expressed as

$$D_{k1} = \frac{U_{k+1}}{U_k + U_{k+1}} \quad D_{k2} = \frac{U_k}{U_k + U_{k+1}}. \tag{5}$$

In both *Modes* 1 and 2, when Q_{k1} or Q_{k2} is ON, the absolute value of inductor current $|i_{\mathrm{Lk}}|$ will increase; when Q_{k1} or Q_{k2} is OFF, $|i_{\mathrm{Lk}}|$ will decrease.

Therefore, the average inductor current I_{Lk} can be regulated by adjusting duty ratio d_{k1} in *Mode* 1, or d_{k2} in *Mode* 2. If $d_{k1} > D_{k1}$ (or $d_{k2} > D_{k2}$), $|I_{\mathrm{Lk}}|$ will increase; if $d_{k1} < D_{k1}$ (or $d_{k2} < D_{k2}$), $|I_{\mathrm{Lk}}|$ will decrease.

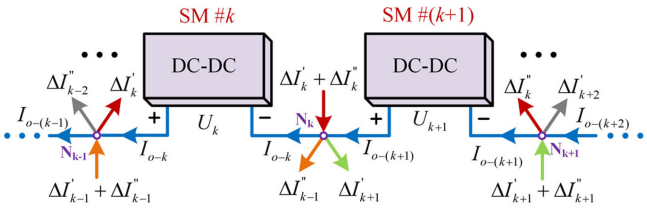

Fig. 5. Output-side equivalent circuit of IIOS converter with PBUs.

From the working principles of PBU#k, $\Delta I'_k$, could be expressed as

$$\Delta I'_k = \begin{cases} D_{k1} I_{\mathrm{Lk}} & \text{Mode } 1 \\ (1 - D_{k2}) I_{\mathrm{Lk}} & \text{Mode } 2 \end{cases} \tag{6}$$

and $\Delta I''_k$ could be expressed as

$$\Delta I''_k = I_{\mathrm{Lk}} - \Delta I'_k = \begin{cases} (1 - D_{k1}) I_{\mathrm{Lk}} & \text{Mode } 1 \\ D_{k2} I_{\mathrm{Lk}} & \text{Mode } 2. \end{cases} \tag{7}$$

With power losses neglected, the average power transferred through PBU#k in one switching cycle, ΔP_k, can be derived as

$$\Delta P_k = \Delta I'_k U_k = \Delta I''_k U_{k+1} \tag{8}$$

in both *Modes* 1 and 2. Thus, from (5)–(8), ΔP_k can be derived as

$$\Delta P_k = \frac{U_k U_{k+1}}{U_k + U_{k+1}} I_{\mathbf{Lk}} \tag{9}$$

which is mainly determined by I_{Lk}. As a result, d_{k1} (or d_{k2}) can be used as the control variable to regulate ΔP_k in *Mode* 1 (or 2).

For the IIOS topology shown in Fig. 3, the equivalent circuit of MVdc side in the steady state could be illustrated as Fig. 5, neglecting the power losses in SMs, it could be derived that

$$P_k = I_{o-k} U_k. \tag{10}$$

With Kirchhoff's current law (KCL) applied to node N_k, we can have

$$\Delta I'_k + \Delta I''_k + I_{o-(k+1)} = I_{o-k} + \Delta I''_{k-1} + \Delta I'_{k+1}. \tag{11}$$

Thus, from (8), (10), (11), it could be derived that

$$\frac{U_k}{U_{k+1}} = \frac{P_k - \Delta P_k + \Delta P_{k-1}}{P_{k+1} + \Delta P_k - \Delta P_{k+1}} = \frac{P'_k}{P'_{k+1}} \tag{12}$$

where P'_k and P'_{k+1} are the equivalent output power of SM#k and SM#$(k+1)$.

Thus, a voltage-feedback-based power balancing control strategy could be designed to eliminate the mismatched power between SM#k and SM#$(k+1)$, as described in Fig. 6.

In outer loop, the error of u_k and u_{k+1}, e_{uk}, is processed by PI regulator to produce the reference i^*_{Lk} for a mode selection and inductor current control. SF_k, which is determined by i^*_{Lk} as (13), is defined as the flag variable for the operation mode selection. If $SF_k = 1$, PBU#k will be operated in *Mode* 1; if $SF_k = 0$, PBU#k will be operated in *Mode* 2.

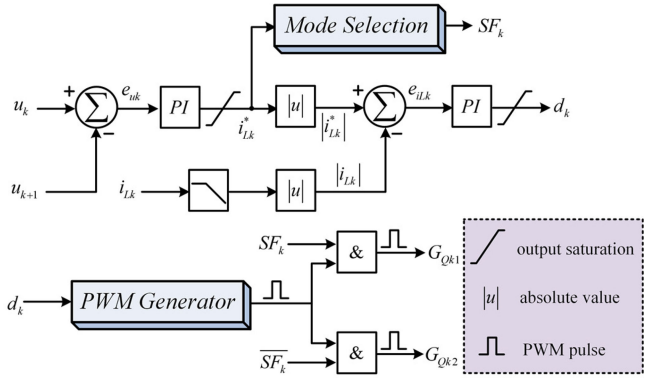

Fig. 6. Power balancing control strategy and PWM generation for PBUs.

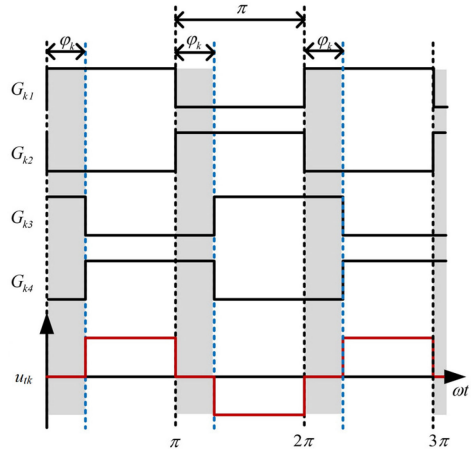

Fig. 7. Phase-shift control of H-bridge SMs and relative waveforms.

$$SF_k = 1 - \overline{SF_k} = \begin{cases} 1, & i^*_{Lk} \geq 0 \\ 0, & i^*_{Lk} < 0. \end{cases} \tag{13}$$

In inner loop, the error of $|i^*_{\mathrm{Lk}}|$ and $|i_{\mathrm{Lk}}|$, e_{iLk}, is processed by PI regulator to calculate d_k, which is adopted as the duty ratio d_{k1} (or d_{k2}) in *Mode* 1 (or 2) for the regulation of average inductor current. Based on SF_k and d_k, the gate pulses G_{Qk1} and G_{Qk2} could be generated (as shown in Fig. 6). With the same power balancing control strategy applied to all PBUs, the equivalent output power of SM#1–SM#n can be automatically balanced in the steady state as

$$e_{uk} = 0 \; k \in 1 \sim (n-1) \quad P'_i = P'_j \quad i, j \in 1 \sim n. \tag{14}$$

C. Operation Principles of SMs

Normally, the SMs are operated in the MPPT modes, in which the phase-shift control is used to regulate the input voltage and current on each PV port. The gate pulses G_{k1}–G_{k4} (for S_{k1}–S_{k4}, respectively) and voltage u_{tk} on the primary side of HF transformer are shown in Fig. 7. For SM#k, the relationship between the average input and output voltage, U_{pv-k} and U_k, in the steady state can be approximately derived as

$$U_k \approx (1 - \varphi_k/\pi) N U_{pv-k} \tag{15}$$

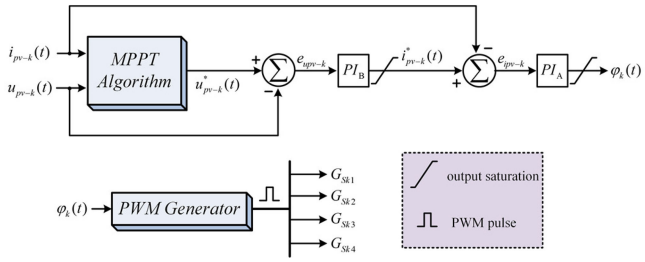

Fig. 8. Control strategy and modulation of H-bridge SMs.

where φ_k is the phase-shift angle of SM#k and N is the turning ratio of HF transformers in each SM. For the accuracy and response speed of MPPT control, a variable step-size P&O algorithm [28]–[31] is adopted. The detailed algorithm of this method is expressed by (16)–(19), with a special variable α introduced for the dynamic regulation of MPPT step size.

$$\Delta p = u_{pv-k}(t) i_{pv-k}(t) - u_{pv-k}(t-1) i_{pv-k}(t-1) \quad (16)$$

$$\Delta u = u_{pv-k}(t) - u_{pv-k}(t-1) \quad (17)$$

$$\alpha = \begin{cases} \mathrm{K} & \Delta p/\Delta u \geq \mathrm{K} \\ \Delta p/\Delta u & |\Delta p/\Delta u| \leq \mathrm{K} \\ -\mathrm{K} & \Delta p/\Delta u \leq -\mathrm{K} \end{cases} \quad (18)$$

$$u^*_{pv-k}(t) = u^*_{pv-k}(t-1) + \alpha \Delta u_{\mathrm{ref}} \quad (19)$$

where K is a positive constant, Δu_{ref} is the base value of MPPT step size, α is the step-size coefficient, $u_{pv-k}(t-1)$ and $u_{pv-k}(t)$ are the input voltage of SM#k in control cycle $t-1$ and t, respectively. $i_{pv-k}(t-1)$ and $i_{pv-k}(t)$ are the input current of SM#k in control cycle $t-1$ and t, respectively. Δp and Δu are increments of input power and input voltage in SM#k. $u^*_{pv-k}(t)$ is the reference of input voltage in control cycle t.

The complete control diagram of SM#k is shown in Fig. 8 for reference.

D. Protection and Emergency Control Under Fault Conditions

As one aspect of topology analysis, the basic protection and emergency control principles under different fault conditions are explored in this part. As shown in Fig. 9, following three types of the faults will be considered.

1) *Fault Type* 1 (*FT*.1): Faults on the input ports or capacitors of SMs.
2) *Fault Type* 2 (*FT*.2): Faults on the output ports or capacitors of SMs.
3) *Fault Type* 3 (*FT*.3): Faults on the PCC of MVdc grid.

FT.1: If *FT*.1 occurs on SM#k, fault current will be injected to the fault point by $C_{\mathrm{in}-k}$. Due to the unidirectional power flow characteristic of SMs, no power could be fed to the fault point from the MVdc side. In this condition, dc breaker BR_{pv-k} will be opened to disconnect PV#k from the fault point while the gate pulses in SM#k (G_{k1}–G_{k4}) will be blocked. As a result, P_k will drop to zero. But the differential power will be compensated by PBUs immediately to keep the converter working normally.

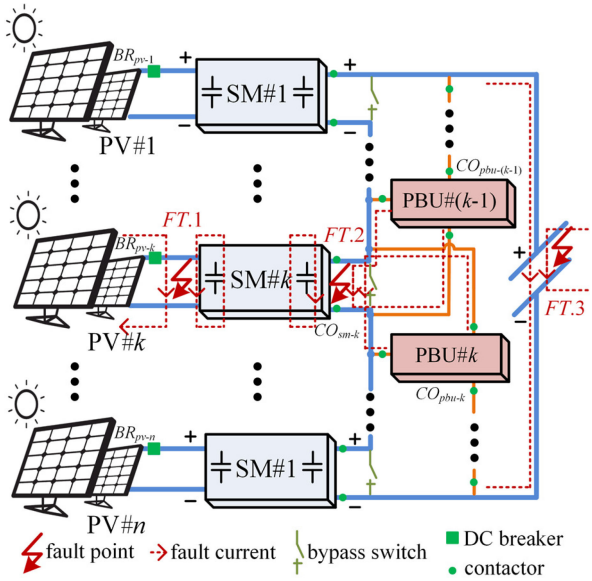

Fig. 9. Typical fault conditions in the proposed system.

FT.2: If *FT*.2 occurs on SM#k, fault current will be injected to the fault point by C_{o-k}, PBU#k, and PBU#$(k-1)$, which means that both PV#k and the MVdc grid feed power to the fault point. In this condition, all gate pulses in SM#k, PBU#k, and PBU#$(k-1)$ will be blocked immediately to suppress the fault current. When the discharging current from C_{o-k} drops to an appropriate level, the contactors $CO_{\mathrm{sm}-k}$, $CO_{\mathrm{pbu}-k}$, and $CO_{\mathrm{pbu}-(k-1)}$ will be opened to isolate the fault part from the converter system. Meanwhile, the bypass switch that is parallel to SM#k will be closed to bear the output current of the series-connected system. By this way, the remaining part of the converter could remain working to ride through the internal fault. Without PBU#k and #$(k-1)$, the equivalent output power of the remaining SMs can only achieve local equalization as

$$P'_i = P'_j \quad i, j \in 1 \sim (k-1) \text{ or } i, j \in (k+1) \sim n. \quad (20)$$

FT.3: If *FT*.3 occurs, fault current will be injected to the fault point by both the IIOS converter and MVdc grid. In this condition, the gate pulses in all SMs and PBUs will be blocked immediately to stop injecting current and power to the fault point. Once the discharging current from the SMs' output capacitors drops to an appropriate level, the contactors CO_{sm-1}–$CO_{\mathrm{sm}-n}$ and CO_{pbu-1}–$CO_{\mathrm{pbu}-(n-1)}$ will be immediately opened. The breakers BR_{pv-1}–BR_{pv-n} will also be opened to isolate the PV arrays.

III. Design of Major Passive Components

The PBU inductance and output capacitance of SMs could be designed according to the boundary operation conditions.

For n-port IIOS dc–dc converter that contains n SMs and $(n-1)$ PBUs (shown in Fig. 3), the rated output voltage and

power of each SM, $U_{\rm ns}$, and $P_{\rm ns}$ could be expressed as

$$U_{ns} = \frac{U_G}{n} \quad P_{ns} = \frac{P_n}{n} \tag{21}$$

where U_G and P_n are the rated output voltage and power of the entire IIOS converter.

Since all the PBUs and SMs in IIOS converter are supposed to have the same parameters, PBU#*k* and SM#*k* could be taken as examples for the design of passive components.

A. Estimation of Differential Power

Neglecting the power losses, the output power of SM#*k* is equal to the input power on *k*th PV port as

$$P_k = P_{pv-k}. \tag{22}$$

It is obvious that the steady-state differential power transferred through PBU#*k* (ΔP_k) is fully determined by the input power on PV ports #1–#*n*. From (12) and (22), the balanced output power in the steady state could be derived as

$$P_1' = P_2' = \cdots = P_n' = \frac{1}{n}\sum_{i=1}^{n} P_{pv-i}. \tag{23}$$

Consider SM#1–SM#*k* along with PBU#1–PBU#($k-1$) as a generalized node in the circuit, ΔP_k can be derived as

$$\Delta P_k = \sum_{i=1}^{k} P_{pv-i} - \sum_{i=1}^{k} P'_i = \sum_{i=1}^{k} P_{pv-i} - \frac{k}{n}\sum_{i=1}^{n} P_{pv-i}. \tag{24}$$

Let λ to be the equal of *k*/*n*, (24) can be expressed as

$$\Delta P_k = (1-\lambda)\sum_{i=1}^{k} P_{pv-i} - \lambda \sum_{i=k+1}^{n} P_{pv-i}. \tag{25}$$

Because $0 \le P_{pv-i} \le P_{\rm ns}$, it can be derived from (25) that

$$-\lambda(n-k)P_{\mathbf{ns}} \le \Delta P_k \le k(1-\lambda)P_{\mathbf{ns}}. \tag{26}$$

Therefore, the maximum power transferred through PBU#*k*, $|\Delta P_k|_{\max}$, can be calculated as

$$|\Delta P_k|_{\max} = k\,(1-k/n)\,P_{\rm ns} = \lambda\,(1-\lambda)\,P_n$$
$$\lambda = k/n, \quad k = 1, 2 \ldots, n-1. \tag{27}$$

For $0 < \lambda < 1$, it could be derived that

$$\frac{d|\Delta P_k|_{\max}}{d\lambda} = 0\Big|_{\lambda=\frac{1}{2}}. \tag{28}$$

So, we can have

$$|\Delta P_k|_{\max} \le |\Delta P_k|_{\max}|_{\lambda=\frac{1}{2}} = \frac{1}{4}P_n. \tag{29}$$

Equation (29) can be used as a reference for the design of passive components.

B. Determination of the Minimum Inductance in PBU

Inductor L_k in PBU#*k* could be designed according to the limit of inductor current ripple. With the maximum differential power $|\Delta P_k|_{\max}$ transferred, the peak value of $i_{\rm Lk}$ could be expressed as

$$|i_{\rm Lk}|_{\max} = |I_{\rm Lk}|_{\max}\,(1 + 0.5\varepsilon_i) \tag{30}$$

where $|I_{\rm Lk}|_{\max}$ and ε_i are the average value and peak-to-peak ripple ratio of $i_{\rm Lk}$, correspondingly. Considering the current limit of Q_{k1} and Q_{k2}, denoted by $I_{\max}$, we can have

$$|i_{\rm Lk}|_{\max} \le I_{\max}. \tag{31}$$

Therefore, with (9) and (29)–(31), the upper limit of ε_i could be derived as

$$\varepsilon_i \le \frac{4U_G I_{\max}}{nP_n} - 2. \tag{32}$$

With ε_i determined by (32), the minimum value of L_k could be derived from (5), (9), (21), and (29) as

$$L_k \ge \frac{U_G^2}{\varepsilon_i n^2 f_s P_n} \tag{33}$$

where f_s is the switching frequency of PBU.

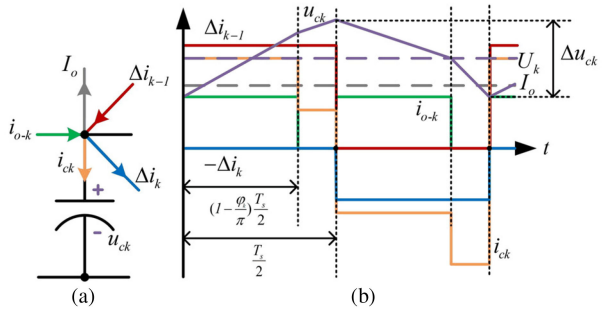

Fig. 10. Ripple analysis of C_{o-k} in the steady state.

C. Determination of the Minimum Output Capacitance in SM

The output capacitance in SMs can be designed according to the limit of output voltage ripple ratio. As shown in Fig. 10(a), it can be derived from KCL that

$$\Delta i_{k-1} + i_{o-k} - \Delta i_k - I_o - i_{\mathbf{ck}} = 0 \tag{34}$$

where Δi_{k-1} is the instantaneous current injected to C_{o-k} by PBU#($k-1$); Δi_k is the instantaneous current drawn from C_{o-k} by PBU#*k*; i_{o-k} is the instantaneous output current of SM#k; I_o is the output current of IIOS converter, which could be regarded as a constant in one switching cycle. $i_{\rm ck}$ is the instantaneous value of charging/discharging current of C_{o-k}. With charge balance principle applied, (34) can be derived as

$$\Delta I_{k-1} + I_{o-k} - \Delta I_k = I_o = \frac{1}{U_G}\sum_{i=1}^{n} P_{pv-i} \tag{35}$$

where ΔI_{k-1}, ΔI_k, and I_{o-k} are the average value of Δi_{k-1}, Δi_k, and i_{o-k} in one switching cycle.

The maximum value of peak-to-peak voltage ripple $\Delta u_{\rm ck}$ could be estimated in the worst condition that PBU#($k-1$) and PBU#*k* are modulated with reverse-phase carrier waves, as shown in Fig. 10(b).

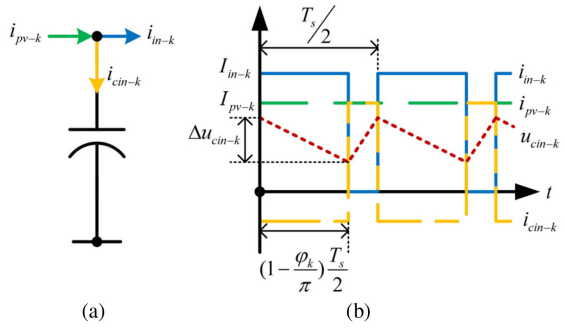

Fig. 11. Ripple analysis of $C_{\mathrm{in}-k}$ in the steady state.

Assuming that the SMs are operated under the same switching frequency (f_s) as the PBUs, the maximum value of Δu_{ck} can be calculated from (9), (12), (15), (21)–(29), (34), and (35).

$$|\Delta u_{\mathrm{ck}}|_{\max} = \frac{n}{2f_s C_{o-k} U_G} \left[\sum_{i=1}^{k-1} P_{pv-i} + (1-u)\sum_{i=1}^{k} P_{pv-i} - u\sum_{i=k+1}^{n} P_{pv-i}\right]$$
$$u = (2k-1)/n. \tag{36}$$

With mathematical techniques, it can be derived from (36) that

$$|\Delta u_{\mathrm{ck}}|_{\max} \le \frac{(n-1)\,P_n}{4f_s C_{o-k} U_G}. \tag{37}$$

Thus, the minimum value of C_{o-k}, can be determined according to the limit of output voltage ripple, expressed as

$$C_{o-k} \ge \frac{n(n-1)P_n}{4r_{\mathrm{vo}} f_s U_G^2} \tag{38}$$

where r_{vo} is the peak-to-peak ripple ratio of the output voltage in each SM.

D. Restriction of LC Resonant Frequency

In order to prevent the series *LC* resonance between C_{o-k} (or C_{o-k+1}) and L_k, the resonant frequency f_{r-k} must be lower than the switching frequency of PBU as

$$f_s > M\ f_{r-k} = \frac{M}{2\pi\sqrt{L_k C_{o-k}}} \tag{39}$$

where *M* is the margin factor. Thus, we can have

$$L_k C_{\mathrm{o-k}} \ge \frac{M^2}{4\pi^2 f_s^2}. \tag{40}$$

As a result, L_k and C_{o-k} could be designed together under the restrictions of (33), (38), (40).

E. Determination of the Minimum Input Capacitance in SM

The input capacitance of SMs could be designed according to the limit of input voltage ripple ratio. As shown in Fig. 11, the peak value of steady-state input current $I_{\mathrm{in}-k}$ could be derived as

$$I_{\mathrm{in}-k} = \frac{\pi P_{pv-k}}{(\pi-\varphi_k)\,u_{pv-k}}. \tag{41}$$

Assuming that PV #*k* is working on its MPP voltage with the rated output power, the peak-to-peak value of input voltage ripple could be calculated as

$$|\Delta u_{\mathrm{cin}-k}|_{\max} = \frac{\varphi_k T_s P_{\mathrm{ns}}}{2\pi C_{\mathrm{in}-k} U_{pv\text{-}mpp}}. \tag{42}$$

As a result, the minimum value of $C_{\mathrm{in}-k}$, can be determined according to the limit of input voltage ripple as

$$C_{\mathrm{in}-k} \ge \frac{\varphi_k P_n}{2\pi n r_{\mathrm{vi}} f_s U_{pv\text{-}mpp}^2} \tag{43}$$

where r_{vi} is the peak-to-peak ripple ratio of the input voltage in each SM.

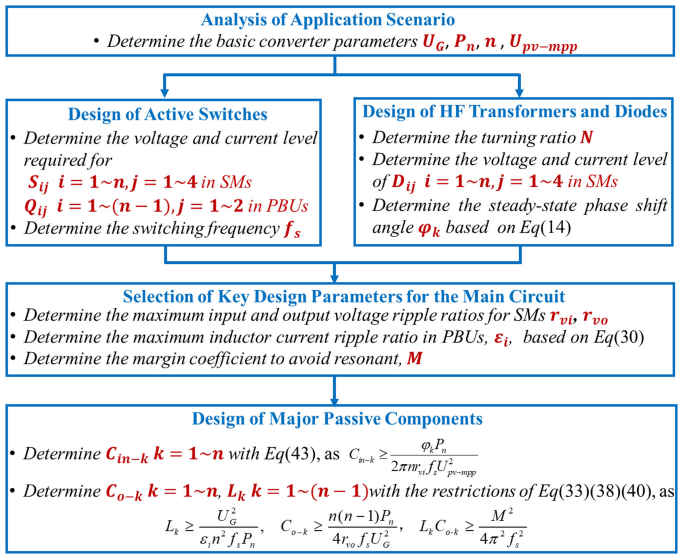

Fig. 12. Flowchart for the circuit design of IIOS converter with PBUs.

F. Specification Definition of IIOS Converter

With the principles discussed in Section III-B–Section III-E, the process of circuit design can be summarized by a flowchart, as shown in Fig. 12. A 400 kW IIOS converter containing eight SMs and seven PBUs is designed as an example for further analysis with its detailed parameters listed in Table I.

IV. Power Efficiency Analysis

Since power efficiency is the one of the main concerns of distributed PV generation system, it is necessary to analyze the power losses in PBUs and SMs. In this section, a quantitative analysis for different kinds of power losses will be performed in the steady state to estimate the panel-to-grid power efficiency of the proposed IIOS converter.

Without loss of generality, PBU#*k* and SM#*k* are taken as examples for the calculation of power losses.

TABLE I
SPECIFICATIONS OF DEFINED 400 KW IIOS CONVERTER

Parameters	Values
MVDC grid voltage U_G	*6 kV*
Converter rated power P_n	*400 kW*
Number of SMs n	*8*
PV arrays connected to input-ports	
Maximum power	*50.4 kW*
Panels in series	*15*
Strings in parallel	*11*
MPP voltage $U_{pv\text{-}mpp}$	*820.5 V*
H-Bridge SMs (SM#k)	
SM rated power P_{ns}	*50 kW*
Rated output voltage U_{ns}	*750 V*
Input voltage range of PV-ports	*550 V~850 V*
Output capacitance $C_{o\text{-}k}$	*350 uF*
Intput capacitance $C_{in\text{-}k}$	*150 uF*
Switching frequency f_s	*10 kHz*
high frequency transformer turning ratio N	*1.5*
Peak-to-peak output voltage ripple ratio r_{vo}	*5%*
Peak-to-peak input voltage ripple ratio r_{vi}	*1%*
Active switches(IGBT)	*1700 V/150 A*
Fast recovery diodes	*1700 V/140 A*
Steady-state phase-shift angle φ_k	*1.2 rad*
PBUs (PBU#k)	
Switching frequency f_s	*10 kHz*
margin coefficient to avoid resonant M	*5*
Peak-to-peak current ripple ratio ε_i	*25%*
Inductance L_k	*0.6 mH*
Active switches(IGBT)	*3300 V/450 A*

A. Calculation of Power Losses in PBU#k

For PBUs, the power losses consist of switching losses, conduction losses, and inductor losses. Following analysis is performed with the assumption that PBU*#k* is operated in *Mode* 1, as defined in Section II-B. For *Mode* 2, the same results could be obtained.

1) Switching Losses of Q_{k1} and Q_{k2}: From circuit analysis in Section II-B, the switching actions of Q_{k1} and Q_{k2} can be summarized as follows:

1) Q_{k1} turns ON and OFF once in every switching cycle, while the corresponding switching voltage and current are $2U_{\rm ns}$ and $i_{\rm Lk}$, respectively.
2) Q_{k2} is kept OFF during the whole cycle, while the reverse recovery losses of its anti-parallel diode occurs at the voltage of $2U_{\rm ns}$ and the current of $i_{\rm Lk}$.

According to the above analysis, the total switching losses of both Q_{k1} and Q_{k2} in the steady state, $P_{\rm SW-PBU-}k$, could be calculated as

$$P_{\rm SW-PBU-}k = \frac{1}{T_s}\int_0^{T_s} \frac{2U_G f_s}{nU_{\rm ref1}I_{\rm ref1}} \times \left(i_{\rm Lk}E_{\rm on1} + i_{\rm Lk}E_{\rm off1} + i_{\rm Lk}E_{\rm DREC1}\right) dt \quad (44)$$

where $E_{\rm on1}$, $E_{\rm off1}$, and $E_{\rm DREC1}$ are the turn-ON, turn-OFF, and reverse recovery energy of Q_{k1} and Q_{k2}; $U_{\rm ref1}$ and $I_{\rm ref1}$ are the reference values for the switching voltage and current of Q_{k1} and Q_{k2}. All above parameters can be referred to in the datasheet of power semiconductor devices.

From (9) and (44), it can be derived that

$$P_{\rm SW-PBU-}k = \frac{4\left|\Delta P_k\right| f_s}{U_{\rm ref1}I_{\rm ref1}}\left(E_{\rm on1} + E_{\rm off1} + E_{\rm DREC1}\right). \quad (45)$$

2) Conduction Losses of Q_{k1} and Q_{k2}: For a specific switching device, the average conduction losses during a switching cycle, $P_{\rm CON}$, can be expressed by

$$P_{\rm CON} = I_{\rm AVE}U_{\rm ON} + I_{\rm RMS}^2 R_{\rm ON} \quad (46)$$

where $U_{\rm ON}$ is the ON-state voltage of both switching device and its antiparallel diode. $R_{\rm ON}$ is the ON-state resistance of both switching device and its antiparallel diode. $I_{\rm AVE}$ and $I_{\rm RMS}$ are the average value and rms value of the steady-state current that flows through the switching device, respectively.

According to the analysis in Section II-B, the conduction losses of Q_{k1} and VD_{k2}, $P_{\rm CON-PBU-}k-1$ and $P_{\rm CON-PBU-}k-2$, can be calculated as

$$P_{\rm CON-PBU-}k-1 = P_{\rm CON-PBU-}k-2 = \frac{1}{2}I_{\rm Lk}U_{\rm ON1} + \frac{1}{2}I_{\rm Lk}^2 R_{\rm ON1} \quad (47)$$

where $U_{\rm ON1}$ and $R_{\rm ON1}$ are the ON-state voltage and resistance of Q_{k1} and VD_{k2}.

From (9) and (47), the total conduction losses in PBU#*k*, $P_{\rm CON-PBU-}k$, can be derived as

$$P_{\rm CON-PBU-}k = \frac{2nU_{\rm ON1}}{U_G}\left|\Delta P_k\right| + \frac{4n^2 R_{\rm ON1}}{U_G^2}\left|\Delta P_k\right|^2. \quad (48)$$

3) Power Losses of Inductor L_k: The inductor losses in PBU#*k* usually include core losses and copper losses. Since the core losses are usually affected by magnetic materials, geometries, and working conditions, it needs a complex estimation with empirical formulas [32], [33]. Here, it is noted that only the steady-state copper losses, $P_{\rm Lk-copper}$, are discussed. With the average inductor current $I_{\rm Lk}$ and parasitic resistance $r_{\rm Lk}$, we have

$$P_{\rm Lk-copper} = I_{\rm Lk}^2 r_{\rm Lk} = \frac{4n^2 r_{\rm Lk}}{U_G^2}\left|\Delta P_k\right|^2 \quad (49)$$

Thus, the total power losses of PBU#*k* can be estimated as

$$P_{\rm loss-PBU-}k = A_1\left|\Delta P_k\right| + A_2\left|\Delta P_k\right|^2 \quad (50)$$

where A_1 and A_2 are the power loss coefficients of PBU, which could be determined by (45), (48), and (49).

B. Calculation of Power Losses in SM#k

For SMs, the power losses consist of switching losses, conduction losses, capacitor losses, and transformer losses, which are analyzed, respectively.

1) Switching Losses of S_{k1}–S_{k4} and D_{k1}–D_{k4}: From circuit analysis in Section II-C, the switching actions of S_{k1}–S_{k4} and D_{k1}–D_{k4} could be summarized as follows.

1) For S_{k1} and S_{k2}, each of them turns ON once in the ZCS mode and turns OFF once in the hard switching mode during every switching cycle. For hard switching mode, the corresponding switching voltage and current are u_{pv-k} and $I_{{\rm in}-k}$, respectively.

2) For S_{k3} and S_{k4}, each of them turns ON once in the hard switching mode and turns OFF once in the ZCS mode during every switching cycle. For hard switching mode, the corresponding switching voltage and current are u_{pv-k} and $I_{\mathrm{in}-k}$, respectively.
3) For D_{k1}–D_{k4}, all of them are turned OFF naturally with a zero voltage, thus no reverse recovery losses are introduced during the operation.
4) Thus, the total switching losses of SM#*k* in the steady state, $P_{\mathrm{SW-SM}-k}$, could be calculated as

$$P_{\mathrm{SW-SM}-k} = \frac{2\pi f_s P_{pv-k}}{(\pi-\varphi_k)\, U_{\mathrm{ref2}} I_{\mathrm{ref2}}} \left(E_{\mathrm{on2}} + E_{\mathrm{off2}}\right) \tag{51}$$

where E_{on2}, E_{off2} are the turn-ON, turn-OFF energy of S_{k1}–S_{k4}; U_{ref2} and I_{ref2} are the reference values for the switching voltage and current of S_{k1}–S_{k4}.

2) Conduction Losses of S_{k1}–S_{k4} and D_{k1}–D_{k4}: According to the analysis in Section II-C, the total conduction losses of S_{k1}–S_{k4}, $P_{\mathrm{CON-SM}-k-1}$, can be calculated based on (46), as follows:

$$P_{\mathrm{CON-SM}-k-1} = \frac{2U_{\mathrm{ON2}}}{u_{pv-k}} P_{pv-k} + \frac{2\pi R_{\mathrm{ON2}}}{(\pi-\varphi_k)\, u_{pv-k}^2} P_{pv-k}^2 \tag{52}$$

where U_{ON2} and R_{ON2} are the ON-state voltage and resistance of S_{k1}–S_{k4}.

With the same method, the total conduction losses of D_{k1}–D_{k4}, $P_{\mathrm{CON-SM}-k-2}$, can be calculated as

$$P_{\mathrm{CON-SM}-k-2} = \frac{2nU_{\mathrm{ON3}}}{U_G} P_{pv-k} + \frac{2\pi n^2 R_{\mathrm{ON3}}}{(\pi-\varphi_k)\, U_G^2} P_{pv-k}^2 \tag{53}$$

where U_{ON3} and R_{ON3} are the ON-state voltage and resistance of D_{k1}–D_{k4}.

3) Capacitor Losses of $C_{\mathrm{in}-k}$ and C_{o-k}: From the circuit analysis in both Sections III-E and III-C (as illustrated in Fig. 9 and Fig. 10), the rms values of input capacitor current, $i_{\mathrm{cin}-k}$, could be derived as

$$\langle i_{\mathrm{cin}-k}\rangle_{\mathrm{rms}} = \frac{P_{pv-k}}{u_{pv-k}} \sqrt{\frac{\varphi_k}{\pi-\varphi_k}}. \tag{54}$$

For the convenience of calculation, the current transferred by PBU#*k* and #($k+1$) are neglected in the estimation of capacitor loss on C_{o-k}, thus the rms value of i_{ck} could be derived as

$$\langle i_{\mathrm{ck}}\rangle_{\mathrm{RMS}}\big|_{\substack{\Delta i_{k-1}=0 \\ \Delta i_k=0}} = \frac{nP_{pv-k}}{U_G} \sqrt{\frac{\varphi_k}{\pi-\varphi_k}}. \tag{55}$$

Thus, the capacitor losses of $C_{\mathrm{in}-k}$ and C_{o-k} could be derived as

$$P_{\mathrm{Cin}-k-\mathrm{loss}} = \langle i_{\mathrm{cin}-k}\rangle_{\mathrm{rms}}^2\, r_{\mathrm{esr1}} \quad P_{\mathrm{Co}-k-\mathrm{loss}} = \langle i_{\mathrm{ck}}\rangle_{\mathrm{RMS}}^2\, r_{\mathrm{esr2}} \tag{56}$$

where r_{esr1} and r_{esr2} are the equivalent series resistance of each input and output capacitor in SMs, respectively.

4) Transformer Losses: The transformer losses in SM#*k* include core losses and copper losses. The core losses $P_{\mathrm{tk-core}}$ could be estimated by Steinmetz formula with related parameters on the datasheet of magnetic material [34]. The copper losses could be calculated according to the rms value of the input current i_{tk} on the primary side of HF transformer as

$$P_{\mathrm{tk-copper}} \approx \langle i_{\mathrm{tk}}\rangle_{\mathrm{RMS}}^2\, R_{\mathrm{tk}} = \frac{\pi R_{\mathrm{tk}} P_{pv-k}^2}{(\pi-\varphi_k)\, u_{pv-k}^2} \tag{57}$$

where R_{tk} is the equivalent resistance of the winds in HF transformer.

Thus, the total power losses of SM#*k* can be estimated as

$$P_{\mathrm{loss-SM}-k} = B_1 P_{pv-k} + B_2 P_{pv-k}^2 + P_{\mathrm{Co}-k-\mathrm{loss}} + P_{\mathrm{tk-core}} \tag{58}$$

where B_1 and B_2 are the power loss coefficients of SMs, which are determined by (51–53) and (56–57).

C. Approximate Estimation for Power Efficiency

With the analysis of power losses in both Sections IV-A and IV-B, an approximate estimation for the power efficiency of the proposed IIOS converter with PBUs could be performed as

$$\eta = 1 - \frac{\sum_{i=1}^{n} P_{\mathrm{loss-SM}-i} + \sum_{j=1}^{n-1} P_{\mathrm{loss-PBU}-j}}{\sum_{i=1}^{n} P_{pv-i}} \tag{59}$$

in which η could be considered as a function of P_{pv-i} ($i = 1-n$).

V. Comparative Study

In this section, the proposed topology (*Topo.*1) will be compared with the IIOS topologies presented in literature [16] (*Topo.*2), and [19] (*Topo.*3) from the aspects of operation range, topology complexity, component stress, and power efficiency.

A. Comparison of Operation Range

For each SM (e.g., SM#*k*) in an IIOS converter that contains *n* SMs, the power mismatch factor (PMF) can be introduced to characterize the degree of power-mismatch phenomenon as

$$\mathrm{PMF}_k = \frac{P_{pv-k}}{\frac{1}{n}\sum_{i=1}^{n} P_{pv-i}} \in [0, n]\,. \tag{60}$$

If $\mathrm{PMF}_k = 1$, there is no mismatched power for SM#*k*; with $0 \le PMF_k < 1$, SM#*k* is operated below the average power; with $1 < PMF_k \le n$, SM#*k* is operated above the average power. The larger the deviation of PMF_k from 1, the higher the degree of power mismatch for SM#*k*.

In *Topo.*1–3, the possible ranges of PMF and input voltage for each SM have been calculated based on their working principles, as listed in Table II.

TABLE II
Comparison of Operation Range

Topo.	Range of PMF for each SM	Range of input voltage
*Topo.*1	$[0, n]$	$\left[U_G/(nN),\, U_{pv-\max}\right]$
*Topo.*2	$\left[0, nu_{dc}^*/U_G\right]$	$\left[u_{dc}^*/N,\, U_{pv-\max}\right]$
*Topo.*3	$\left[0, nU_{SM-\max}/U_G\right]$	$\left[U_G(\pi-2\alpha_m)/(nN\pi),\, U_{pv-\max}\right]$

TABLE III
COMPARISON OF TOPOLOGY COMPLEXITY

Components	Topology Type		
	*Topo.*1	*Topo.*2	*Topo.*3
switches	6*n*-2	6*n*	4*n*
diodes	4*n*	4*n*	5*n*
capacitors	2*n*	2*n*	3*n*
inductors	*n*-1	0	2*n*
HF transformers	*n*	*n*	*n*

TABLE IV
COMPARISON OF COMPONENT STRESS

Components	Topology Type		
	*Topo.*1	*Topo.*2	*Topo.*3
Switches^A	$u_s=U_{pv\text{-}max}$ $i_s=P_n/(n*U_{pv\text{-}mpp})$ $num=4n$	$u_s=U_{pv\text{-}max}$ $i_s=P_n/(n*U_{pv\text{-}mpp})$ $num=4n$	$u_s=\pi U_{pv\text{-}max}/(\pi\text{-}2\alpha_m)$ $i_s=P_n/(n*U_{pv\text{-}mpp})$ $num=4n$
Switches^B	$u_s=2U_G/n$ $i_s=n*P_n/(2U_G)$ $num=2n\text{-}2$	$u_s=u^*_{dc}$ $i_s=P_n/U_G$ $num=2n$	*none*
Diodes^A	*none*	*none*	$u_s=2U_{SM\text{-}max}/N$ $i_s=P_n/(n*U_{pv\text{-}mpp})$ $num=n$
Diodes^B	$u_s= N*U_{pv\text{-}max}$ $i_s=P_n/U_G$ $num=4n$	$u_s= N*U_{pv\text{-}max}$ $i_s=P_n/(n*u^*_{dc})$ $num=4n$	$u_s=\pi N*U_{pv\text{-}max}/(\pi\text{-}2\alpha_m)$ $i_s=P_n/U_G$ $num=4n$
Capacitors^A	$u_s=U_{pv\text{-}max}$ $num=n$	$u_s=U_{pv\text{-}max}$ $num=n$	$u_s=U_{SM\text{-}max}/N$ $num=2n$
Capacitors^B	$u_s=U_G/n$ $num=n$	$u_s=u^*_{dc}$ $num=n$	$u_s=U_G/n$ $num=n$
Inductors^A	*none*	*none*	$i_s= P_n/(n*U_{pv\text{-}mpp})$ $num=2n$
Inductors^B	$i_s=nP_n/(2U_G)$ $num=n\text{-}1$	*none*	*none*

Note: I. ^{A} and ^{B} denote the components on PV side and grid side, respectively
II. $u^*_{\rm dc}$, $U_{\rm SM-max}$, $U_{pv-\max}$, α_m and *N* have the same definition as Table II.

where

$u^*_{\rm dc}$ is the reference value for dc-link voltage in *Topo.*2, $u^*_{\rm dc} > U_G/n$

$U_{\rm SM-max}$ is the max. output voltage of SMs in *Topo.*3, $U_{\rm SM-max} > U_G/n$

$U_{pv-\max}$ is the maximum output voltage of PV arrays

α_m is the maximum shoot-through angle in *Topo.*3

N is the turning ratio of HF transformer.

B. Comparison of Topology Complexity and Component Stress

With the assumption of *n* SMs, the topology complexity of *Topo.*1–3 can be compared by the total number of active and passive components, which can be referred to in Table III. It should be noted that SM in *Topo.*2 is the "half-bridge chopper with full-bridge MPPT converter." [16] The component stress is also a major concern in the design of converters, which affects the sizing and cost of hardware. The voltage and current stress, u_s and i_s, for major components in *Topo.*1–3 are calculated and listed in Table IV for reference.

C. Comparison of Power Efficiency

The power losses in *Topo.*1 have been investigated in Section IV. The similar methods could be used to estimate the power losses in *Topo.*2 and *Topo.*3.

The 2-SMs converters with *Topo.*1–3 are considered as the examples for the calculation of power efficiency. For *Topo.*1, the H-bridge SMs and half-bridge PBUs are designed as Table I. For *Topo.*2, the parameters of H-bridge MPPT converters and half-bridge dc-MMC are designed with the same output voltage and rated power as *Topo.*1, according to [16]. The qZSDC SMs in *Topo.*3 are also designed with the same output voltage and rated power according to [19]. The turning ratio *N* in *Topo.*1–3, $u^*_{\rm dc}$ in *Topo.*2 , $U_{\rm SM-max}$ and α_m in *Topo.*3 are all selected with the consideration of both input voltage range and PMF range.

The relevant parameters in *Topo.*1–3 are selected as Tables III and IV. Besides, the SEMiX155GD17E4 (1700 V/150 A) and SKM450GB33F (3300 V/450 A) IGBT modules are used as active switches in *Topo.*1–3, while the SKN140F17 (1700 V/140 A) fast-recovery diodes are used as passive switches. All the HF transformers are designed with the same materials and similar geometries.

An approximate numerical calculation of power efficiency for the 2-SMs converters with *Topo.*1–3 is conducted with the assistant of MATLAB. The relationship between converter efficiency and the input power, P_{pv-1} and P_{pv-2}, are presented in Figs. 13(a)–(c), respectively.

To conclude, the proposed IIOS topology with H-bridge SMs and half-bridge PBUs has a higher steady-state efficiency (especially when the mismatched power is low) and larger operation range without increasing the general topology complexity and component stress, compared with the existing elementary topologies.

The main advantage of the proposed topology lies in.

1) The input power is converted only once in the single-stage isolated SMs. Only the mismatched power is processed by the PBUs. As a result, the power efficiency could be improved significantly under a balanced power input, which is the most common condition.
2) With the assistant of PBUs, the output voltage of SMs are decoupled from the input power on PV-ports in the steady state, which means larger operation range and enhanced capability to cope with the power-mismatch phenomenon.

VI. SIMULATION AND EXPERIMENTAL VERIFICATION

To validate the theoretical analysis, the system simulations are carried out on MATLAB–Simulink platform. Meanwhile, a down-scaled experimental prototype has also been established.

A. Simulation Analysis

A simulation model of 400 kW dc–dc converter with 6 kV MVdc output and 550–850 V PV input has been built to verify the performance of IIOS converter with PBUs. There are eight SMs and seven PBUs in the simulation model. The key parameters are selected as Table I. Simulations in the normal operation conditions and fault conditions are performed to validate the intermodule power balancing and internal fault ride-through capability of the proposed converter, respectively.

1) Normal Operation Conditions: The simulation starts from 0.05 s when the system enters a steady state. Then at $t = 0.1$ s and 0.3 s, the step-changes of irradiance are introduced to excite the intermodule power-mismatch phenomenon. During the whole simulation process, the specific irradiance values of each distributed PV array are listed in Table V for reference.

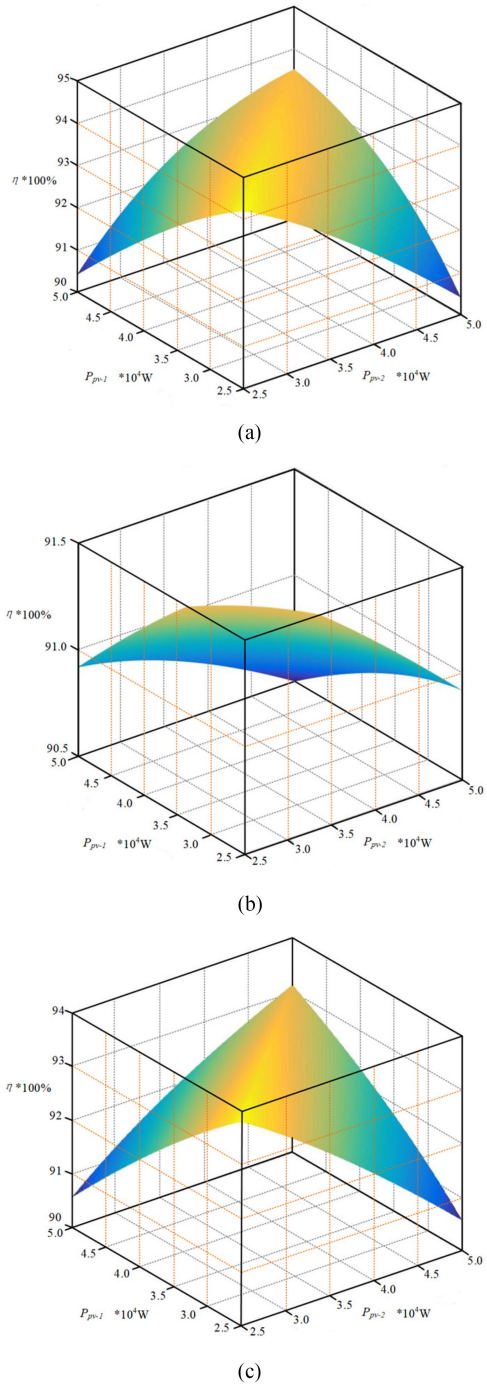

Fig. 13. Power efficiency of *Topo.*1–3 under different input power. (a) Efficiency of *Topo.*1. (b) Efficiency of *Topo.*2. (c) Efficiency of *Topo.*3.

TABLE V
CHANGES OF IRRADIANCE ON PV ARRAYS

PV Port NO.	irradiance (W/m²)		
	before 0.1s	0.1-0.3s	after 0.3s
1	1000	1000	300
2	1000	900	400
3	1000	800	500
4	1000	700	600
5	1000	600	700
6	1000	500	800
7	1000	400	900
8	1000	300	1000

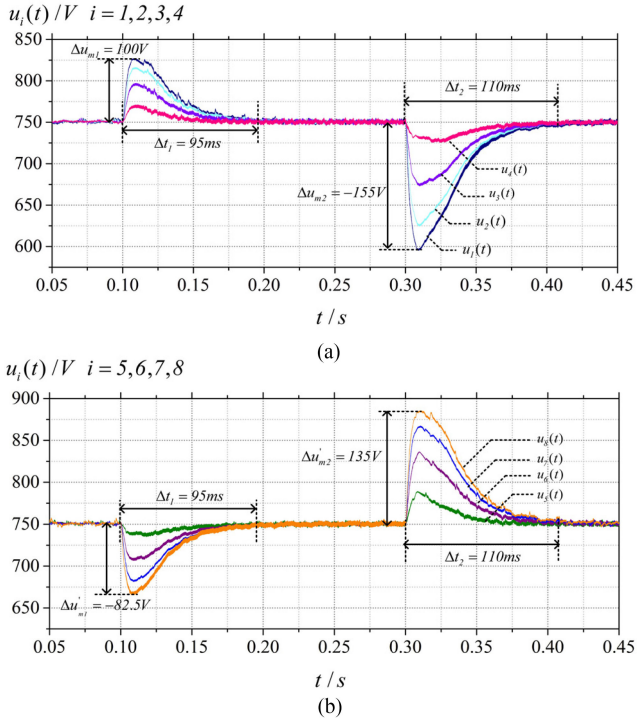

Fig. 14. Output voltages of SM#1–#8. (a) Output voltage of SM#1–#4. (b) Output Voltage of SM#5–#8.

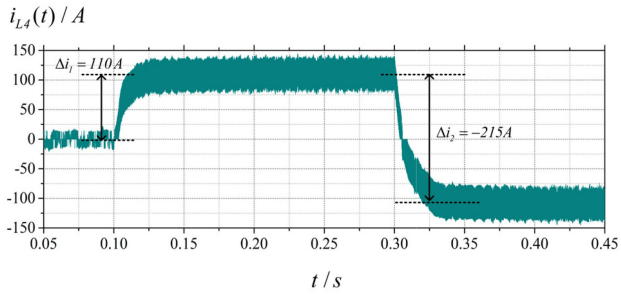

Fig. 15. Inductor current of PBU #4.

The output voltage of SM#1–#4, $(u_i i = 1\text{–}4)$ and SM#5–#8, $(u_i i = 5\text{–}8)$ during 0.05–0.45 s are presented in Fig. 14(a)–(b), respectively. The inductor currents of PBU #4, i_{L4}, during 0.05–0.45 s are presented in Fig. 15.

As shown in Fig. 14, before 0.1 s, SM#1–#8 are operated in the steady state with equal input power and equal output voltage (750 V).

At $t = 0.1$ s, the step-changes of irradiance with different amplitudes are applied to the PV arrays. With the input power exceeding the average value, SM#1–#4 have ridden through a transient over-voltage ($\Delta u_{m1} = 100$ V, $\Delta t_1 = 95$ ms) before the intermodule power mismatch is eliminated by PBUs. On the contrary, a transient under-voltage ($\Delta u'_{m1} = -82.5$ V, $\Delta t_1 = 95$ ms) has been observed on SM#5–#8. In this process, the average inductor current of PBU #4 has increased from 0 to 110 A.

TABLE VI
IRRADIANCE ON PV ARRAYS

PV Port NO.	irradiance (W/m^2)
1~4	800
5~8	900

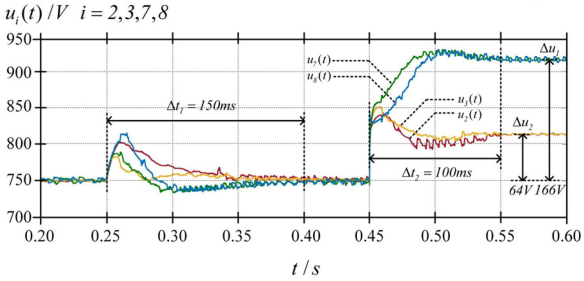

Fig. 16. Output voltages of SM#2/3/7/8.

At $t = 0.3$ s, the intermodule power-mismatch phenomena is introduced again by changing the irradiance on PV arrays. With the input power below the average value, SM#1–#4 have ridden through a transient under-voltage ($\Delta u_{m2} = -155$ V, $\Delta t_2 = 110$ ms) before the power mismatch is eliminated by PBUs. On the contrary, a transient over-voltage ($\Delta u'_{m2} = 135$ V, $\Delta t_2 = 110$ ms) has been observed on SM#5–#8. In this process, the average inductor current of PBU #4 has changed from 110 to -105 A.

The simulation results are in good agreement with the theoretical analysis.

2) Fault Conditions: The simulation starts from 0.20 s when the system enters a steady state. Then at $t = 0.25$ and 0.45 s, *FT*.1 and *FT*.2 (as the faults type defined in Section II-D) are introduced to SM#5. During the whole simulation process, the irradiance values of each distributed PV array are listed in Table VI. The output voltage of SM#2/3/7/8, (u_i $i = 2, 3, 7, 8$) during 0.20–0.60 s are selected to be presented in Fig. 16.

As shown in Fig. 16, before 0.25 s, SM#2/3/7/8 are operated in the steady state with equal output voltage (750 V) in spite of the different irradiance on corresponding PV arrays.

At $t = 0.25$ s, *FT*.1 occurs on SM#5 and the relevant protective control strategy is activated. With the output power of SM#5 dropped to zero, SM#2/3/7/8 have ridden through a transient over-voltage ($\Delta t_1 = 150$ ms) before the mismatched power is eliminated by PBUs.

At $t = 0.45$ s, *FT*.2 occurs on SM#5. With the relevant protective control activated, PBU#4 and 5 are cutoff from the converter system together with SM#5. With only seven SMs, the output voltage of all remaining SMs will increase from 750 V. After a transient process ($\Delta t_2 = 100$ ms), the equivalent output power of SM#1–4 and SM#6 and 7 are locally balanced. With a relatively higher input power, the output voltage of SM#7 and 8 (u_7 and u_8) increase to 916 V ($\Delta u_1 = 166$ V), while the output voltage of SM#2 and 3 (u_2 and u_3) increase to 814 V ($\Delta u_2 = 64$ V) with a relatively lower input power.

The simulation results are in good agreement with the theoretical analysis.

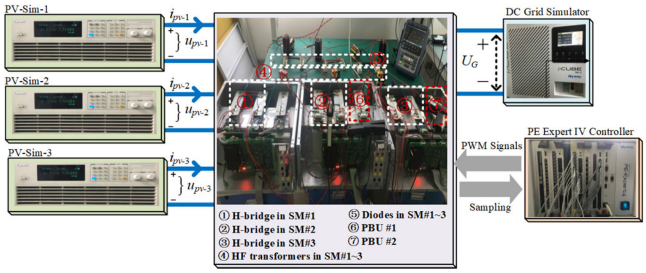

Fig. 17. Experimental setup of 3-SMs IIOS converter with 2 PBUs.

TABLE VII
DOWN-SCALED EXPERIMENT UNDER THE STEADY-STATE CONDITION

Parameters	Values
Number of SMs ***n***	*3*
Number of PBUs ***n*-1**	*2*
PBU Inductance L_1 & L_2	*1.5 mH*
SM output capacitance $C_{o\text{-}1}$ & $C_{o\text{-}2}$ & $C_{o\text{-}3}$	*3000 uF*
SM input capacitance $C_{in\text{-}1}$ & $C_{in\text{-}2}$ & $C_{in\text{-}3}$	*3000 uF*
SM & PBU Switching frequency f_s	*10 kHz*
Grid voltage U_G	*120 V*
Rated output voltage of SMs U_{ns}	*40 V*
Input MPP voltage $U_{pv\text{-}mpp}$	*30 V*
Input power $P_{pv\text{-}1}$	*180 W*
Input power $P_{pv\text{-}2}$	*120 W to 240 W*
Input power $P_{pv\text{-}3}$	*180 W*
Switching devices	*SKM75GB063D(600 V/75 A)*

B. Experimental Validation

For further validation of theoretical analysis results, the proposed topology and control strategies have been tested on a down-scaled experimental setup, which is composed of four programmable dc power supplies and one IIOS converter that containing three H-bridge SMs and two PBUs, as shown in Fig. 17.

Three *Chroma 62150H* dc power supplies are operated in their controlled-current-source mode to serve as PV simulators, while the *Myway pCube* is operated in its constant voltage mode with bidirectional power flow to simulate the dc grid. Each of the specially designed converter modules consists of three independent half-bridge arms, two of which compose an H-bridge, while the third arm is used as PBU. HF transformers with turning ratio $N = 2$ are used for voltage step-up and isolation. The parameters and conditions in experiment are summarized as Table VII.

During the experiment, the input power P_{pv-1} and P_{pv-3} are kept at 180 W while P_{pv-2} go through a step change from 120 to 240 W. In this process, the related waveforms are recorded as Figs. 18–21, respectively.

As shown in Fig. 18, with the input power of SM#2, P_{pv-2}, stepping up from 120 to 240 W, the input current of SM#2, i_{pv-2} increases from 4 to 8 A. During this procedure, the output voltage of SM#1–3 (u_1, u_2, u_3) are kept around the rated value $U_{\rm ns} = 40$ V without significant deviation.

In Fig. 19, the inductor currents of PBU#1 and #2, i_{L1} and i_{L2} are presented along with i_{pv-2}. In the initial state ($P_{pv-1} = 180$ W, $P_{pv-2} = 120$ W, $P_{pv-3} = 180$ W), the average currents in L_1 and L_2, I_{L1} and I_{L2} are 0.875 and -0.875 A, which means that the power transferred by PBU#1 and #2 are

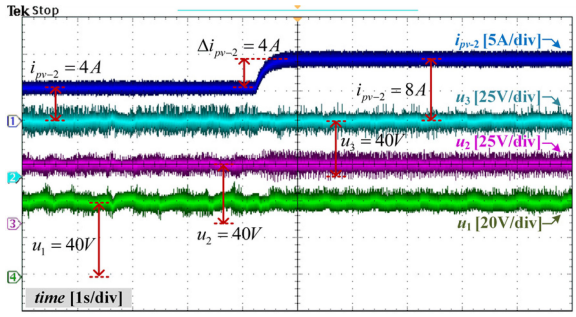

Fig. 18. Output voltage of SM#1–3 and input current of SM#2.

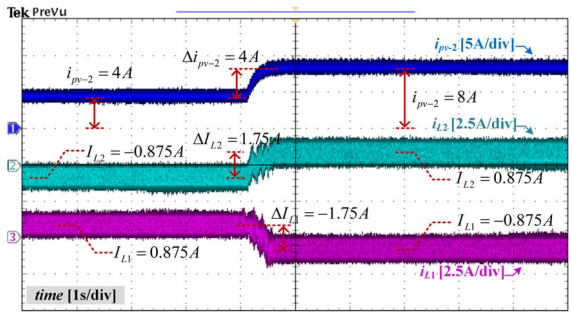

Fig. 19. Inductor current of PBU#1–2 and input current of SM#2.

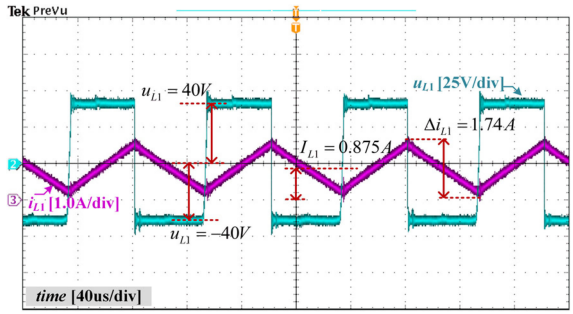

Fig. 20. Zoomed-in waveforms of steady-state inductor current and voltage in PBU#1.

17.5 and −17.5 W, respectively. After P_{pv-2} steps up from 120 to 240 W, which means the average value of i_{pv-2} (I_{pv-2}) increases from 4 to 8A, a new steady state is achieved with $I_{L1} = -0.875$ A and $I_{L2} = 0.875$ A, in which the power transferred by PBU#1 and #2 are −17.5 and 17.5 W, respectively. Considering the power losses, we can see that the steady-state equivalent output power of SM#1–3 are kept balanced.

The zoomed-in waveforms of steady-state inductor current i_{L1} and inductor voltage u_{L1} in PBU#1 are shown in Fig. 20. It could be seen that the waveform of u_{L1} is symmetrical square wave with a duty ratio of 0.5 and 80 V peak-to-peak value. For i_{L1}, the average value $I_{L1} = 0.875$ A while the peak-to-peak value $\Delta i_{L1} = 1.74$ A.

In Fig. 21, the input voltage u_{pv-1} and output voltage u_1 of SM#1 are presented, respectively. It could be seen that u_{pv-1} is kept at 30 V $(U_{pv\text{-}mpp})$ with the regulation of SM#1 while u_1 is kept at 40 V $(U_{\rm ns})$ with the assistant of PBUs. Besides, the primary side transformer voltage u_{t1} is also presented.

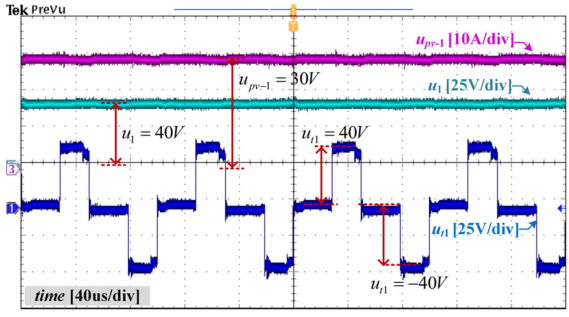

Fig. 21. Input, output, and primary side transformer voltage in SM#1.

To summarize, all the experimental results are in good agreement with the theoretical analysis.

VII. Conclusion

In this paper, a novel topology of IIOS-connected-modular dc–dc converter that consists of isolated SMs and intermodule PBUs is proposed. The working principles in both normal and fault conditions are investigated. The major passive components could be designed according to the boundary operation conditions. A comparative study has been conducted based on the quantitative and qualitative analysis of operation range, topology complexity, component stress and steady-state power efficiency. It has been verified that the proposed topology has several advantages to serve as the interface for multiport MVdc integration of distributed PV, which could be summarized as follows.

1) Strong capability to cope with power mismatch.
2) High power efficiency.
3) High voltage conversion ratio for MVdc applications.

Through system simulation and down-scaled experiments, the performance of the proposed topology and control strategies are tested in various conditions for validation.

The proposed topology has a potential industrial application value in the scenario of future MVdc distribution system with high-penetration distributed PV. As for the next step of research, the small-signal modeling and stability analysis of IIOS converter with PBUs would be considered. Moreover, other possible topologies for the energy transfer circuits in PBUs would be explored for higher voltage and power-level applications in HVdc system.

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