Impedance-Oriented Transient Instability Modeling of SiC MOSFET Intruded by Measurement Probes

Zheng Zeng, *Member, IEEE*, Xin Zhang, *Member, IEEE*, Frede Blaabjerg, *Fellow, IEEE*, and Linjing Miao

***Abstract*—Due to the breakneck switching speed, SiC MOSFET is extremely sensitive to parasitics in the power device, circuit layout, and also measurement probe. It is not clear how the parasitics of measurement probes affect the transient stability of SiC MOSFET, and it poses an unsolved challenge for the industrial field. This paper focuses to uncover the transient instability mechanism of SiC MOSFET intruded by probes. Mathematical and circuit models of voltage and current probes are created, by considering the parasitics, input impedance, and bandwidth issues. To reveal the stability principles of SiC MOSFET associated with probes, impedance-oriented and heterogeneity-synthesized models combining device with probes are proposed. Furthermore, an assessment methodology and root locus analysis are presented to demonstrate the transient stability schemes and the stable boundaries of SiC MOSFET influenced by multiple factors, including probe parasitics, device parameters, gate resistances, and snubber circuits. Comparative experiments are presented to confirm the transient behaviors of SiC MOSFET intruded by probe parasitics and regulated by control circuits. It is proven that, because of low bandwidth specifications, the large input capacitance of the voltage probe and coil inductance of the current probe degrade the transient stability of SiC MOSFET. Due to the deteriorated stability margin of SiC MOSFET intruded by the inserted parasitics of probes, instability may also be activated by using the small gate resistance. The snubber circuit is helpful to enhance the transient stability. Advanced probes with high bandwidth and high impedance are crucially needed for stable measurement of wide bandgap power devices like SiC MOSFET.**

***Index Terms*—Impedance modeling, measurement probes, SiC MOSFET, transient instability.**

I. Introduction

BENEFITTING from the high electron velocity, wide bandgap, and strengthened breakdown field, silicon carbide is an advanced power semiconductor material for next-generation power electronic devices [1], [2]. Due to the high-frequency, high-temperature, and high-voltage capabilities, SiC MOSFETs are growingly concerned and implemented in the industrial fields, like electrified transportation, renewable energy, and also the utility [3], [4]. Compared with Si counterparts, due to the smaller chip size and junction capacitances, SiC MOSFET performs faster switching speed, as well as shows higher di/dt and dv/dt [5], [6]. As a result, SiC MOSFET is much more sensitive to parasitics than Si counterparts. Due to the bonding wires of the device package, power traces of the circuit layouts, and detection circuits of the measurement probes [7], inevitable parasitics lead to switching ringing and overshooting. These issues degrade the transient stability of SiC MOSFET and even damage the device [8], [9]. Therefore, transient stability deteriorated by multiscale parasitics poses unsolved challenges for the safe operation of SiC MOSFET.

Recently, some researches attempted to address the parasitic-dependent stability of SiC MOSFET influenced by parasitics in device, circuit, and probe levels. In the device level, direct through of phase leg caused by Miller capacitance of SiC MOSFET is modeled, tested, confirmed, and suppressed in [10]–[12]. Taking the parasitic inductances of the package into account, by using the classical transfer function theorem, detailed mathematical models are proposed to characterize the switching ringing of SiC MOSFET [13], [14]. Snubber capacitor is integrated into the power module package to suppress the influence of parasitics [15], [16]. Thanks to the canceled magnetic field and shortened power loop in SiC device, advanced package concepts are proposed to minimize the parasitics by using creative planar package, 3D stacked package, flex thin-film package, etc. [17], [18]. In the circuit level, the parasitics in the gate loop have been considered in [19]–[22], and the instability of SiC MOSFET is modeled by Nyquist theorem. By using the state-space approach, the small-signal model is proposed to analyze the transient stability of SiC MOSFET considering the parasitic inductances of the printed circuit board (PCB) layout. The Lyapunov energy function is defined as a criterion to justify stability [23]. Multiple degrees of freedom of the gate driver are demonstrated to immunize the transient instability of SiC MOSFET caused by circuit parasitics [24]. By using adjustable gate voltage, gate current, or gate resistance, the ingenious active gate drivers are proposed to enhance the transient stability and reduce the switching loss of SiC MOSFET [25]–[27]. In the probe level, the propagation delay of the probes is modeled and confirmed in [28], focusing on the high-frequency transient measurement of semiconductor

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devices. Due to the very short switching time, it is proven that propagation delay caused by the parasitics of probes profoundly challenges the accurate measurement of the switching loss [29]. Besides, targeting at high-precise measurement, some current probes with different bandwidths are compared in [30]. By using novel structures and optimized designs, some innovative probes with smaller parasitics and higher bandwidth are proposed [31]–[35]. With respect to the parasitics caused by measurement, some general methodologies are proposed for the high-speed and high-precise measurement of SiC device [36]–[39].

The transient behavior of SiC MOSFET is affected by the parasitics of power devices, layout circuits, and measurement probes. The impedance of the power device is capacitive. Interacting with the inductive parasitics of package, circuit, and probes, the transient instability of SiC MOSFET may be activated by complex LC resonances. The parasitics of probes not only amplify the measurement error but also intrude the transient stability of SiC MOSFET, which interferes in the safe operation of the SiC device. Field experience shows that the SiC device may be unstable and even damaged if the probes are not properly utilized. However, parasitics introduced by the measurement probes are usually ignored in the industrial field. The ON–OFF trajectories of SiC MOSFET intruded by probes are also neglected. In the test bench, the mathematical or circuit models of probes considering parasitics are not highlighted. The parasitic-dependent input impedance and bandwidth of probes are not addressed either. How probes intrude the power loop and influence the transient stability of SiC MOSFET is also poorly understood. Mathematical modeling and mechanism analyzing are crucially needed to illustrate the emerging instability issues of the SiC devices.

This paper focuses to reveal the transient instability mechanism of SiC MOSFET intruded by measurement instruments, from the perspective of impedance; general mathematical models of measurement probes and probe–device interaction are proposed, analyzed, and confirmed by experiments. The rest of this paper is organized as follows. In Section II, the instability of SiC MOSFET caused by measurement is described. In Section III, considering the parasitics, mathematical and circuit models are created to characterize the impedance and response principles of probes. In Section IV, in terms of the impedance, the general model is proposed to reveal the stability mechanism of SiC MOSFET intruded by probes. In Section V, by using root locus analysis, a case study is presented to show the stability schemes of device–probe coupling system influenced by multiple factors, including probe parasitics, device parameters, gate resistances, and snubber circuits. In Section VI, experimental results are presented to demonstrate the proposed models and analyses. Finally, Section VII summarizes the paper.

II. Measurement Inaccuracy and Transient Instability of SiC Mosfet Influenced by Probes

A. Test Bench for Transient Measurement of SiC MOSFET

To understand the transient behavior of SiC MOSFET affected by probes, an inductor-clamped double pulse test bench is employed, as shown in Fig. 1. Variables in Fig. 1 are listed in Table I. S_1 and S_2 are SiC MOSFET devices under test (DUT).

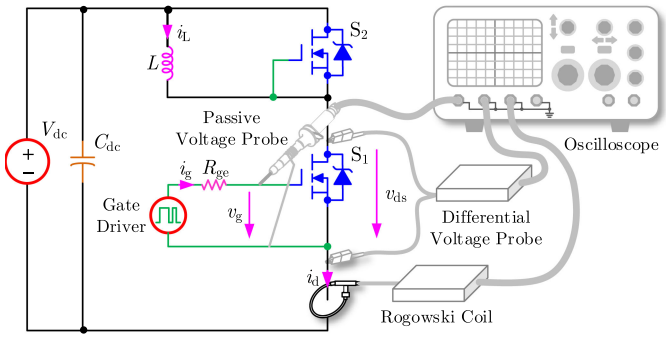

Fig. 1. Schematic of SiC device under test associated with measurement probes.

TABLE I
VARIABLES IN A DOUBLE PULSE TEST BENCH SHOWN IN FIG. 1

Variables	Descriptions	Variables	Descriptions
V_{dc}	DC-link voltage	R_{ge}	External gate resistance
C_{dc}	DC-link capacitance	v_g	Output voltage of gate driver
L	Load inductor	v_{ds}	Drain-source voltage
i_L	Load current	i_d	Drain current
S_1, S_2	Devices under test	i_g	Gate current

TABLE II
TYPICAL PROBES IN TEST BENCH

Instrument	Peak Value	Bandwidth (MHz)	Rise Time (ns)	Measurement	Image
HIPV probe	400 V	100 – 500	0.7 – 2.35	v_{gs}	
DV probe	1.5 kV	70 – 200	1.75 – 5	v_{ds}	
Rogowski coil	60 A	10 – 200	2 – 7	i_d	

In Fig. 1, some measurement probes are implemented, as summarized in Table II. A high-impedance passive voltage (HIPV) probe is used to measure voltage v_g of S_1, while a differential voltage (DV) probe is used to observe the drain–source voltage v_{ds}. A Rogowski coil is utilized to capture the drain current i_d. These probes are individually connected to the analog channels of the digital oscilloscope by cables. Input channels of the oscilloscope are commonly grounded.

B. State-of-the-Art of Voltage and Current Probes

According to the commercialized products of leading companies like Tektronix [40], Keysight [41], Lecroy [42], and Cal Test [43], the state-of-the-art of HIPV probes is surveyed, as shown in Fig. 2. It is found that the input capacitance of the HIPV probe decreases with the bandwidth. The input capacitance of HIPV probe arranges from several pF to several hundred pF within bandwidth 15 MHz to 1.5 GHz. The bandwidth-dependent input capacitance can be modeled as

$$\lg C_{in} = k_c \lg f_c + C_{in0} \tag{1}$$

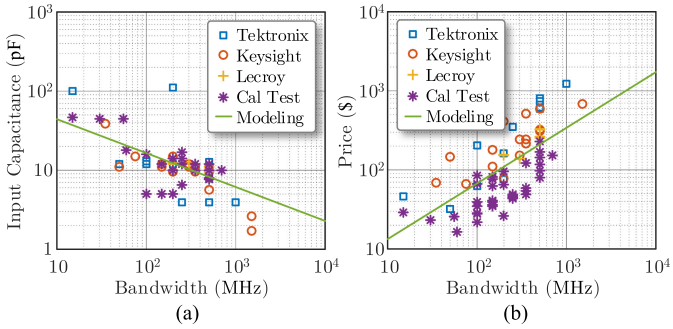

Fig. 2. The surveyed high-impedance passive voltage probes. (a) Input capacitance versus bandwidth. (b) Price versus bandwidth.

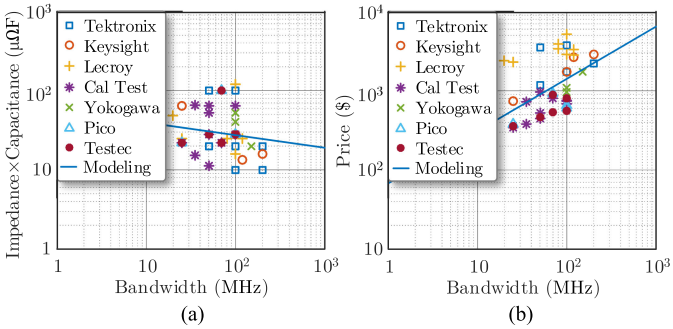

Fig. 3. The surveyed differential voltage probes. (a) Input impedance versus bandwidth. (b) Price versus bandwidth.

where $C_{\rm in}$ and $f_{\rm c}$ are the input capacitance and bandwidth of the probe. $k_{\rm c}$ and C_{in0} are capacitance coefficient and fundamental capacitance of the HIPV probe, respectively. According to (1) and the samples in Fig. 2(a), the constants $k_{\rm c}$ and C_{in0} are estimated as $k_{\rm c} = -0.43$ and $C_{in0} = 2.07$.

As indicated in Fig. 2(b), the price of HIPV probe increases with the bandwidth. The bandwidth-dependent price can be written as

$$\lg p_{\rm HIPV} = k_{\rm p,HIPV} \lg f_{\rm c} + p_{0,\rm HIPV} \tag{2}$$

where $p_{\rm HIPV}$ is the price of the HIPV probe. $k_{\rm p,HIPV}$ and $p_{0,HIPV}$ are the price coefficient and fundamental price of the HIPV probe. According to (2) and the samples in Fig. 2(b), the constants can be identified as $k_{\rm p,HIPV} = 0.7$ and $p_{0,HIPV} = 0.42$.

Similarly, the available DV probes from Tektronix [44], Keysight [45], Lecroy [46], Cal Test [47], Yokogawa [48], Pico [49], and Testec [50] are surveyed, as shown in Fig. 3. As seen, the input impedance of the DV probe decreases with the bandwidth; whereas its price increases with the bandwidth.

As shown in Fig. 3(a), it can be seen that the complex impedance index (input impedance multiplying input capacitance) decreases with the bandwidth of the DV probe. The input impedance performance of the DV probe can be modeled as

$$\lg Z_{\rm in} = k_{\rm Z} \lg f_{\rm c} + Z_{\rm in0} \tag{3}$$

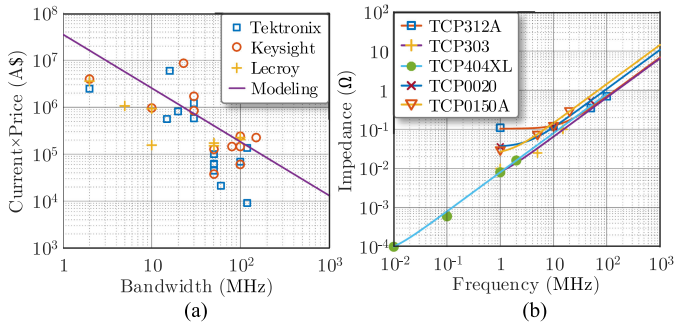

Fig. 4. The surveyed current probes. (a) Current rating versus bandwidth. (b) Impedance versus bandwidth of current probe from Tektronix.

where $Z_{\rm in}$ is the complex impedance index of the DV probe. $k_{\rm z}$ and $Z_{\rm in0}$ are the impedance coefficient and fundamental complex impedance index, respectively. According to (3) and the samples in Fig. 3(a), the coefficients in (3) can be estimated as $k_{\rm Z} = -0.16$ and $Z_{\rm in0} = 1.76$.

Similarly, the price of the DV probe is also dependent on its bandwidth, as presented in Fig. 3(b). As seen, the price of the DV probe increases with the bandwidth. The price-bandwidth principle of the DV probe can be modeled as

$$\lg p_{\rm DV} = k_{\rm p,DV} \lg f_{\rm c} + p_{0,\rm DV} \tag{4}$$

where $p_{\rm DV}$ is the price of the DV probe. $k_{\rm p,DV}$ and $p_{0,\rm DV}$ are the price coefficient and fundamental price of the DV probe. According to the samples in Fig. 3(b), the constants in (4) are identified as $k_{\rm p,DV} = 0.66$ and $p_{0,\rm DV} = 1.83$.

Concerning the current probe, the state-of-the-art of current probes from Tektronix [51], Keysight [52], and Lecroy [53] are overviewed in Fig. 4(a). As seen, there is a tradeoff to concurrently pursue high-bandwidth and high-capacity current probe. The statistical principle of the current probe can be modeled as

$$\lg(I_{\rm n} p_{\rm RC}) = k_{\rm pn} \lg f_{\rm c} + p_{\rm pn} \tag{5}$$

where $I_{\rm n}$ and $p_{\rm RC}$ are the current rating and price of the current probe, respectively. $k_{\rm pn}$ and $p_{\rm pn}$ are coefficients. According to (5) and the samples in Fig. 4(a), the coefficients can be estimated as $k_{\rm pn} = -1.14$ and $p_{\rm pn} = 7.6$.

Few producers provide the impedance information of the current probe. The impedance of the current probe from Tecktronix is shown in Fig. 4(b). The inserted impedance of the current probe can be expressed as

$$Z_{\rm RC} = \sqrt{(2\pi f L_{\rm RC})^2 + R_{\rm RC}^2} \tag{6}$$

where $L_{\rm RC}$ and $R_{\rm RC}$ are the inserted inductance and resistance of the current probe. According to (6) and the samples in Fig. 4(b), the parasitics of the probes can be estimated. In Fig. 4(b), the marker points are the samples from Tektronix, and the solid lines are the fitting data according to the model in (6).

In summary, according to the state-of-the-art of probes, the specifications of probes highly depend on the bandwidth. A high-level probe having wide bandwidth also means expensive. Low-cost probe usually induces large parasitics into the tested bench.

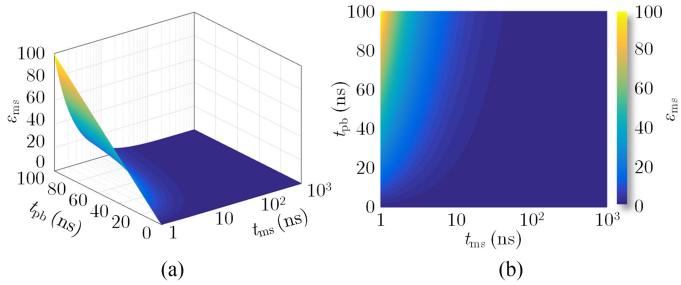

Fig. 5. Calculated rise time of measured signal influenced by measurement probes. (a) 3D distribution of relative deviation and (b) its 2D map.

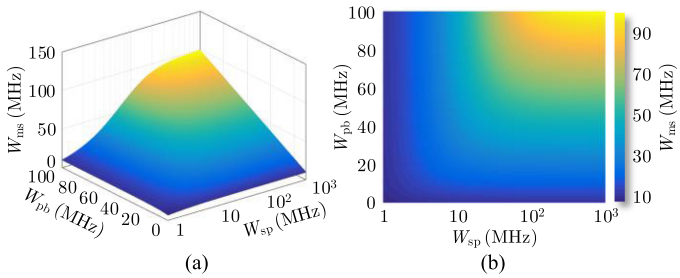

Fig. 6. Calculated bandwidth of measured signal influenced by measurement probes. (a) 3D distribution of measurement bandwidth and (b) its 2D map.

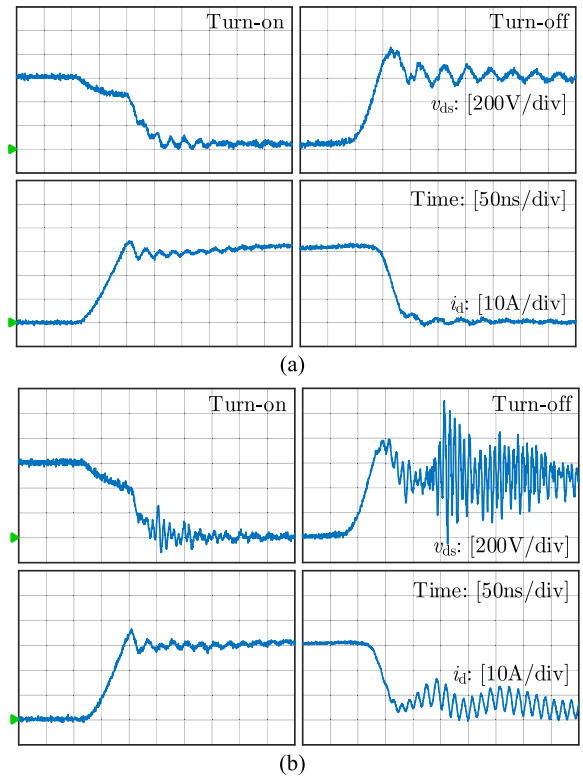

Fig. 7. Experimental results of SiC MOSFET transient trajectories. (a) Stable mode in condition of high-bandwidth HIPV probe and short ground lead. (b) Unstable mode activated by low-bandwidth HIPV probe and long ground lead.

C. Measurement Accuracy of SiC MOSFET Degraded by Probes

The probes influence the accurate measurement of SiC MOSFET's ON–OFF trajectories. It can be summarized as

$$\begin{cases} t_{\mathrm{r}} = \sqrt{t_{\mathrm{ms}}^2 + t_{\mathrm{pb}}^2 + t_{\mathrm{sp}}^2} \\ t_{\mathrm{r}} \cong \frac{0.35}{W_{\mathrm{ms}}} \\ W_{\mathrm{ms}} = \frac{W_{\mathrm{pb}} W_{\mathrm{sp}}}{\sqrt{W_{\mathrm{pb}}^2 + W_{\mathrm{sp}}^2}} \\ t_{\mathrm{d}} = t_{\mathrm{dpb}} + t_{\mathrm{dsp}} \end{cases} \tag{7}$$

where t_{r}, t_{ms}, t_{pb}, and t_{sp} are the rise time of the observed signal, the original signal under test, the probe, and the oscilloscope, respectively. W_{ms}, W_{pb}, and W_{sp} are the bandwidths of the measurement path, the probe, and the oscilloscope, respectively. t_{d}, t_{dpb}, and t_{dsp} are the propagation delay of the measurement path, the probe, and the oscilloscope, respectively [54]–[56]. It can be seen that the probes slow down the test signal, reduce the channel bandwidth, and introduce the propagation delay.

According to (7), Fig. 5 illustrates the rise time of the measured signal affected by the probe. The relative deviation ε_{t} is defined as $\varepsilon_{\mathrm{ms}} = (t_{\mathrm{r}} - t_{\mathrm{ms}})/t_{\mathrm{ms}}$. When the rise time of the signal under test decreases, the rise time of the probe should be correspondingly minimized to ensure an accurate measurement.

According to (7), Fig. 6 depicts the bandwidth of the measured signal affected by the probe. Generally, the bandwidth of the probe is narrower than that of the oscilloscope. The bandwidth of the measured signal is mainly limited by the bandwidth of the probe. Generally, the bandwidth of the probes should be more than five times of the bandwidth of signal under test to guarantee accurate measurement.

D. Transient Stability of SiC MOSFET Intruded by Probes

Except for the measurement accuracy, the probes also influence the transient stability of SiC MOSFET. According to the double-pulse test bench in Fig. 1, the experimental results in stable and unstable modes are shown in Fig. 7(a) and (b), respectively. By using a low bandwidth HIPV probe and a long ground lead, the activated unstable switching ringing damages the SiC MOSFET, as depicted in Fig. 7(b).

It is observed that the probes may introduce extra parasitics and reshape the impedance of the test circuit. The parasitics intruded by improper probes may change the transient trajectories of SiC devices, which causes severe instability and even damage the device.

E. Technique Bottlenecks of Transient Instability of SiC MOSFET Intruded by Probes

To obtain an insightful understanding of the stability mechanism of SiC MOSFET intruded by probes, some issues should be addressed.

1) Issue 1: How to create mathematical and circuit models of probes considering the parasitics, impedance, and bandwidth issues.

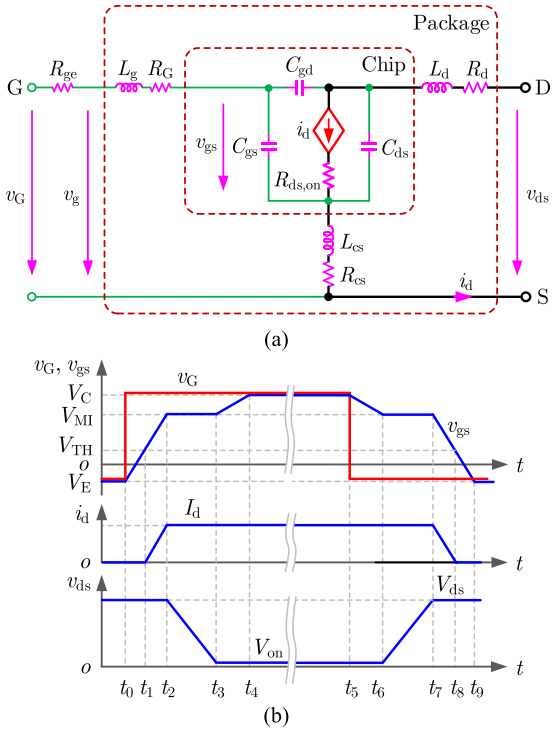

Fig. 8. Schematic diagram of SiC MOSFET. (a) Impedance model. (b) Switching trajectory.

2) Issue 2: How to model the mechanism of device–probe interaction and reveal its stability principles concerning the influences of multiple factors.

III. Impedance-Oriented Modeling of SiC MOSFET and Measurement Probes

Based on the test bench in Fig. 1 and focusing on the issue 1 in Section II, the mathematical and circuit models of SiC MOSFET, HIPV probe, DV probe, and current probe are created in this Section. Also, concerning the stability and accuracy of the measurements, the impedance and bandwidth of the probes are addressed.

A. Impedance Modeling of SiC MOSFET

The SiC MOSFET can be modeled as a voltage-controlled current source, as shown in Fig. 8(a). Switching trajectory of SiC MOSFET is illustrated in Fig. 8(b). Variables of the tested SiC MOSFET in Fig. 8 are listed in Table III.

The drain current of SiC MOSFET can be expressed as

$$i_d = \begin{cases} 0 & 0 \le v_{gs} < V_{TH} \\ g_{\rm m}(v_{gs} - V_{TH}) & V_{TH} \le v_{gs} \le V_{\rm MI} \end{cases} \tag{8}$$

where $V_{\rm TH}$ is the threshold voltage. $g_{\rm m}$ is the transconductance. $V_{\rm MI}$ is the Miller plateau voltage [21], [57]. The gate–source voltage $v_{\rm gs}$ can be expressed as

$$v_{gs} = \begin{cases} G_{gs}(s)v_G, & \text{if } v_{gs} < V_{\rm MI} \text{ or } v_{\rm ds} \ge V_{\rm on} \\ V_{\rm MI}, & \text{else} \end{cases} \tag{9}$$

TABLE III
Variables of Tested SiC MOSFET in Fig. 5

Variables	Descriptions
$L_{\rm g}$	Parasitic inductance of gate loop
$R_{\rm G}$ and $R_{\rm ge}$	Inner and external gate resistance
$L_{\rm d}$ and $R_{\rm d}$	Parasitic inductance and resistance of drain terminal
$L_{\rm cs}$ and $R_{\rm cs}$	Common source parasitic inductance and resistance
$C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm ds}$	Gate-source, gate-drain, and drain-source capacitances
$R_{\rm ds,on}$	On-resistance
$v_{\rm gs}$	Voltage on $C_{\rm gs}$
$v_{\rm G}$	Gate voltage provided by the gate driver
$V_{\rm C}$ and $V_{\rm E}$	Maximum and minimum voltages of $v_{\rm G}$

TABLE IV
Typical Parameters of SiC MOSFET Device

Variables	$V_{\rm th}$	$g_{\rm m}$	$C_{\rm gs}$	$L_{\rm d}$	$L_{\rm g}$	$L_{\rm cs}$	$R_{\rm ge}$	$R_{\rm G}$	$V_{\rm C}/V_{\rm E}$
Values	2.6 V	8.1 S	950 pF	5.9 nH	9.2 nH	7.5 nH	5 Ω	4.6 Ω	20/−5 V

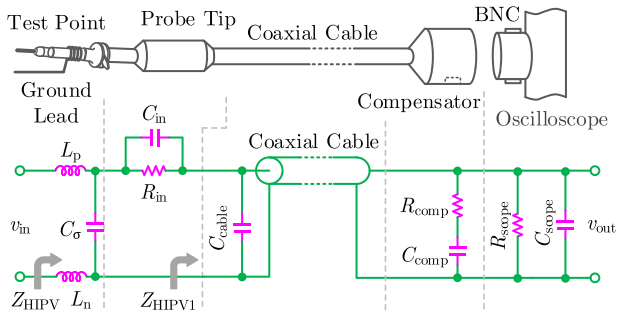

Fig. 9. Schematic diagram of HIPV probe.

where $V_{\rm on} = R_{\rm ds,on} I_{\rm d}$ is the ON-state voltage of $v_{\rm ds}$. $I_{\rm d}$ is the load current in steady state. According to Fig. 8, the transfer function model $G_{\rm gs}(s)$ from $v_{\rm G}$ to $v_{\rm gs}$ can be expressed as

$$G_{gs}(s) = \frac{1}{(L_{\rm g} + L_{\rm cs})C_{\rm gs}s^2 + (R_{\rm ge} + R_{\rm G} + R_{\rm cs})C_{\rm gs}s + 1}. \tag{10}$$

Taking the SiC MOSFET C2M0080120D from Wolfspeed/Cree as an example, the parameters from its datasheet are given in Table IV [58]. The parasitic resistances $R_{\rm d}$ and $R_{\rm cs}$ are small enough to be ignored.

B. Impedance Modeling of High-Impedance Voltage Probe (HIPV)

The HIPV probe is usually used to measure $v_{\rm gs}$, and its maximum input voltage is generally limited to 400 V. The commonly used HIPV probe can be generally modeled by the circuit, as illustrated in Fig. 9.

In Fig. 9, $L_{\rm p}$ and $L_{\rm n}$ are parasitic inductances of the test point and ground lead. C_σ is the parasitic capacitance of the ground lead. $R_{\rm in}$ and $C_{\rm in}$ are the input resistance and capacitance of the probe. $C_{\rm cable}$ is parasitic capacitance of the coaxial cable. $R_{\rm comp}$ and $C_{\rm comp}$ are resistance and capacitance of compensator which is used to correct the impedance of the probe and avoid

TABLE V
PARAMETERS OF HIPV PROBE PP026 AND OSCILLOSCOPE 715ZI

	Ground Lead		Probe Tip		Cable	Compensator		Oscilloscope	
Variables	$L_{\rm p}$	$L_{\rm n}$	$R_{\rm in}$	$C_{\rm in}$	$C_{\rm cable}$	$R_{\rm comp}$	$C_{\rm comp}$	$R_{\rm scope}$	$C_{\rm scope}$
Values	10 nH	10 nH	9 MΩ	10 pF	120 pF	500 Ω	20 pF	1 MΩ	16 pF

the distortion of the measurement. $R_{\rm scope}$ and $C_{\rm scope}$ are input resistance and capacitance of the digital oscilloscope.

According to Fig. 9, the total equivalent impedance of the cable, compensator, and oscilloscope can be derived as

$$Z_{\rm HIPV1} = \frac{1}{sC_{\rm cable} + \frac{sC_{\rm comp}}{sC_{\rm comp}R_{\rm comp}+1} + \frac{1}{R_{\rm scope}} + sC_{\rm scope}} = \frac{b_1 s + b_0}{a_2 s^2 + a_1 s + 1} \tag{11}$$

where

$$\begin{cases} a_2 = R_{\rm scope}R_{\rm comp}(C_{\rm cable} + C_{\rm scope})C_{\rm comp} \\ a_1 = R_{\rm scope}(C_{\rm cable} + C_{\rm comp} + C_{\rm scope}) + R_{\rm comp}C_{\rm comp} \\ b_1 = R_{\rm scope}R_{\rm comp}C_{\rm comp} \\ b_0 = R_{\rm scope}. \end{cases} \tag{12}$$

The input impedance of the HIPV probe can be written as

$$Z_{\rm HIPV2} = (L_{\rm p} + L_{\rm n})s + \frac{\left(\frac{R_{\rm in}}{R_{\rm in}C_{\rm in}s+1} + Z_{\rm HIPV1}\right)\frac{1}{C_\sigma s}}{\frac{R_{\rm in}}{R_{\rm in}C_{\rm in}s+1} + Z_{\rm HIPV1} + \frac{1}{C_\sigma s}}. \tag{13}$$

Ignoring the very small parasitics of the cable, compensator, and oscilloscope, (13) can be simplified to

$$Z_{\rm HIPV} = (L_{\rm p} + L_{\rm n})s + \frac{R_{\rm in} + R_{\rm scope}}{(R_{\rm in} + R_{\rm scope})C_{\rm in}s + 1}. \tag{14}$$

The transfer function from the test voltage $v_{\rm in}$ to the measured voltage $v_{\rm out}$ can be derived as

$$G_{\rm HIPV}(s) = \frac{v_{\rm out}}{v_{\rm in}} = \frac{Z_{\rm HIPV1}}{Z_{\rm HIPV2}}. \tag{15}$$

According to the datasheets of utilized HIPV probe PP026 and oscilloscope 715Zi from Lecroy [59], [60], the parameters of models in (11)–(15) are listed in Table V.

The parasitics of ground lead can be estimated by using the long wire model, which can be expressed as [39], [61]

$$\begin{cases} L_\sigma[\rm nH] = 0.127l\left[\ln\frac{4l}{d} - 1\right] \\ C_\sigma[\rm mF] = \frac{2\pi\varepsilon l}{\Lambda}\left\{1 + \frac{1}{\Lambda}(1 - \ln 2) + \frac{1}{\Lambda^2}\left[1 + (1 - \ln 2)^2 - \frac{\pi^2}{12}\right]\right\} \end{cases} \tag{16}$$

where parasitic inductance L_σ is $L_{\rm p}$ or $L_{\rm n}$. l and d, in mm, are the length and diameter of the ground lead wire. Coefficient Λ is defined as $\Lambda = \ln(l/d)$. By using a shortened ground lead with $l = 35$ mm and $d = 1.2$ mm, the parasitics of ground lead can be calculated as $L_\sigma = 10$ nH and $C_\sigma = 0.8$ pF. The C_σ is small enough to be ignored.

The values of $R_{\rm in}$, $C_{\rm in}$, $R_{\rm comp}$, and $C_{\rm comp}$ can be observed from the datasheet of the probe. Concerning the coaxial cable,

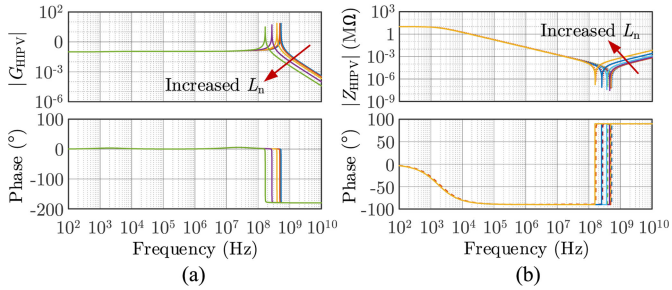

Fig. 10. Calculated characteristics of HIPV probe affected by $L_{\rm n}$ from 1 to 100 nH. (a) Transfer function $G_{\rm HIPV}$ and (b) input impedance $Z_{\rm HIPV}$ (solid line: full-order model $Z_{\rm HIPV2}$; dotted line: reduced-order model $Z_{\rm HIPV}$).

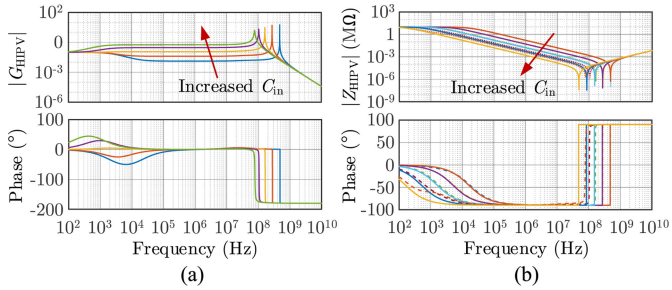

Fig. 11. Calculated characteristics of HIPV probe affected by $C_{\rm in}$ from 1 to 100 pF. (a) Transfer function $G_{\rm HIPV}$ and (b) input impedance $Z_{\rm HIPV}$ (solid line: full-order model $Z_{\rm HIPV2}$; dotted line: reduced-order model $Z_{\rm HIPV}$).

the parasitic capacitance of per meter $C_{\rm cable}$ can be expressed as [62]

$$C_{\rm cable} = \frac{2\pi\varepsilon_0\varepsilon_{\rm r}}{\ln(D/c)} \tag{17}$$

where D and c are the diameters of the cable and core, respectively. Constant ε_0 is the vacuum permittivity, and coefficient $\varepsilon_{\rm r} = 2.25$ is the relative permittivity of dielectric material polyethylene for cable. Concerning commonly used CAT II coaxial cable for HIPV probe, there are $D = 2$ mm and $c = 0.53$ mm. Therefore, for a 1.3-m length cable, the $C_{\rm cable}$ of the HIPV probe can be calculated as 120 pF according to (17). Besides, the values of $R_{\rm scope}$ and $C_{\rm scope}$ can be found from the datasheet of employed oscilloscope 715Zi [60].

According to (14) and (15), considering the influence of $L_{\rm n}$ and $C_{\rm in}$, the characteristics of the probe in the frequency domain can be calculated, as depicted in Figs. 10 and 11. Similar characteristics affected by $R_{\rm in}$, $L_{\rm p}$, and $R_{\rm scope}$ can also be obtained.

In Fig. 10, the bandwidth of the HIPV probe can be found above 100 MHz. The input impedance is resistive, capacitive, and inductive in low-, medium-, and high-frequency segments, respectively. Generally, the resonance frequency of SiC MOSFET during transient processes is about 20–40 MHz. The high-frequency impedance of the HIPV probe in this frequency range is not large enough to be ignored. The inserted impedance of the HIPV probe might affect the transient stability of the SiC MOSFET device.

Moreover, the cut-off frequency of the HIPV probe decreases with the increasing parasitic inductance, which further degrades

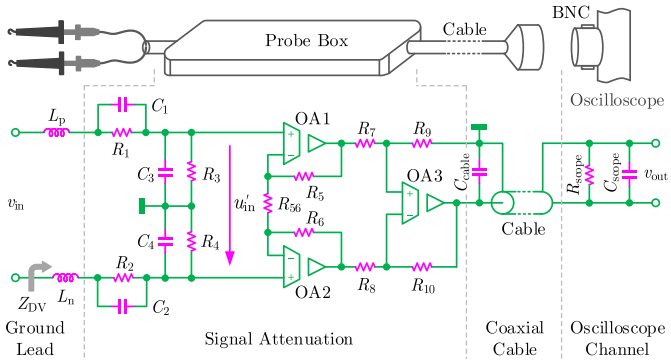

Fig. 12. Schematic diagram of DV probe.

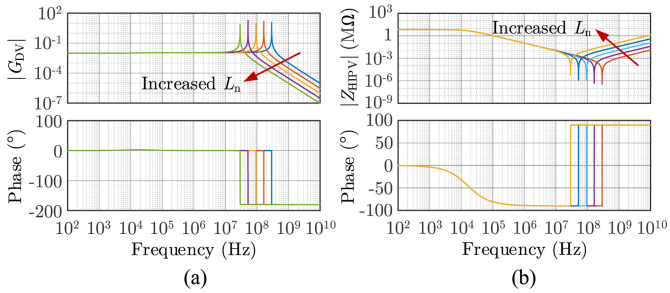

Fig. 13. Calculated characteristics of DV probe affected by L_n from 10 nH to 1 μH. (a) Transfer function G_{DV} and (b) input impedance Z_{DV} (solid line: full-order model Z_{DV1}; dotted line: reduced-order model Z_{DV}).

TABLE VI
PARAMETERS OF DV PROBE HVD3106

	Ground Lead		Attenuation							
Variables	L_p	L_n	R_1	C_1	R_3	C_3	R_{56}	R_5	R_7	R_9
Values	315 nH	315 nH	5 MΩ	5 pF	0.1 MΩ	250 pF	100 kΩ	470 Ω	470 Ω	470 Ω

the bandwidth and affects the transient behavior of DUTs. Thanks to the improved measurement bandwidth and reduced high-frequency impedance, reducing the parasitic inductance caused by the measurement probe is helpful for accurate and stable measurements. Additionally, it is proven that the simplified impedance model Z_{HIPV} is accurate enough to characterize the frequency-domain properties of the full-order model Z_{HIPV2}.

In Fig. 11, the input capacitance C_{in} influence on the magnitude of G_{HIPV} can be seen, which may deteriorate the accuracy of the measurement and degrade the bandwidth of the probe. The mismatched magnitude can be calibrated by regulating the capacitance of the compensator. Besides, the input impedance of the probe is also determined by the C_{in}. A large C_{in} reduces the impedance, and it may intrude the transient stability of SiC device.

C. Impedance Modeling of Differential Voltage Probe

To measure a v_{ds} larger than 400 V having galvanic isolation considerations, the DV probe is needed [63]. According to the existing models of DV probe, a general equivalent circuit for the DV probe is proposed, as illustrated in Fig. 12 [64]–[66]. Usually, $L_p = L_n$, $R_1C_1 = R_3C_3$, $R_1 = R_2$, $R_3 = R_4$, $R_5 = R_6$, $R_7 = R_8$, $R_9 = R_{10}$. Taking the employed DV probe HVD3106 into account, the values of the variables in Fig. 12 can be identified by using the datasheet [67], as listed in Table VI.

According to Fig. 12, the transfer function from the detected input voltage v_{in} to the input voltage of the isolated operational amplifier (OA) v'_{in} can be derived as

$$G_{DV1}(s) = \frac{v'_{in}}{v_{in}} = \frac{B_1 s + B_0}{A_3 s^3 + A_2 s^2 + A_1 s + A_0} \tag{18}$$

where

$$\begin{cases} A_3 = R_1R_3(L_p + L_n)C_1C_3 \\ A_2 = (R_1C_1 + R_3C_3)(L_p + L_n) \\ A_1 = (L_p + L_n + 2R_3R_1C_1 + 2R_1R_3C_3) \\ A_0 = 2R_1 + 2R_3 \\ B_1 = 2R_3R_1C_1 \\ B_0 = 2R_3. \end{cases} \tag{19}$$

The transfer function from the v'_{in} to the output voltage v_{out} can be expressed as

$$G_{DV2}(s) = \frac{v_{out}}{v'_{in}} = \frac{R_9}{R_7}\left(1 + \frac{R_5}{R_{56}} + \frac{R_6}{R_{56}}\right). \tag{20}$$

The transfer function of the DV probe can be yielded as

$$G_{DV}(s) = \frac{v_{out}}{v_{in}} = \frac{v'_{in}}{v_{in}} \times \frac{v_{out}}{v'_{in}} = G_{DV1}(s)G_{DV2}(s). \tag{21}$$

The input impedance of the DV probe can be written as

$$Z_{DV1} = (L_p + L_n)s + 2\frac{R_1}{R_1C_1s + 1} + 2\frac{R_3}{R_3C_3s + 1}. \tag{22}$$

Since $R_1 >> R_3$ and $R_1C_1 \approx R_3C_3$, the third term in Z_{DV1} can be ignored. Therefore, (22) can be simplified to

$$Z_{DV} = (L_p + L_n)s + 2\frac{R_1}{R_1C_1s + 1}. \tag{23}$$

According to (21) and (23), considering the influence of L_n and C_1, the transfer function and input impedance characteristics of the DV probe are indicated in Figs. 13 and 14.

As seen in Fig. 13, the bandwidth of DV probe approximates to 100 MHz. A long power loop of test points increases the parasitic inductance L_n, which reduces the measurement bandwidth and increases the high-frequency impedance. It is also found that the simplified impedance model Z_{DV} is accurate to characterize Z_{DV1}.

As indicated in Fig. 14, the large C_1 increases the low-frequency gain and decreases the high-frequency impedance of the DV probe. Furthermore, the impedance of the probe is not large enough to decouple the probe from the test circuit. The degraded impedance might affect the transient behavior of DUT in the frequency range of 20–40 MHz.

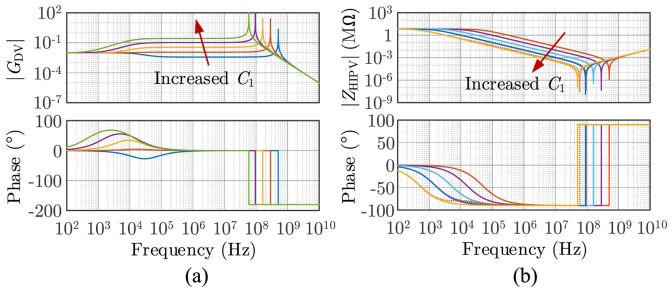

Fig. 14. Calculated characteristics of DV probe affected by C_1 from 1 to 100 pF. (a) Transfer function $G_{\rm DV}$ and (b) input impedance $Z_{\rm DV}$ (solid line: full-order model $Z_{\rm DV1}$; dotted line: reduced-order model $Z_{\rm DV}$).

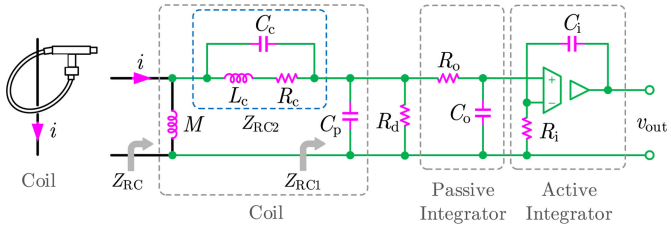

Fig. 15. Schematic diagram of current probe.

D. Impedance Modeling of Current Probe

To measure the high-frequency current of SiC MOSFET, current probes based on Hall Effect or Rogowski coil are mostly used. These probes implement magnetic coupling principle and have similar circuit models. Taking the Rogowski coil as an example, its schematic configuration and equivalent circuit are demonstrated in Fig. 15 [68]–[70]. M is the mutual inductance of the coil. $C_{\rm c}$ and $C_{\rm p}$ are parasitic capacitances of the coil. $L_{\rm c}$ and $R_{\rm c}$ are self-inductance and parasitic resistance of the coil. $R_{\rm d}$ is the damping resistance to suppress the possible LC resonance of the coil. $R_{\rm o}$ and $C_{\rm o}$ are the resistance and capacitance of the passive integrator. $R_{\rm i}$ and $C_{\rm i}$ are the resistance and capacitance of active integrator. In general, the passive and active integrators satisfy $R_{\rm o}C_{\rm o} = R_{\rm i}C_{\rm i}$.

According to Fig. 15, the equivalent impedances Z_{RC1} and Z_{RC2} can be derived as

$$Z_{\rm RC1} = \frac{1}{C_{\rm p}s + \frac{1}{R_{\rm d}} + \frac{C_{\rm o}s}{R_{\rm o}C_{\rm o}s+1}} \tag{24}$$

$$Z_{\rm RC2} = \frac{1}{C_{\rm c}s + \frac{1}{L_{\rm c}s+R_{\rm c}}}. \tag{25}$$

The input impedance of the Rogowski coil can be written as

$$Z_{\rm RC3} = \frac{(Z_{\rm RC1} + Z_{\rm RC2})Ms}{Ms + Z_{\rm RC1} + Z_{\rm RC2}}. \tag{26}$$

Ignoring the very small parasitics, the input impedance in (26) can be simplified to

$$Z_{\rm RC} = \frac{Ms}{MC_{\rm c}s^2 + 1}. \tag{27}$$

TABLE VII
PARAMETERS OF CURRENT PROBE CP9006S

	Coil						Integrator	
Variables	M	$L_{\rm c}$	$R_{\rm c}$	$C_{\rm c}$	$C_{\rm p}$	$R_{\rm d}$	$R_{\rm o}$ ($R_{\rm i}$)	$C_{\rm o}$ ($C_{\rm i}$)
Values	10 nH	21 µH	4.4 Ω	0.09 pF	2.6 pF	0.2 MΩ	0.1 MΩ	100 µF

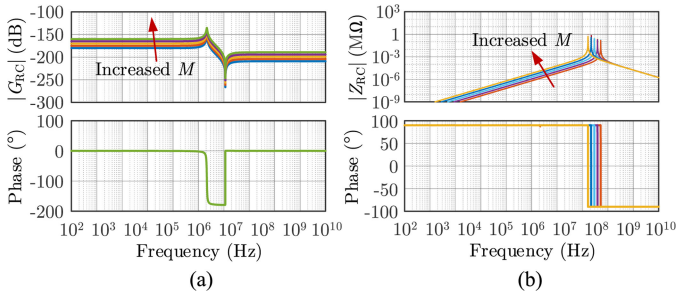

Fig. 16. Calculated characteristics of Rogowski coil affected by M from 1 to 100 nH. (a) Transfer function $G_{\rm RC}$ and (b) input impedance $Z_{\rm RC}$ (solid line: full-order model Z_{RC3}; dotted line: reduced model $Z_{\rm RC}$).

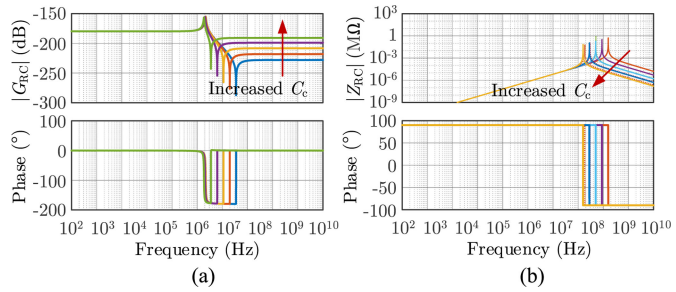

Fig. 17. Calculated characteristics of Rogowski coil affected by $C_{\rm c}$ from 0.1 to 10 pF. (a) Transfer function $G_{\rm RC}$ and (b) input impedance $Z_{\rm RC}$ (solid line: full-order model Z_{RC3}; dotted line: reduced model $Z_{\rm RC}$).

The transfer function from the measured current i to the output voltage $v_{\rm out}$ can be expressed as

$$G_{\rm RC}(s) = \frac{i}{v_{\rm out}} = Ms\frac{Z_{\rm RC1}}{Z_{\rm RC1} + Z_{\rm RC2}}\frac{1}{R_{\rm o}C_{\rm o}s+1}. \tag{28}$$

According to the datasheet of the employed current probe CP9006S [68]–[70], the values of the proposed model are listed in Table VII. According to (27) and (28), the frequency-domain characteristics of the coil influenced by M and $C_{\rm c}$ are calculated, as demonstrated in Figs. 16 and 17.

In Fig. 16, it can be found that the bandwidth of the Rogowski coil is approximate to 10 MHz. The gain of $G_{\rm RC}(s)$ and input impedance Z_{RC3} increases with mutual inductance M. Due to the inserted mutual inductance, the input impedance of current probe is inductive in the low-frequency segment, whereas the high-frequency impedance is capacitive determined by $C_{\rm c}$. Additionally, it is proven that the simplified impedance model $Z_{\rm RC}$ is precise enough to characterize the coil.

In Fig. 17, the influence of coil capacitance is demonstrated. Large coil capacitance $C_{\rm c}$ improves the high-frequency gain of $G_{\rm RC}$, which is undesired for noise rejection. Besides, the high-frequency impedance of $Z_{\rm RC}$ is decreased by large $C_{\rm c}$, which

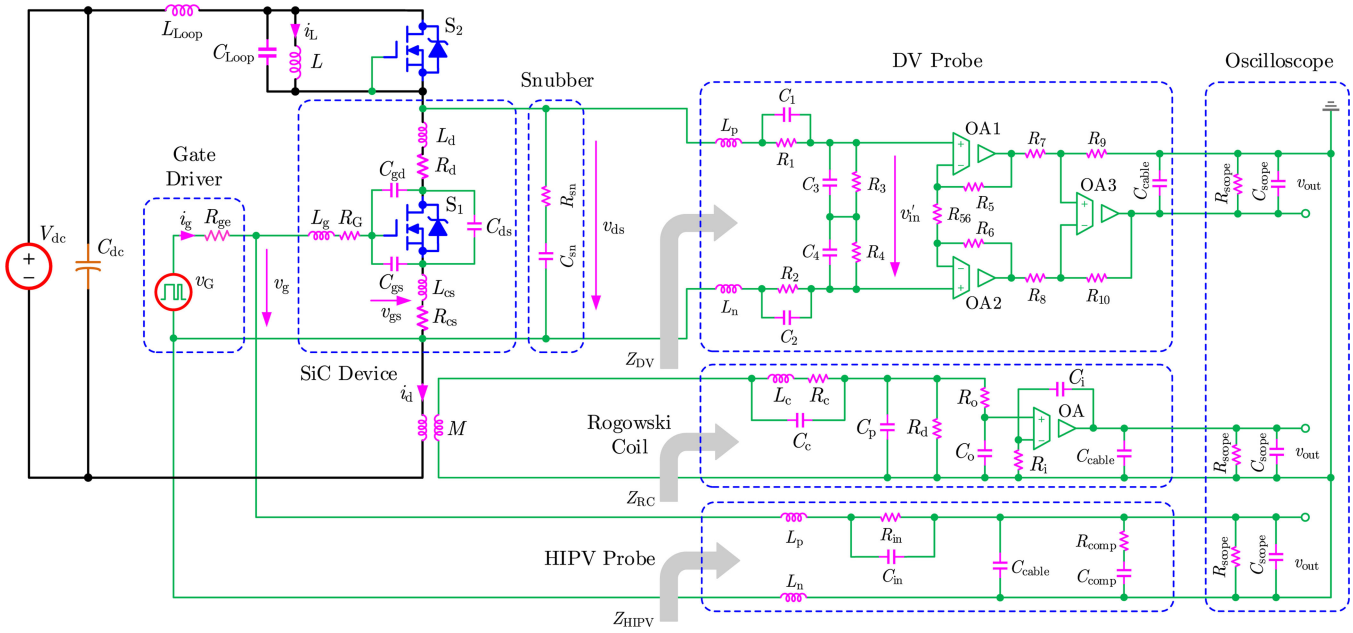

Fig. 18. Synthesized impedance model of SiC MOSFET including the probes.

may interfere in the transient behavior of SiC MOSFET device under test.

IV. Synthesis Model and Stability Mechanism of Coupled SiC MOSFET and Measurement Probes

Focusing on issue 2 in Section II, to reveal the stability mechanism and interaction principles between SiC MOSFET and probes, the circuit and mathematical models are established in this Section. A methodology is proposed to assess the stability boundaries of the coupled device–probe system.

A. Mechanism Modeling of Device–Probe Interaction

According to the impedance models of SiC MOSFET and probes mentioned before, the schematic circuit in Fig. 1 can be fully extended, as illustrated in Fig. 18. $L_{\rm loop}$ is the parasitic inductance in power loop caused by circuit traces. $C_{\rm loop}$ is the parasitic capacitance in power loop caused by load inductor and freewheeling diode of S_2. Concerning the influence of snubber circuit, $R_{\rm sn}$ and $C_{\rm sn}$ are resistance and capacitance of the snubber circuit.

To reveal the stability mechanism of SiC MOSFET intruded by measurement probes, the probes in Fig. 18 can be replaced by impedances $Z_{\rm HIPV}$, $Z_{\rm DV}$, and $Z_{\rm RC}$. Therefore, the model in Fig. 18 can be simplified to the one in Fig. 19(a).

Considering the small-signal model, the equivalent circuit in Fig. 19(b) can be further simplified to Fig. 19(c), where the impedances in star connection can be expressed as

$$\begin{cases} Z_1 = Z_{\rm g} + Z_{\rm HIPV}R_{\rm ge}/\left(Z_{\rm HIPV}+R_{\rm ge}\right) \\ Z_2 = Z_{\rm cs} \\ Z_3 = Z_{\rm d} + Z'_{\rm DV}(Z_{\rm Loop}+Z_{\rm RC})/\left(Z_{\rm Loop}+Z'_{\rm DV}+Z_{\rm RC}\right) \end{cases} \tag{29}$$

where

$$\begin{cases} Z_{\rm g} = L_{\rm g}s + R_{\rm G} \\ Z_{\rm d} = L_{\rm d}s + R_{\rm d} \\ Z_{\rm cs} = L_{\rm cs}s + R_{\rm cs} \\ Z'_{\rm DV} = Z_{\rm DV}Z_{\rm sn}/\left(Z_{\rm DV}+Z_{\rm sn}\right) \\ Z_{\rm sn} = R_{\rm sn} + 1/\left(C_{\rm sn}s\right) \\ Z_{\rm loop} = L_{\rm loop}s + 1/\left(C_{\rm loop}s\right). \end{cases} \tag{30}$$

The impedances in star connection can be changed to the ones in delta connection as shown in Fig. 19(d), which can be written as

$$\begin{cases} Z_{\rm GS} = \left(Z_1Z_2 + Z_1Z_3 + Z_2Z_3\right)/Z_3 \\ Z_{\rm GD} = \left(Z_1Z_2 + Z_1Z_3 + Z_2Z_3\right)/Z_2 \\ Z_{\rm DS} = \left(Z_1Z_2 + Z_1Z_3 + Z_2Z_3\right)/Z_1. \end{cases} \tag{31}$$

The transfer function model from $i_{\rm d}$ to $v_{\rm gs}$ can be expressed as

$$v_{\rm gs} = F(s)i_{\rm d} = -\frac{Z'_{\rm DS}}{Z'_{\rm GD}+Z'_{\rm GS}+Z'_{\rm DS}}Z'_{\rm GS}i_{\rm d} \tag{32}$$

where $F(s)$ is the gain of the feedback path. The impedances associated with parallel capacitances can be expressed as

$$\begin{cases} Z'_{\rm GS} = Z_{\rm GS}/\left(C_{\rm GS}sZ_{\rm GS}+1\right) \\ Z'_{\rm GD} = Z_{\rm GD}/\left(C_{\rm GD}sZ_{\rm GD}+1\right) \\ Z'_{\rm DS} = Z_{\rm DS}/\left(C_{\rm DS}sZ_{\rm DS}+1\right). \end{cases} \tag{33}$$

According to the block diagram in Fig. 20, the model of the SiC MOSFET intruded by the probes can be expressed as

$$i_{\rm d} = G(s)v_{\rm g} = \frac{A(s)}{1-A(s)F(s)}v_{\rm g}$$

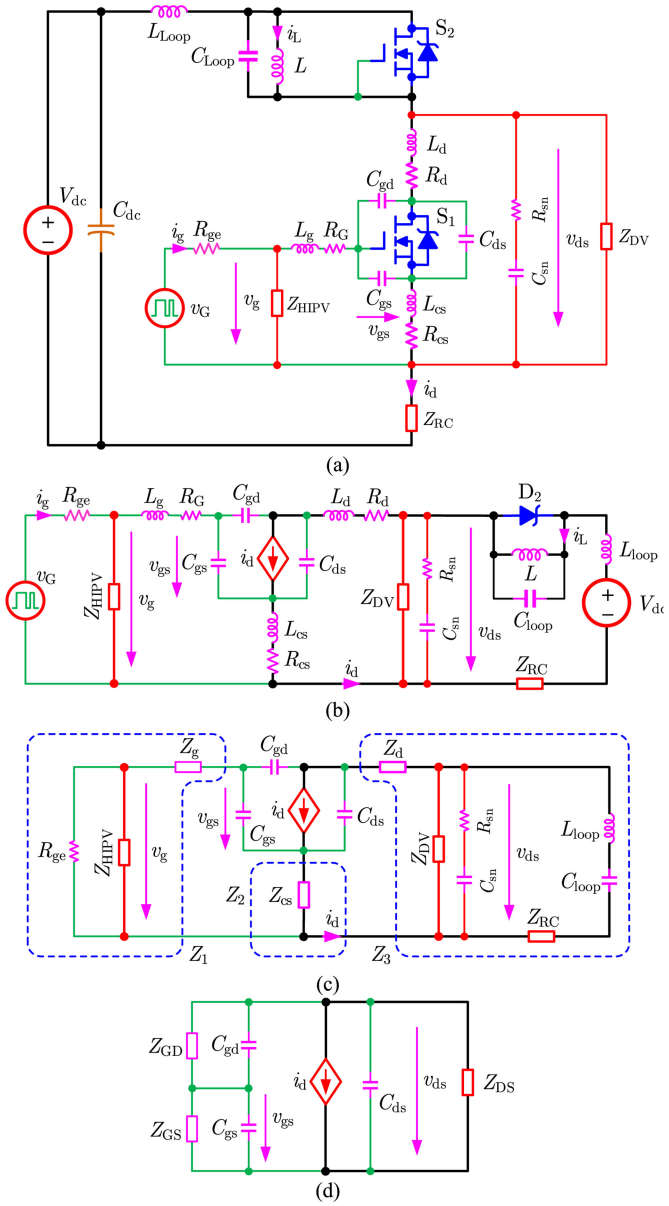

Fig. 19. Impedance-based model of SiC MOSFET intruded by measurement probes. (a) Impedance-oriented circuit of test bench. (b) Simplified equivalent circuit. (b) Small-signal circuit model. (c) Star-delta transferred circuit model.

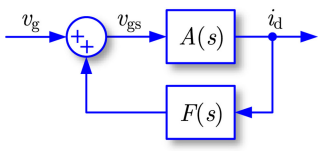

Fig. 20. Block diagram of impedance-based model.

$$= \frac{g_{\mathrm{m}}(Z'_{\mathrm{GD}} + Z'_{\mathrm{GS}} + Z'_{\mathrm{DS}})}{Z'_{\mathrm{GD}} + Z'_{\mathrm{GS}} + Z'_{\mathrm{DS}} - g_{\mathrm{m}} Z'_{\mathrm{GS}} Z'_{\mathrm{DS}}} v_{\mathrm{g}} \tag{34}$$

where $A(s)$ is the gain in the forward path. According to (8), it can be expressed as

$$A(s) = \frac{\partial i_{\mathrm{d}}}{\partial v_{\mathrm{gs}}} = g_{\mathrm{m}}. \tag{35}$$

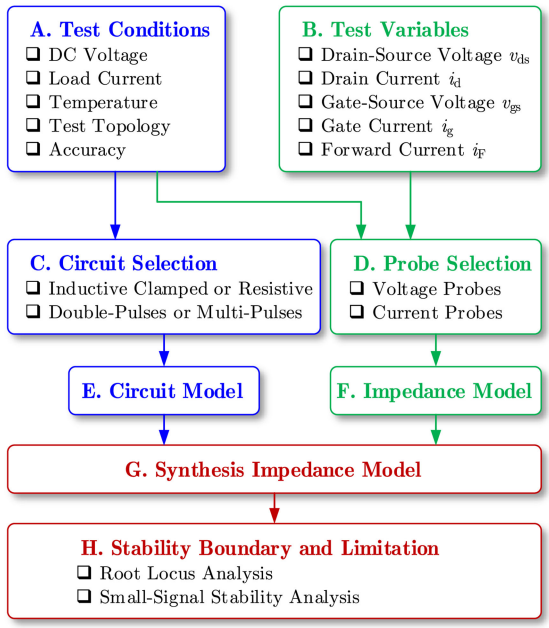

Fig. 21. Methodology of SiC MOSFET transient stability assessment concerning probes.

To justify the stability of SiC MOSFET intruded by probes, the characteristic equation in (34) can be expressed as

$$\Delta(s) = \prod_i (s - p_i) = 0. \tag{36}$$

Concerning either pole p_i of $\Delta(s)$, it can be written as

$$p_i = \sigma_i + j\omega_i = \sigma_i + j2\pi f_i \tag{37}$$

where σ_i and ω_i are real and imaginary parts of the pole. f_i is the resonance frequency. The damping ratio ξ_i can be defined as

$$\xi_i = -\frac{\sigma_i}{\sqrt{\sigma_i^2 + \omega_i^2}} = -\frac{\sigma_i}{\omega_{\mathrm{d}i}} \tag{38}$$

where $\omega_{\mathrm{d}i}$ is the damped resonant frequency. The real part of the pole σ_i determines the stability of the test system. Positive σ_i means negative damping and unstable mode of the transient measurement. Negative σ_i far away from the imaginary axis means sufficient damping ratio and stable mode.

B. Assessment Methodology of Device–Probe Stability

Considering the interaction between device and probes, a methodology is proposed to assess the stability boundaries and limitations of SiC MOSFET intruded by measurement probes, as illustrated in Fig. 21. The proposed assessment procedure in Fig. 21 is split into two parallel paths to create a synthesis impedance model combined circuit model with the impedance model. The circuit model is determined by the desired test conditions and corresponding test circuit. The impedance model is determined by the desired measurement variables and corresponding instruments. Once the synthesis impedance model is set up, stability boundaries can be identified by using root locus analysis or small-signal analysis approaches.

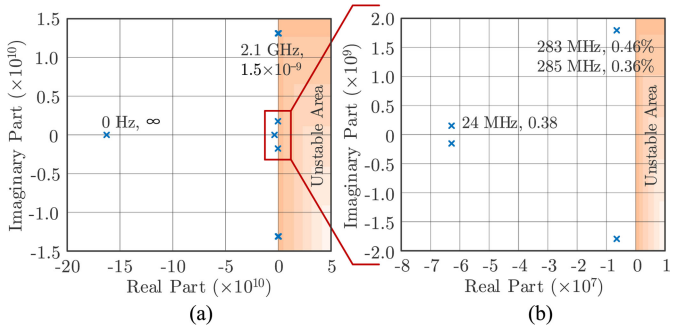

Fig. 22. Calculated poles of interaction model between SiC MOSFET and probes. (a) Pole distribution and (b) zoom in.

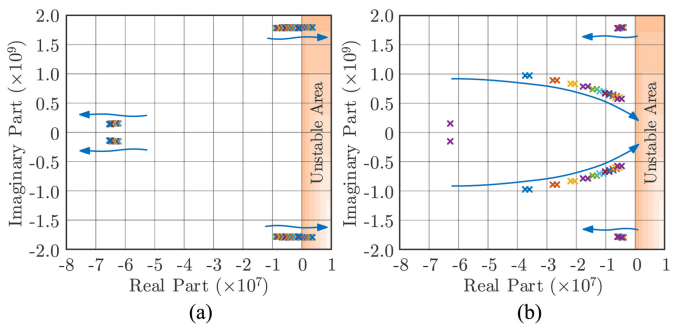

Fig. 23. Calculated root locus of SiC MOSFET influenced by HIPV probe parasitics. (a) $C_{\rm in}$ from 1 to 100 pF. (b) $L_{\rm n}$ from 50 to 300 nH.

V. Case Study: Transient Stability of Device–Probe Interaction Influenced by Multiple Factors

According to the parameters of the test bench in Section III and the methodology of the stability assessment in Section IV, the poles of closed-loop model $G(s)$ in (34) are calculated, as shown in Fig. 22. Due to the complex LC resonances caused by inductive and capacitive parasitics, the device–probe coupling system contains more than 40 poles. Among them, there are two pairs of conjugated poles close to the imaginary axis. The resonant frequencies and damping ratios approximate 283 and 285 MHz, 0.46% and 0.36%, respectively. Besides, there is a pair of poles close to the real axis, and its frequency and damping ratio are 24 MHz and 0.38%. Influenced by the disturbances of measurement, these poles may move across the imaginary axis to the unstable area, which will lead to the transient instability of the SiC MOSFET.

Taking the parasitic capacitance $C_{\rm in}$ and inductance $L_{\rm n}$ into account, Fig. 23 demonstrates the influence of HIPV probe. As seen, large $C_{\rm in}$ degrades the stability of SiC MOSFET. HIPV probe leads to instability in the condition of $C_{\rm in} > 47$ pF. The large parasitic inductance $L_{\rm n}$ caused by long ground lead drives two pairs of conjugate poles close to the imaginary axis, which reduces the damping ratio and the stability margin.

Concerning the impact of DV probe, Fig. 24 indicates the trajectories of poles with different input capacitance C_1 and inductance $L_{\rm n}$. Caused by low bandwidth probe and long ground lead, the increased C_1 and $L_{\rm n}$ drive a pair of poles to the imaginary axis, which decreases the damping ratio and degrades the stability margin.

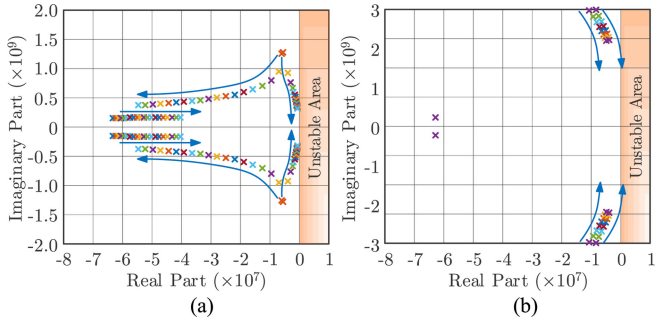

Fig. 24. Calculated root locus of SiC MOSFET influenced by DV probe parasitics. (a) C_1 from 1 to 100 pF. (b) $L_{\rm n}$ from 50 to 300 nH.

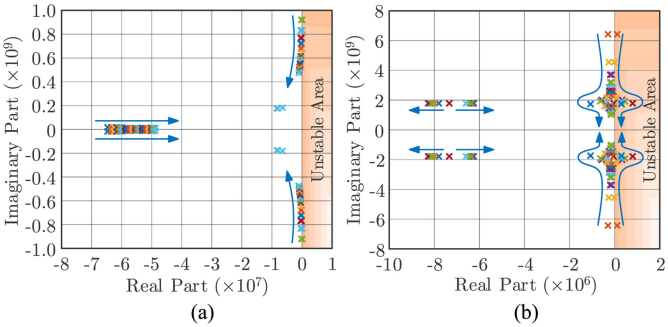

Fig. 25. Calculated root locus of SiC MOSFET influenced by Rogowski coil parasitics. (a) M from 1 to 100 nH and $C_{\rm c}$ from 0.01 to 100 pF.

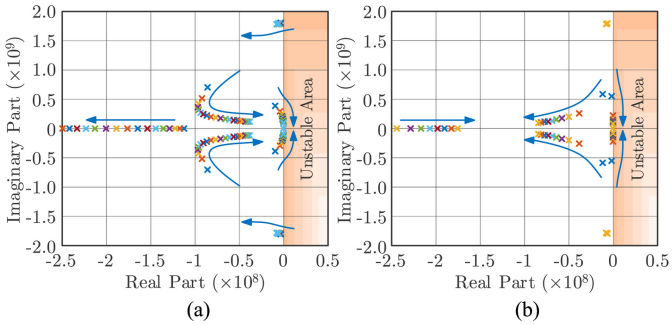

Fig. 26. Calculated root locus of SiC MOSFET influenced by loop parasitics. (a) $L_{\rm loop}$ from 10 to 500 nH. (b) $C_{\rm Loop}$ 10 to 500 pF.

Fig. 25 demonstrates the influence of the Rogowski coil. The mutual inductance M hardly degrades the stability of device–probe coupling system. Nevertheless, the capacitance of the current probe can lead to instability when $C_{\rm c}$ is changed from 5 to 20 pF.

As shown in Fig. 26, due to the parasitics in the power loop, for instance, $L_{\rm loop} = 100$ nH and $C_{\rm loop} = 200$ pF, one pair of poles is driven to the imaginary axis. It is easily unstable suffering from other disturbances.

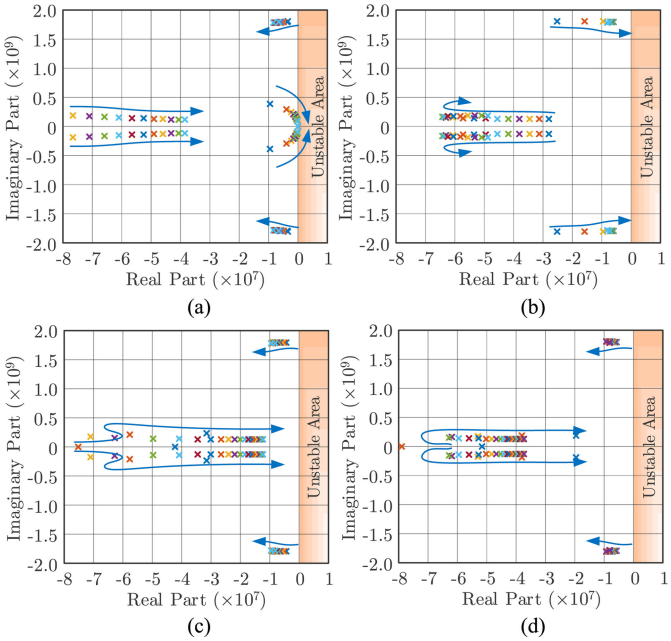

Fig. 27. Calculated root locus of SiC MOSFET influenced by SiC MOSFET parasitics. (a) $C_{\rm gs}$ from 5 pF to 4 nF. (b) $C_{\rm ds}$ from 5 to 400 pF. (c) $C_{\rm gd}$ from 5 to 100 pF. (d) $g_{\rm m}$ from 1 to 25 S.

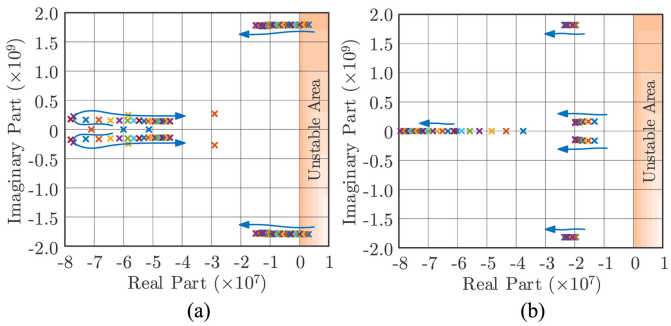

Fig. 28. Calculated root locus of SiC MOSFET affected by gate resistance $R_{\rm ge}$ from 1 to 25 Ω (a) without snubber circuit and (b) with snubber circuit.

The influence of device parameters is indicated in Fig. 27. Generally, the input impedance is capacitive in the high-frequency segment. Large parasitic capacitances of device drive poles to the imaginary axis, which reduces the damping ratio of switching ringing.

As indicated in Fig. 28(a), by using a large gate resistance, the stability of the tested system can be enhanced. When the total gate resistance $R_{\rm G} + R_{\rm ge} < 7\,\Omega$, the tested system might be unstable. Additionally, Fig. 28(b) demonstrates the root locus by using a snubber circuit $R_{\rm sn} = 10\,\Omega$ and $C_{\rm sn} = 220$ pF. Compared with Fig. 28(a), it can be found from Fig. 28(b) that the snubber circuit reshapes the synthesized impedance of device–probe and eliminates the unstable poles caused by the small gate resistance.

VI. Experimental Results

To confirm the proposed models and analyses, a double-pulse test bench is prepared, as shown in Fig. 29. The test

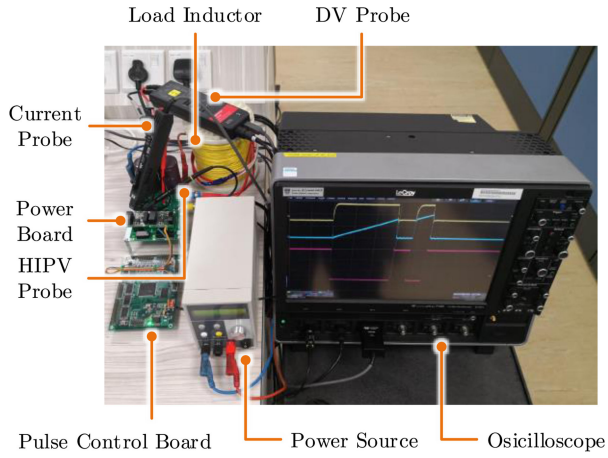

Fig. 29. Configuration of test bench.

TABLE VIII
Comparatively Tested HIPV Probes

Manufacturer	Probe	Bandwidth (MHz)	$C_{\rm in}$ (pF)	Impedance (MΩ)
Agilent	10071A	150	15	10
Tektronix	TPP0200	200	12	10
Lecroy	PP026	500	10	10

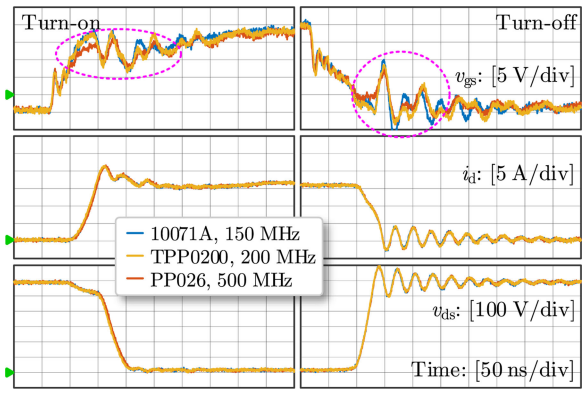

Fig. 30. Experimental turn ON–OFF behaviors of SiC MOSFET by using different HIPV probes as seen in Table VIII.

conditions are selected as $V_{\rm dc} = 600\,{\rm V}$, $I_{\rm d} = 15\,{\rm A}$, $R_{\rm ge} = 10\,\Omega$, and $V_{\rm C}/V_{\rm E} = 20/-5\,{\rm V}$. Digital oscilloscope 715Zi from LeCroy (bandwidth 1.5 GHz and sample rate 20 GS/s) is employed to capture the waveforms. The transient stability influenced by the HIPV probe, DV probe, current probe, gate resistance, device parasitics, and snubber circuit is comparatively studied as follows.

By using different HIPV probes given in Table VIII, the experimental results are presented in Fig. 30. It is seen that the ringing amplitude of the $v_{\rm gs}$ by using low-bandwidth HIPV probe is apparently larger than the ones by using high-bandwidth probes. As indicated in Section III, the HIPV probe having high bandwidth also corresponds to small input capacitance $C_{\rm in}$. As a result, the transient instability effect of SiC MOSFET interfered by the high-bandwidth probe is weaker compared with the low-bandwidth probe. Moreover, owing to the minimum bandwidth of the considered HIPV probe, 150 MHz, which is remarkably

TABLE IX
COMPARATIVELY TESTED DV PROBES

Manufacturer	Probe	Bandwidth (MHz)	C_1 (pF)	Impedance (MΩ)
Pico	TA044	70	10	10
Lecroy	ADP305	100	7	4
Lecroy	HVD3106	120	5	5
Cybertek	DP6150B	200	4	5

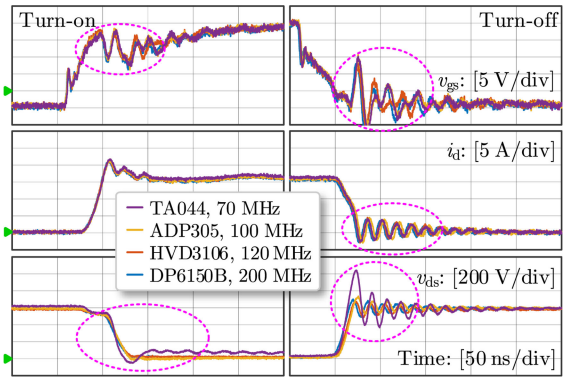

Fig. 31. Experimental ON–OFF trajectories of SiC MOSFET by using different DV probes as specified in Table IX.

TABLE X
COMPARATIVELY TESTED CURRENT PROBES

Manufacturer	Principle	Probe	Bandwidth (MHz)	Rise Time (ns)
Cybertek	Rogowski Coil	CP9006S	30	–
Lecroy	Hall Effect	AP015	50	7
Lecroy	Hall Effect	CP030	50	7
Pearson	Hall Effect	2877	200	2

larger than the intrinsic frequency of the probe–device coupled test bench, the interactions among v_{gs}, i_d, and v_{ds} are not observed. The measured i_d and v_{ds} are hardly affected by the tested HIPV probes.

Considering the influence of DV, different DV probes are compared, as given in Table IX. It can be observed that the input capacitance determines the bandwidth, as analyzed in Section III. The DV probe having higher bandwidth performs smaller input capacitance C_1. The measured results are shown in Fig. 31. The DV probes directly affect the accurate measurement of v_{ds}. Besides, the altered propagation delay of i_d is found by using DV probes with different bandwidths. Additionally, the transient behavior of v_{gs} is also intruded by the DV probes.

Different kinds of current probes are comparatively investigated and listed in Table X. As shown in Fig. 32, the current probes directly intrude the measurement of i_d, in terms of the di/dt, propagation delay, resonant frequency, etc. It is seen that the current probes with different bandwidths introduce inconsistent propagation delay, which will result in inaccurate measurement of power loss as discussed in Section II. Additionally, as the studied probes have different bandwidths and impedances, the ringing amplitudes of measured current waveforms are altered. Moreover, it is confirmed that the measured variables i_d, v_{gs}, and v_{ds} are coupled with each other, as predicted in the proposed circuit and mathematical models in Section IV. The inserted

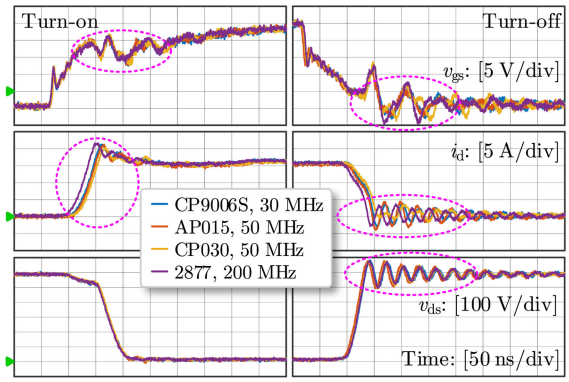

Fig. 32. Experimental ON–OFF trajectories of SiC MOSFET by using different current probes as specified in Table X.

TABLE XI
COMPARATIVELY TESTED POWER DEVICES

Type	Manufacturer	Device	Rating (@ 25°C)	R_G (Ω)	C_{gs} (pF)
C2M0080120D	Cree	SiC MOSFET	36 A	4.6	950
SCH2080KE	Rohm	SiC MOSFET	40 A	6.3	1850
H1M120F060	Hestia	SiC MOSFET	41 A	4	1800
LSIC1MO120E0080	Littelfuse	SiC MOSFET	39 A	1	1825
IHW20N120R3	Infineon	Si IGBT	40 A	0	1503

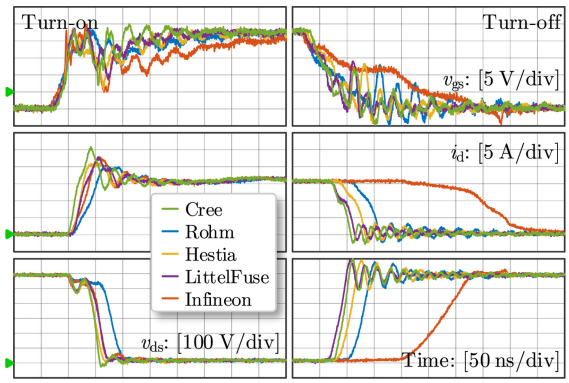

Fig. 33. Experimental ON–OFF trajectories of different devices specified in Table XI.

impedances by current probes also interfere in the transient behaviors of gate-driver loop and power loop.

By using devices from different manufacturers as listed in Table XI, the influences of the device specifications are confirmed, as depicted in Fig. 33. It is seen that the device with smaller R_G and C_{gs} performs much faster switching speed, which deteriorates the stability of probe–device coupling system. With respect to transient stability, compared to Si IGBT, the SiC MOSFET is much more sensitive to the parasitics of the test bench and measurement probes.

The influences of the external gate resistance R_{ge} on the device–probe coupling system are exploited, as indicated in Fig. 34. In the condition of different R_{ge} between 2.4 Ω and 30 Ω, the stability of the test bench is enhanced by using a large gate resistance. The damping ratio of the device–probe coupling

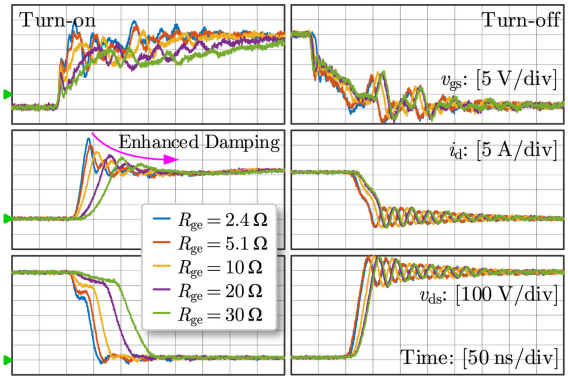

Fig. 34. Experimental ON–OFF trajectories of SiC MOSFET in condition of different gate resistances.

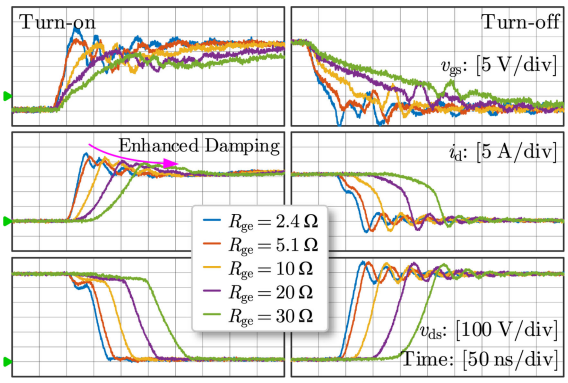

Fig. 35. Experimental ON–OFF trajectories of SiC MOSFET by using snubber circuit in condition of different gate resistances.

system increases with gate resistance. However, the switching loss of the SiC MOSFET also increases.

By using a snubber circuit $R_{sn} = 10\ \Omega$ and $C_{sn} = 220\,\text{pF}$, the switching trajectories of SiC MOSFET in the condition of different R_{ge} are demonstrated in Fig. 35. Compared with Fig. 34, the snubber circuit reduces the switching ringing and overshooting, and improves the transient stability. However, the snubber circuit also reduces the di/dt and dv/dt, and the correspondingly increased switching time leads to much more switching losses. Therefore, there is a tradeoff between transient stability and switching loss.

Taking the resonant current waveforms in Fig. 34 as an example, the resonant frequency and damping ratio of drain current can be theoretically calculated by the models in (34)–(38), and these items can also be identified by the experimental results. By using the matrix pencil method [71]–[73], the experimental and modeled current waveforms are demonstrated in Fig. 36(a). It is found that the matrix pencil method can effectively obtain the resonant modes of the drain current. The extracted resonant frequency and damping ratio are presented in Fig. 36(b), which highly agree with the prediction of the proposed models. As seen, the presented models and analyses are matched with the experiments.

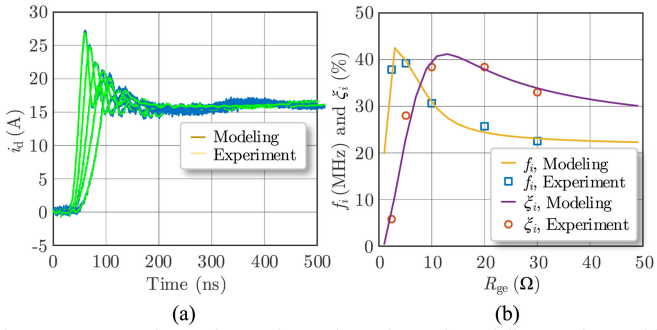

Fig. 36. Comparison of experimental results and modeling analyses. (a) Comparison of waveforms achieved by experiments and models. (b) Comparison of resonant frequency and damping ratio achieved by models and experiments.

VII. Conclusion

Very fast switching speed of SiC MOSFET is a double-edged sword. On the one hand, it is helpful to reduce switching loss and elevate switching frequency of SiC MOSFET. On the other hand, it challenges the transient stability of SiC MOSFET because of the high di/dt and inevitable parasitics. Targeting at the instability issues of SiC MOSFET intruded by the parasitics of instruments, systemic models are proposed to reveal the parasitic-dependent impedance and bandwidth of the measurement probes. From the perspective of impedance, the synthesized circuit and mathematical models are created to exploit the underlying interaction principles of the coupling system combining SiC MOSFET with probes. It is found that the capacitance and inductance of probes degrade the input impedance and bandwidth, which leads to measurement inaccuracy and transient instability of SiC MOSFET. The parasitic inductance caused by the test point and the ground lead of probes also degrade the stability of SiC MOSFET. Besides, the transient stability may be deteriorated by using small gate resistance in high-frequency and fast switching scenarios; however, the snubber circuit is useful to enhance the transient stability. Compared with Si counterpart, the transient instability of SiC MOSFET is much more sensitive to the probe parasitics.

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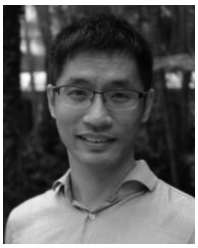

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