Highly Effective Cell Equalization in a Lithium-Ion Battery Management System

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***Abstract*—This paper proposes a highly effective voltage cell equalization method for lithium-ion (Li-ion) battery management systems (BMSs) for several applications, such as nearly zero energy buildings, microgrids, and electric vehicles. The concept of the suggested method is the proper control of the charging current of each cell of a battery stack through the suitable regulation of the gate source of each cell's parallel-connected MOSFET. Thus, the MOSFET can act as a controllable current source for providing the proper equalization current according to the specific needs of each battery cell. The correct voltage level of the gate-source of each MOSFET is determined by a cell equalization controller through the comparison of the performance of each cell of a battery stack with the healthier cell, which is detected by an aging estimation algorithm based on the evaluation of the internal resistor and the capacity fade of each cell. Therefore, smoother and faster cell equalization is achieved compared to the conventional dissipative method. The practicality and the high effectiveness of the proposed cell equalization technique have been experimentally validated. Several experimental results are presented to demonstrate the operational improvements of the proposed cell equalization technique against the conventional one.**

***Index Terms*—Battery cell equalization, battery management system (BMS), energy storage system, electric vehicle, microgrid, nearly zero energy building.**

I. Introduction

IT IS well known that the electric energy storage is a key technology that can play a crucial role in the improvement of the energy sustainability, in several sectors of the everyday life [1]. Thus, it is expected that the batteries will be the critical element to addressing some of the most important challenges of the contemporary era, such as the increasing demand for energy saving, the growing use of electric vehicles as an eco-friendly solution for transportation, the increasing penetration of the renewable energy sources, and the requirements for improved flexibility and effectiveness in the energy management of the grid [2], [3].

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However, despite the significant progress in materials and electrochemistry of the batteries, there is considerable margin for further efficiency improvement and increase in the exploitation of the energy storage capability [4]. The key role for these objectives plays the energy management, in which critical internal variables are the accurate monitoring and the battery cell equalization, since they not only augment the performance of the ESS but also can facilitate avoiding catastrophic hazards and premature failure and can contribute to the improvement of the battery durability [5].

The lithium-ion (Li-ion) batteries have several competitive advantages against the other battery types, such as high energy density and high charge/discharge rate [6], [7]. Since each battery cell has low voltage, several cells should be connected in series to meet the voltage requirements. However, this may cause imbalance problems that are also worsen by the repetitive charge and discharge of the battery systems, which are usually realized with variable current. This results in the increase of the internal resistance and capacity fading of the battery system [8]. Mentioned earlier are the two important factors that significantly influence the performance of a battery system and lead to the decrease of its lifespan [9].

To avoid the aforementioned adverse operating conditions, an improved energy management system is required that should not only monitor each battery cell operation so as the current, voltage, and temperature are within safety limits but mainly attain voltage equalization of the battery cells as well [10]. The control schemes that have been proposed in the technical literature are classified in energy dissipative and nondissipative [11], according to whether the electric energy is wasted in heat or transferred to other cells during the equalization procedure, respectively.

In the *energy dissipative equalization methods*, the equalization energy is consumed by an ohmic resistance and they are categorized as passive and active techniques. In a passive dissipative equalization circuit, a resistance is connected in parallel with each battery cell to absorb the excess energy [12], while in an active dissipative equalization system, a power switch with an ohmic resistance in series connection is used to regulate the rate of the energy absorption [13]. Although the passive method is simpler and cost-effective compared to the active method, it is less energy efficient [14].

In the *energy nondissipative equalization methods*, the equalization energy is exploited by the other cells of a battery stack [15]. Depending on how that energy is transferred, they are classified in the cell-to-cell [16], the cell-to-pack [17], [18],

the pack-to-cell [19], [20], and the cell-to-pack-to-cell control schemes [21], [22]. Some nondissipative techniques use inductors or capacitors for temporarily storing the equalization energy [23], while some others utilize power converters to transfer the equalization energy between the cells or to diffuse it in the whole battery pack according to the need of each cell for voltage equalization [24]. The energy nondissipative equalization systems are more efficient compared to the dissipative counterparts; however, they are more expensive and complicated in the implementation and, thus, more vulnerable to faults [25], [26].

From the aforementioned discussion, it is concluded that the decision between a dissipative and a nondissipative method for a battery management system (BMS) is a difficult dilemma. Specifically, it should be evaluated how much benefit would be provided by making a heavy investment in additional hardware to have a slightly more efficient battery cell equalization with a nondissipative scheme compared to a low cost, simpler, and highly reliable dissipative energy equalization technique. Moreover, considering the high technological progress in the materials, the electrochemistry, and consequently, the performance of the batteries, it should be evaluated if a nondissipative technique could be practically and effectively advantageous against a dissipative technique that could justify the increase in the cost and complexity of the cell equalization system [27].

Therefore, the two techniques appear to follow parallel paths with respect to their utilization. Thus, the decision for the correct selection is obtained by evaluating the importance of the techno-economic advantages that each technique can provide in a battery energy storage application [28]. The aforementioned statement is confirmed by the fact that almost all the semiconductor manufactures produce appropriate equipment for both dissipative and nondissipative battery cell balancing systems [29], [30]. The same also holds for manufacturers of BMS modules for Li-ion batteries, for both industrial and domestic applications [31].

Since the dissipative equalization technique is a potential choice for a large number of battery energy storage applications, the improvement of the BMS performance and reliability without affecting the complexity and cost is highly important. An interesting approach can be the utilization of the MOSFET of each battery cell as a controllable equalization device, instead of using it for simply switching ON/OFF the equalization current that flows through a constant value resistor, as holds in the existing dissipative equalization techniques. Thus, the MOSFET acts as a controllable current source and the resistance value that is faced by each cell is properly regulated with respect to the specific need for voltage equalization. Therefore, smoother and faster equalization performance can be attained compared to the conventional dissipative equalization method. This is accomplished by properly controlling the gate-source voltage of the MOSFET, and thus, the level of the saturation region current is accordingly regulated.

For the correct implementation of the proposed method, the performance of each cell is accurately monitored. Thus, by introducing an advanced cell evaluation algorithm, the healthier cell of each battery stack is detected which can be used as a driver for the proper voltage equalization of the other cells of the battery stack. Specifically, the internal resistance and the capacity fade of each battery cell are online determined through the appropriate estimation algorithms. Then, the healthier cell is detected by means of an estimator algorithm that is based on the fuzzy-logic method. Finally, the correct gate-source voltage of the equalization MOSFET of each battery cell is determined through a fuzzy-logic voltage cell equalization controller (VCEC).

A first attempt to utilize the MOSFET as a controllable device for battery cell equalization has been presented in [32]–[34]. However, no control on the equalization current has been applied, and thus, none of the benefits that the MOSFET can provide as a controllable source have been exploited. Therefore, an integrated and highly effective control system is required that can provide fast, smooth, and cost-effective voltage equalization of the battery cells.

The aim of this paper is to propose an active energy dissipative equalization technique that is based on the proper control of the gate-source voltage of the parallel-connected MOSFET to each battery cell so that the MOSFET can behave as a controllable current source for the voltage equalization. A control algorithm is presented that accurately monitors the cells performance and online detects the healthier cell of each stack of the battery pack. The healthier cell is used as a driver to determine the correct gate-source voltages of the parallel-connected MOSFETs of the other cells. Thus, the level of the saturation region current of each MOSFET is regulated according to the need of each of the respective cell for voltage equalization. Therefore, smooth and fast voltage equalization is attained with the proposed method, in contrast to the highly pulsating current and slower performance of the conventional dissipative equalization method.

From the aforementioned discussion, it is concluded that protection of the battery lifespan and, thus, of the whole battery storage system can be achieved with the suggested cell equalization method. The high effectiveness and the operational improvements of the proposed system have been experimentally validated and selective experimental results are presented to demonstrate the advantages against the conventional system.

II. Description of the Proposed Methodology

It is well known that in a power switch, as a MOSFET that is commonly used in battery cell equalization schemes, there are two conducting regions. In the *ohmic region*, the drain current has a linear response to changes of the drain-source voltage $(V_{\rm DS})$ and if the gate-source voltage $V_{\rm GS}$ exceeds a threshold value $V_{\rm th}$ $(V_{\rm GS} > V_{\rm th})$ and also $V_{\rm DS} > V_{\rm GS} - V_{\rm th}$, the MOSFET operation enters to the *saturation region*, where the drain current I_D increases with the increase of the $V_{\rm GS}$ voltage [35].

In the ohmic region, the MOSFET operates as a constant value resistor and the conduction current I_D is controlled by the drain-source voltage $V_{\rm DS}$. In the saturation region, the MOSFET behaves as a controllable current source and therefore, the conduction current I_D is controlled by the gate-source voltage $V_{\rm GS}$. By exploiting the latter feature, the MOSFET can be employed as a controllable device for smoothly regulating the equalization current for the voltage balancing of battery cells. Fig. 1 illustrates the typical characteristics of an *n*-channel MOSFET, with gray

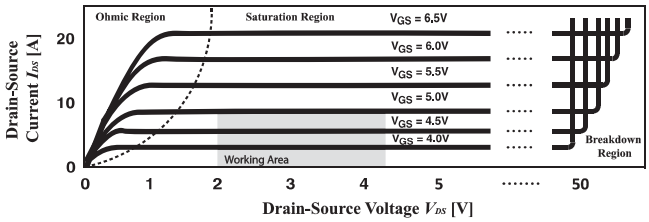

Fig. 1. Typical operation characteritics of an n-channel MOSFET. The dashed parabola indicates the boundary between ohmic and saturation regions.

denoting the operating region that the MOSFET can be utilized as a controllable device for the cell equalization.

The concept of the proposed equalization method in comparison with the conventional one is explained in Fig. 2, which shows the structure overview of the voltage equalization scheme of n battery cells. In the proposed technique of Fig. 2(a), the voltage cell equalization is attained by regulating the current I_D that is realized through the proper control of the MOSFET voltage $V_{\rm GS}$. On the contrary, in the conventional cell equalization scheme of Fig. 2(b), since a fixed-value resistance is used, the average value of the equalization current is regulated by controlling the conduction intervals of the MOSFET. Therefore, the battery cell equalization in the proposed technique is realized with a smooth current profile against the highly pulsating equalization current that is applied in the conventional method, as can be seen in the typical waveforms of Fig. 2(c) and (d), for the proposed and conventional techniques, respectively.

From the aforementioned discussion, it is concluded that the proposed cell equalization technique is faster and more effective since the cell equalization is accomplished by a current of variable amplitude, while the current of the conventional technique is strongly related to the initially selected resistor value and the control of the conduction period. In order to increase the speed and effectiveness of the cell equalization process with the conventional method, the value of the resistance should be reduced and the switching frequency should be increased. However, this results in the increase of the frequency of the pulsating current that adversely affects the performance and the lifespan of the battery. On the contrary, since a smooth equalization current is provided with the proposed technique, the battery lifespan is protected.

In the proposed cell equalization scheme of Fig. 2(a), the series-connected resistor is avoided, and thus, it is slightly cheaper and also slightly smaller in size compared with the other dissipative systems. The heat caused by the cell's equalization energy in the proposed system is dissipated through the MOSFET heat sink. Therefore, the thermal management is more effective compared with other conventional dissipative methods, in which the cell's equalization energy is dissipated through a resistor.

In case some MOSFETs fail, the equalization system continues its operation. The cell's equalization of the failed MOSFET is partially realized by the other MOSFETs of the stack, since all the cells are in serial connection. However, the accuracy in the equalization of the cells with the failed MOSFETs has been decreased. The aforementioned statement holds for both open-circuit as well as short-circuit faults of MOSFETs, since each MOSFET is protected by a fuse. Note that an advanced fault tolerance system or a backup system to replace any potential problematic MOSFETs is avoided, since it will considerably increase the cost, the complexity, and the size of the system.

III. Structure of the Proposed Control Scheme

The structure of the proposed control scheme for the battery cell equalization is shown in Fig. 3. As can be seen, a MOSFET is parallel-connected with each battery cell and a shunt resistor is used for monitoring the equalization current through the measuring unit. From the measurement of the drain-source voltage $V_{\rm DS}$ of the MOSFET and the voltage at the shunt resistor, the voltage of each battery cell V_C can be determined. The temperature sensors are used for monitoring the thermal condition of each cell. A microcontroller is utilized to accumulate the measurement signals of voltage, current, and temperature, and through a control algorithm, the correct pulsewidth-modulated (PWM) signal is determined that is provided to each drive unit to control the gate-source voltage $V_{\rm GS}$ of the MOSFET.

The schematic layout of the MOSFET drive unit is given in Fig. 4. It consists of an optocoupler to isolate the circuit from the microcontroller that provides the PWM signal and an *RC* filter to convert the PWM to analog signal that then drives the noninverting input of an operational amplifier (Op-Amp).

The proposed topology is based on the current control of the MOSFET via the feedback measurement from a shunt resistor. Specifically, the MOSFET current is regulated by controlling the voltage drop across the feedback shunt resistor, instead of directly controlling the $V_{\rm GS}$ voltage via the MOSFET curve. In other words, the concept of the control is based on a closed-loop logic, and therefore, it is not affected by the temperature variation of any of the hardware components (Op-Amp, optocoupler, etc.) nor it is based on the ideal curve of the MOSFET.

IV. Control Algorithm of the Proposed Battery Cell Equalization Method

The aim of the control system is to produce the correct PWM signal that is determined considering the battery cells performance, and then it is converted to an analog signal to drive the MOSFET for the cell equalization. For the implementation of the control system, online detection of the healthier cell in a battery stack is required that it is used as a basis to determine the voltage equalization needs of the other cells of the battery stack.

The flowchart that describes the proposed battery cell equalization technique is given in Fig. 5. It runs successively for each of the n cells of a battery stack and needs the measurements of the voltage and current of the dc link, $V_{\rm dc}$ and $I_{\rm dc}$, respectively, and the voltage and current of each ith cell, V_{c_i} and I_{c_i}, respectively. It consists of two parts, i.e., the battery cell evaluation algorithm and the equalization procedure. The cell evaluation algorithm contains three estimators, i.e., the internal resistance estimator (IRE), the capacity fade estimator (CFE), and the healthier cell estimator (HCE). The outcomes of the IRE and CFE are utilized to detect the healthier hth cell of a battery stack by the HCE, and then it is used as a reference to determine the proper gate-source voltage of each cell's MOSFET through the voltage cell equalization controller (VCEC).

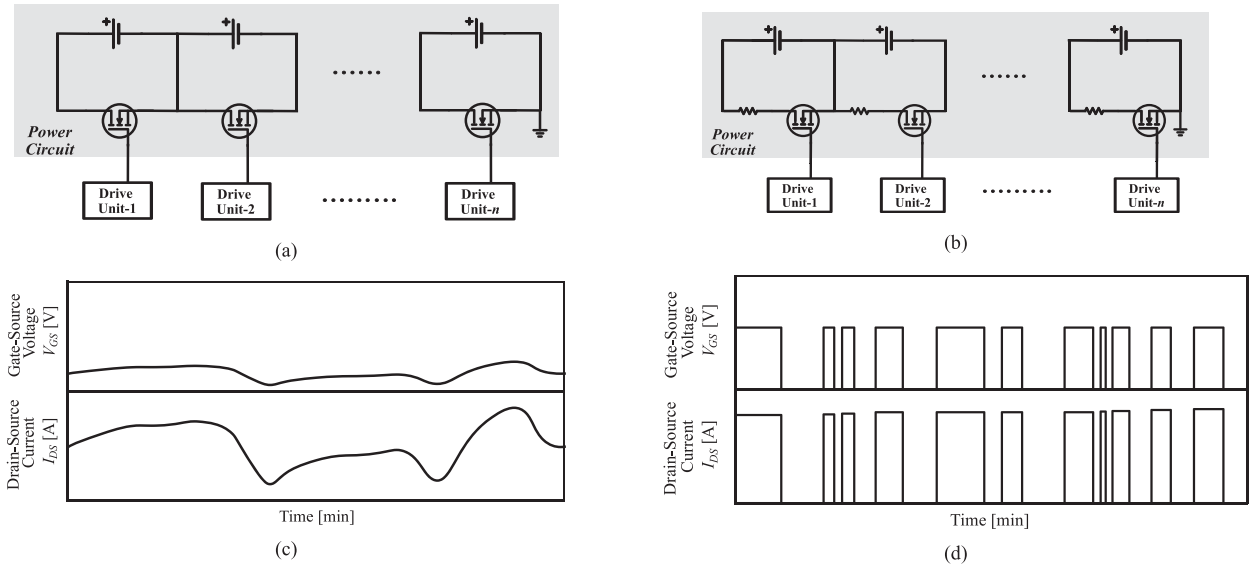

Fig. 2. Structure overview of the battery cell equalization system and typical performance waveforms. (a) and (c) proposed technique. (b) and (d) conventional technique.

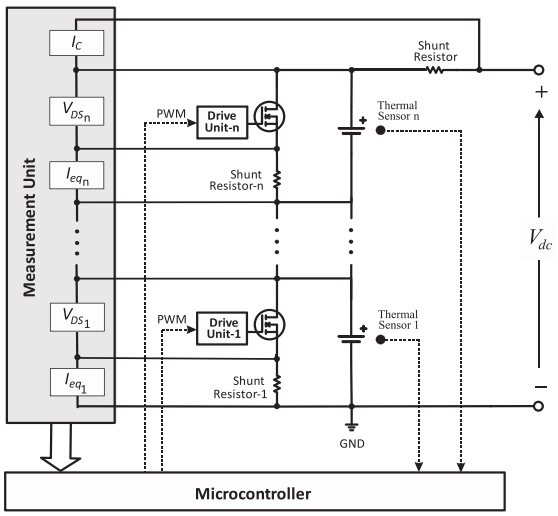

Fig. 3. Schematic layout of the BMS with the proposed energy dissipative scheme for the battery cell equalization.

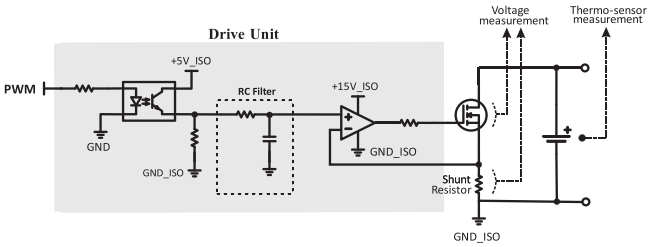

Fig. 4. Schematic layout of the electronic circuit of a MOSFET drive unit to implement the proposed energy dissipative scheme for the battery cell equalization.

The CFE and the HCE algorithms as well as the VCEC run at the same sampling frequency f_k that is selected considering the sensors accuracy, the desired equalization accuracy, and the microcontroller capacity. The IRE does not run at a fixed frequency but asynchronously, and the exact frequency is

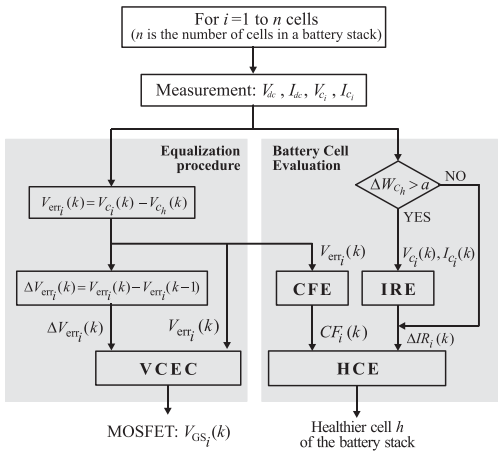

Fig. 5. Flowchart of the proposed battery cell equalization technique.

decided according to the change in the accumulated charging energy by the healthier h-cell W_{C_h}, as defined by

$$W_{C_h}(k) = \sum_{x=1}^{k} [V_{C_i}(x) I_{C_i}(x) t_k]. \tag{1}$$

Specifically, the IRE runs when ΔW_{C_h} is greater than a predetermined value a

$$\Delta W_{C_h}(k) > a \tag{2}$$

where

$$\Delta W_{C_h}(k) = \frac{W_{C_h}(k) - W_{C_h}(k-1)}{W_{C_{\text{nom}}}}. \tag{3}$$

The value of the a is decided by seeking a correct balance between the fact that a high value of the a and thus a low sampling frequency may result in low estimation of the internal resistor, while a low value of the a and thus a high sampling frequency may increase the needed time for the charging process of the battery.

The operation of the equalization algorithm of Fig. 5, for the ith cell, is as follows. From the healthier hth cell voltage of the current sampling step $V_{c_h}(k)$ and the measured voltage of the ith cell $V_{c_i}(k)$, $V_{err_i}(k)$ and $\Delta V_{err_i}(k)$ are determined. $V_{c_h}(k)$ is determined by the estimation of the HCE at the previous sampling step $k-1$ considering the outcomes of the CFE and the IRE algorithms. $V_{err_i}(k)$ is the error between the measured $V_{c_i}(k)$ and the voltage of the healthier h-cell $V_{c_h}(k)$, while $\Delta V_{err_i}(k)$ is the difference between the current and the previous step error voltage of the ith cell, $V_{err_i}(k)$, and $V_{err_i}(k-1)$, respectively. Since the initial value for the $V_{c_h}(1)$ is considered the maximum cell voltage of the battery stack, we have $V_{err_i}(0)=0$. Finally, based on $V_{err_i}(k)$ and $\Delta V_{err_i}(k)$, the VCEC provides the correct gate-source voltage $V_{GS_i}(k)$ for the equalization MOSFET of the i battery cell.

It is worth noting that a battery pack consists of a certain number of series-connected cells to meet the voltage requirements. Also, several of stacks of series-connected cells are connected in parallel to attain the energy that is required by the application. Since for practical reasons of mounting, connections, service needs, etc., the series as well as the parallel-connected cells are divided into stacks, with each stack having its own cells' equalization system. Therefore, the computational load of the microcontroller is not burdened as the number of the cells is increased, but it depends on the architectural layout of the battery pack (number of series-/parallel-connected stacks) and the number of cells per stack.

A. IRE

It is well known that the internal resistance is a determinant parameter for the cell aging estimation [36], and its increase is caused by a complex combination of various electrochemical mechanisms. Also, it depends on several operating factors, such as the depth of discharge, the charge/discharge rate, and temperature variations [37]. The basic methodology that is followed in the technical literature for the cell internal resistance estimation is based on applying current or voltage pulses in a battery cell for either online or off-line operation [38]. Then, the internal resistance is determined by the evaluation of the voltage and current waveforms utilizing a simple or more intricate model, depending on the desired accuracy, the acceptable computational complexity, and the specific needs of the application.

The equivalent circuit model that is generally used to describe the behavior of a battery is a first-order Thevenin model [39], as illustrated in Fig. 6(a). It consists of an ideal voltage source V_{OC}, an ohmic resistance R_0, and a polarization circuit $R_p - C_p$, which describes the dynamic behavior of the battery. During the discharging mode, the terminal voltage of the cell is given by

$$V_c = V_{oc} - R_o I_c - V_p \tag{4}$$

where V_p is the polarization voltage that is expressed as

$$\frac{dV_p}{dt} = \frac{I_C}{C_p} - \frac{V_p}{R_p C_p}. \tag{5}$$

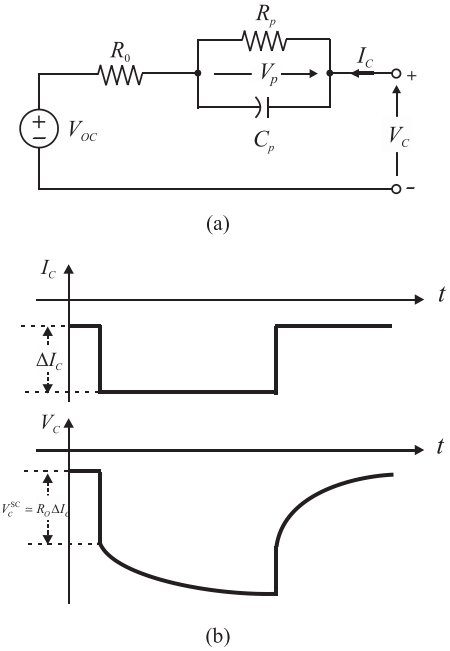

Fig. 6. (a) Battery cell equivalent circuit. (b) Battery cell response in a charging current impulse.

If a current impulse ΔI_c is imposed in a battery cell, the voltage response has the waveform of Fig. 6(b) [40]. As can be seen, the capacitance C_p initially behaves as a short circuit, and thus, the terminal voltage is approximately given by

$$\Delta V_c^{SC} \simeq R_O \Delta I_c. \tag{6}$$

The latter performance of the battery cell is utilized by the IRE algorithm to effectively determine the internal resistor.

The step current for the internal resistance estimation is provided by properly changing the duty cycle of the PWM input signal to the drive unit (see Fig. 4). The amplitude of the step current is properly selected, depending on the technical characteristics of the battery cells and the desired accuracy of the internal resistance estimation. The duration of the step current is decided by the IRE control algorithm.

The operation of the IRE algorithm is explained in the flowchart of Fig. 7(a). The IRE runs when the condition (2) is satisfied and determines the linear change of the cell voltage that is observed when the current impulse ΔI_c is applied. Specifically, it counts the linear change of the voltage for all k steps until the $\Delta V_{c_i}(k)$ becomes lower than a threshold voltage $V_{\rm th}$. When $\Delta V_{c_i}(k) < V_{\rm th}$, it means that the polarization impedance effect on the cell performance is initiated, and thus, $\Delta V_{c_i}^{SC}(k)$ becomes equal to the result of the counter of the last k-step. Therefore, the internal resistance of the k-step is

$$\mathrm{IR}_i(k) = \frac{\Delta V_{c_i}^{SC}(k)}{\Delta I_{c_i}(k)}. \tag{7}$$

Then, it is examined if the estimated internal resistance of this cell is lower than the other cells of the stack and if yes, gives

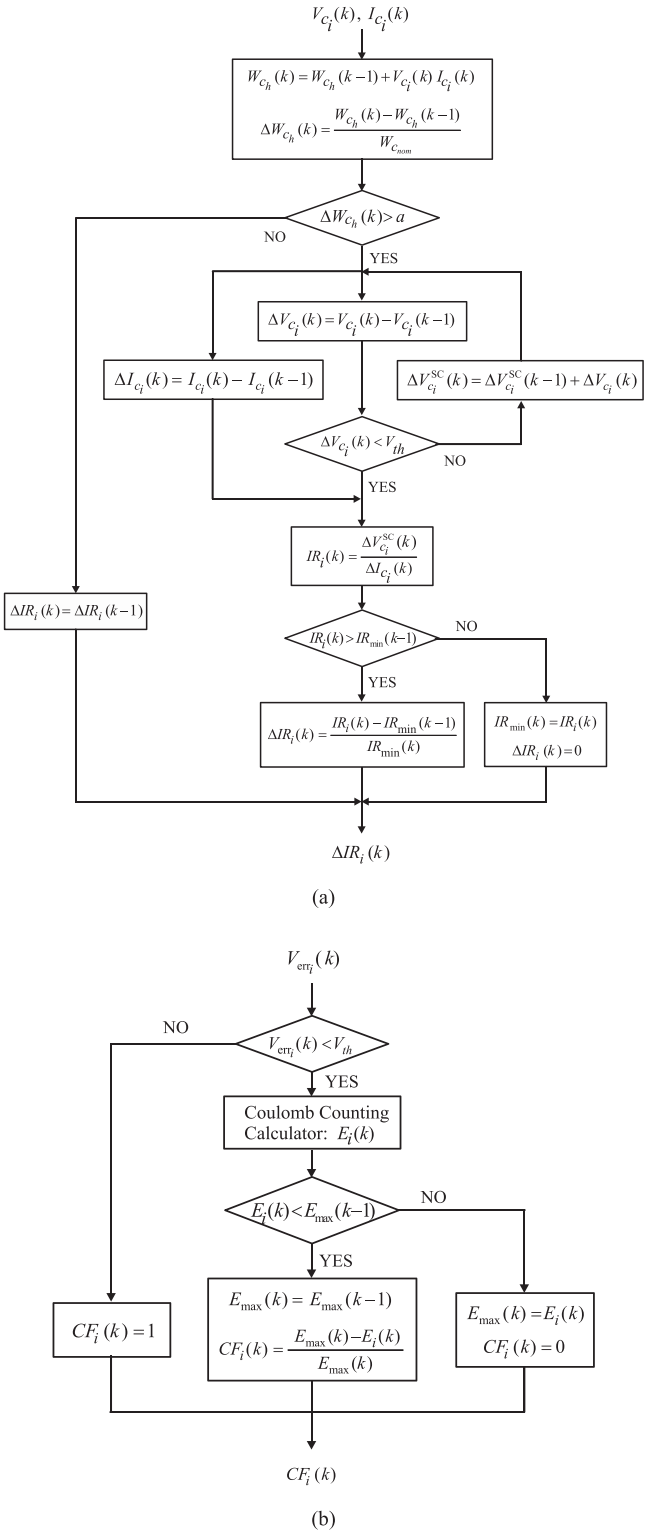

Fig. 7. Flowcharts of the (a) IRE and (b) CFE algorithms.

$\Delta \mathrm{IR}_i(k) = 0$. Otherwise, the internal resistance increase is determined with respect to the internal resistance of the healthier cell that has been determined in the $k-1$th sampling step.

In case errors in the voltage and current measurements are observed, the maximum error in the internal resistance estimation is given by [46]

$$\mathrm{IR}_i^{\mathrm{err}} = \Delta V_{\mathrm{sens}} \frac{\partial IR_i}{\partial \Delta V_{c_i}} + \Delta I_{\mathrm{sens}} \frac{\partial IR_i}{\partial \Delta I_{c_i}} = \frac{\Delta V_{\mathrm{sens}}}{\Delta I_{c_i}} + \frac{\Delta V_{c_i}}{(\Delta I_{c_i})^2} \Delta I_{\mathrm{sens}} \tag{8}$$

where ΔV_{sens} and ΔI_{sens} are the maximum error of the voltage and current measurements, respectively, due to sensors' error. If the aforementioned internal resistance estimation accuracy is not satisfactory, it can be increased by either using sensors with higher accuracy or increasing the amplitude of the step current.

It should be noted that the proposed system is not based on the estimation of the exact value of the internal resistance, but on the difference between the internal resistance estimation of the examined ith cell with that of the healthier cell. Therefore, the accuracy of the $\Delta \mathrm{IR}_i$ is not highly affected by the accuracy of the current and voltage sensors.

B. CFE

The battery capacity fade is caused due to the repetitive charging/discharging, and it is affected by almost the same operating factors, as the internal resistance increases. Several studies have been conducted aiming to effectively estimate the capacity fade of a battery. Most of them have been based on well-known techniques, such as the Kalman filter [41], neural network [42], and sliding-mode observer technique [43]. Although, the aforementioned methods can provide highly accurate results, they significantly increase the computational complexity, and consequently, they can hardly be applied in online applications. An online capacity fade estimation technique has been proposed in [44] that is based on the difference between the measured and the calculated voltage waveform of the battery, for various impulse responses that have been stored in a lookup table. However, the temperature variation has not been considered in the reference voltage waveforms, and consequently, incorrect estimations of the battery capacity fade may be resulted.

In this paper, the actual capacity fade of each battery cell is not required, since the proposed method is based on comparison between the cells' capacity fade of a battery stack. Therefore, the temperature variation does not affect the result, since the comparisons for the capacity fade are conducted at the same temperature condition for all cells. Thus, an effective CFE algorithm is introduced and the flowchart is provided in Fig. 7(b). The CFE is based on the Coulomb counting method, which calculates the integral over time of each battery cell current and, thus, estimates the charging energy. Thereby, the cell which absorbs the lower energy has the higher capacity fade. However, the aforementioned condition holds if all the cells of a battery stack have equal voltage. Hence, it is initially checked if the error between the voltage of the examined cell and the healthier cell of the battery stack is lower than a threshold value $V_{err_i}(k) < V_{\mathrm{th}}$. If this does not hold, the CF value for the examined ith cell becomes equal to 1, and for that time step, the outcome of the CFE is not considered by the HCE. If $V_{err_i}(k) < V_{\mathrm{th}}$, the Coulomb counting calculator $E_i(k)$ provides the integral of the ith cell

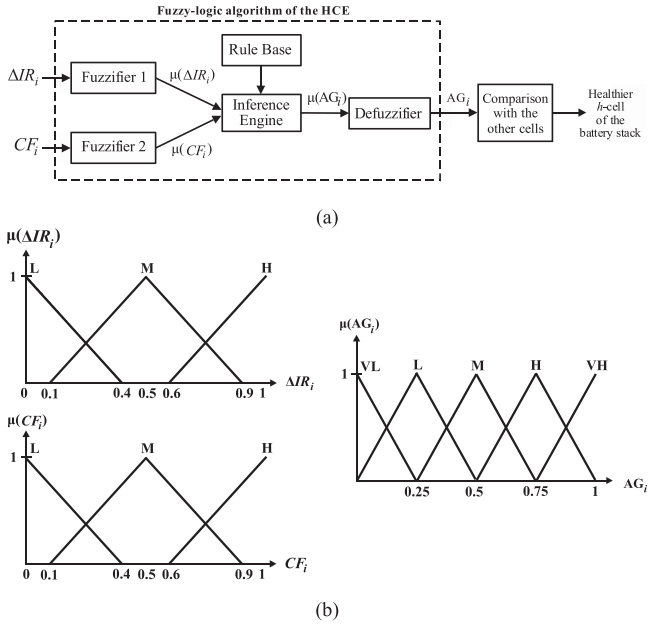

Fig. 8. HCE. (a) Block diagram. (b) Input and output membership functions.

current over time

$$E_i(k) = \sum_{x=1}^{k} I_{c_i}(k) t_k \tag{9}$$

and then $E_i(k)$ is compared with $E_i(k-1)$. If $E_i(k) < E_{\max}(k-1)$, $E_{\max}(k)$ takes the value of the previous sampling step $E_{\max}(k-1)$ and the capacity fade is given by

$$\mathrm{CF}_i(k) = \frac{E_{\max}(k) - E_i(k)}{E_{\max}(k)}. \tag{10}$$

Otherwise, it becomes $E_{max}(k) = E_i(k)$ and the capacity fade is zero. The initial value of the Coulomb counting calculator is obtained equal to zero $E_i(0) = 0$.

C. HCE

The HCE is used to detect the healthier cell that can then act as the reference cell at the equalization procedure. The HCE utilizes the *Mamdani*-type fuzzy-logic technique and the block diagram is shown in Fig. 8(a).

The concept of the fuzzy-logic algorithm of the HCE is to provide the normalized aging rate of each battery cell considering the capacity fade with respect to the internal resistance rate. Thus, inputs to the HCE is the internal resistance growth $\Delta\mathrm{IR}_i$ and the capacity fade CF_i of each ith cell that are determined by the IRE and the CFE, respectively. The HCE gives the aging (AG) of each cell of the battery stack with respect to the healthier hth cell estimated at the $(k-1)$th sampling step. Then, by comparing the AG of all the cells, it is determined that the healthier hth cell is at the kth sampling step.

The membership functions of the HCE are shown in Fig. 8(b), and the fuzzy rules are given in Table I. The input fuzzy variables are $\mathrm{L} = \mathrm{Low}$, $\mathrm{M} = \mathrm{Medium}$, and $\mathrm{H} = \mathrm{High}$, while the output fuzzy variables are $\mathrm{VL} = \mathrm{Very\,Low}$, $\mathrm{L} = \mathrm{Low}$, $\mathrm{M} = \mathrm{Medium}$, $\mathrm{H} = \mathrm{High}$, and $\mathrm{VH} = \mathrm{Very\,High}$.

TABLE I
FUZZY RULES OF THE HCE

CF_i \ ΔIR_i	L	M	H
L	VL	L	M
M	L	M	H
H	M	H	VH

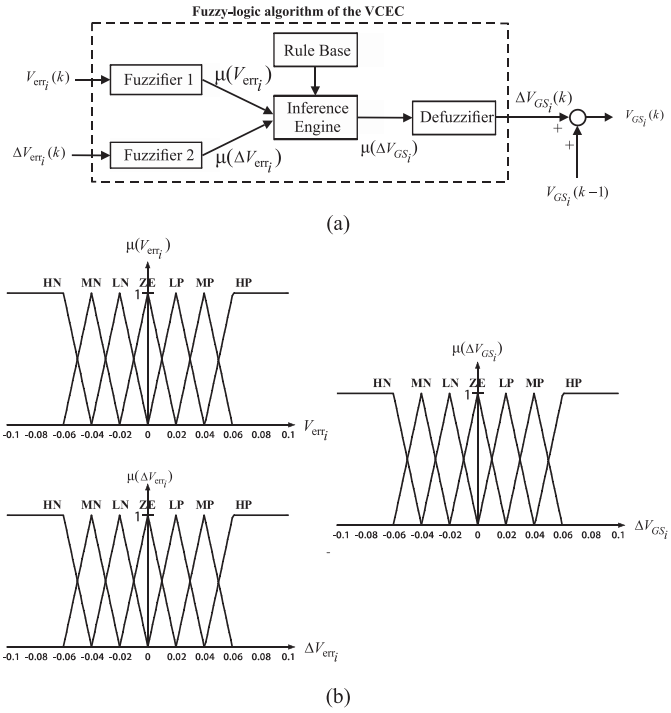

Fig. 9. VCEC. (a) Block diagram. (b) Input and output membership functions.

TABLE II
FUZZY RULES OF THE V CEC

$\Delta V_{\mathrm{dif}_i}$ \ V_{dif_i}	HN	MN	LN	ZE	LP	MP	HP
HN	HN	MN	MN	LN	LN	LN	ZE
MN	NM	NM	NS	NS	NS	ZE	ZE
LN	MN	MN	LN	LN	ZE	LP	MP
ZE	HN	MN	LN	ZE	LP	MP	MP
LP	LN	LN	ZE	LP	LP	MP	MP
MP	LN	ZE	LP	LP	LP	MP	MP
HP	ZE	LP	LP	MP	MP	HP	HP

D. VCEC

The VCEC determines the proper gate-source voltage V_{GS_i} of the ith MOSFET by considering $V_{err_i}(k)$ and $\Delta V_{err_i}(k)$.

A *Mamdani*-type fuzzy-logic controller is introduced that consists of similar parts, as the HCE, and the block diagram is shown in Fig. 9(a). The concept of the fuzzy-logic algorithm of the VCEC is to determine the alteration that is needed in the V_{GS} of the ith MOSFET by considering $V_{err_i}(k)$ and its variation with respect to the previous sampling time $\Delta V_{err_i}(k)$. The membership functions for the VCEC are shown in Fig. 9(b), and the construction of the fuzzy rules is given in Table II. The input and the output fuzzy variables are divided

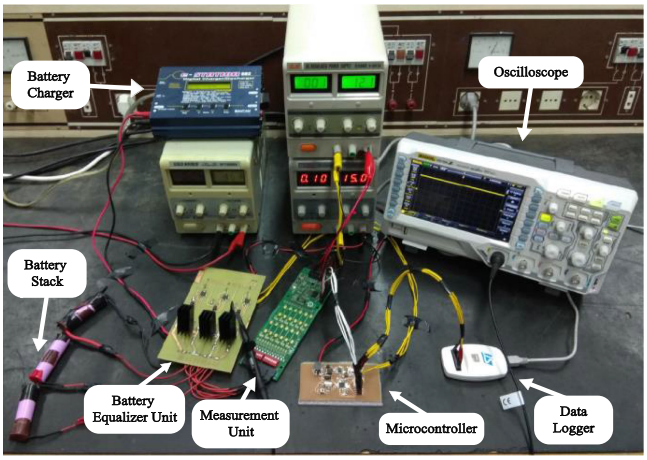

Fig. 10. Layout of the experimental system with the proposed battery cell equalization technique.

into HN = High Negative, MN = Medium Negative, LN = Low Negative, ZE = Zero, LP = Low Positive, MP = Medium Positive, and HP = High Positive.

V. Experimental Results

The theoretical considerations of this paper have been experimentally verified on a BSS with three Li-ion cells (Samsung ICR 18650-26J), as shown in Fig. 10. The working voltage range of each battery cell is $2.75-4.2$ V, and the maximum charging current is 2.6 A. The control software is realized on the microcontroller STM32F103C8T6 and the measurement unit LTC6803 is used to measure the voltages and currents. The temperature monitoring is implemented with LTC6803, and the thermistors are placed on the battery tabs. The temperature measurement signal is transferred to the microcontroller by means of the serial peripheral interface (SPI) communication technique.

The frequency of the PWM signal provided by the microcontroller is 10 kHz and the cut-off frequency of the *RC* low-pass filter is selected equal to 58.9 Hz (the *R* and the *C* components are 2.7 kΩ and 1 μF, respectively). The parameter a of the IRE is 0.2, and the threshold voltage $V_{\rm th}$ for the IRE and CFE algorithms is 0.02 V.

The three initially unused battery cells have been undergone separately to consecutive charging/discharging cycles of different number of cycles for each cell, in order to form a layout of battery cells of different operating characteristics (i.e., 10 cycles at Cell-1, 40 cycles at Cell-2, and 70 cycles at Cell-3). A commercial charger in constant-current-constant-voltage (CC-CV) operating mode has been used. In each charging/discharging cycle, each cell is fully charged (100% of the nominal SoC) and then is discharged up to 40% of the nominal SoC in a power resistor. Each of the charging/discharging cycles mentioned earlier has been realized with constant current (CC) of 1.3 A.

The CC-CV operating mode of the charger is conducted as follows: It initially operates in the CC mode of 1.3 A $(0.5\,\text{C})$, and when the maximum voltage of 4.2 V is reached, the charger turns to constant voltage (CV) mode and the current exponentially decreases to zero. When the aforementioned preparation procedure has been completed, the parameters of each cell have been determined with the pulse current method, as per [39] and [45]. The parameters of each cell are reported in Table III.

TABLE III
Measured Parameters of the Battery Cells

Par. / Cell No	Capacity (Ah)	Internal Resistance (mΩ)
Cell-1	2.58	54
Cell-2	2.50	61
Cell-3	2.42	67

The experiments for validating the effectiveness and the operating improvements of the proposed cell equalization method have been conducted by using the same charger in the CC-CV mode. The three cells are connected in series, as in the schematic layout of Fig. 3, and thus, the charger turns from CC to CV when the total voltage of the stack reaches 12.6 V.

Fig. 11 illustrates the performance of the proposed cell equalization system by using the MOSFET as a controllable source, during the CC-CV charging procedure. Fig. 12 illustrates the performance of the conventional dissipative system by using a series resistor of 16 Ω and applying the proposed cell equalization technique of Fig. 11. Thus, from the comparison between Figs. 11 and 12, the benefits of using the MOSFET as a controllable source can be validated. Fig. 13 shows the performance of the conventional dissipative system by using a series resistor of 16 Ω, as in Fig. 12, and employing the cell voltage as control variable for the equalization. Thus, the comparison of Figs. 13 with 11 verifies the advantages of both the proposed cell equalization technique and the usage of MOSFET as a controllable source.

The kth sampling frequency for all the examined cases is 1 kHz, while the IRE algorithm runs asynchronously depending on the condition (2). It should be noted that in the proposed system of Fig. 11, the MOSFET does not switched ON/OFF, since the equalization current is controlled by the equalization algorithm of Fig. 5. Therefore, 1 kHz is the maximum control frequency, while the actual operating frequency depends on the output of the equalization algorithm. The same holds for Fig. 12. In this case, 1 kHz is the maximum switching frequency for the MOSFET. Finally, 1 kHz is also the maximum switching frequency for the case of Fig. 13, while the exact switching frequency depends on the equalization algorithm, where the cell voltage is employed as a control variable.

In Fig. 11, Cell-1 has been detected by the IRE and CFE that it has the lower internal resistance and capacity fade, respectively, and thus, it is considered as a healthier cell by the HCE. Therefore, Cell-1 acts as the reference for the voltage equalization of Cell-2 and Cell-3, and as can be seen, smooth cell equalization is attained.

The resolution of the LTC6803 sensor, which has been used in the experiments, is 12 bit, and consequently, the maximum resolution errors in the voltage and current measurements

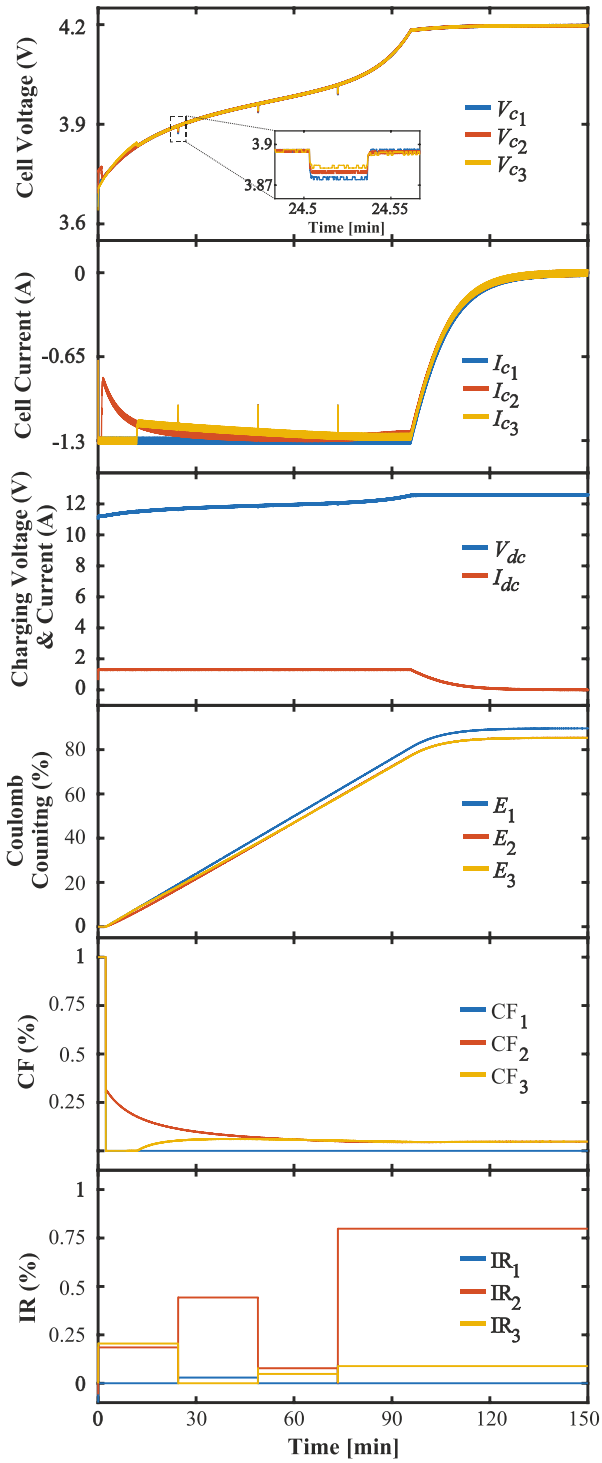

Fig. 11. Experimental results of the performance of the proposed cell equalization system by using the MOSFET as a controllable source, during the CC-CV charging procedure.

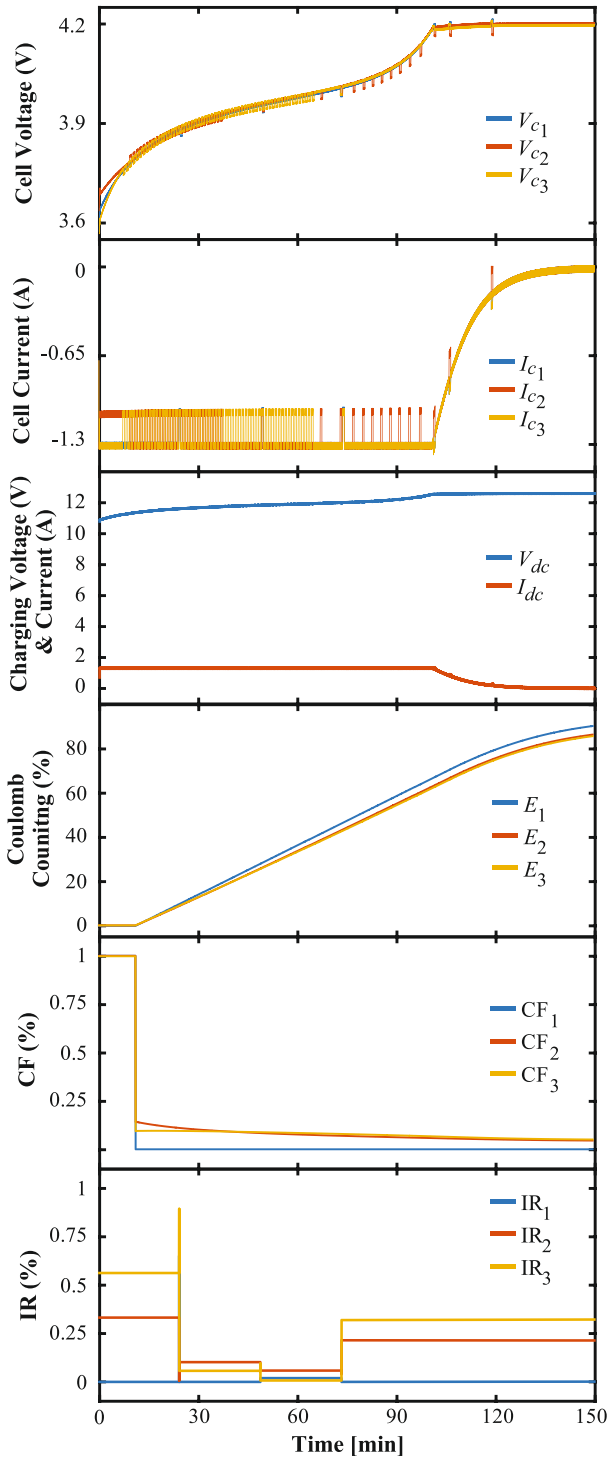

Fig. 12. Experimental results of the performance of the conventional dissipative system during the CC-CV charging procedure by using a series resistor of 16 Ω and applying the proposed cell equalization technique.

are $\Delta V_{\text{sens}} = \pm 0.61\,\text{mV}$ and $\Delta I_{\text{sens}} = \pm 3.05\,\text{mA}$. From (8), it is concluded that the internal resistance resolution error is $\text{IR}_i^{\text{err}} = 2.5\,\text{m}\Omega$ and considering that the equivalent internal resistance of the examined ICR 18650-26J battery cell is 50 mΩ [47], IR_i^{err} mentioned earlier corresponds to a maximum error of 5.09%. From the experimental results of Fig. 11, it can be concluded that the cells' equalization is satisfactory with the aforementioned sensor resolution accuracy. However, if improved accuracy is required, a sensor with higher resolution could be used. For example, if we use the LTC6811 sensor such that the resolution is 16 bit, the maximum voltage and current resolution errors are $\Delta V_{\text{sens}} = \pm 0.038\,\text{mV}$ and $\Delta I_{\text{sens}} = \pm 0.19\,\text{mA}$, respectively, and therefore, the internal resistance resolution error IR_i^{err} reduces to 0.16 mΩ that corresponds to an

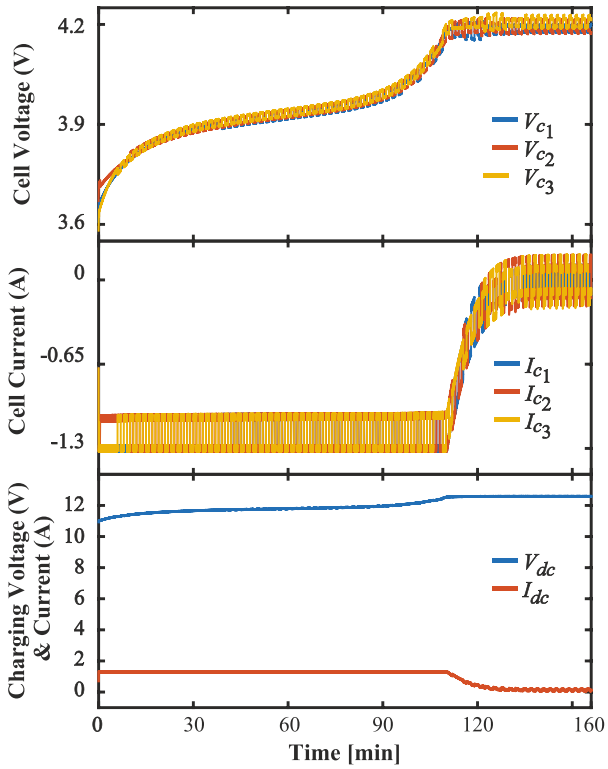

Fig. 13. Experimental results of the performance of the conventional dissipative system during the CC-CV charging procedure by using a series resistor of 16 Ω and the cell voltage as control variable for the equalization.

error of 0.32%. If the amplitude of the step current increases to 1 A and the sensor LTC6811 is used, $\mathrm{IR}_i^{\mathrm{err}}$ internal resistance resolution error further reduces to 0.041 mΩ that corresponds to an error of 0.08%.

In Fig. 12, similar control action, as in Fig. 11, is carried out and Cell-1 is used as the reference cell. Specifically, the internal resistance and the capacity fade have been estimated by employing the IRE and CFE algorithms, and thus, a similar control technique, as in the proposed system of Fig. 11, is employed for controlling the MOSFET. Therefore, the switching frequency is almost the same for both Figs. 11 and 12 (please compare the cell voltage diagrams of those figures), and thus, almost the same switching and conducting losses are observed, as well as almost the same efficiency. However, since the equalization is conducted through the series-connected resistor of 16 Ω by switching the MOSFET ON/OFF, the equalization current is highly pulsating that stresses the battery cells and adversely affects their lifespan (please compare the diagrams of the cells' current of the aforementioned figures). Therefore, more effective and smoother cells' equalization is achieved in Fig. 11, and consequently, the procedure is faster than Fig. 12 (it lasts 100 min for Fig. 12 against 93 min of Fig. 11).

In Fig. 13, the cell equalization is realized by controlling the cells' voltage through the MOSFET and the series-connected resistor of 16 Ω. Consequently, a more highly pulsating current and a more slower equalization procedure are observed compared with both Figs. 11 and 12 (the equalization process lasts

TABLE IV
EVALUATION OF THE CELLS' EQUALIZATION METHOD

Valuation Criteria \ Equalization Methods	Dissipative methods: Proposed method (uses the MOSFET as a controllable source) (Fig. 11)	Dissipative methods: Conventional method (the proposed equalization technique with a series resistor) (Fig. 12)	Dissipative methods: Conventional method (series resistor, controllable variable is the cell voltage) (Fig. 13)	Non-dissipative methods
Efficiency	**	**	*	****
Low complexity	****	***	***	*
Cost-effectiveness	****	**	**	*
Protection of the cell's lifespan	****	**	*	****
Lower size	****	***	***	*
Duration of the equalization	****	***	**	***
Thermal management	***	*	*	****
Reliability	****	***	***	*

108 min for Fig. 13 against 100 min of Fig. 12 and 93 min of Fig. 11). Moreover, since the charging process stops abruptly any time that a cell needs equalization, the system absorbs more energy by the charger that is dissipated to the series resistor, and consequently, the efficiency is lower than the proposed system.

It should be noted that if it is desirable to reduce the frequency of the pulsating current in the equalization process of Figs. 12 and 13, the value of the series-connected resistor should be reduced. However, this will increase the amplitude of the pulsating current and the needed time for the cells' equalization.

From the earlier discussion, it is concluded that the proposed method provides smooth and fast voltage equalization of the battery cells compared with the conventional dissipative methods. Moreover, it is highly reliable and cost effective compared with the nondissipative methods. The aforementioned conclusions are summarized in Table IV (the higher number of asterisks denotes higher score in the evaluation of the criteria).

VI. CONCLUSION

In this paper, an active battery cell equalization technique has been proposed that improves the battery performance and protects its lifespan. The suggested control technique regulates the charging current of each cell of a battery stack through the proper regulation of the gate-source voltage of the parallel-connected MOSFET of each cell. The above procedure is accomplished by estimating the healthier cell of the battery stack through the IRE and CFE algorithms and then, the healthier cell acts as a reference for the voltage equalization of the other cells. Therefore, smooth and fast cell equalization is attained compared to the conventional dissipative method. Moreover, it is highly reliable and cost effective compared with the nondissipative methods. The high effectiveness and the practicality in the implementation of the proposed cell equalization technique have been experimentally validated. Several experimental results in comparison with the conventional energy dissipative systems have been presented to demonstrate the advantages of the proposed system.

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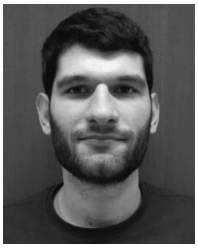

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