Balanced Power Device Currents Based Modulation Strategy for Full-Bridge Three-Level DC/DC Converter

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***Abstract*—This paper proposes a new modulation strategy with balanced power device currents for the full-bridge three-level dc/dc converter. The proposed modulation strategy has two working patterns, which cannot only realize zero-voltage switching (ZVS) but also satisfy the wide input voltage range. More significantly, the two working patterns of the proposed strategy can balance the currents both among the power switches and clamping diodes in comparison with the conventional control strategies which cause current imbalances among the power switches and clamping diodes. Consequently, the proposed strategy can balance the thermal stresses among the power switches and clamping diodes, which would, thus, improve the converter's reliability. Finally, the experimental results, obtained using a built 1.5-kW experimental prototype, verify almost zero current difference and zero thermal-stress difference among the inner power switches, outer power switches, and clamping diodes under the proposed strategy.**

***Index Terms*—Balanced power device currents, full-bridge three-level (FBTL) dc/dc converter, wide input voltage range, zero-voltage switching (ZVS).**

I. Introduction

THE three-level (TL) dc/dc converter is attractive for high voltage applications, such as three-phase power-factor correction systems, renewable energy systems, electric vehicle charging systems, and distributed power systems [1]–[5], because the voltage stresses on the power switches are only half of the input voltage ($V_{\rm in}/2$) in the TL dc/dc converter [6], [7]. So far, many studies about the TL dc/dc converter have been carried out [8]–[20]. In [8], a zero-voltage and zero-current switching half-bridge (HB) TL dc/dc converter was proposed, in which the phase-shift control strategy can be applied into the TL dc/dc converter by adding a flying capacitor in the primary side. Based on [8], a TL dc/dc converter with auxiliary circuit was proposed to reduce the circulating current for the converter's efficiency improvement [9]. An improved zero-voltage switching (ZVS) dc/dc converter with series-connected transformers was proposed in [10], which can both realize the ZVS within nearly entire load range and balance the output currents. In [11], a novel ZVS TL dc/dc converter was proposed, which features a simple and compact circuit structure by removing two clamped diodes and connecting the mid-points of the input capacitors and switching pairs. Based on [11], four types of new pulsewidth modulated TL dc/dc converters with wide-range soft-switching are proposed for industrial applications in [12], and a new ZVS modulation strategy with input capacitors' current balancing control strategy was proposed in [13] for the TL d/dc converter. Additionally, a secondary-side phase-shift-controlled ZVS dc/dc converter with wide voltage gain was proposed in [14] for high voltage applications, which can effectively reduce the circulating current.

The above studies mainly focus on the HB TL dc/dc converters, but they are not suitable for high power electronic systems because of the higher current stresses on the power switches in comparison with the full-bridge (FB) dc/dc converters [21]–[23]. In addition, the modulation strategy of the FB circuit structure is different from that of the HB circuit structure and even more complex because of more power devices in comparison with the HB circuit structure. In [15] and [16], two hybrid ZVS full-bridge three-level (FBTL) dc/dc converters were proposed for high power applications, which are both composed of a TL leg and a two-level leg in the primary side. A zero-voltage and zero-current switching FBTL with reduced circulating current and an improved FBTL dc/dc converter with input capacitors' voltage balancing control strategy were proposed in [17] and [18] respectively, but they cannot satisfy wide input voltage range. Two modulation strategies, chopping phase-shift (CPS) strategy and double phase-shift (DPS) strategy, were proposed in [19] and [20], respectively, for the FBTL dc/dc converter, which can both satisfy the wide input voltage range.

When it comes to the modulation strategies for FBTL dc/dc converters, there are mainly three objectives that the previous research aimed to achieve: 1) soft switching; 2) wide input voltage range; and 3) reliability of input capacitors (capacitors' voltages and currents balancing methods). However, there are few studies that pay attention on the current balancing among the power devices in the FBTL dc/dc converter, which is closely related with

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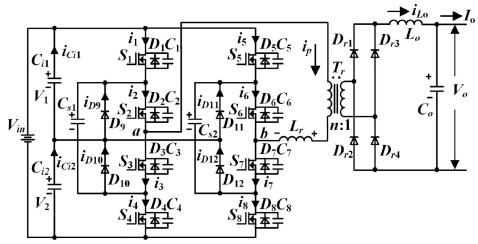


Fig. 1. Circuit structure of FBTL dc/dc converter.

the reliability of the converter because the unbalanced currents among the power devices would result in the power-loss imbalances and thermal-stress imbalances among the power devices [24]–[26].

In this paper, the issue of current imbalance in power devices under the conventional modulation strategies in the FBTL dc/dc converter is pointed out and analyzed in detailed. Then, a new modulation strategy is proposed for the FBTL dc/dc converter to eliminate these current imbalances. In addition, the proposed strategy is composed of two working patterns for satisfying the wide input voltage range. These two working patterns can both realize ZVS and have the ability of seamless transition. More importantly, the two working patterns can both balance the currents among power switches and clamping diodes. Accordingly, the proposed strategy would balance the power losses and thermal stresses among the power switches and clamping diodes, which is helpful for improving the reliability of the converter. The performances of the FBTL dc/dc converter under the proposed strategy are analyzed in detail and verified using experimental results.

This paper is organized as follows. Section II analyzes the current-imbalance issue in the power devices under the conventional strategies. Section III introduces the proposed modulation strategy and analyzes the operation principles of the proposed strategy in detail. Section IV presents the detailed analysis about the characteristics and performances of the proposed strategy. Section V demonstrates the experimental results to verify the proposed strategy. Finally, the main contributions of this paper are summarized in Section VI.

II. Current-Imbalance Issue Under Conventional Strategies

Fig. 1 shows the circuit structure of the FBTL dc/dc converter.

In Fig. 1, on the primary side, C_{i1} and C_{i2} are two input capacitors, which split the input voltage $V_{\rm in}$ into V_1 and V_2; S_1, S_4, S_5, and S_8 are outer switches, and D_1, D_4, D_5, and D_8 are their body or paralleled diodes; S_2, S_3, S_6, and S_7 are inner power switches, and D_2, D_3, D_6, and D_7 are their body or paralleled diodes; C_1–C_8 are the parasitic capacitors of S_1–S_8; C_{s1} and C_{s2} are two flying capacitors; D_9–D_{12} are four clamping diodes; T_r is the isolation transformer; L_r is the leakage inductor of T_r plus added inductor in series with T_r. On the secondary side, D_{r1}–D_{r4} are four output rectifier diodes; L_o and C_o are output filter inductor and output filter capacitor, respectively. In addition, $V_{\rm in}$ is the input voltage; V_1 and V_2 are the voltage on the input capacitors C_{i1} and C_{i2}; i_{Ci1} and i_{Ci2} are the currents on the input capacitor C_{i1} and C_{i2}; V_{ab} is the voltage between point a and b; i_p is the primary current of the transformer T_r; i_1–i_8 are the currents on the primary power switches (S_1, D_1)–(S_1, D_8); i_{D9}–i_{D12} are the currents on the clamping diodes D_9–D_{12}; n is the turns ratio of the transformer T_r; i_{Lo} is the current through the output filter inductor L_o; V_o and I_o are the output voltage and output current, respectively.

In order to simplify the following analysis, the following assumptions are made.

1) All the switches and diodes are ideal.
2) The two input capacitors C_{i1} and C_{i2} are large enough to be considered as two voltage sources with the values of the half of the input voltage ($V_{\rm in}$/2).
3) The two flying capacitors C_{s1} and C_{s2} are considered as two voltage sources with the values of $V_{\rm in}$/2 but only provide charging and discharging paths for the switches' parasitic capacitors.
4) The output filter inductor L_o is large enough to be considered as a constant current source.
5) The parasitic capacitors of S_1–S_8 are the same, which means $C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C_7 = C_8 = C_j$.

Fig. 2 presents the currents through the power switches (i_1–i_8) and currents through the clamping diodes (i_{D9}–i_{D12}) under the DPS strategy as an example to explain the current-imbalance issue under the conventional modulation strategies, in which d_{rv1}–d_{rv8} are the driving signals for power switches S_1–S_8; T_s is one switching period; α_1, α_2, and θ are phase-shift delays. It needs to be mentioned that currents i_1–i_8 and i_{D9}–i_{D12} under the CPS strategy are the same as that under the DPS strategy.

From Fig. 2, the following can be observed.

1) For the currents on the outer power switches (i_1, i_4, i_5, and i_8) as marked by red color, i_1 and i_4 are the same besides 180° phase difference; i_5 and i_8 are the same besides 180° phase difference; i_5 and i_8 are higher than i_1 and i_4.
2) For the currents on the inner power switches (i_2, i_3, i_6, and i_7) as marked by blue color, i_2 and i_3 are the same besides 180° phase difference; i_6 and i_7 are the same besides 180° phase difference; the root mean square (rms) values of i_2, i_3, i_6, and i_7 are the same, but the average value of i_2 and i_3 are smaller than that of i_6 and i_7.
3) For the currents on the clamping diodes (i_{D9}, i_{D10}, i_{D11}, and i_{D12}) as marked by orange color, i_{D9} and i_{D10} are the same besides 180° phase difference; i_{D11} and i_{D12} are zero, so i_{D9}, i_{D10} are higher than i_{D11}, i_{D12}.

Therefore, on the basis of the above analysis, it can be concluded that the currents among the outer power switches (i_1, i_4, i_5, and i_8), inner power switches (i_2, i_3, i_6, and i_7), and clamping diodes (i_{D9}, i_{D10}, i_{D11}, and i_{D12}) are unbalanced under the conventional strategies.

Table I presents the calculation equations about the rms and average values of i_1–i_8 and i_{D9}–i_{D12} under the DPS strategy according to Fig. 2.

III. Proposed Modulation Strategy

In order to eliminate the current imbalances among the power devices under the conventional strategies, a new modulation strategy with balanced power device currents is proposed for the FBTL dc/dc converter.

TABLE I
THEORETICAL EQUATIONS ABOUT RMS AND AVERAGE VALUES OF CURRENTS ON PRIMARY POWER DEVICES UNDER THE DPS STRATEGY

		Three-level mode	Two-level mode
i_1, i_4	RMS value	$\sqrt{\frac{I_o^2\cdot(T_s-2\cdot\alpha_1)}{2\cdot n^2\cdot T_s}-\frac{4\cdot L_r\cdot I_o^3}{3\cdot V_{in}\cdot n^3\cdot T_s}}$	$\sqrt{\frac{I_o^2\cdot\alpha_2}{n^2\cdot T_s}+\frac{L_r\cdot I_o^3}{3\cdot V_{in}\cdot n^3\cdot T_s}}$
	Average value	$\frac{I_o\cdot(T_s-2\cdot\alpha_1-4\cdot\alpha_2)}{2\cdot n\cdot T_s}-\frac{2\cdot L_r\cdot I_o^2}{V_{in}\cdot n^2\cdot T_s}$	$-\frac{I_o\cdot\alpha_2}{n\cdot T_s}-\frac{L_r\cdot I_o^2}{2\cdot V_{in}\cdot n^2\cdot T_s}$
i_5, i_8	RMS value	$\sqrt{\frac{I_o^2}{2\cdot n^2}-\frac{4\cdot L_r\cdot I_o^3}{3\cdot V_{in}\cdot n^3\cdot T_s}}$	$\sqrt{\frac{I_o^2}{2\cdot n^2}-\frac{2\cdot L_r\cdot I_o^3}{V_{in}\cdot n^3\cdot T_s}}$
	Average value	$\frac{I_o}{2\cdot n}-\frac{2\cdot L_r\cdot I_o^2}{V_{in}\cdot n^2\cdot T_s}$	$\frac{I_o}{2\cdot n}-\frac{5\cdot L_r\cdot I_o^2}{2\cdot V_{in}\cdot n^2\cdot T_s}$
i_2, i_3	RMS value	$\sqrt{\frac{I_o^2}{2\cdot n^2}-\frac{4\cdot L_r\cdot I_o^3}{3\cdot V_{in}\cdot n^3\cdot T_s}}$	$\sqrt{\frac{I_o^2}{2\cdot n^2}-\frac{2\cdot L_r\cdot I_o^3}{V_{in}\cdot n^3\cdot T_s}}$
	Average value	$\frac{I_o\cdot(T_s-4\cdot\alpha_2)}{2\cdot n\cdot T_s}-\frac{2\cdot L_r\cdot I_o^2}{V_{in}\cdot n^2\cdot T_s}$	$\frac{I_o\cdot(T_s-4\cdot\alpha_2)}{2\cdot n\cdot T_s}-\frac{5\cdot L_r\cdot I_o^2}{2\cdot V_{in}\cdot n^2\cdot T_s}$
i_6, i_7	RMS value	$\sqrt{\frac{I_o^2}{2\cdot n^2}-\frac{4\cdot L_r\cdot I_o^3}{3\cdot V_{in}\cdot n^3\cdot T_s}}$	$\sqrt{\frac{I_o^2}{2\cdot n^2}-\frac{2\cdot L_r\cdot I_o^3}{V_{in}\cdot n^3\cdot T_s}}$
	Average value	$\frac{I_o}{2\cdot n}-\frac{2\cdot L_r\cdot I_o^2}{V_{in}\cdot n^2\cdot T_s}$	$\frac{I_o}{2\cdot n}-\frac{5\cdot L_r\cdot I_o^2}{2\cdot V_{in}\cdot n^2\cdot T_s}$
i_{D9}, i_{D10}	RMS value	$\frac{I_o}{n}\sqrt{\frac{\alpha_1}{T_s}}$	$\sqrt{\frac{I_o^2\cdot(T_s-2\cdot\alpha_2)}{2\cdot n^2\cdot T_s}-\frac{7\cdot L_r\cdot I_o^3}{3\cdot V_{in}\cdot n^3\cdot T_s}}$
	Average value	$\frac{I_o\cdot\alpha_1}{n\cdot T_s}$	$\frac{I_o\cdot(T_s-2\cdot\alpha_2)}{2\cdot n\cdot T_s}-\frac{2\cdot L_r\cdot I_o^2}{V_{in}\cdot n^2\cdot T_s}$
i_{D11}, i_{D12}	RMS value	0	0
	Average value	0	0

A similar current balancing method was proposed in [13], but it is for the HB TL dc/dc converter. Comparing between the HB TL dc/dc converter and the FBTL dc/dc converter, the FBTL dc/dc converter is more suitable for high power applications, and the modulation strategies between the HB TL dc/dc converter and the FBTL dc/dc converter are quite different. The modulation strategy of the FBTL dc/dc converter is more complex than that of the HB TL dc/dc converter not only because the circuit structure of the FBTL dc/dc converter is more complex but also because the modulation strategy for the FBTL dc/dc converter normally needs to satisfy the wide input voltage range. In order to satisfy the wide input voltage range, the proposed modulation strategy is composed of two working patterns. More significantly, these two working patterns can effectively balance the currents among the power devices, and the transition between these two working patterns is seamless.

Fig. 3(a) and (b) shows the operation principles of the two working patterns, respectively, in which d_{rv1}–d_{rv8} are the driving signals of power switches S_1–S_8; d_1 and d_2 are the duty ratios in one switching period, T_s.

1) *Working pattern I:* is used for the low input voltage. In working pattern I, the output voltage V_o is adjusted by changing the duty ratio, d_1. Working pattern I operates by swapping the duty ratios for switching pairs (S_1, S_8) and (S_4, S_5), respectively, in every switching period to make the currents through the power devices balanced in every two switching periods. Therefore, working pattern I has two operation modes, as marked in Fig. 3(a), as follows: in mode I as [t_3–t_{15}], the duty ratio of d_{rv1} and d_{rv4} are both d_1, and the duty ratio of d_{rv2}, d_{rv3}, d_{rv5}, d_{rv6}, d_{rv7}, and d_{rv8} are all 0.5 if neglecting the dead time; but, in mode II as [t_{15}–t_{27}], the duty ratio of d_{rv5} and d_{rv8} are both d_1, and the duty ratio of d_{rv1}, d_{rv2}, d_{rv3}, d_{rv4}, d_{rv6}, and d_{rv7} are all 0.5 if neglecting the dead time. By adjusting the value of d_1, the time length of the third-level voltages ($V_{\rm in}$ and $-V_{\rm in}$), as marked by red color in Fig. 3(a), can be changed, which would, thus, change the output voltage V_o. For instance, if upon reducing d_1, the time length of the third-level voltages ($V_{\rm in}$ and $-V_{\rm in}$) would decrease, which means that the output voltage V_o would decrease.

2) *Working pattern II:* is used for high input voltage when d_1 reduces to zero. In working pattern II, the output voltage V_o is adjusted by changing the duty ratio, d_2. Working pattern II operates by swapping the duty ratios for switching pairs (S_1, S_8), (S_2, S_7), (S_3, S_6), and (S_4, S_5), respectively, in every switching period to balance the currents through the power devices in every two switching periods. Therefore, working pattern II also has two operation modes, as marked in Fig. 3(b), as follows: in mode I as [t_3–t_{17}], the duty ratios of d_{rv1} and d_{rv4} are both 0, the duty ratio of d_{rv2} and d_{rv3} both d_2, and the duty ratio of d_{rv5}, d_{rv6}, d_{rv7}, and d_{rv8} are all 0.5 if neglecting the dead time; but, in mode II as [t_{17}–t_{31}], the duty ratio of d_{rv5} and d_{rv8} are both 0, the duty ratio of d_{rv6} and d_{rv7} both d_2, and the duty ratio of d_{rv1}, d_{rv2}, d_{rv3}, and d_{rv4} are all 0.5 if neglecting the dead time. By adjusting the value of d_2, the time length of the second-level voltages ($V_{\rm in}$/2 and $-V_{\rm in}$/2), as marked by blue color in Fig. 3(b), can be changed, which would,

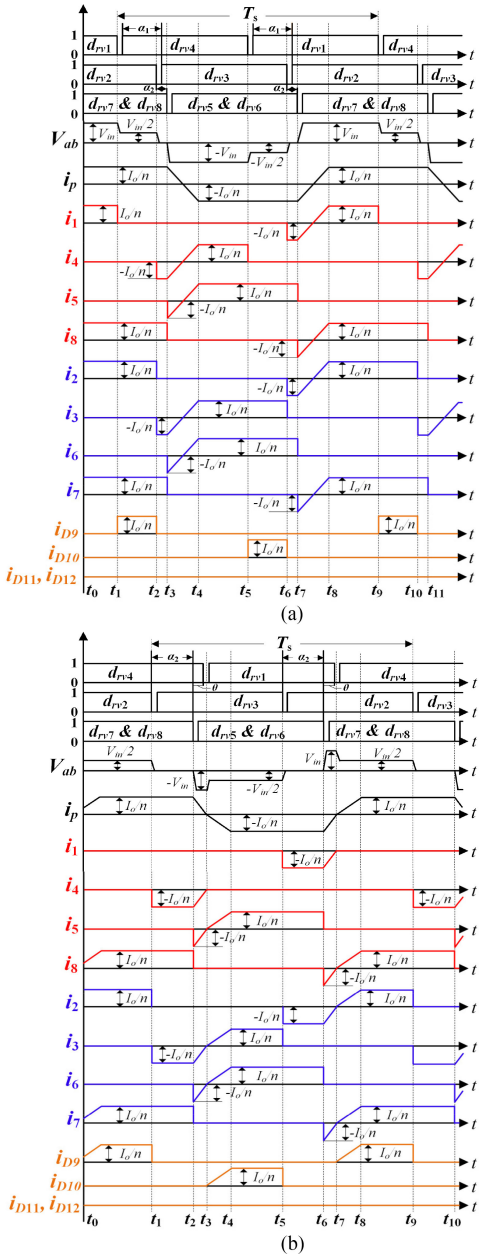


Fig. 2. Currents on primary power devices under the DPS strategy. (a) TL mode. (b) Two-level mode.

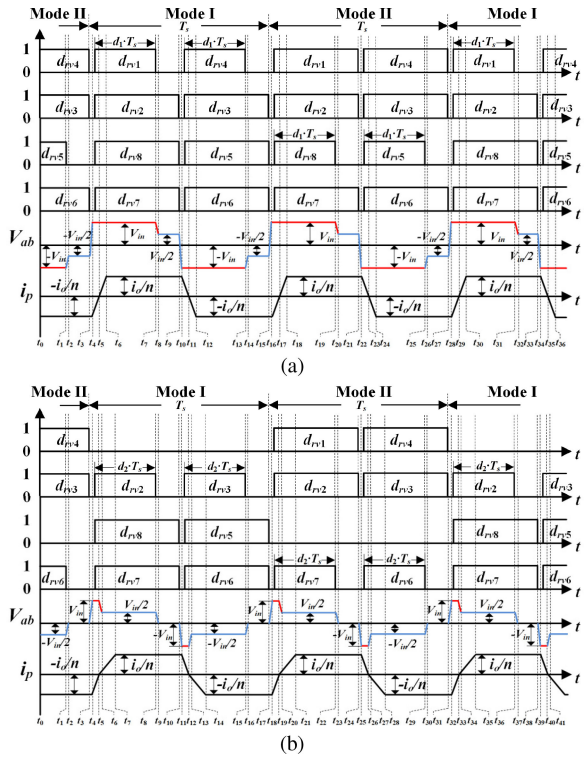


Fig. 3. Proposed modulation strategy. (a) Working pattern I. (b) Working pattern II.

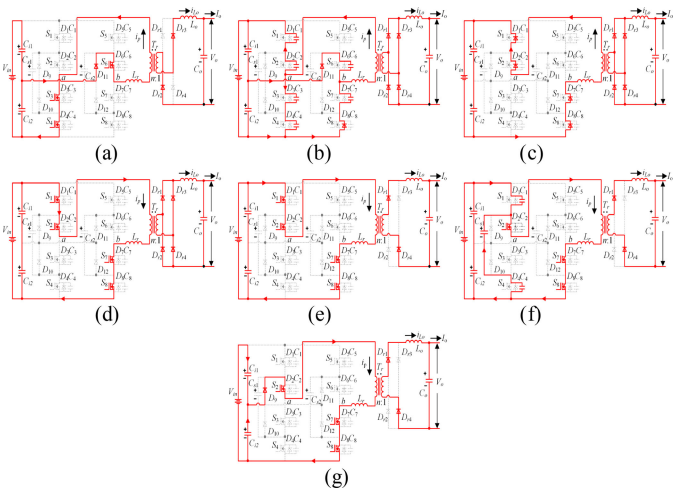


Fig. 4. Equivalent circuits under working pattern I of the proposed strategy. (a) [before t_3]. (b) [t_3–t_4]. (c) [t_4–t_5]. (d) [t_5–t_6]. (e) [t_6–t_7]. (f) [t_7–t_8]. (g) [t_8–t_9].

thus, change the output voltage V_o. For instance, if upon reducing d_2, the time length of the second-level voltages ($V_{\rm in}$/2 and $-V_{\rm in}$/2) would decrease, which means that the output voltage V_o would decrease.

Fig. 4 presents the equivalent circuits of working pattern I shown in Fig. 3(a) as an example to analyze the operation principle of the proposed strategy. The analysis of the operation principle in working pattern II is similar to that in working pattern I, which is not repeated here.

Stage 1 [before t_3]: The power switches S_3, S_4, and S_6 are all in the ON-state, so the primary voltage V_{ab} is equal to $-V_{\rm in}/2$, and the input power transfers to the load from D_{r2} and D_{r3}. The primary current of the transformer, $i_{\rm p}$, is $-I_{\rm o}/n$.

Stage 2 [t_3–t_4]: At t_3, the power switches S_3, S_4, and S_6 are turned OFF. Then, the parasitic capacitors C_3, C_4, and C_6 are charged and C_1, C_2, and C_7 discharged. The primary current i_p starts to increase and is not enough to provide output current, so the output rectifier diodes D_{r1}, D_{r2}, D_{r3}, and D_{r4} conduct simultaneously, which clamps both the primary and secondary voltages of the transformer at 0 V.

Stage 3 [t_4–t_5]: At t_4, the voltages on C_3, C_4, and C_6 increase to $V_{\rm in}$/2, and the voltages on C_1, C_2, and C_7 decrease to 0 V, so the primary voltage V_{ab} reaches $V_{\rm in}$. Then, the primary current i_p flows through D_1, D_2, D_7, and D_8, which clamps the voltage

TABLE II
COMPARISON RESULTS ABOUT DUTY CYCLE LOSS

Item		CPS Strategy	DPS Strategy	Proposed Strategy
Duty Cycle Loss	Three-level mode/ Working pattern I	$\frac{4\cdot L_r\cdot I_o}{n\cdot V_{in}\cdot T_s}+\frac{2\cdot\theta}{T_s}$	$\frac{4\cdot L_r\cdot I_o}{n\cdot V_{in}\cdot T_s}+\frac{2\cdot\theta}{T_s}$	$\frac{4\cdot L_r\cdot I_o}{n\cdot V_{in}\cdot T_s}$
	Two-level mode/ Working pattern II	$\frac{6\cdot L_r\cdot I_o}{n\cdot V_{in}\cdot T_s}$	$\frac{8\cdot L_r\cdot I_o}{n\cdot V_{in}\cdot T_s}-\frac{2\cdot\alpha}{T_s}$	$\frac{6\cdot L_r\cdot I_o}{n\cdot V_{in}\cdot T_s}$

Note: θ is the phase-shift time between the driving signals of S_2 and (S_7, S_8) or the driving signals S_3 and (S_5, S_6) in the CPS and DPS strategies. α is a constant overlap time between the driving signals of S_1 and (S_7, S_8) or the driving signals S_4 and (S_5, S_6) in the DPS strategy.

on S_1, S_2, S_7, and S_8 at 0 V. Therefore, S_1, S_2, S_7, and S_8 can be turned ON with zero-voltage. During this time period, the primary current $i_{\rm p}$ increases linearly because the voltage on L_r is the input voltage $V_{\rm in}$.

Stage 4 [t_5–t_6]: At t_5, the primary current i_p increases to 0 A, which means the current direction of i_p would change. During this time period, the primary current i_p still increases linearly because the voltage on L_r maintains $V_{\rm in}$.

Stage 5 [t_6–t_7]: At t_6, the primary current i_p increases to the positive reflected output current whose value is I_o/n. Then, the output rectifier diodes D_{r2} and D_{r3} are turned OFF, and the input power would transfer to load from D_{r1} and D_{r4}.

Stage 6 [t_7–t_8]: At t_7, the power switch S_1 is turned OFF. Then, the parasitic capacitor C_1 is charged and C_4 is discharged.

Stage 7 [t_8–t_9]: At t_8, the voltage on C_1 increases to $V_{\rm in}$/2, and the voltage on C_4 decreases to 0 V. Then, the clamping diode D_9 conducts, and the primary current i_p flows through D_9, S_2, S_7, and S_8. During this time period, the primary voltage, V_{ab}, is $V_{\rm in}$/2.

At t_9, the power switches S_2, S_7, and S_8 are turned OFF. The second half cycle [t_9–t_{15}] of mode I starts, whose analysis is similar to that in the first half cycle [t_3–t_9]. The analysis of mode II is similar to that of mode I, which is not repeated here.

IV. CHARACTERISTICS AND PERFORMANCES OF THE PROPOSED STRATEGY

A. Duty Cycle Loss

In working pattern I shown in Fig. 3(a), [t_3–t_6], [t_9–t_{12}] and [t_{15}–t_{18}], [t_{21}–t_{24}] are the time intervals of the duty cycle loss in modes I and II, respectively, and these four time intervals are the same. If neglecting the quite short time intervals [t_3–t_4], [t_9–t_{10}], [t_{15}–t_{16}], and [t_{21}–t_{22}], they can be calculated as

$$t_6-t_3=t_{12}-t_9=t_{18}-t_{15}=t_{24}-t_{21}=\frac{2\cdot L_r\cdot I_o}{n\cdot V_{\rm in}} \quad (1)$$

On the basis of (1), the duty cycle loss in every switching period T_s under working pattern I, namely, $d_{\rm loss\_}I$, can be obtained as

$$d_{\rm loss\_}I=\frac{t_6-t_3}{T_s}=\frac{t_{12}-t_9}{T_s}=\frac{t_{18}-t_{15}}{T_s}=\frac{t_{24}-t_{21}}{T_s}=\frac{2\cdot L_r\cdot I_o}{n\cdot V_{\rm in}\cdot T_s} \quad (2)$$

In working pattern II shown in Fig. 3(b), [t_3–t_7], [t_{10}–t_{14}] and [t_{17}–t_{21}], [t_{24}–t_{28}] are the time intervals of the duty cycle loss in modes I and II, respectively, and these four time intervals are the same. If neglecting the quite short time intervals [t_3–t_4], [t_{10}–t_{11}], [t_{17}–t_{18}], and [t_{24}–t_{25}], they can be calculated as

$$t_7-t_3=t_{14}-t_{10}=t_{21}-t_{17}=t_{28}-t_{24}=\frac{3\cdot L_r\cdot I_o}{n\cdot V_{\rm in}} \quad (3)$$

On the basis of (3), the duty cycle loss in every switching period T_s under working pattern II, namely, $d_{\rm loss\_}II$, can be obtained as

$$d_{\rm loss\_}II=\frac{t_7-t_3}{T_s}=\frac{t_{14}-t_{10}}{T_s}=\frac{t_{21}-t_{17}}{T_s}=\frac{t_{28}-t_{24}}{T_s}=\frac{3\cdot L_r\cdot I_o}{n\cdot V_{\rm in}\cdot T_s} \quad (4)$$

Table II presents the comparison results about the duty cycle loss under the conventional strategies and the proposed strategy. From Table II, the following can be observed.

1) The duct cycle loss of working pattern I under the proposed strategy is smaller than that of the TL mode under the conventional strategies.
2) The duty cycle loss of working pattern II under the proposed strategy is the same as that of the two-level mode under the CPS strategy.

B. Output Characteristics

If neglecting the effect of the dead time, the average output voltage in working pattern I, namely, V_{o_I} and that in working pattern II, namely, V_{o_II}, can be calculated, respectively, using (5) and (6)

$$V_{o\_I}=\frac{2\cdot[\int_0^{(d_1-d_{\rm loss\_I})\cdot T_s}\frac{V_{\rm in}}{n}+\int_0^{(0.5-d_1)\cdot T_s}\frac{V_{\rm in}}{2\cdot n}]}{T_s}=\frac{V_{\rm in}}{n}\cdot(0.5+d_1-2\cdot d_{\rm loss\_I})=\frac{V_{\rm in}}{n}\cdot\left(0.5+d_1-\frac{4\cdot L_r\cdot I_o}{n\cdot V_{\rm in}\cdot T_s}\right) \quad (5)$$

$$V_{o\_II}=\frac{2\cdot[\int_0^{(d_2-d_{\rm loss\_II})\cdot T_s}\frac{V_{\rm in}}{2\cdot n}]}{T_s}=\frac{V_{\rm in}}{n}\cdot(d_2-d_{\rm loss\_II})=\frac{V_{\rm in}}{n}\cdot\left(d_2-\frac{3\cdot L_r\cdot I_o}{n\cdot V_{\rm in}\cdot T_s}\right) \quad (6)$$

TABLE III
COMPARISON RESULTS ABOUT ZVS ACHIEVEMENT CONDITIONS

Item			CPS Strategy	DPS Strategy	Proposed Strategy
ZVS Range	Three-level mode/ Working pattern I	$I_o \geq$	$n \cdot V_{in} \cdot \sqrt{\frac{C_j}{L_r}}$	$n \cdot V_{in} \cdot \sqrt{\frac{C_j}{L_r}}$	$n \cdot V_{in} \cdot \sqrt{\frac{3 \cdot C_j}{2 \cdot L_r}}$
	Two-level mode/ Working pattern II		$n \cdot V_{in} \cdot \sqrt{\frac{C_j}{L_r}}$	$n \cdot V_{in} \cdot \sqrt{\frac{C_j}{L_r}}$	$n \cdot V_{in} \cdot \sqrt{\frac{C_j}{L_r}}$

C. ZVS Achievement Conditions

1) Working pattern I: In mode I, the zero-voltage switch-ON of power switches S_4 and S_8 is mainly determined by the reflected current from the output filter inductor. Normally, the output filter inductance is quiet large enough to make power switches S_4 and S_8 achieve zero-voltage switch-ON, even at light loads. For instance, in order to ensure the zero-voltage switch-ON of the power switch S_4 in Fig. 3(a), energy E_1 is needed to discharge capacitor C_4 from $V_{\rm in}/2$ to 0 V and charge capacitor C_1 from 0 V to $V_{\rm in}/2$, whose expression is given as

$$E_1 \geq \frac{1}{2} \cdot C_1 \cdot \left(\frac{V_{\rm in}}{2}\right)^2 + \frac{1}{2} \cdot C_4 \cdot \left(\frac{V_{\rm in}}{2}\right)^2 = \frac{1}{4} \cdot C_j \cdot V_{\rm in}^2 \tag{7}$$

In mode I, the energy stored in inductor L_r is used to realize the zero-voltage switch-ON for the power switches S_1, S_2, S_3, S_5, S_6, and S_7. For instance, in order to achieve the zero-voltage switch-ON for power switches S_3, S_5, and S_6 in Fig. 3(a), capacitors C_3, C_5, C_6 need to be discharged from $V_{\rm in}/2$ to 0 V, and capacitors C_2, C_7, and C_8 need to be charged from 0 V to $V_{\rm in}/2$. Accordingly, the following condition should be satisfied to achieve the zero-voltage switch-ON of S_3, S_5, and S_6:

$$\frac{1}{2} L_r \cdot \left(\frac{I_o}{n}\right)^2 \geq \frac{1}{2} \cdot (C_1 + C_2 + C_3 + C_5 + C_6 + C_7) \cdot \left(\frac{V_{\rm in}}{2}\right)^2 = \frac{3}{4} \cdot C_j \cdot V_{\rm in}^2 \tag{8}$$

In mode II, the reflected current from the output filter inductor is used to realize the zero-voltage switch-ON for the power switches, S_1 and S_5; the energy stored in inductor L_r is used to realize the zero-voltage switch-ON for switches S_2, S_3, S_4, S_6, S_7, and S_8. The requirements for the power switches to achieve zero-voltage switch-ON in mode II are same as those in operation mode I, which is not repeated here.

Therefore, on the basis of (8), the load range of ZVS achievement in working pattern I, namely, $I_{o\_{\rm ZVS}\_I}$, can be obtained as

$$I_{o\_{\rm ZVS}\_I} \geq n \cdot V_{\rm in} \cdot \sqrt{\frac{3 \cdot C_j}{2 \cdot L_r}} \tag{9}$$

2) Working pattern II: In mode I, the zero-voltage switch-ON of power switches S_3, S_7, and S_8 is mainly determined by the reflected current from the output filter inductor. Normally, the output filter inductance is large enough to make the power switches S_3, S_7, and S_8 achieve zero-voltage switch-ON, even at light loads. For instance, in order to ensure the zero-voltage switch-ON of the power switch S_3 in Fig. 3(b), energy E_2 is needed to discharge capacitor C_3 from $V_{\rm in}/2$ to 0 V and charge capacitor C_2 from 0 V to $V_{\rm in}/2$, whose expression can be given as

$$E_2 \geq \frac{1}{2} \cdot C_2 \cdot \left(\frac{V_{\rm in}}{2}\right)^2 + \frac{1}{2} \cdot C_3 \cdot \left(\frac{V_{\rm in}}{2}\right)^2 = \frac{1}{4} \cdot C_j \cdot V_{\rm in}^2 \tag{10}$$

In mode I, the energy stored in inductor L_r is used to realize the zero-voltage switch-ON for the power switches S_2, S_5, and S_6. For instance, in order to achieve the zero-voltage switch-ON for the power switches S_5 and S_6 in Fig. 3(b), capacitors C_5, C_6 need to be discharged from $V_{\rm in}/2$ to 0 V, and capacitors C_7, C_8 need to be charged from 0 V to $V_{\rm in}/2$. Accordingly, the following condition should be satisfied to achieve the zero-voltage switch-ON of S_5 and S_6:

$$\frac{1}{2} L_r \cdot \left(\frac{I_o}{n}\right)^2 \geq \frac{1}{2} \cdot (C_5 + C_6 + C_7 + C_8) \cdot \left(\frac{V_{\rm in}}{2}\right)^2 = \frac{1}{2} \cdot C_j \cdot V_{\rm in}^2 \tag{11}$$

In mode II, the reflected current from the output filter inductor is used to realize the zero-voltage switch-ON for the power switches S_1, S_2, and S_6; the energy stored in inductor L_r is used to realize the zero-voltage switch-ON for switches S_3, S_4, and S_7. The requirements for the power switches to achieve zero-voltage switch-ON in mode II are same as those in operation mode I, which is not repeated here.

Therefore, on the basis of (11), the load range of ZVS achievement in working pattern I, namely, $I_{o\_{\rm ZVS}\_II}$, can be obtained as

$$I_{o\_{\rm ZVS}\_II} \geq n \cdot V_{\rm in} \cdot \sqrt{\frac{C_j}{L_r}} \tag{12}$$

Table III presents the comparison results about the ZVS range under the conventional strategies and the proposed strategy. From Table III, the following can be observed.

1) The ZVS range of working pattern II under the proposed strategy is the same as that of the TL mode under the conventional strategies.
2) The ZVS range of working pattern I under the proposed strategy is little smaller than that of the TL mode under the

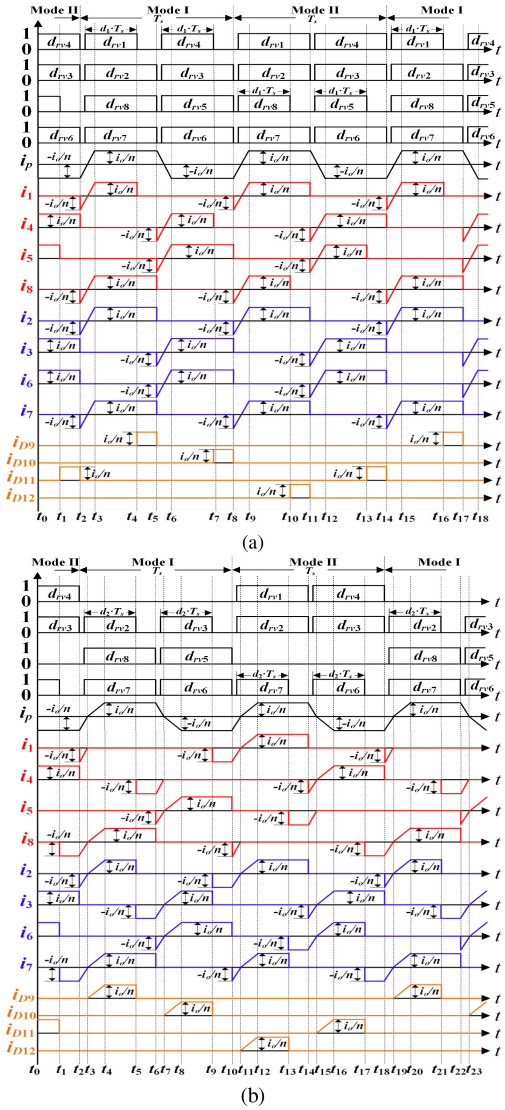


Fig. 5. Currents on primary power devices under the proposed strategy. (a) Working pattern I. (b) Working pattern II.

conventional strategies because the conventional strategies could realize the ZVS of one more power switch by increasing the duty cycle loss.

D. Currents on Power Devices

Fig. 5 shows the currents flowing through the primary power devices under the proposed strategy. From Fig. 5, it can be observed that:

1) under the working pattern I, the currents on the outer power switches i_1, i_4, i_5, i_8, on the inner power switches i_2, i_3, i_6, i_7, and on the clamping diodes i_{D9}, i_{D10}, i_{D11}, i_{D12} are the same besides phase difference, respectively;
2) under the working pattern II, the rms and average values of i_1, i_4, i_5, i_8 are the same respectively, the rms and average values of i_2, i_3, i_6, i_7 are also the same respectively, and $i_{D9}, i_{D10}, i_{D11}, i_{D12}$ are the same besides phase difference.

On the basis of the above analysis, it can be concluded that the two working patterns of the proposed strategy can balance the currents both among the power switches and clamping diodes.

Table IV presents the calculation equations about the rms and average values of i_1–i_8 and i_{D9}–i_{D12} under the proposed strategy according to Fig. 5.

According to the equations in Tables I, IV, and circuit parameters in Appendix, the theoretical comparison results about the currents on the primary power devices are presented in Figs. 6–8, in which $i_{1\_rms\_three\_DPS}$– $i_{8\_rms\_three\_DPS}$, $i_{1\_avg\_three\_DPS} - i_{8\_avg\_three\_DPS}$ and $i_{1\_rms\_two\_DPS} - i_{8\_rms\_two\_DPS}$, $i_{1\_avg\_two\_DPS} - i_{8\_avg\_two\_DPS}$ are the rms value, average value of the currents on the power switches (S_1, D_1)–(S_8, D_8) under the TL and two-level mode of the DPS strategy, respectively; $i_{D9\_rms\_three\_DPS}$–$i_{D12\_rms\_three\_DPS}$, $i_{D9\_avg\_three\_DPS}$–$i_{D12\_avg\_three\_DPS}$ and $i_{D9\_rms\_two\_DPS}$–$i_{D12\_rms\_two\_DPS}$, $i_{D9\_avg\_two\_DPS}$–$i_{D12\_avg\_two\_DPS}$ are the rms value, average value of the currents on the clamping diodes D_9–D_{12} under the TL and two-level mode of the DPS strategy, respectively; $i_{1\_rms\_I}$–$i_{8\_rms\_I}$, $i_{1\_avg\_I}$–$i_{8\_avg\_I}$ and $i_{1\_rms\_II}$–$i_{8\_rms\_II}$, $i_{1\_avg\_II}$–$i_{8\_avg\_II}$ are the rms value, average value of the currents on the power switches (S_1, D_1)–(S_8, D_8) under working patterns I and II of the proposed strategy, respectively; $i_{D9\_rms\_I}$–$i_{D12\_rms\_I}$, $i_{D9\_avg\_I}$–$i_{D12\_avg\_I}$ and $i_{D9\_rms\_II}$–$i_{D12\_rms\_II}$, $i_{D9\_avg\_II}$–$i_{D12\_avg\_II}$ are the rms value, average value of the currents on the clamping diodes D_9–D_{12} under working patterns I and II of the proposed strategy, respectively.

From Figs. 6–8, the following can be observed.

1) For the currents on the outer power switches (i_1, i_4, i_5, and i_8) in Fig. 6, the rms and average values of i_5 and i_8 are larger than that of i_1 and i_4 under the conventional strategy; but the rms and average values of them become the same under the proposed strategy.
2) For the currents on the inner power switches (i_2, i_3, i_6, and i_7) in Fig. 7, the rms values of them are the same, but the average value of i_6 and i_7 are larger than that of i_2 and i_3 under the conventional strategy; the rms and average values of them become the same under the proposed strategy.
3) For the currents on the clamping diodes (i_{D9}, i_{D10}, i_{D11}, and i_{D12}) in Fig. 8, the rms and average values of i_{D9} and i_{D10} are larger than that of i_{D11} and i_{D12} under the conventional strategy; but, the rms and average values of them become the same under the proposed strategy.
4) The differences among the currents on outer power switches, inner power switches, and clamping diodes under the conventional strategy would become larger with the increasing of the output power.

E. Implementation of the Proposed Strategy

For working pattern I, the duty cycle d_1 calculated by the control loop would be changed in every two switching periods to adjust the output voltage V_o in the practical application.

TABLE IV
THEORETICAL EQUATIONS ABOUT THE RMS AND AVERAGE VALUES OF THE CURRENTS ON PRIMARY POWER DEVICES UNDER THE PROPOSED STRATEGY

		Working pattern I	Working pattern II
i_1, i_4, i_5, i_8	RMS value	$\sqrt{\frac{I_o^2\cdot(1+2\cdot d_1)}{4\cdot n^2}-\frac{4\cdot L_r\cdot I_o^3}{3\cdot V_{in}\cdot n^3\cdot T_s}}$	$\sqrt{\frac{I_o^2\cdot(1-d_2)}{2\cdot n^2}-\frac{5\cdot L_r\cdot I_o^3}{6\cdot V_{in}\cdot n^3\cdot T_s}}$
	Average value	$\frac{I_o\cdot(1+2\cdot d_1)}{4\cdot n}-\frac{2\cdot L_r\cdot I_o^2}{V_{in}\cdot n^2\cdot T_s}$	$\frac{I_o\cdot d_2}{2\cdot n}-\frac{3\cdot L_r\cdot I_o^2}{2\cdot V_{in}\cdot n^2\cdot T_s}$
i_2, i_3, i_6, i_7	RMS value	$\sqrt{\frac{I_o^2}{2\cdot n^2}-\frac{4\cdot L_r\cdot I_o^3}{3\cdot V_{in}\cdot n^3\cdot T_s}}$	$\sqrt{\frac{I_o^2}{2\cdot n^2}-\frac{2\cdot L_r\cdot I_o^3}{V_{in}\cdot n^3\cdot T_s}}$
	Average value	$\frac{I_o}{2\cdot n}-\frac{2\cdot L_r\cdot I_o^2}{V_{in}\cdot n^2\cdot T_s}$	$\frac{I_o\cdot d_2}{n}-\frac{5\cdot L_r\cdot I_o^2}{2\cdot V_{in}\cdot n^2\cdot T_s}$
i_{D9}, i_{D10}, i_{D11}, i_{D12}	RMS value	$\frac{I_o}{n}\cdot\sqrt{\frac{1-2\cdot d_1}{4}}$	$\sqrt{\frac{I_o^2\cdot d_2}{2\cdot n^2}-\frac{7\cdot L_r\cdot I_o^3}{6\cdot V_{in}\cdot n^3\cdot T_s}}$
	Average value	$\frac{I_o\cdot(1-2\cdot d_1)}{4\cdot n}$	$\frac{I_o\cdot d_2}{2\cdot n}-\frac{L_r\cdot I_o^2}{V_{in}\cdot n^2\cdot T_s}$

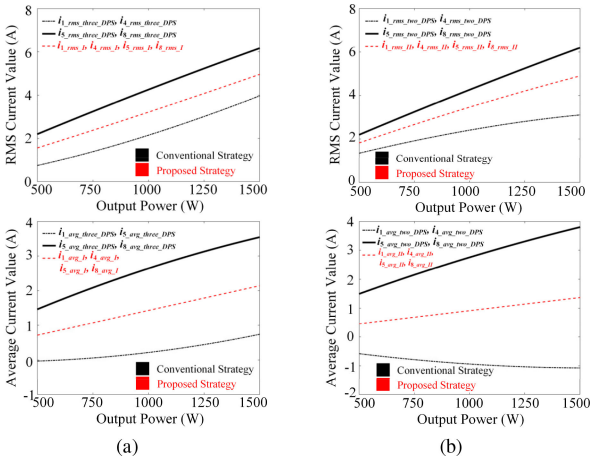


Fig. 6. Theoretical calculation about the rms and average values of the currents on outer power switches. (a) TL mode of the DPS strategy and working pattern I of the proposed strategy ($V_{\rm in}$ = 350 V, V_o = 50 V). (b) Two-level mode of the DPS strategy and working pattern II of the proposed strategy ($V_{\rm in}$ = 550 V, V_o = 50 V).

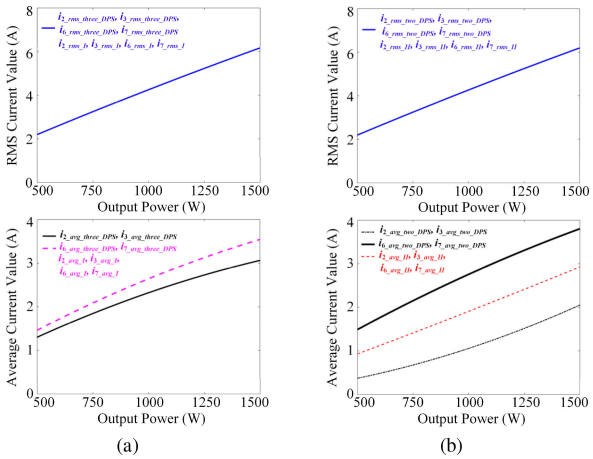


Fig. 7. Theoretical calculation about the rms and average values of the currents on inner power switches. (a) TL mode of the DPS strategy and working pattern I of the proposed strategy ($V_{\rm in}$ = 350 V, V_o = 50 V). (b) Two-level mode of the DPS strategy and working pattern II of the proposed strategy ($V_{\rm in}$ = 550 V, V_o = 50 V).

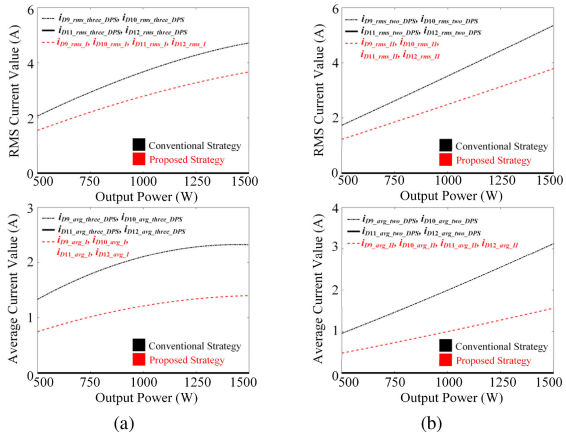


Fig. 8. Theoretical calculation about the rms and average values of the currents on clamping diodes. (a) TL mode of the DPS strategy and working pattern I of the proposed strategy ($V_{\rm in}$ = 350 V, V_o = 50 V). (b) Two-level mode of the DPS strategy and working pattern II of the proposed strategy ($V_{\rm in}$ = 550 V, V_o = 50 V).

As shown in Fig. 3(a), in the first switching period, the calculated d_1 is set for the driving signals of power switches S_1, S_4, and the duct cycle 0.5 minus the dead time divided by T_s is set for the driving signals of power switches S_2, S_3, S_5, S_6, S_7, and S_8; in the second switching period, the calculated d_1 is set for the driving signals of power switches S_5, S_8, and the duct cycle 0.5 minus the dead time divided by T_s is set for the driving signals of power switches S_1, S_2, S_3, S_4, S_6, and S_7. Upon increasing the input voltage, d_1 would decrease to maintain the output voltage at the constant value. When d_1 reduces to zero, working pattern II starts to be utilized and d_1 is kept at zero, so the transition between the two working patterns is seamless. For working pattern II, the duty cycle d_2 calculated by the control loop would be changed in every two switching periods to adjust the output voltage V_o in the practical application. As shown in Fig. 3(b), in the first switching period, the calculated d_2 is set for the driving signals of power switches S_2, S_3, and the duct cycle 0.5 minus the dead time divided by T_s is set for the driving signals of power switches S_5, S_6, S_7, and S_8; in the second switching period, the calculated d_2 is set for the driving signals of power switches S_6,

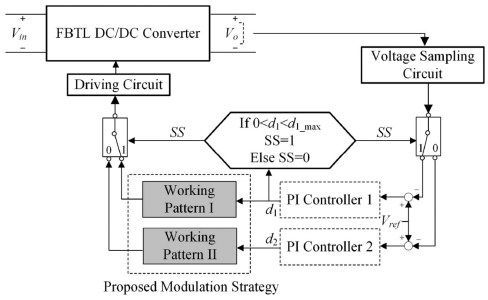
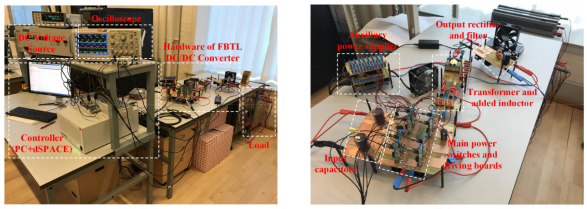


Fig. 9. Diagram about the implementation of the proposed control strategy.



(a) (b)

Fig. 10. (a) Experimental setup. (b) Hardware of the FBTL dc/dc converter.

S_7, and the duct cycle 0.5 minus the dead time divided by T_s is set for the driving signals of power switches S_1, S_2, S_3, and S_4.

Under the steady operations, duty cycles d_1 and d_2 calculated using the control algorithms are adjusted in every two switching periods to control the output voltage and balance the currents on the primary power devices. Under the dynamic changes, duty cycles d_1 and d_2 calculated using the control algorithms can be adjusted in every switching period to control the converter, which would, thus, make dynamic responses as the conventional modulation strategies, because both working patterns I and II have the feature that modes I and II (see Fig. 3) can be utilized alone separately to control the output voltage and have the same output characteristics.

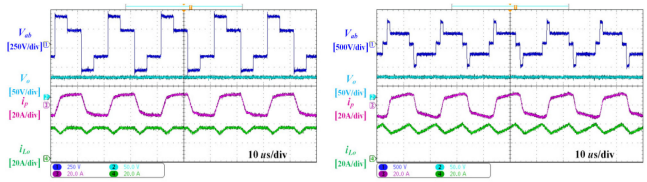
Fig. 9 presents the diagram about the implementation of the proposed modulation strategy, in which the conventional proportional-integral control algorithm is utilized to calculate duty cycles d_1 and d_2. As shown in Fig. 9, working pattern I is used for the low input voltage by adjusting duty cycle d_1 from the maximum value d_{1_max} to 0; when d_1 decreases to 0 due to the increasing of the input voltage, working pattern II would be used for the higher input voltage by adjusting duty cycle d_2.

V. Experimental Verification

In order to verify the proposed modulation strategy, a 1.5-kW experimental prototype is established, whose circuit parameters are presented in the Appendix. Fig. 10(a) and (b) presents the experimental setup and hardware of the FBTL dc/dc converter.

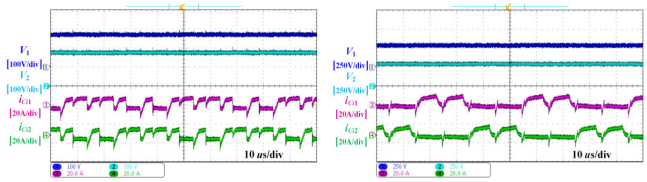
Figs. 11(a) and 10(b) present the experimental results including the primary voltage V_{ab}, output voltage V_o, primary current i_p, and current through the output filter inductor i_{Lo} under working patterns I and II.

Fig. 12 presents the experimental results including the voltages and currents on the input capacitors $(V_1, V_2, i_{Ci1}$, and $i_{Ci2})$ when the output voltage V_o is 50 V and



(a) (b)

Fig. 11. Experimental results including V_{ab}, V_o, i_p, and i_{Lo} (V_o = 50 V, P_o = 1.5 kW). (a) Working pattern I of the proposed strategy ($V_{\rm in}$ = 350 V). (b) Working pattern II of the proposed strategy ($V_{\rm in}$ = 550 V).



(a) (b)

Fig. 12. Experimental results including V_1, V_2, i_{Ci1}, and i_{Ci2} (V_o = 50 V, P_o = 1.5 kW). (a) Working pattern I of the proposed strategy ($V_{\rm in}$ = 350 V). (b) Working pattern II of the proposed strategy ($V_{\rm in}$ = 550 V).

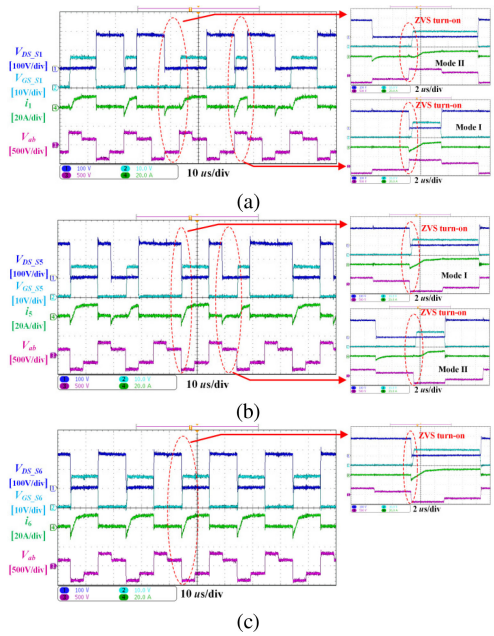


Fig. 13. ZVS achievement performances under working pattern I ($V_{\rm in}$ = 350 V, V_o = 50 V, P_o = 1.5 kW). (a) S_1. (b) S_5. (c) S_6.
Note: In Fig. 13, $V_{\rm GS\_S1}$, $V_{\rm GS\_S5}$, and $V_{\rm GS\_S6}$ are the gate-source voltages of S_1, S_5, and S_6; $V_{\rm DS\_S1}$, $V_{\rm DS\_S5}$, and $V_{\rm DS\_S6}$ are the drain-source voltages of S_1, S_5, and S_6.

output power P_o is 1.5 kW. From Fig. 12, the following can be observed under the proposed modulation strategy.

1) The voltages on the input capacitors (V_1, V_2) are balanced.
2) The currents on the input capacitors (i_{Ci1}, i_{Ci2}) are also balanced, and the rms of i_{Ci1}, i_{Ci2} under working pattern I ($V_{\rm in}$ = 350 V) and II ($V_{\rm in}$ = 550 V) are approximately 5.1 and 4.5 A, respectively.

Fig. 13(a)–(c) shows the ZVS achievement performances of power switches S_1, S_5, and S_6 under working pattern I, in which it can be observed that S_1, S_5, and S_6 realize ZVS-ON. Fig. 14(a)

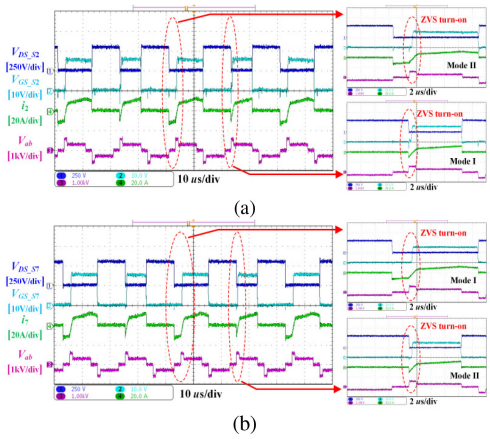


Fig. 14. ZVS achievement performances under working pattern II ($V_{\rm in}$ = 550 V, V_o = 50 V, P_o = 1.5 kW). (a) S_2. (b) S_7.
Note: In Fig. 14, $V_{\rm GS\_S2}$ and $V_{\rm GS\_S7}$ are the gate-source voltages of S_2 and S_7; $V_{\rm DS\_S2}$ and $V_{\rm DS\_S7}$ are the drain-source voltages of S_2 and S_7.

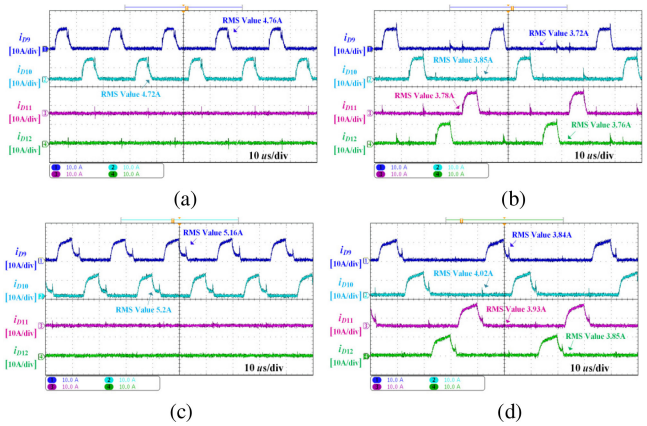


Fig. 15. Experimental results of clamping diode currents i_{D9}, i_{D10}, i_{D11}, and i_{D12} (V_o = 50 V, P_o = 1.5 kW). (a) TL mode of the DPS strategy ($V_{\rm in}$ = 350 V). (b) Working pattern I of the proposed strategy ($V_{\rm in}$ = 350 V). (c) Two-level mode of the DPS strategy ($V_{\rm in}$ = 550 V). (d) Working pattern II of the proposed strategy ($V_{\rm in}$ = 550 V).

and (b) presents the ZVS achievement performances of power switches S_2 and S_7 under working pattern II, in which it can be observed that S_2 and S_7 realize ZVS-ON. The ZVS achievement performances of other power switches are similar to the results in Figs. 13–14, which are not repeated here.

Figs. 15–17 present the experimental results about the clamping diode currents i_{D9}, i_{D10}, i_{D11}, i_{D12}, outer switch currents i_1, i_4, i_5, i_8, and inner switch currents i_2, i_3, i_6, i_7, respectively, under the DPS strategy and the proposed strategy.

From Figs. 15–17, the following can be observed.

1) The clamping diode currents i_{D9}, i_{D10}, i_{D11}, i_{D12}, the outer switch currents i_1, i_4, i_5, i_8, and inner switch currents i_2, i_3, i_6, i_7 are unbalanced under the DPS strategy.
2) But, by utilizing the proposed strategy, the clamping diode currents i_{D9}, i_{D10}, i_{D11}, i_{D12}, the outer switch currents i_1, i_4, i_5, i_8, and inner switch currents i_2, i_3, i_6, i_7 can be balanced.

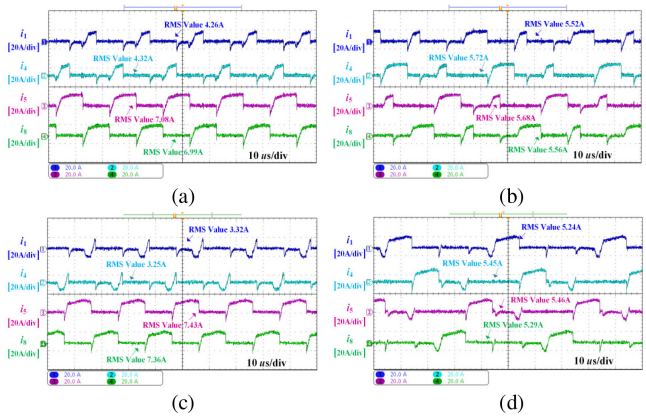


Fig. 16. Experimental results of outer switch currents i_1, i_4, i_5, and i_8 (V_o = 50 V, P_o = 1.5 kW). (a) TL mode of the DPS strategy ($V_{\rm in}$ = 350 V). (b) Working pattern I of the proposed strategy ($V_{\rm in}$ = 350 V). (c) Two-level mode of the DPS strategy ($V_{\rm in}$ = 550 V). (d) Working pattern II of the proposed strategy ($V_{\rm in}$ = 550 V).

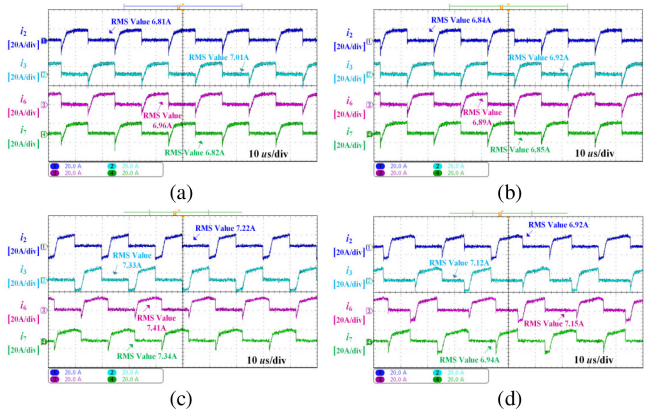


Fig. 17. Experimental results of inner switch currents i_2, i_3, i_6, and i_7 (V_o = 50 V, P_o = 1.5 kW). (a) TL mode of the DPS strategy ($V_{\rm in}$ = 350 V). (b) Working pattern I of the proposed strategy ($V_{\rm in}$ = 350 V). (c) Two-level mode of the DPS strategy ($V_{\rm in}$ = 550 V). (d) Working pattern II of the proposed strategy ($V_{\rm in}$ = 550 V).

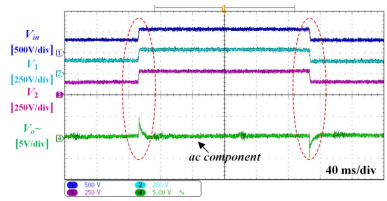


Fig. 18. Experimental results about the transition performance between the two working patterns when V_o = 50 V and P_o = 1.5 kW.

3) The experimental results shown in Figs. 15–17 are consistent with the theoretical analysis in Sections II and IV-D.

Fig. 18 shows the experimental results about the transition performance between the two working patterns, which includes the input voltage ($V_{\rm in}$), voltages on the two input capacitors (V_1, V_2), and ac component of the output voltage V_o ∼. In Fig. 18, the input voltage steps up from 300 to 550 V and is finally set back to 300 V when the output voltage V_o is 50 V and output power P_o 1.5 kW. From Fig. 18, it can be observed that there

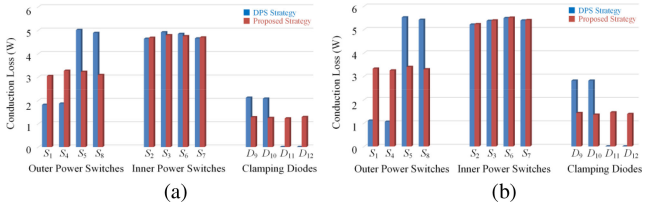


Fig. 19. Loss breakdown of primary power devices ($V_o = 50$ V and $P_o = 1.5$ kW). (a) Working pattern I ($V_{\rm in} = 350$ V). (b) Working pattern II ($V_{\rm in} = 550$ V).

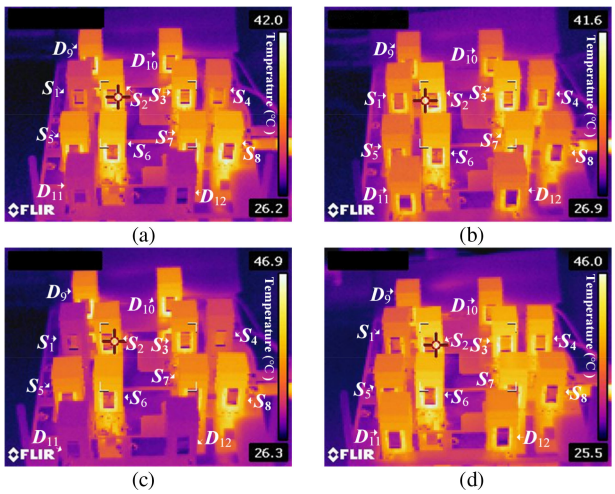


Fig. 20. Experimental results about the thermal stresses on primary power devices by FLIR thermal camera. ($V_o = 50$ V, $P_o = 1.5$ kW, ambient temperature = 25 °C). (a) TL mode of the DPS strategy ($V_{\rm in} = 350$ V). (b) Working pattern I of the proposed strategy ($V_{\rm in} = 350$ V). (c) Two-level mode of the DPS strategy ($V_{\rm in} = 550$ V). (d) Working pattern II of the proposed strategy ($V_{\rm in} = 550$ V).

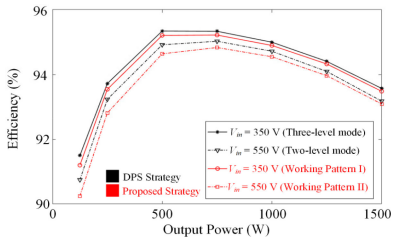


Fig. 21. Experimental comparison results about efficiencies.

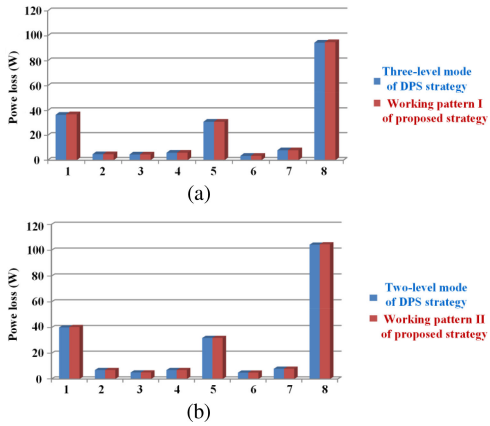


Fig. 22. Comparison results about the loss breakdown when $V_o = 50$ V and $P_o = 1.5$ kW. (a) $V_{\rm in} = 350$ V. (b) $V_{\rm in} = 550$ V.
Note: 1) Primary power devices' conduction loss. 2) Primary power switches' switching loss. 3) Transformer's core loss. 4) Transformer's copper loss. 5) Output rectifier diodes' loss. 6) Output filter inductor's loss. 7) PCB loss. 8) Total loss.

is no abnormal votlage spike on the two input capacitors during the transitions between the two working patterns.

Normally, the conduction power loss and thermal stress on the power device is closely related to the current flowing through it. Figs. 19 and 20 present the comparison results about the loss breakdown and thermal stresses of the primary power devices between the conventional strategy and the proposed strategy, respectively.

From Fig. 19, the following can be observed.

1) Under the DPS strategy, the conduction losses among the inner power switches are balanced because the rms values of the currents through the inner power switches are almost the same and because MOSFET is used for the primary power switches in the built prototype, but the conduction losses among the outer power switches and clamping diodes are unbalanced.
2) After utilizing the proposed strategy, the conduction losses among the outer power switches, inner power switches, and clamping diodes become balanced.

It needs to be mentioned that if IGBT is used for the power switches, the conduction losses among the inner power switches would become unbalanced under the conventional strategy because the average values of the currents through the inner power switches are different. These power-loss imbalances under the conventional strategy would result in the thermal-stress imbalance among the primary power devices, as shown in Fig. 20. Under the DPS strategy, the thermal stress of D_9, D_{10} are higher than that of D_{11}, D_{12}, and the thermal stress of (S_1, D_1), (S_4, D_4) are lower than that of other power switches, as shown in Fig. 20(a) and (c), which means that the thermal stresses among the power switches and clamping diodes are unbalanced. After utilizing the proposed strategy, the thermal stresses among clamping diodes D_9–D_{12}, outer power switches (S_1, D_1), (S_4, D_4), (S_5, D_5), (S_8, D_8), and inner power switches (S_2, D_2), (S_3, D_3), (S_6, D_6), (S_7, D_7) become balanced, as shown in Fig. 20(b) and (d).

Fig. 21 shows the experimental comparison results about the efficiencies between the conventional strategy and the proposed strategy. From Fig. 21, the following can be observed.

1) The efficiencies under working pattern I of the proposed strategy are almost the same as those under the TL mode of the DPS strategy.
2) The efficiencies under working pattern II of the proposed strategy are slightly lower than those under the TL mode of the DPS strategy.

Fig. 22 presents the loss breakdown of the main components in the FBTL dc/dc converter under the conventional DPS strategy and the proposed strategy when P_o is 1.5 kW. From Fig. 22, the following can be observed.

1) The conduction losses of the primary power switches under the DPS strategy and the proposed strategy are almost the same.
2) The DPS strategy and the proposed strategy both realize ZVS, and the switching-OFF losses are almost the same, so the switching losses of the primary power switches would be almost the same.
3) The power losses of the transformer under the two strategies would be almost the same because the primary voltage and the primary voltage on the transformer are almost the same.
4) The secondary components' power losses would be almost the same because the secondary voltage and current are almost the same.

It needs to be mentioned that: with the decreasing of the output power, the conduction losses of the primary power devices under working pattern I of the proposed strategy and the TL mode of the DPS strategy are almost the same, but the conduction losses of the primary power devices under working pattern II of the proposed strategy become higher than those under the two-level mode of the DPS strategy, which results in that the converter's efficiencies under working pattern II become lower than that under the two-level mode with the decreasing of the output power, as shown in Fig. 21. The reason causing lower efficiencies is that the MOSFET is used for the power switches in the established prototype. When using the MOSFET, the primary current i_p flows through the two body diodes of the power switches instead of the power switches themselves during the free-wheeling time periods [as [t_5–t_6], [t_9–t_{10}], [t_{13}–t_{14}], and [t_{17}–t_{18}] in Fig. 5(b)] under working pattern II of the proposed strategy. With the decreasing of the output power, the free-wheeling time periods would become longer, which would, thus, increase the conduction losses in comparison with the DPS strategy because the conduction loss of power switch is lower than that of its body diode when the same current flows through them [27]. However, when the IGBT is used for the power switches to satisfy the higher voltage and power applications, the primary current i_p would both flow through the two power switches and two body diodes during the free-wheeling time periods under the two-level mode and working pattern II.

VI. Conclusion

This paper points out that there exists the current-imbalance issue of primary power devices under the conventional strategies in the FBTL dc/dc converter based on the detailed analysis. Then, in order to eliminate these current imbalances, a new modulation strategy is proposed for the FBTL dc/dc converter. In addition, the proposed strategy is composed of two working patterns, which cannot only realize ZVS but also satisfy the wide input voltage range. The transition between these two working patterns is seamless. More significantly, these two working patterns of the proposed strategy can effectively balance the currents both among the power switches and clamping diodes, which would, thus, improve the reliability of the FBTL dc/dc converter by balancing the thermal stresses among the power switches and clamping diodes. Finally, a 1.5-kW experimental prototype is established, and the experimental results verify that the current difference and thermal-stress difference among the inner power switches, outer power switches, and clamping diodes are almost zero under the proposed strategy.

Appendix

See Table V.

TABLE V
Parameters of the Experimental Prototype

Component	Description
Power Devices $S_1/D_1 - S_8/D_8$	SPW47N60C3
Clamping Diodes $D_9 - D_{12}$	DSEI30-10AR
Rectifier Diodes $D_{r1} - D_{r4}$	MBR40250TG
Turns Ratio of Transformer T_r ($n:1$)	25 : 8
Added inductor plus Leakage Inductor L_r (uH)	47.7
Input Capacitors C_{i1} and C_{i2} (uF)	470
Flying Capacitors C_{s1} and C_{s2} (uF)	47
Output Filter Capacitor C_o (uF)	470
Output Filter Inductor L_o (uH)	140
Switching Frequency (kHz)	50

The derivation of the current expressions in Table IV are presented as below based on Fig. 5.

1) Under working pattern I:

$$i_{1\_\mathrm{rms}\_I} = i_{4\_\mathrm{rms}\_I} = i_{5\_\mathrm{rms}\_I} = i_{8\_\mathrm{rms}\_I}$$

$$= \sqrt{\frac{\begin{array}{c} 2\cdot\int_0^{\frac{2\cdot L_r\cdot I_o}{n\cdot V_{\mathrm{in}}}}\left(\frac{V_{\mathrm{in}}}{L_r}\cdot t-\frac{I_o}{n}\right)^2\cdot dt \\ +\int_0^{\frac{T_s}{2}-\frac{2\cdot L_r\cdot I_o}{n\cdot V_{\mathrm{in}}}}\left(\frac{I_o}{n}\right)^2\cdot dt+\int_0^{d_1\cdot T_s-\frac{2\cdot L_r\cdot I_o}{n\cdot V_{\mathrm{in}}}}\left(\frac{I_o}{n}\right)^2\cdot dt \end{array}}{2\cdot T_s}}$$

$$= \sqrt{\frac{I_o^2\cdot(1+2\cdot d_1)}{4\cdot n^2}-\frac{4\cdot L_r\cdot I_o^3}{3\cdot V_{\mathrm{in}}\cdot n^3\cdot T_s}}$$

$$i_{1\_\mathrm{avg}\_I} = i_{4\_\mathrm{avg}\_I} = i_{5\_\mathrm{avg}\_I} = i_{8\_\mathrm{avg}\_I}$$

$$= \frac{\begin{array}{c} 2\cdot\int_0^{\frac{2\cdot L_r\cdot I_o}{n\cdot V_{\mathrm{in}}}}\left(\frac{V_{\mathrm{in}}}{L_r}\cdot t-\frac{I_o}{n}\right)\cdot dt+\int_0^{\frac{T_s}{2}-\frac{2\cdot L_r\cdot I_o}{n\cdot V_{\mathrm{in}}}}\left(\frac{I_o}{n}\right)\cdot dt \\ +\int_0^{d_1\cdot T_s-\frac{2\cdot L_r\cdot I_o}{n\cdot V_{\mathrm{in}}}}\left(\frac{I_o}{n}\right)\cdot dt \end{array}}{2\cdot T_s}$$

$$= \frac{I_o\cdot(1+2\cdot d_1)}{4\cdot n}-\frac{2\cdot L_r\cdot I_o^2}{V_{\mathrm{in}}\cdot n^2\cdot T_s}$$

$$i_{2\_\mathrm{rms}\_I} = i_{3\_\mathrm{rms}\_I} = i_{6\_\mathrm{rms}\_I} = i_{7\_\mathrm{rms}\_I}$$

$$= \sqrt{\frac{\begin{array}{c} 2\cdot\int_0^{\frac{2\cdot L_r\cdot I_o}{n\cdot V_{\mathrm{in}}}}\left(\frac{V_{\mathrm{in}}}{L_r}\cdot t-\frac{I_o}{n}\right)^2\cdot dt \\ +2\cdot\int_0^{\frac{T_s}{2}-\frac{2\cdot L_r\cdot I_o}{n\cdot V_{\mathrm{in}}}}\left(\frac{I_o}{n}\right)^2\cdot dt \end{array}}{2\cdot T_s}}$$

$$= \sqrt{\frac{I_o^2}{2\cdot n^2}-\frac{4\cdot L_r\cdot I_o^3}{3\cdot V_{\mathrm{in}}\cdot n^3\cdot T_s}}$$

$$i_{2\_avg\_I} = i_{3\_avg\_I} = i_{6\_avg\_I} = i_{7\_avg\_I}$$
$$= \frac{2 \cdot \int_0^{\frac{2 \cdot L_r \cdot I_o}{n \cdot V_{in}}} \left(\frac{V_{in}}{L_r} \cdot t - \frac{I_o}{n} \right) \cdot dt + 2 \cdot \int_0^{\frac{T_s}{2} - \frac{2 \cdot L_r \cdot I_o}{n \cdot V_{in}}} \left(\frac{I_o}{n} \right) \cdot dt}{2 \cdot T_s}$$
$$= \frac{I_o}{2 \cdot n} - \frac{2 \cdot L_r \cdot I_o^2}{V_{in} \cdot n^2 \cdot T_s}$$

$$i_{D9\_rms\_I} = i_{D10\_rms\_I} = i_{D11\_rms\_I} = i_{D12\_rms\_I}$$
$$= \sqrt{\frac{\int_0^{\frac{T_s}{2} - d_1 \cdot T_s} \left(\frac{I_o}{n} \right)^2 \cdot dt}{2 \cdot T_s}} = \frac{I_o}{n} \cdot \sqrt{\frac{1 - 2 \cdot d_1}{4}}$$

$$i_{D9\_avg\_I} = i_{D10\_avg\_I} = i_{D11\_avg\_I} = i_{D12\_avg\_I}$$
$$= \frac{\int_0^{\frac{T_s}{2} - d_1 \cdot T_s} \left(\frac{I_o}{n} \right) \cdot dt}{2 \cdot T_s} = \frac{I_o \cdot (1 - 2 \cdot d_1)}{4 \cdot n}$$

2) Under working pattern II:

$$i_{1\_rms\_II} = i_{4\_rms\_II} = i_{5\_rms\_II} = i_{8\_rms\_II}$$
$$= \sqrt{\frac{2 \cdot \int_0^{\frac{L_r \cdot I_o}{n \cdot V_{in}}} (\frac{V_{in}}{L_r} \cdot t - \frac{I_o}{n})^2 \cdot dt + \int_0^{\frac{2 \cdot L_r \cdot I_o}{n \cdot V_{in}}} (\frac{V_{in}}{2 \cdot L_r} \cdot t)^2 \cdot dt + \int_0^{\frac{T_s}{2} - \frac{3 \cdot L_r \cdot I_o}{n \cdot V_{in}}} (\frac{I_o}{n})^2 \cdot dt + \int_0^{\frac{T_s}{2} - d_2 \cdot T_s} (\frac{I_o}{n})^2 \cdot dt}{2 \cdot T_s}}$$
$$= \sqrt{\frac{I_o^2 \cdot (1 - d_2)}{2 \cdot n^2} - \frac{5 \cdot L_r \cdot I_o^3}{6 \cdot V_{in} \cdot n^3 \cdot T_s}}$$

$$i_{1\_avg\_II} = i_{4\_avg\_II} = i_{5\_avg\_II} = i_{8\_avg\_II}$$
$$= \frac{2 \cdot \int_0^{\frac{L_r \cdot I_o}{n \cdot V_{in}}} (\frac{V_{in}}{L_r} \cdot t - \frac{I_o}{n}) \cdot dt + \int_0^{\frac{2 \cdot L_r \cdot I_o}{n \cdot V_{in}}} (\frac{V_{in}}{2 \cdot L_r} \cdot t) \cdot dt + \int_0^{\frac{T_s}{2} - \frac{3 \cdot L_r \cdot I_o}{n \cdot V_{in}}} (\frac{I_o}{n}) \cdot dt + \int_0^{\frac{T_s}{2} - d_2 \cdot T_s} (\frac{I_o}{n}) \cdot dt}{2 \cdot T_s}$$
$$= \frac{I_o \cdot d_2}{2 \cdot n} - \frac{3 \cdot L_r \cdot I_o^2}{2 \cdot V_{in} \cdot n^2 \cdot T_s}$$

$$i_{2\_rms\_II} = i_{3\_rms\_II} = i_{6\_rms\_II} = i_{7\_rms\_II}$$
$$= \sqrt{\frac{\begin{array}{l} 2 \cdot \int_0^{\frac{L_r \cdot I_o}{n \cdot V_{in}}} (\frac{V_{in}}{L_r} \cdot t - \frac{I_o}{n})^2 \cdot dt + 2 \cdot \int_0^{\frac{2 \cdot L_r \cdot I_o}{n \cdot V_{in}}} (\frac{V_{in}}{2 \cdot L_r} \cdot t)^2 \cdot dt + \int_0^{\frac{T_s}{2} - \frac{3 \cdot L_r \cdot I_o}{n \cdot V_{in}}} (\frac{I_o}{n})^2 \cdot dt \\ + \int_0^{\frac{T_s}{2} - d_2 \cdot T_s} (\frac{I_o}{n})^2 \cdot dt + \int_0^{d_2 \cdot T - \frac{3 \cdot L_r \cdot I_o}{n \cdot V_{in}}} (\frac{I_o}{n})^2 \cdot dt \end{array}}{2 \cdot T_s}}$$
$$= \sqrt{\frac{I_o^2}{2 \cdot n^2} - \frac{2 \cdot L_r \cdot I_o^3}{V_{in} \cdot n^3 \cdot T_s}}$$

$$i_{2\_avg\_II} = i_{3\_avg\_II} = i_{6\_avg\_II} = i_{7\_avg\_II}$$
$$= \frac{\begin{array}{l} 2 \cdot \int_0^{\frac{L_r \cdot I_o}{n \cdot V_{in}}} (\frac{V_{in}}{L_r} \cdot t - \frac{I_o}{n}) \cdot dt + 2 \cdot \int_0^{\frac{2 \cdot L_r \cdot I_o}{n \cdot V_{in}}} (\frac{V_{in}}{2 \cdot L_r} \cdot t) \cdot dt + \int_0^{\frac{T_s}{2} - \frac{3 \cdot L_r \cdot I_o}{n \cdot V_{in}}} (\frac{I_o}{n}) \cdot dt \\ + \int_0^{\frac{T_s}{2} - d_2 \cdot T_s} (\frac{I_o}{n}) \cdot dt + \int_0^{d_2 \cdot T - \frac{3 \cdot L_r \cdot I_o}{n \cdot V_{in}}} (\frac{I_o}{n}) \cdot dt \end{array}}{2 \cdot T_s}$$
$$= \frac{I_o \cdot d_2}{n} - \frac{5 \cdot L_r \cdot I_o^2}{2 \cdot V_{in} \cdot n^2 \cdot T_s}$$

$$i_{D9\_\mathrm{rms}\_II} = i_{D10\_\mathrm{rms}\_II} = i_{D11\_\mathrm{rms}\_II} = i_{D12\_\mathrm{rms}\_II}$$

$$= \sqrt{\frac{\int_0^{\frac{2\cdot L_r\cdot I_o}{n\cdot V_{\mathrm{in}}}} (\frac{V_{\mathrm{in}}}{2\cdot L_r}\cdot t)^2\cdot dt + \int_0^{d_2\cdot T-\frac{3\cdot L_r\cdot I_o}{n\cdot V_{\mathrm{in}}}} (\frac{I_o}{n})^2\cdot dt}{2\cdot T_s}}$$

$$= \sqrt{\frac{I_o^2\cdot d_2}{2\cdot n^2} - \frac{7\cdot L_r\cdot I_o^3}{6\cdot V_{\mathrm{in}}\cdot n^3\cdot T_s}}$$

$$i_{D9\_avg\_II} = i_{D10\_avg\_II} = i_{D11\_avg\_II} = i_{D12\_avg\_II}$$

$$= \frac{\int_0^{\frac{2\cdot L_r\cdot I_o}{n\cdot V_{\mathrm{in}}}} (\frac{V_{\mathrm{in}}}{2\cdot L_r}\cdot t)\cdot dt + \int_0^{d_2\cdot T-\frac{3\cdot L_r\cdot I_o}{n\cdot V_{\mathrm{in}}}} (\frac{I_o}{n})\cdot dt}{2\cdot T_s}$$

$$= \frac{I_o\cdot d_2}{2\cdot n} - \frac{L_r\cdot I_o^2}{V_{\mathrm{in}}\cdot n^2\cdot T_s}$$

REFERENCES

[1] P. M. Barbosa, F. Canales, J. M. Burdio, and F. C. Lee, "A three-level converter and its application to power factor correction," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1319–1327, Nov. 2005.

[2] M. A. Moonem and H. Krishnaswami, "Control and configuration of three-level dual-active-bridge dc-dc converter as a front-end interface for photovoltaic system," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 3017–3020.

[3] K. Jin and X. Ruan, "Hybrid full-bridge three-level LLC resonant converter-a novel DC-DC converter suitable for fuel-cell power system," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1492–1503, Oct. 2006.

[4] L. Tan, N. Zhu, and B. Wu, "An integrated inductor for eliminating circulating current of parallel three-level dc–dc converter based EV fast charger," *IEEE Trans. Ind. Electron.*, vol. 63, no. 3, pp. 1362–1371, Mar. 2016.

[5] S. Byeong-Mun, R. McDowell, A. Bushnell, and J. Ennis, "A three-level DC–DC converter with wide-input voltage operations for ship-electric-power-distribution systems," *IEEE Trans. Plasma Sci.*, vol. 32, no. 5, pp. 1856–1863, Oct. 2004.

[6] J. R. Pinheiro and I. Barbi, "The three-level ZVS-PWM DC-to-DC converter," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 486–492, Jul. 1993.

[7] X. Ruan, B. Li, Q. Chen, S. C. Tan, and C. K. Tse, "Fundamental considerations of three-level DC-DC converters: Topologies, analyses, and control," *IEEE Trans. Circuits Syst. I, Reg. Papers.*, vol. 55, no. 11, pp. 3733–3743, Dec. 2008.

[8] F. Canales, P. Barbosa, and F. C. Lee, "A zero-voltage and zero-current switching three-level dc/dc converter," *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 898–904, Nov. 2002.

[9] Z. Guo, K. Sun, and D. Sha, "Improved ZVS three-level dc-dc converter with reduced circulating loss," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6394–6404, Sep. 2016.

[10] B. Lin and S. Chung, "New parallel ZVS converter with less active switches and smaller output inductance," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3297–3307, Jul. 2014.

[11] I. Barbi, R. Gules, R. Redl, and N. O. Sokal, "DC/DC converter: Four switches Vpk = Vin /2, capacitive turn-off snubbing, ZV turn-on," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 918–927, Jul. 2004.

[12] Y. Shi and X. Yang, "Wide range soft switching PWM three-level DC–DC converters suitable for industrial applications," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 603–616, Feb. 2014.

[13] D. Liu, F. Deng, Q. Zhang, and Z. Chen, "Zero-voltage switching PWM strategy based capacitor current-balancing control for half-bridge three-level DC/DC converter," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 357–369, Jan. 2018.

[14] W. Li, S. Zong, F. Liu, H. Yang, X. He, and B. Wu, "Secondary-side phase-shift-controlled ZVS DC/DC converter with wide voltage gain for high input voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5128–5139, Nov. 2013.

[15] X. Ruan, Z. Chen, and W. Chen, "Zero-voltage-switching PWM hybrid full-bridge three-level converter," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 395–404, Mar. 2005.

[16] W. Chen and X. Ruan, "Zero-voltage-switching PWM hybrid full-bridge three-level converter with secondary-voltage clamping scheme," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 644–654, Feb. 2008.

[17] J. A. Carr, B. Rowden, and J. C. Balda, "A three-level full-bridge zero-voltage zero-current switching converter with a simplified switching scheme," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 329–338, Feb. 2009.

[18] F. Deng and Z. Chen, "Control of improved full-bridge three-level DC/DC converter for wind turbines in a DC grid," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 314–324, Jan. 2013.

[19] Z. Zhang and X. Ruan, "Zero-voltage-switching PWM full-bridge three-level converter," in *Proc. 4th Int. Power Electron. Motion Control Conf.*, 2004, pp. 1085–1090.

[20] Z. Zhang and X. Ruan, "A novel double phase-shift control scheme for full-bridge three-level converter," in *Proc. 20th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2005, pp. 1240–1245.

[21] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1184–1194, Sep. 2004.

[22] I.-O. Lee and G. W. Moon, "Soft-switching DC/DC converter with a full ZVS range and reduced output filter for high-voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 112–122, Jan. 2013.

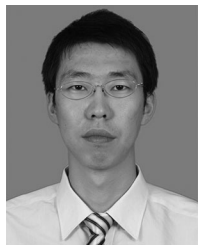
[23] K. Park and Z. Chen, "A double uneven power converter based dc-dc converter for high-power DC grid systems," *IEEE Trans. Ind. Electron.*, vol. 62, no. 12, pp. 7599–7608, Dec. 2015.

[24] H. Wang, M. Liserre, and F. Blaabjerg, "Toward reliable power electronics: Challenges, design tools, and opportunities," *IEEE Ind. Electron. Mag.*, vol. 7, no. 2, pp. 17–26, Jun. 2013.

[25] S. Yang, A. T. Bryant, P. A. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, May/Jun. 2011.

[26] K. Ma, M. Liserre, F. Blaabjerg, and T. Kerekes, "Thermal loading and lifetime estimation for power device considering mission profiles in wind power converter," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 590–602, Feb. 2015.

[27] M. T. Zhang, M. M. Jovanovic, and F. C. Lee, "Design considerations and performance evaluations of synchronous rectifications in flyback converters," *IEEE Trans. Power Electron.*, vol. 13, no. 3, pp. 538–546, May 1998.



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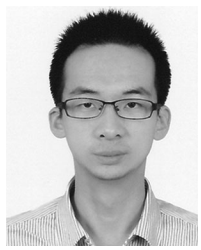

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