# An Isolated Modular Multilevel Converter (I-M$^2$C) Topology Based on High-Frequency Link (HFL) Concept

Chuang Liu, *Member, IEEE*, Chao Liu, Guowei Cai, Hong Ying, Zhenbin Zhang, *Senior Member, IEEE*, Renzhong Shan, Zhongchen Pei, and Xiaomin Song

***Abstract*—This paper introduces the high-frequency link concept into the modular multilevel converter (MMC) topology, which can totally reduce the individual dc-link capacitors at the high-voltage side. The proposed converter, called isolated MMC, has basic triple ports of medium-voltage ac, medium-voltage dc, and low-voltage dc. Thus, it is especially suitable for hybrid dc and ac applications in power generation and transmission, such as solid-state transformer. The fundamental principle and applied control scheme of phase-shift pulsewidth modulation are presented in detail. The design of the voltage clamping circuit and analysis of duty loss are carried out. The experimental results are given to illustrate the efficient operation characteristics.**

***Index Terms*—High-frequency link (HFL), hybrid ac and dc power conversion, isolated modular multilevel converter (I-M$^2$C), solid-state transformer (SST).**

## NOMENCLATURE

| | |
|---|---|
| $C_{\mathrm{dc}L}$ | LVdc capacitor. |
| $C_{\mathrm{dc}H}$ | HVdc split capacitor. |
| $C_{dH}$ | HVdc capacitor. |
| $C_k$ | Voltage clamping capacitor. |
| $D$ | DC modulation ratio. |
| DLP | Double line-frequency power. |
| $D_{\mathrm{pr}}$ | Equivalent primary modulation ratio. |
| $D_{\mathrm{se}}$ | Equivalent secondary modulation ratio. |
| $d_a$ | AC modulation ratio. |
| $d_{u(l)}$ | Upper (lower) SM modulation ratio. |
| $d_{p(n)}$ | Leading (lagged)-leg modulation ratio. |
| $E_r$ | Resonant energy. |
| $f_c$ | Carrier wave frequency. |
| $i_{\mathrm{acu}}$ | Upper arm current. |
| $i_{\mathrm{acl}}$ | Lower arm current. |
| $i_{1(2)}$ | Primary (secondary) current of transformer. |
| $I_{\mathrm{dc}L}$ | LVdc side current. |
| $I_{\mathrm{dc}H}$ | HVdc side current. |
| $i_L$ | Filter inductor current. |
| $k$ | Turn ratio of transformer. |
| $L_f$ | Filter inductor. |
| $L_{um}$ | Arm inductor. |
| $L_r$ | Transformer leakage inductor. |
| $R_k$ | Voltage clamping resistance. |
| $T_c$ | Carrier cycle. |
| $T_s$ | Switching cycle. |
| $v_{su}$ | Upper arm voltage. |
| $v_{sl}$ | Lower arm current. |
| $V_{\mathrm{dc}L}$ | LVdc port voltage. |
| $v_{\mathrm{ac}}$ | HVac port voltage. |
| $V_{\mathrm{dc}H}$ | HVdc port voltage. |
| $v_{1(2)}$ | Primary (secondary) voltage of transformer. |

Manuscript received August 30, 2018; revised November 19, 2018, January 14, 2019, March 8, 2019, and April 20, 2019; accepted May 31, 2019. Date of publication June 16, 2019; date of current version November 12, 2019. This work was supported in part by The National Natural Science Foundation of China under Grant 51877035 and in part by the Science and Technology project of Zhejiang Huayun Clean Energy Co. Ltd. under Grant 0111_201804_F_PWSYB_000. Recommended for publication by Associate Editor Dr. Harish Krishnamoorthy. *(Corresponding author: Chuang Liu.)*

Chuang Liu, Chao Liu, G. Cai, Z. Pei, and X. Song are with the School of Electrical Engineering, Northeast Electric Power University, Jilin 132012, China (e-mail: victorliuchuang@163.com; 774416591@qq.com; cai4806439@126.com; 84868286@qq.com; 616031625@qq.com).

H. Ying is with the Zhejiang Huayun Clean Energy Co. Ltd., Hangzhou, China (e-mail: Ying_Hong@zj.sgcc.com.cn).

Z. Zhang and R. Shan are with the School of Electrical Engineering, Shandong University, Jinan 250100, China (e-mail: zbz@sdu.edu.cn).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2019.2923355

## I. INTRODUCTION

CURRENTLY, solid-state transformer (SST) has been conceived as a good replacement for the conventional line-frequency transformer because of its inherent advantages such as small volume, light weight, controllability, multiports, and other aspects [1]–[5]. SST-based solid-state substation (SSS) has received a good deal of attention as a key equipment for the flexible grid integration of renewable energy systems [6]–[8]. The SST systems are generally based on the input-series output-parallel (ISOP) configuration of submodules (SMs), since modular architecture has significant advantages in scalability and maintenance of power and voltage, fault-tolerance strategy implementation. The modular SST topologies could be classified into two broad categories: the structures based on cascaded H-bridge (CHB) converter [9]–[13] and modular multilevel converter (MMC) [5], [14].

As Fig. 1(a) shows, the SST based on CHB converter consists of a cascaded H-Bridge converter and high-frequency isolated dc–dc converters. A lot of isolated dc–dc converter topologies have been employed in this type SST to inject/drag power from the CHB cells, such as phase-shift H-bridge (PSHB) converter

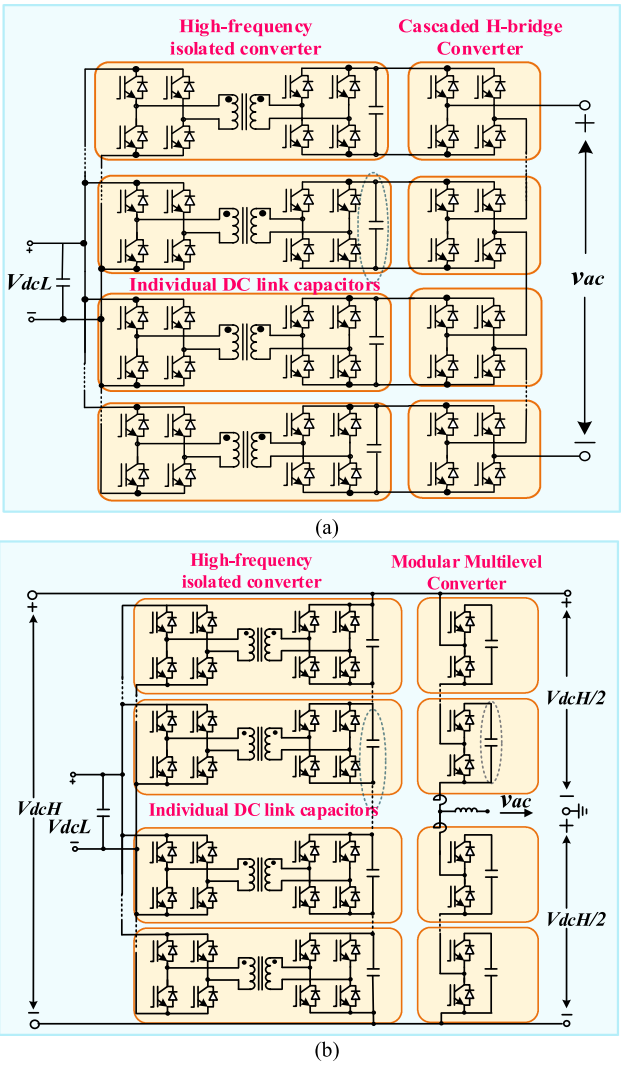



Fig. 1. Two typical SST topologies. (a) Single-phase CHB converter-based SST topology. (b) Single-phase MMC-based SST topology.

[12], [15], *LLC*/*CLLC* resonant converter [16]–[19], dual-active-bridge (DAB) converter [11], [20]–[23]. A detailed analysis and design of such cascaded systems can be found in [13] where using power semiconductors with blocking voltage of 1.2/1.7 kV has been identified to be an optimum scheme in terms of efficiency and power density. Additionally, the SM of CHB can be replaced with dual-buck/boost converter [9], neutral-point-clamped converter (NPC) [24], etc.

As Fig. 1(b) shows, the MMC-based SST can be seen as an evolution of the SST based on CHB converter. The major advantage of MMC-based SST is the added medium-voltage dc (MVdc) link, which is an additional connection point of SST. It is a potential way to integrate new loads and renewable sources, such as fast charging electric vehicle (EV) stations, distributed renewable energy systems, large photovoltaic, and wind power plants and battery energy storage systems. To provide power conversion between the MVdc and low-voltage dc (LVdc) ports, the high-frequency isolated dc–dc converters-based ISOP configuration is usually adopted in SST [25]–[27].

In order to overcome the MVdc side faults, the basic half-bridge SM (HBSM) of MMC can be replaced with hybrid SM topologies [28], such as the full-bridge SM (FBSM), the clamp double SM (CDSM), the clamp single SM (CSSM), and the improved hybrid SM. However, it will make the SST more complex and costly.

MMC has been widely used in the SST because of its modular realization, multilevel waveform, MVac, dc ports, etc. [29], [30]. However, it still has several drawbacks due to its structural characteristics. For instance, there are bulky capacitors of SMs to limit the voltage fluctuation since the power conversion between MVac and MVdc is handled by each SM, which reduces the power density and increases the system costs. Moreover, the resulting complicated capacitor voltage balance control strategy is another major problem.

For overcoming the abovementioned problems, this paper introduces the high-frequency link (HFL) concept [31]–[39] into the MMC structure and proposes an innovative HFL isolated modular multilevel converter (I-M$^2$C) topology. The novel topology not only inherits the main merits of conventional MMC such as modular structure, multiport and multilevel waveform, but also realizes the single-stage power conversion between MVdc/ac sides and LVdc side, which eliminates the bulky dc-link capacitors at high-voltage (HV) side and the complicated capacitor voltage balance control strategy. Compared with the matrix-based single-stage SSTs, the proposed topology does not need bidirectional switches at HV side and the complicated commutation control strategy, since the voltage of the SM in I-M$^2$C is always positive.

The rest of this paper is organized as following. In Section II, the concept of the HFL I-M$^2$C is introduced. A detailed single-phase structure and its basic high-frequency-link SM (HFL-SM) are explained. In Section III, the modulation strategy and operation principles of I-M$^2$C are described. Power transfer steady analysis among multiports is provided in Section IV. Then, the design of the voltage clamping circuit and analysis of duty loss are carried out in Section V. In Section VI, the experimental results verify the feasibility of the novel I-M$^2$C topology.

## II. HFL Isolated Modular Multilevel Converter (HFL I-M$^2$C)

### A. Concept of Single-Phase I-M$^2$C

The diagram of single-phase HFL I-M$^2$C is depicted in Fig. 2. The single-phase I-M$^2$C is formed by two arms. Each arm consists of $n$ HFL-SMs, which are parallel connected at common LV side and series connected at HV side. Regardless of the voltage drop of leakage and arm inductors, the voltage of upper and lower arms can be obtained by

$$\begin{cases} v_{\mathrm{su}} = n \times \frac{V_{\mathrm{dcL}}}{k} \times d_u = n \times \frac{V_{\mathrm{dcL}}}{k} \times (D + d_a) \\ v_{\mathrm{sl}} = n \times \frac{V_{\mathrm{dcL}}}{k} \times d_l = n \times \frac{V_{\mathrm{dcL}}}{k} \times (D - d_a). \end{cases} \tag{1}$$

According to (1), the equivalent circuit of I-M$^2$C at HV side is shown in Fig. 3. Based on the KVL voltage principle, the

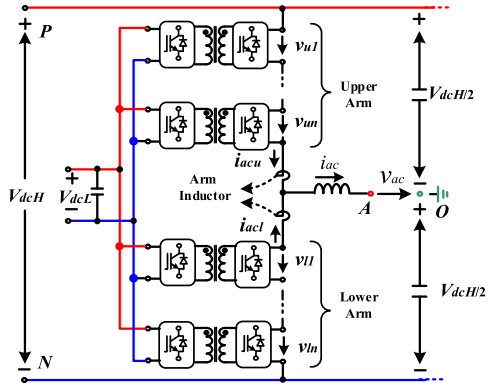



Fig. 2. Topology structure of the proposed single-phase I-M$^2$C.

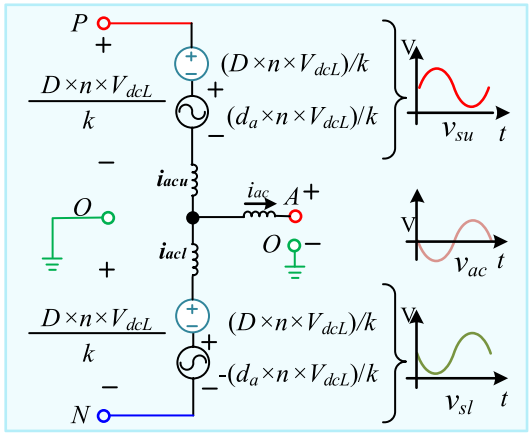



Fig. 3. Equivalent circuit of HV side in the proposed single-phase HFL I-M$^2$C leg.

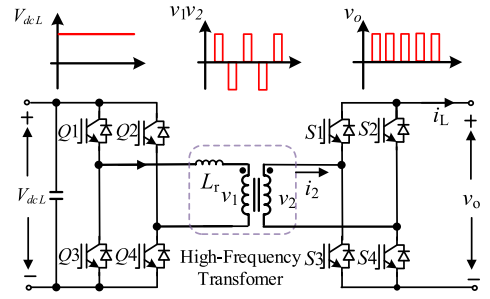



Fig. 4. Topology structure of HFL-SM.

voltages of the HVac and HVdc ports can be derived by

$$\begin{cases} V_{\mathrm{dc}H} = D \cdot 2n \cdot V_{\mathrm{dc}L} \\ v_{\mathrm{ac}} = -d_a \cdot n \cdot V_{\mathrm{dc}L}. \end{cases} \tag{2}$$

### B. Circuit Description of HFL-SM

The circuit configuration of HFL-SM in I-M$^2$C is shown in Fig. 4, where the proposed SM consists of primary full-bridge ($Q_1$–$Q_4$), secondary full-bridge ($S_1$–$S_4$), and high-frequency transformer (HFT) with primary equivalent leakage inductor $L_r$.

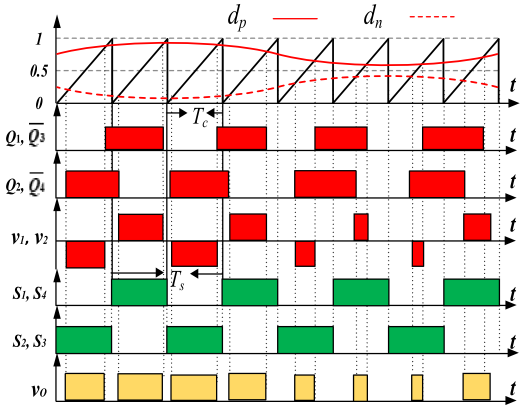



Fig. 5. Unified modulation strategy for HFL-SM.

HFT performs the task of voltage level conversion and the electrical isolation. Due to the positive output voltage, the operation modes of HFL-SM can be divided into two basic types based on the direction of the output current ($i_L$): buck mode ($i_L > 0$) and boost mode ($i_L < 0$).

A unified modulation strategy for two modes is illustrated in Fig. 5, where $Q_1$–$Q_4$ and $S_1$–$S_4$ are driven signals of the corresponding switches; $d_p$ and $d_n$ are modulation signals of leading-leg and lagging-leg in primary full-bridge, respectively; $v_1$ and $v_2$ are primary and secondary pulsewidth voltages of the HFT, respectively; $v_o$ is output voltage of the HFL-SM. As Fig. 5 shows, the secondary devices are switched during the time when $v_o$ equals to zero due to the proposed modulation strategy. Thus, the voltage oscillation caused by current commutation is avoided. It is noted that the switching cycle period is two times as much as the carrier cycle period.

According to (2), the modulation ratios for I-M$^2$C can be derived by

$$\begin{cases} d_{\mathrm{up}} = 0.5 + d_u = 0.5 + 0.5 \times [D + d_a] \\ d_{\mathrm{un}} = 0.5 - d_u = 0.5 - 0.5 \times [D + d_a] \\ d_{\mathrm{lp}} = 0.5 + d_l = 0.5 + 0.5 \times [D - d_a] \\ d_{\mathrm{ln}} = 0.5 - d_l = 0.5 - 0.5 \times [D - d_a] \end{cases} \tag{3}$$

where $d_{\mathrm{up}(n)}$ is leading-leg (lagging-leg) modulation signal for HFL-SMs in upper arm; $d_{\mathrm{lp}(n)}$ is leading-leg (lagging-leg) modulation signal for HFL-SMs in lower arm.

Different from CHB converter and MMC-based SST structures, the DLP is buffered by the common capacitors at LVdc side in I-M$^2$C instead of the intermediary dc-link capacitors. Hence, the proposed topology eliminates intermediary dc-link capacitors at HV side. Additionally, a simply auxiliary circuit with power decoupling control can be employed at the primary side to further improve the power density [38]. The detailed multilevel modulation scheme and the operation principle of the HFL I-M$^2$C will be illustrated in the following chapter.

## III. Modulation Strategy and Operation Principle of HFL I-M$^2$C

Due to the modularized topology, phase-shift pulsewidth modulation (PSPWM) is the optimum modulation method for

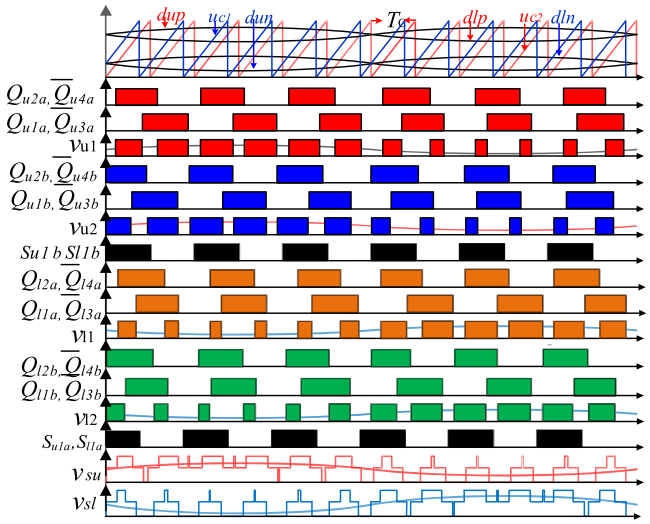



Fig. 6. Driven signal modulation strategy for proposed I-M$^2$C.

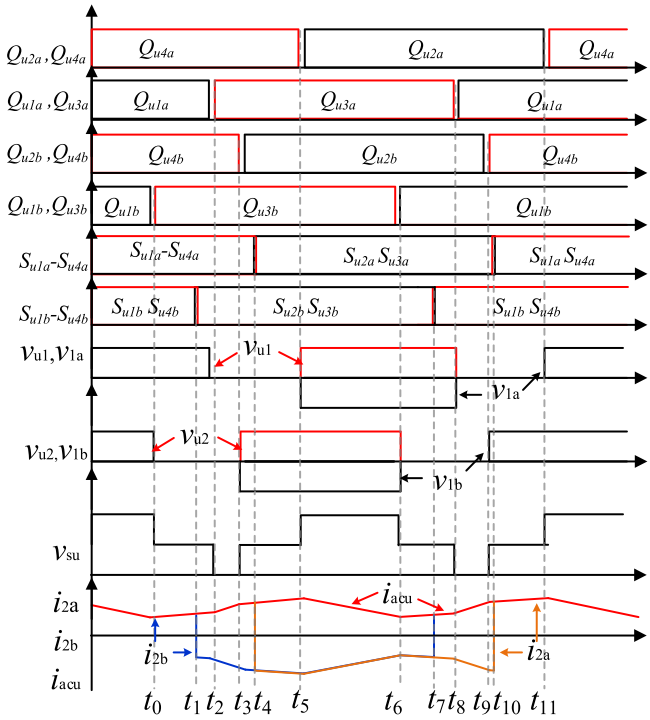



Fig. 7. Theoretical waveforms of upper arm of I-M$^2$C in boost mode.

I-M$^2$C. The modulation strategy can achieve the effect of high equivalent switching frequency at a lower switching frequency, which improves the output performance and reduces the requirement of filter. Thus, it is widely used in the modular high-power electrical devices. The proposed modulation scheme based on (3) is briefly explained with the aid of Fig. 6, where $u_{c1}$ and $u_{c2}$ are the carrier waves for SM$_{u(l)\,1}$ and SM$_{u(l)2}$, respectively. In Fig. 4, $u_{c2}$ is delayed by $T_c/4$ compared with $u_{c1}$, and the equivalent switching frequency of the arm voltage is two times as much as that of HFL-SMs. The following part will only introduce the boost working mode of upper arm in detail because the operating mode of the lower arm is symmetrical with that of the upper arm and the operation principle of buck mode of the HFL-SM is similar to the conventional PSFB converter with the varying duty ratio. To simplify the analysis, this paper assumes that the body capacitance of switches is negligible and current commutation process is so little that it can be viewed as instantaneous fulfilled.

The theoretical waveforms and commutation step diagrams of upper arm of I-M$^2$C in boost operating mode are shown in Figs. 7 and 8, where $Q_{u1a(b)}$–$Q_{u4a(b)}$ and $S_{u1a(b)}$–$S_{u4(a)b}$ represent driven signals of corresponding switches; HFT$_1$ and HFT$_2$ are the HFTs of SM$_{u1}$ and SM$_{u2}$, respectively; $i_{1b}$ and $i_{1a}$ are primary currents of HFT$_1$ and HFT$_2$, respectively; $i_{2b}$ and $i_{2a}$ are secondary currents of HFT$_1$ and HFT$_2$, respectively; $v_{1b}$ and $v_{1a}$ are primary voltages of HFT$_1$ and HFT$_2$, respectively; $v_{u1}$ and $v_{u2}$ are output voltages of SM$_{u1}$ and SM$_{u2}$, respectively; $i_{\rm acu}$ is the inductor current of the upper arm.

One complete switching cycle of upper arm is divided into 12 steps in this mode. The operation conditions of the latter six steps are symmetric with the former six steps. The former six steps are explained in detail as follows.

*Stage 0.* *[before $t_0$, Fig. 8(a)]:* Prior to $t_0$, $Q_{u2b}$ and $Q_{u3b}$ are in off-state and $S_{u1b}$ and $S_{u4b}$ are in on-state. The operating state of SM$_{u2}$ is same as that of SM$_{u1}$ because of the same driven signals. The energy at the HV side backflows to the common LVdc side. Thus, $i_{\rm acu}$ decreases over time. In this process, $v_{su} = 2V_{{\rm dc}L}$.

*Stage 1.* *[$t_0$–$t_1$, Fig. 8(b)]:* This interval starts at $t_0$ when $Q_{u3b}$ is turned on. In SM$_{u1}$, $i_{1b}$ is commutated from the antiparallel diode of $Q_{u1b}$ to $Q_{u3b}$. $i_{1b}$ only flows through the antiparallel diode of $Q_{u1b}$ instead of $Q_{u1b}$, which realizes ZVS switching of $Q_{u1b}$. $i_{1b}$ can be viewed as maintained constant since the filter inductor is reflected to the primary side of HFT$_1$. The working mode of SM$_{u2}$ is same as that in the stage 0. The energy at the HV side backflows to the common LVdc side by SM$_{u2}$. In this process, $v_{su} = V_{{\rm dc}L}$.

*Stage 2.* *[$t_1$–$t_2$, Fig. 8(c)]:* In SM$_{u1}$, $S_{u2b}$ and $S_{u3b}$ are turned on while $S_{u1b}$ and $S_{u4b}$ are turned off. In practice, an overlap high level dead band must be guaranteed for commutation of $i_{2b}$. The trend of $i_{1b}$ is consistent with that of $i_{1a}$. The working mode of SM$_{u2}$ is same as that in the stage 0. In this process, $v_{su} = V_{{\rm dc}L}$.

*Stage 3.* *[$t_2$–$t_3$, Fig. 8(d)]:* $Q_{u3a}$ is turned on at $t_2$. At the same time, $i_{1a}$ is commutated from the antiparallel diode of $Q_{u1a}$ to $Q_{u3a}$. $i_{1a}$ only flows through the antiparallel diode of $Q_{u1a}$ instead of $Q_{u1a}$, which realizes ZVS switching of $Q_{u1a}$. In this stage, the working mode of SM$_{u2}$ is same as that of SM$_{u1}$ in Stage1. The HV side stops transferring power to common LV side. $v_{su} = 0$ and $i_{\rm acu}$ increases during this stage.

*Stage 4.* *[$t_3$–$t_4$, Fig. 8(e)]:* In SM$_{u1}$, $Q_{u4b}$ is turned off. At the same time, $i_{1a}$ is commutated from $Q_{u4b}$ to the antiparallel diode of $Q_{u2b}$. Then, $Q_{u2b}$ is turned on with

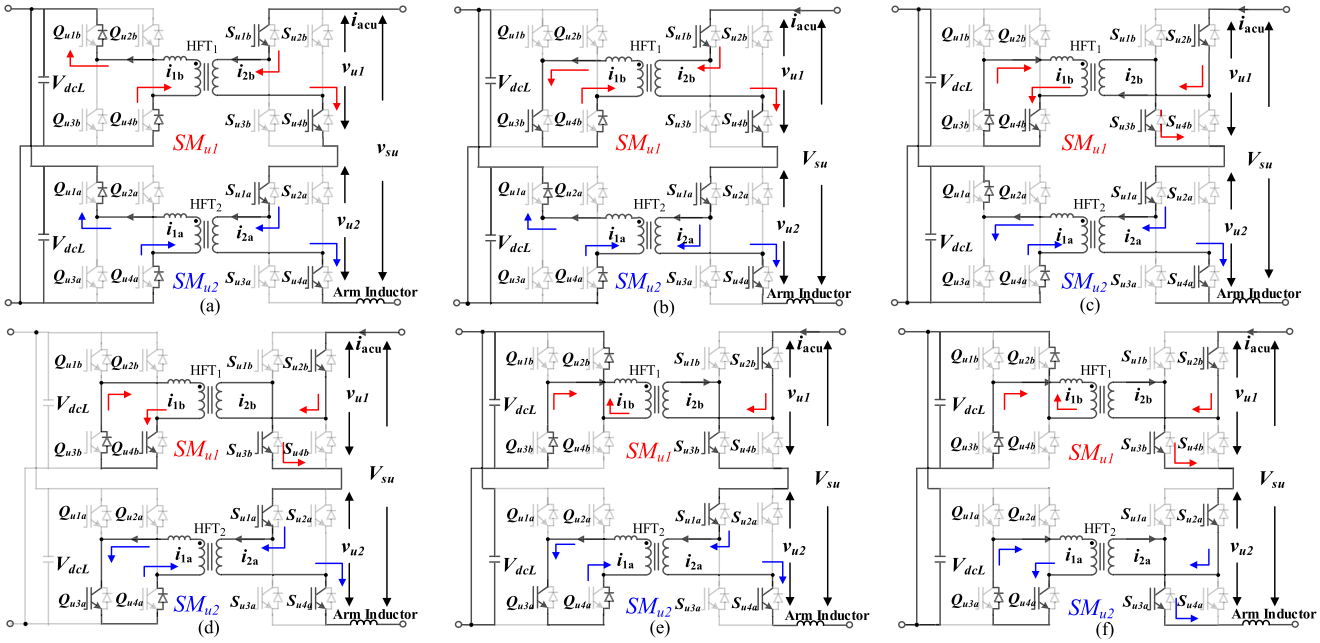



Fig. 8. Commutation step diagrams of upper arm of I-M$^2$C in boost mode. (a) Stage 0. (b) Stage 1. (c) Stage 2. (d) Stage 3. (e) Stage 4. (f) Stage 5.

ZVS. In this stage, $\mathrm{SM}_{u1}$ transfers power from HV side to LV side. $\mathrm{SM}_{u2}$ remains the pervious working mode in this interval and $v_{su} = V_{\mathrm{dc}L}$.

*Stage 5.* *[$t_4$–$t_5$, Fig. 8(f)]:* In $\mathrm{SM}_{u2}$, $S_{u2a}$ and $S_{u3a}$ are turned on while $S_{u1a}$ and $S_{u4a}$ are turned off. In this stage, the working state of $\mathrm{SM}_{u2}$ is same as that of $\mathrm{SM}_{u1}$ in Stage 2 and $v_{su} = V_{\mathrm{dc}L}$.

At $t_5$, $Q_{u4a}$ is turned off while $i_{2a}$ is commutated from $Q_{u4a}$ to antiparallel diode of $Q_{u2a}$ and the latter six stages start. The operation states of $\mathrm{SM}_{u1}$ and $SM_{u2}$ in stage 6 are symmetrical with that in stage 0, which transfers power to LV side.

## IV. Power Transfer Steady-State Analysis Among HVAC, HVDC, and LVDC Ports in I-M$^2$C

Because of the three basic power-transfer ports, I-M$^2$C has a set of average power transfer (APF) operating modes, such as conventional MMC mode (power flows between HVac and HVdc ports), isolated cascade converter mode (power flows between HVac and LVdc ports), dc-transformer mode (power flows between HVdc and LVdc ports), and SSS mode (power flows among HVac, HVdc, and LVdc ports). The following will give the detailed power transfer steady-state analysis.

### A. Equivalent Average Model of Single-Phase I-M$^2$C

Fig. 9 shows the equivalent average model of the single-phase I-M$^2$C leg. The SMs' terminals at the HV side are represented by the controlled voltage sources $v_{ui}$ or $v_{li}$ $(i = 1, \ldots, n)$ with the hybrid ac and dc modulation ratios, which is found in (3). Equation (4) shows the relation among arm current $i_{\mathrm{acu}(l)}$ and

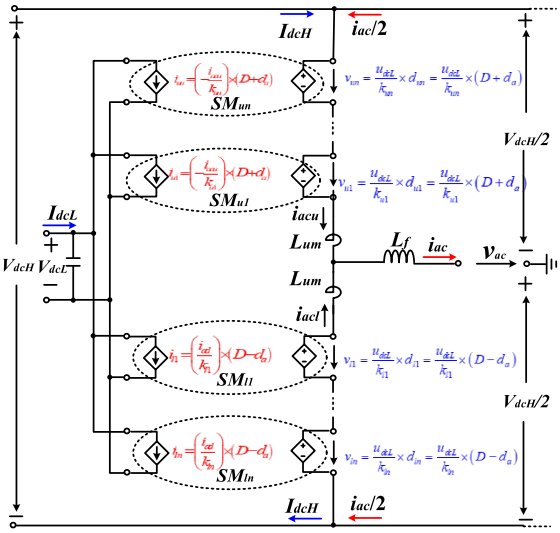



Fig. 9. Equivalent average model of single-phase I-M$^2$C leg.

HV port currents $I_{\mathrm{dc}H}$ and $i_{\mathrm{ac}}$

$$\begin{cases} i_{\mathrm{acu}} = I_{\mathrm{dc}H} + \frac{i_{\mathrm{ac}}}{2} \\ i_{\mathrm{acl}} = -I_{\mathrm{dc}H} + \frac{i_{\mathrm{ac}}}{2}. \end{cases} \tag{4}$$

According to (1) and (4), the HV terminal instantaneous output power of the proposed HFL-SMs is given by

$$\begin{cases} p_{ui}(t) = -\frac{V_{\mathrm{dc}L}}{K_{ui}}\left(D + d_a\right)\left(I_{\mathrm{dc}H} + \frac{i_{\mathrm{ac}}}{2}\right) \\ p_{li}(t) = \frac{V_{\mathrm{dc}L}}{K_{li}}\left(D - d_a\right)\left(-I_{\mathrm{dc}H} + \frac{i_{\mathrm{ac}}}{2}\right) \end{cases} \quad (i = 1, \ldots, n) \tag{5}$$

where $d_u = D + d_a$, $d_l = D - d_a$, $k_{ui} = k_{li} = k(i = 1, \ldots, n)$.

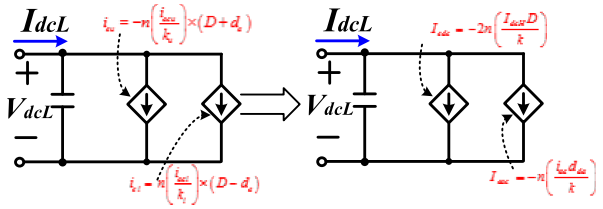



Fig. 10. Equivalent average model at the common LVdc side of single-phase I-M$^2$C leg.

Based on (5), it can be seen that $P_{ui}$ or $P_{li}$ $(i = 1, \ldots, \mathrm{n})$, the average power of $\mathrm{SM}_{ui}$ or $\mathrm{SM}_{li}$, consists of two parts: $P_{\mathrm{HVacu}(l)i}$ and $P_{\mathrm{HVdcu}(l)i}$ $(i = 1, \ldots, \mathrm{n})$. They are given by

$$\begin{aligned} P_{u(l)i} &= \frac{1}{T_g}\int_t^{t+T_g} p_{u(l)i}(t)dt \\ &= P_{\mathrm{HVacu}(l)i} + P_{\mathrm{HVdcu}(l)i}\ (i = 1, \ldots, n) \end{aligned} \tag{6}$$

where $T_g$ is the line-frequency period.

Moreover, because the total sum of three-phase DLP fluctuation is nearly constant, the three-phase I-M$^2$C system can cut down the number of common LVdc capacitors, which effectively reduces the volume and cost.

Based on (4), the equivalent average model at the common LVdc side is shown in Fig. 10. And the equivalent injecting instantaneous current $I_{\mathrm{edc}}$ and $I_{eac}$ at the common dc side are given by (7), which are equal to the sum of the all SMs' current components. The common LVdc current $I_{\mathrm{dc}L}$ is an average of $(I_{\mathrm{edc}} + I_{\mathrm{eac}})$, which is derived by

$$\begin{cases} I_{\mathrm{edc}}(t) = -2n(I_{\mathrm{dc}H}D)/k \\ I_{eac}(t) = -n(i_{\mathrm{ac}}d_a)/k \end{cases} \tag{7}$$

$$\begin{aligned} I_{\mathrm{dc}L} &= \frac{1}{T_g}\int_t^{t+T_g} \left[-2n(I_{\mathrm{dc}H}D)/k - n(i_{\mathrm{ac}}d_a)/k\right] dt \\ &= -2n(I_{\mathrm{dc}H}D)/k - \frac{n}{kT_g}\int_t^{t+T_g} \left[(i_{\mathrm{ac}}d_a)\right] dt. \end{aligned} \tag{8}$$

### *B. Steady-State Analysis of APF in I-M$^2$C*

According to the equivalent average model of single-phase I-M$^2$C leg, the voltage loop equations at the HVac and dc sides are given by

$$\begin{cases} v_{\mathrm{ac}} = -n\frac{V_{\mathrm{dc}L}}{k}(D + d_a) - \left(L_f + \frac{L_{um}}{2}\right)\frac{di_{ac}}{dt} + \frac{V_{\mathrm{dc}H}}{2} \\ v_{\mathrm{ac}} = n\frac{V_{\mathrm{dc}L}}{k}(D - d_a) - \left(L_f + \frac{L_{um}}{2}\right)\frac{di_{\mathrm{ac}}}{dt} - \frac{V_{\mathrm{dc}H}}{2} \end{cases} \tag{9}$$

$$V_{\mathrm{dc}H} = n\frac{V_{\mathrm{dc}L}}{k}(D + d_a) + n\frac{V_{\mathrm{dc}L}}{k}(D - d_a) = 2n\frac{V_{\mathrm{dc}L}}{k}D \tag{10}$$

where the current ripple of $I_{\mathrm{dc}H}$ is not considered and $D$ is usually set at 0.5.

From (9) and (10), the simplified (9) is given by

$$v_{\mathrm{ac}} = -n\frac{V_{\mathrm{dc}L}}{k}d_a - \left(L_f + \frac{L_{um}}{2}\right)\frac{di_{\mathrm{ac}}}{dt}. \tag{11}$$

And if $v_{\mathrm{ac}}$ and $i_{\mathrm{ac}}$ are set as (12), $d_a$ can be given by

$$\begin{cases} v_{\mathrm{ac}} = V_{gp}\sin(\omega t) \\ i_{\mathrm{ac}} = I_{gp}\sin(\omega t - \varphi) \end{cases} \tag{12}$$

$$d_a = \frac{\sqrt{a^2 + b^2}\sin(\omega t + \phi_a)}{n\frac{V_{\mathrm{dc}L}}{k}} \tag{13}$$

where

$$\begin{cases} a = -V_{gp} - I_{gp}\omega\left(L_f + \frac{L_m}{2}\right)\sin\varphi \\ b = -I_{gp}\omega\left(L_f + \frac{L_m}{2}\right)\cos\varphi \\ \varphi_a = \arctan\left(\frac{b}{a}\right). \end{cases} \tag{14}$$

Ignoring the loss of SMs and inductor, the active power $P_{\mathrm{HVac}}$ can be calculated by

$$\begin{aligned} P_{\mathrm{HVac}} &= \sum_{i=1}^{n} P_{\mathrm{HVacu}(l)i} \\ &= -\frac{V_{\mathrm{dc}L}}{kT_g}\sum_{i=1}^{n}\int_t^{t+T_g}(d_a i_{\mathrm{ac}})dt. \\ &\approx V_{gp}I_{gp}\cos\varphi/2 \end{aligned} \tag{15}$$

If $\varphi = 0$ ($P_{\mathrm{HVac}}$ is transferred from HVdc and LVdc sides to HVac side) or $\varphi = \pi$ ($P_{\mathrm{HVac}}$ is transferred from HVac side to HVdc and LVdc sides), no reactive power $Q_{\mathrm{HVac}}$ is delivered to the HVac grid. Considering modular and redundant design, the same active power operation mode of HFL-SMs is usually adopted in real high-power applications. The required HVac grid current $i_{\mathrm{ac}}$ is generated by controlling the same ac modulation ratio $d_a$ of upper and lower arm in together. The same active power $P_{\mathrm{HVacu}(l)i}$ $(i = 1, \ldots, n)$ is delivered between each SM terminal and HVac grid because of the same ac modulation ratio.

The SM terminal power $P_{\mathrm{HVacu}(l)i}$ $(i = 1, \ldots, n)$ can be supported by HVdc and LVdc ports. The active power $P_{\mathrm{HVdcu}(l)i}$ $(i = 1, \ldots, n)$ delivering between each SM and HVdc side should be satisfied as

$$\begin{cases} P_{\mathrm{HVdc}} = V_{\mathrm{dc}H} \times I_{\mathrm{dc}H} = 2n\frac{V_{\mathrm{dc}L}}{k}D \times I_{\mathrm{dc}H} \\ P_{\mathrm{HVdcui}} = -\frac{V_{\mathrm{dc}L}}{K_{ui}}D_i \times I_{\mathrm{dc}H} = -\frac{V_{\mathrm{dc}L}}{K}D \times I_{\mathrm{dc}H} \\ P_{\mathrm{HVdcli}} = -\frac{V_{\mathrm{dc}L}}{K_{li}}D_i \times I_{\mathrm{dc}H} = -\frac{V_{\mathrm{dc}L}}{K}D \times I_{\mathrm{dc}H} \\ \sum_{i=1}^{n} P_{\mathrm{HVdcui}} + \sum_{i=1}^{n} P_{\mathrm{HVdcli}} = -P_{\mathrm{HVdc}}. \end{cases} \tag{16}$$

Based on (8), the input power $P_{\mathrm{dc}L}$ at the common LVdc side is given by

$$\begin{aligned} P_{\mathrm{dc}L} &= V_{\mathrm{dc}L} \times I_{\mathrm{dc}L} \\ &= -2n\frac{V_{\mathrm{dc}L}}{k}I_{\mathrm{dc}H}D - n\frac{V_{\mathrm{dc}L}}{kT_g}\int_t^{t+T_g}\left[(i_{\mathrm{ac}}d_a)\right]dt \\ &= -P_{\mathrm{HVdc}} + P_{\mathrm{HVac}}. \end{aligned} \tag{17}$$

It has two equivalent parts: dc power $P_{\mathrm{HVdc}}$ flowing from HVdc grid, ac active power $P_{\mathrm{HVac}}$ flowing from HVac grid. Thus, the detailed calculation of different APF operation modes can be easily derived for the system analysis and control design based on the above analysis among $P_{\mathrm{HVac}}$, $P_{\mathrm{HVdc}}$, and $P_{\mathrm{LVdc}}$.

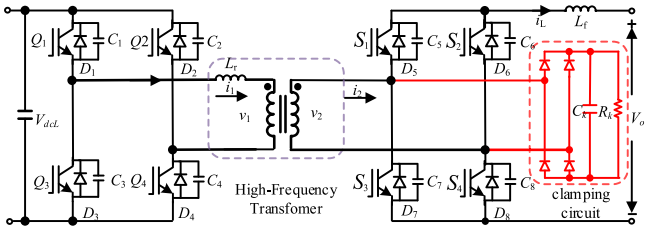



Fig. 11. Topology structure of HFL-SM with clamping circuit.

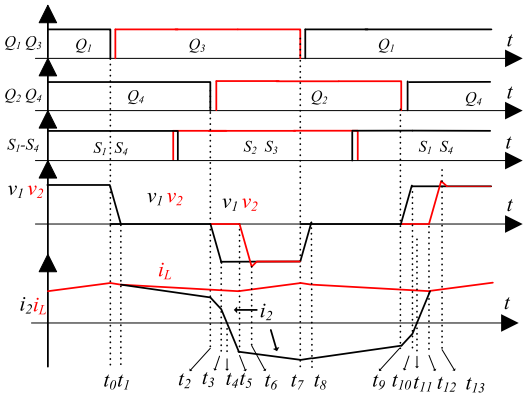


Fig. 12. Theoretical waves of HFL-SM with clamping circuit.

## V. Design of Voltage Clamping Circuit and Analysis of Duty Loss

There is a spike voltage and shock on conventional PSFB converter vice side rectifier diodes, which reduces the system reliability. When the proposed topology works in buck mode, it has the same problem because of the similar operation principle. An resistance, capacitor and diode (RCD) method of auxiliary absorption circuit is employed to suppress the spike voltage, as shown in Fig. 11. Considering the stray capacitances, the theoretical waves of HFL-SM with the clamping circuit in buck operation mode are shown in Fig. 12. The following will introduce the operation principle of the clamping circuit.

As Fig. 12 shows, one complete switching cycle of the proposed structure can be divided into 14 steps. And the working states of the latter seven steps are symmetric with the former seven steps. The equivalent circuits for former seven operating stages are shown in Fig. 13, and the corresponding stage is explained in detail as follows.

*Stage 0.* *[Before $t_0$, Fig. 13(a)]:* Before $t_0$, $Q_1$ and $Q_4$ are conducting at primary side; $D_5$ and $D_8$ are conducting at secondary side. $C_6$ and $C_7$ are fully charged. The stage is called the power transfer stage since primary side transfers power to secondary side.

*Stage 1.* *[$t_0$–$t_1$, Fig. 13(b)]:* At the instant $t_0$, $Q_1$ is turned off. $C_1$ begins to charge while $C_3$ begins to discharge at primary side; $C_6$ and $C_7$ discharge at secondary side. The voltages and currents across primary side and secondary side of the HFT begin to decrease. The primary side of the proposed SM stops transferring power to the secondary side. However, the decreasing

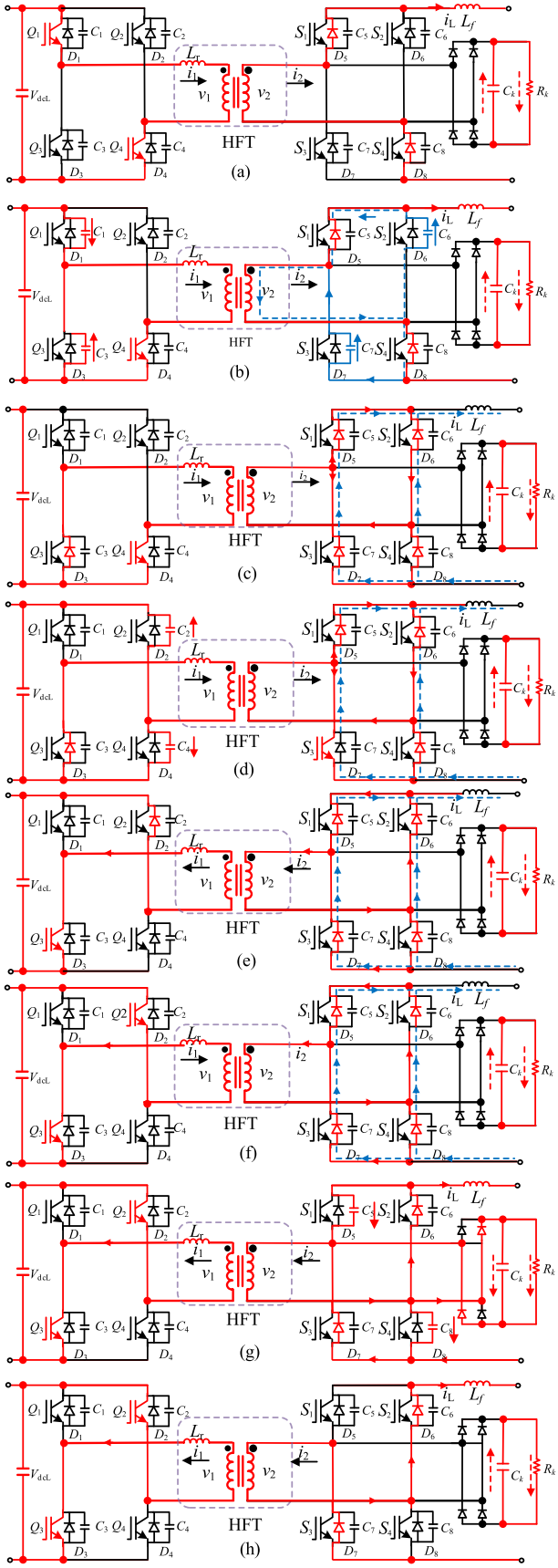



Fig. 13. Commutation step diagrams of the HFL-SM with clamping circuit. (a) Stage 0. (b) Stage 1. (c) Stage 2. (d) Stage 3. (e) Stage 4. (f) Stage 5. (g) Stage 6. (h) Stage 7.

rate of $i_L$ is very small because of the large filter inductance.

*Stage 2.* *[$t_1$–$t_2$, Fig. 13(c)]:* This stage begins when the voltage of $C_1$ increases to $V_{\mathrm{dc}L}$ and the voltage of $C_3$ decreases to zero. In this stage, $D_3$ is conducting. Thereby, $Q_3$ can be turned on at zero voltage. At the same time, the voltages of $C_6$ and $C_7$ and $v_2$ decrease to zero. All secondary side diodes are conducting since the filter inductance is so large that it can be seen as a constant current source. Secondary side of the transformer is shorted and the inductor current is freewheeling. Due to the filter inductance is much larger than the leakage inductance, the decreasing rate of the $i_2$ is bigger than that of $i_L$. In this stage, the switching actions of $S_1$–$S_4$ can be neglected because of the secondary freewheeling state.

*Stage 3.* *[$t_2$–$t_3$, Fig. 13(d)]:* At $t_2$, $Q_4$ is turned off. Then $C_2$ starts to discharge and $C_4$ starts to charge.

*Stage 4.* *[$t_3$–$t_4$, Fig. 13(e)]:* This stage starts when voltage of $C_4$ increases to $V_{\mathrm{dc}L}$ and the voltage of $C_2$ decreases to zero. $D_2$ is conducting, and $i_2$ reduces rapidly because $v_1$ is equal to $-V_{\mathrm{dc}L}$. Then $Q_2$ is turned on at zero voltage because the current flows through the $D_2$. Power cannot be transmitted from primary side to secondary side since $|i_2|$ is smaller than $i_L$.

*Stage 5.* *[$t_4$–$t_5$, Fig. 13(f)]:* At $t_4$, $i_1$ decreases to zero and $Q_2$ is conducting. Then $i_1$ increases in the opposite direction, which flows through the $Q_2$ and $Q_3$. Because $|i_2|$ is still smaller than $i_L$, $v_2$ remains zero and power still cannot be transmitted from primary side to secondary side.

*Stage 6.* *[$t_5$–$t_6$, Fig. 13(g)]:* At $t_5$, $|i_2|$ increases to $i_L$. Then $D_5$ and $D_8$ are cut-off. At the same time, $L_r$ starts to be resonant with $C_5$ and $C_8$. However, the spike voltage is suppressed by the $C_k$. Because $C_k$ is larger than stray capacitors of $S_1$–$S_4$, it can absorb the most energy of the $L_r$, which can suppress the spike voltage and oscillation, effectively.

*Stage 7.* *[$t_6$–$t_7$, Fig. 13(h)]:* The stage begins when $v_2$ is smaller than the voltage of $C_k$. From this stage, $C_k$ starts to discharge to $R_k$. The working conditions of this stage are symmetric with the stage 0. The latter steps begin.

It is noted that the minimum voltage of $C_k$ is required to maintain beyond the expected output voltage. Otherwise, $C_k$ would absorb the energy transmitted from LV side to HV side, which decreases the efficiency.

The resonance energy of $L_r$ can be calculated by

$$E_r = 0.5 \times L_r \times i_1^2. \tag{18}$$

And in each switching cycle, the absorbed and released energy of $C_k$ is equal to $E_r$. Hence, $C_k$ can be determined by

$$0.5 \times L_r \times i_L^2 = 0.5 \times c_k \times \left(U_p^2 - U_o^2\right) \tag{19}$$

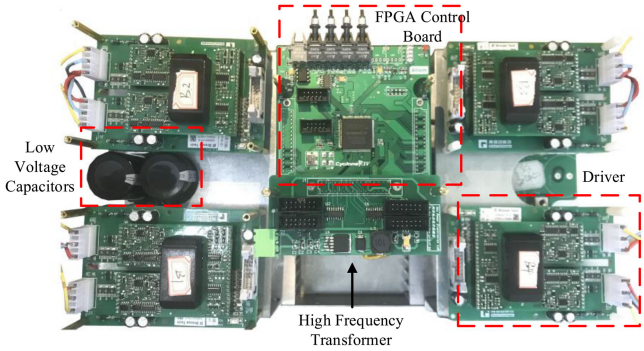



Fig. 14. Experimental prototype of the proposed HFL-SM.

where $c_k$ is the value of the $C_k$; $U_p$ is the peak value of the $v_o$; $U_o$ is the expected value of the $v_o$, and $R_k$ can be determined by

$$U_p = U_o \times e^{(-t/\tau)}. \tag{20}$$

From $t_3$ to $t_5$, $v_1$ is equal to $-V_{\mathrm{dc}L}$ but $v_2$ is equal to zero. This progress is called duty loss since the power cannot be transmitted to HV side in this progress. The relationship of primary duty ratio $D_{\mathrm{pr}}$ and secondary duty ratio $D_{\mathrm{se}}$ can be determined by

$$D_{\mathrm{se}} = D_{\mathrm{pr}} - \Delta D \tag{21}$$

where $\Delta D$ is the duty loss of the secondary duty. And $\Delta D$ can be calculated by

$$\Delta D = \frac{k}{\left(\frac{V_{\mathrm{dc}L}}{L_r}\right)\left(\frac{T_S}{2}\right)}\left[2i_L - \frac{U_0}{L_f}(1 - D_{\mathrm{pr}})\frac{T_S}{2}\right]. \tag{22}$$

As (22) shows, larger arm inductance, higher switching frequency, and larger primary current would lead higher duty loss.

## VI. Power Transfer Steady-State Analysis Among HVAC, HVDC, and LVDC Ports in I-M$^2$C

To verify the operation principle and the theoretical analysis of I-M$^2$C, a single-phase I-M$^2$C prototype and a three-phase I-M$^2$C system have been implemented.

### A. Experimental Results of the Single-Phase I-M$^2$C Prototype

First, a prototype of the proposed HFL-SM has been built and tested to verify the operation principle. The photo of the prototype is shown in Fig. 14. The main parameters are listed in Table I.

The performance of the proposed SM was verified by the experimental prototype, as shown in Figs. 15–17. Fig. 15 shows the performance of the proposed voltage clamping circuit at $C_k = 1\ \mu$F and $R_k = 2\ \mathrm{k}\Omega$, where $V_{c5}$ and $V_{c6}$ are the voltage values of $C_5$ and $C_6$, respectively; $v_2$ and $i_2$ are the secondary voltage and current of the HFT, respectively. As Fig. 15(a) shows, the peak value of $|v_2|$ exceeds 580 V without the voltage clamping circuit. As shown in Fig. 15(b), the voltage increasing speed across the IGBT is restricted and peak value of $|v_2|$ is limit under 270 V with the help of the voltage clamping circuit. It can be seen that the adopted voltage clamping circuit is very effective.

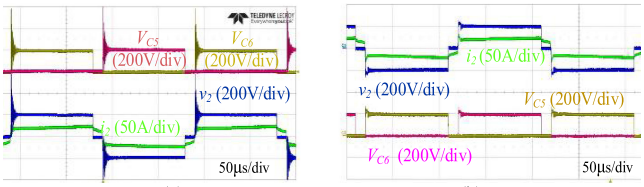



Fig. 15. Experimental waveforms of secondary side in HFL-SM prototype. (a) Experimental waveforms of HFL-SM without voltage clamping circuit. (b) Experimental waveforms of HFL-SM with voltage clamping circuit.

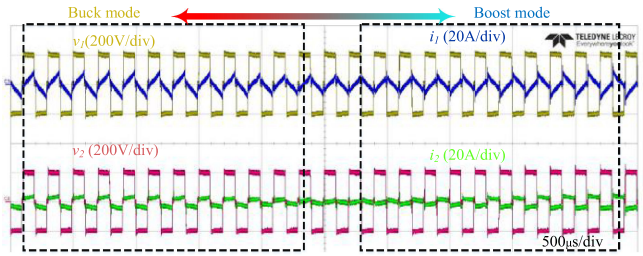



Fig. 16. Experimental waveforms of HFL-SM from buck mode to boost mode.

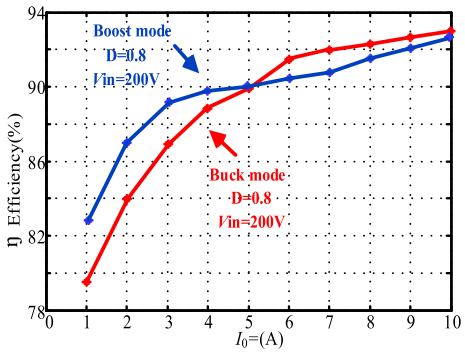



Fig. 17. Measured efficiency of the HFL-SM prototype.

Fig. 16 shows the process of switching of the two modes (from buck mode to boost mode), where $v_1$ and $v_2$ are voltages of primary side and secondary side in HFL-SM prototype; $i_1$ and $i_2$ are voltages of primary side and secondary side in HFL-SM prototype. Thanks to the unified modulation strategy, the switching process of the operating mode is seamless and the changes of voltages and currents of the HFL-SM are smooth and automatic.

Fig. 17 shows the measured efficiency values in buck and boost working modes. The maximum efficiency values of both two modes can reach to 92%. In order to further improve the efficiency, the optimum design of circuit parameters is the future research focus.

As Fig. 18 shows, a scaled-down laboratory single-phase prototype based on the HFL-SM prototype is constructed.

There are two SMs in each arm in this single-phase prototype. The common LVdc side is supported by the dc voltage source. The HVdc side is connected to resistors, and the HVac side is connected to the inductive and resistive load. To construct the

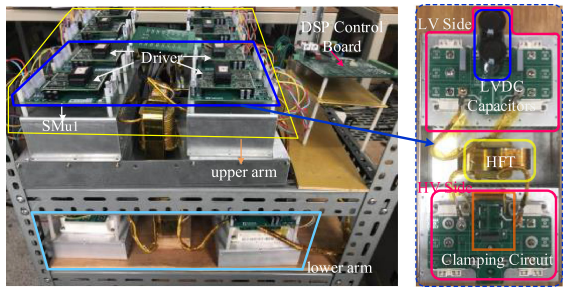



Fig. 18. Experimental prototype of the proposed single-phase I-M$^2$C prototype with 2 SMs/arm.

TABLE I
CIRCUIT PARAMETERS OF PROPOSED HFL-SM PROTOTYPE

| Parameter | Symbol | Value |
|---|---|---|
| LVDC voltage | $V_{dcL}$ | 200 V |
| LVDC capacitor | $C_{dcL}$ | 2 mF |
| HFT turn ratio | $k$ | 17:17.5 |
| HFT leakage inductor | $L_r$ | 3 μH |
| Clamping capacitor | $C_k$ | 1 μF |
| Clamping resistor | $R_k$ | 2 kΩ |
| Carrier frequency | $f_c$ | 10 kHz |
| DC modulation ratio | $D$ | 0.8 |
| AC modulation ratio | $d_a$ | 0 |

TABLE II
CIRCUIT PARAMETERS OF PROPOSED SINGLE-PHASE I-M$^2$C PROTOTYPE

| Parameter | Symbol | Value |
|---|---|---|
| LVDC voltage | $V_{dcL}$ | 200 V |
| HVDC voltage | $V_{dcH}$ | 400 V |
| HVAC voltage | $v_{ac}$ | 120 Vrms |
| Arm inductor | $L_{um}$ | 0.5 mH |
| Spilt DC capacitor | $C_{dcH}$ | 2×2 mF |
| HVAC output filter | $L_f$,$C_f$ | 0.5 mH, 2 μF |
| DC modulation ratio | $D$ | 0.5 |
| AC modulation ratio | $d_a$ | $0.8\sin(\omega t)$ |

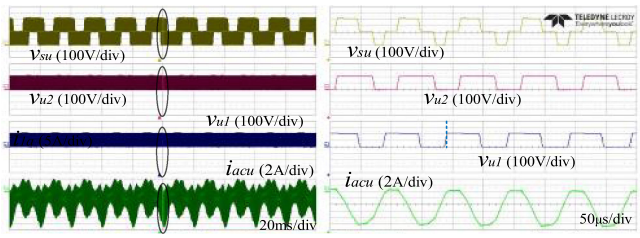



Fig. 19. Experimental waveforms of upper arm in the single-phase I-M$^2$C prototype.

HVac current loop, the split capacitors are adopted at the HVdc side. The circuit parameters of the single-phase I-M$^2$C system are listed in the Table II.

Figs. 19–22 show steady-state experimental waveforms at dc load $R_{\rm dc} = 160\ \Omega$ and ac load $Z_{\rm ac} = (160 + {\rm j}\ 48.4)\ \Omega$. Fig. 19 shows the overall and detailed output voltage waveforms of the upper arm. It shows that the output voltage frequency of each arm is twice as much as that of each SM by proposed PSPWM modulation strategy.

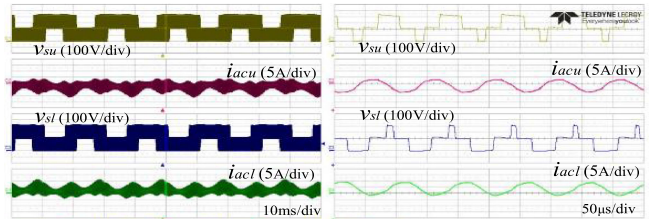



Fig. 20. Experimental waveforms of upper and lower arms in the single-phase I-M$^2$C prototype.

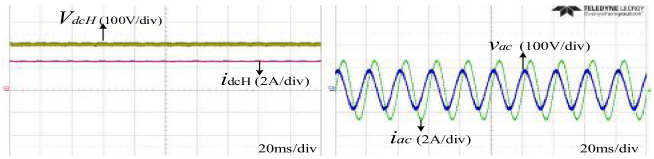



Fig. 21. Experimental waveforms of HVdc and HVac ports in single-phase I-M$^2$C system. (a) Voltage and current waveforms of HVdc port. (b) Voltage and current waveforms of HVac port.

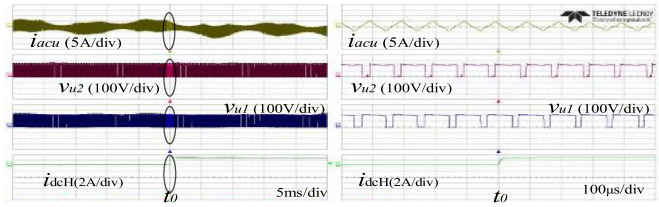



Fig. 22. Transient-state experimental waveforms of upper arm.

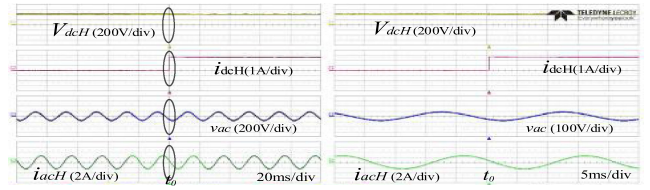



Fig. 23. Transient-state experimental waveforms of HV ports.

Fig. 20 shows the overall and detailed experimental waveforms of the upper and lower arms. These waveforms show that the currents of arms can flow freely in the two direction. Hence, the switching process between buck mode and boost mode is a natural step.

Fig. 21 shows the waveforms of HVdc and HVac ports at $V_{\mathrm{dc}L} = 200$ V and $I_{\mathrm{dc}L} = 6.88$ A. It can be seen that the proposed converter has high-quality output voltages and currents.

The transient waveforms of the proposed converter of step change in HVdc load are shown in Figs. 22 and 23. To verify the transient performance of the topology, HVdc side load is changed from $\infty$ to 160 $\Omega$ at $t_0$. Fig. 22 shows the overall and detailed experimental waveforms of upper arm, and Fig. 23 shows the overall and detailed experimental transient-state waveforms of HV ports. From Figs. 22 and 23, it can be validated that power can flow among LVdc, HVdc, and HVac sides freely. The single-phase I-M$^2$C prototype has good transient performance.

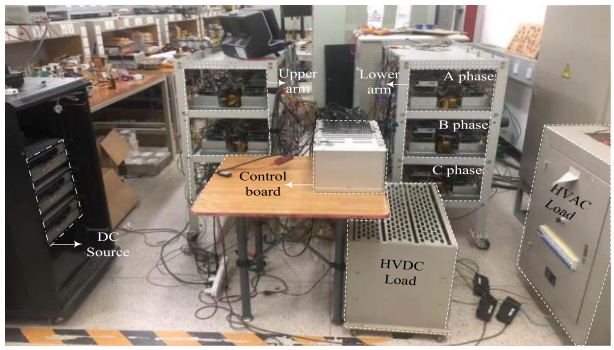



Fig. 24. Experimental prototype of the three-phase I-M$^2$C with 4 SMs/arm.

TABLE III
CIRCUIT PARAMETERS OF PROPOSED THREE-PHASE I-M$^2$C PROTOTYPE

| Parameter | Symbol | Value |
|---|---|---|
| LVDC voltage | $V_{dcL}$ | 200 V |
| LVDC capacitor | $V_{dcH}$ | 800 V |
| HVAC voltage | $v_{ac}$ | 240 Vrms |
| Arm inductor | $L_{um}$ | 0.5 mH |
| HVDC capacitor | $C_{dc}$ | 75 μF |
| HVAC output filter | $L_f C_f$ | 0.5 mH, 2 μF |
| DC modulation ratio | $D$ | 0.5 |
| AC modulation ratio | $d_a$ | $0.8\sin(\omega t)$ |

### *B. Experimental Results of the Three-Phase I-M$^2$C System*

On the basis of the single-phase I-M$^2$C prototype, a three-phase system (4 SMs/arm) is constructed, as shown in Fig. 24. Compared with the single-phase prototype, the three-phase system eliminates the spilt capacitors, which further reduces the number of capacitors.

The circuit parameters of the three-phase system are listed in Table III.

Fig. 25 shows the experimental waveforms of the three-phase prototype at $V_{\mathrm{dc}L} = 200$ V, $D = 0.5$, and $da = 0.8\sin(\omega t)$. Fig. 25(a) shows the experimental waveforms of each HFL-SM in A-phase upper arm, where $V_{au1}$, $V_{au2}$, $V_{au3}$, and $V_{au4}$ are the voltages of SMs in A-phase upper arm. Fig. 25(b) shows the experimental waveforms of upper and lower arm in A-phase, where $V_{\mathrm{sua}}$ and $V_{\mathrm{sla}}$ are voltages of A-phase upper and lower arm, respectively; $i_{\mathrm{sua}}$ and $i_{\mathrm{sla}}$ are currents of A-phase upper and lower arm, respectively. Fig. 25(c) shows the experimental waveforms of upper arm in each phase, where $V_{\mathrm{sua}}$, $V_{\mathrm{sub}}$, and $V_{\mathrm{suc}}$ are voltages of A-phase upper arm, B-phase upper arm, and C-phase upper arm.

As Figs. 23–25 show, the PSPWM modulation strategy increases the frequency of arm voltage, which is explained in Section III.

Fig. 26(a) and (b) show the experimental waveforms of HVac and HVdc ports, where $V_a$, $V_b$, and $V_c$ are voltages of three phases; $I_a$, $I_b$, and $I_c$ are currents of three phases. As Fig. 26 shows, the proposed three-phase I-M$^2$C prototype system has high-quality output voltages and currents.

All the abovementioned experimental results have demonstrated that the proposed HFL I-M$^2$C has good performances. These results also have verified the feasibility and availability

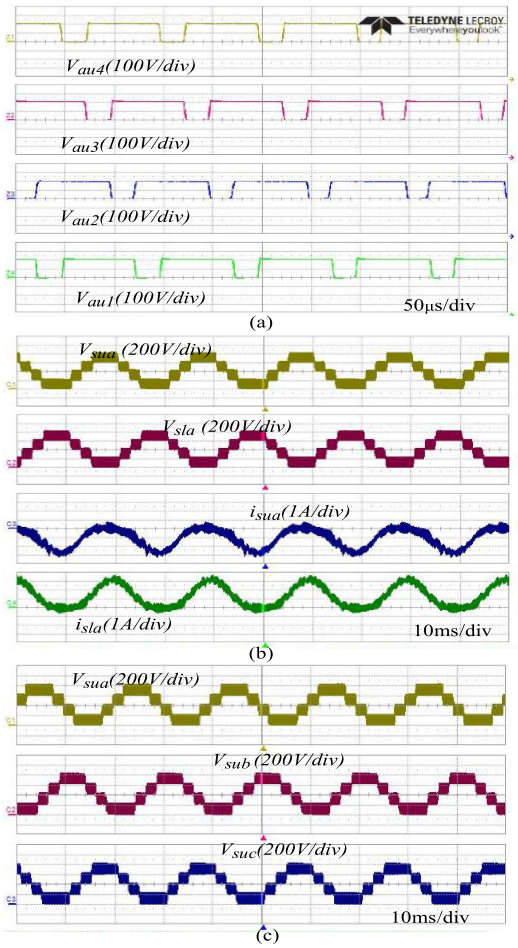



Fig. 25. Experimental waveforms of the three-phase I-M$^2$C with 4 SMs/arm. (a) Voltages waveforms of each SM in A-phase upper arm. (b) Experimental waveforms of A-phase upper and lower arms. (c) Voltages waveforms of upper arms in each phase.

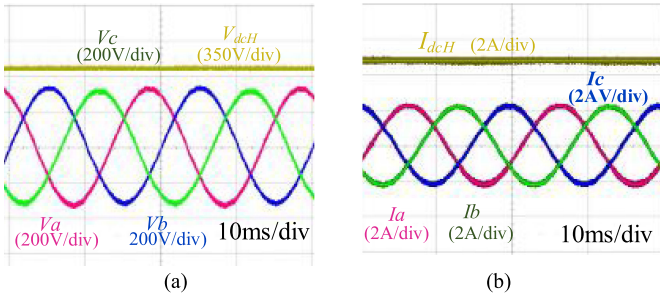



Fig. 26. Experimental waveforms of HVdc and HVac ports in three-phase I-M$^2$C system. (a) Voltage waveforms of HVdc and HVac ports. (b) Currents waveforms of HVdc and HVac ports.

of this novel topology. In the end, I-M$^2$C has an important potential value for hybrid dc and ac application in future power generation and transmission.

## VII. Conclusion

This paper has introduced the topology of the novel I-M$^2$C and its relevant characteristics. The steady-state APF and the voltage clamping circuit have been analyzed in detail. The scaled-down laboratory single-phase and three-phase prototypes have verified the feasibility and availability of this novel HFL I-M$^2$C topology. Compared with the conventional MMC-based SST topologies, the novel I-M$^2$C topology has main advantages in the following aspects.

1) Multiports structure: The proposed structure has three basic ports (LVdc, HVdc, and HVac ports), which is appropriate for future hybrid ac/dc grids.
2) Single-stage power conversion between LV side and HV side: The proposed structure inherits the main merits of single-stage power conversion, such as high power density, high efficiency, and low cost.
3) Simply control strategy: Due to the eliminated SM capacitors, the proposed structure avoids applying complicated SM voltage balance control strategy.

## References

[1] J. E. Huber and J. W. Kolar, "Applicability of solid-state transformers in today's and future distribution grids," *IEEE Smart Grid*, vol. 10, no. 1, pp. 317–326, Aug. 2017.
[2] L. F. Costa, G. De Carne, G. Buticchi, and M. Liserre, "The smart transformer: A solid-state transformer tailored to provide ancillary services to the distribution grid," *IEEE Power Electron. Mag.*, vol. 4, no. 2, pp. 56–67, Jun. 2017.
[3] J. E. Huber and J. W. Kolar, "Solid-state transformer: On the origins and evolution of key concepts," *IEEE Ind. Electron. Mag.*, vol. 10, no. 3, pp. 19–28, Sep. 2016.
[4] A. Q. Huang, "Medium-voltage solid-state transformer: Technology for a smarter and resilient grid," *Electron. Mag.*, vol. 10, no. 3, pp. 29–42, Sep. 2016.
[5] M. Liserre, G. Buticchi, M. Andresen, G. De Carne, L. F. Costa, and Z.-X. Zou, "The smart transformer: Impact on the electric grid and technology challenges," *IEEE Ind. Electron. Mag.*, vol. 10, no. 2, pp. 46–58, Jun. 2016.
[6] K. Mainali *et al.*, "A transformerless intelligent power substation: A three-phase SST enabled by a 15-kV SiC IGBT," *IEEE Power Electron. Mag.*, vol. 2, no. 3, pp. 31–43, Sep. 2015.
[7] G. Li *et al.*, "Overview of topology structure and power flow control of DC grid," *J. Northeast Elect. Power Univ.*, vol. 39, no. 2, pp. 1–9, 2019.
[8] R. Gao, X. She, I. Husain, and A. Q. Huang, "Solid-state transformer interfaced permanent magnet wind turbine distributed generation system with power management functions," *IEEE Trans. Ind. Appl.*, vol. 53, no. 4, pp. 3849–3861, Jul./Aug. 2017.
[9] C. Liu *et al.*, "Cascade dual-boost/buck active-front-end converter for intelligent universal transformer," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4671–4680, Dec. 2012.
[10] X. She, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 3, pp. 186–198, Sep. 2013.
[11] L. Wang, D. L. Zhang, Y. Wang, B. Wu, and H. S. Athab, "Power and voltage balance control of a novel three-phase solid-state transformer using multilevel cascaded H-bridge inverters for microgrid applications," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3289–3301, Apr. 2016.
[12] D. Wang *et al.*, "A 10-kV/400-V 500-kVA electronic power transformer," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 6653–6663, Nov. 2016.
[13] J. E. Huber and J. W. Kolar, "Optimum number of cascaded cells for high-power medium-voltage AC-DC converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 213–232, Mar. 2017.
[14] F. Briz, M. Lopez, A. Rodriguez, and M. Arias, "Modular power electronic transformers: Modular multilevel converter versus cascaded H-bridge solutions," *IEEE Ind. Electron. Mag.*, vol. 10, no. 4, pp. 6–19, Dec. 2016.
[15] A. K. Tripathi *et al.*, "Design considerations of a 15-kV SiC IGBT-based medium-voltage high-frequency isolated DC–DC converter," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3284–3294, Jul./Aug. 2015.
[16] X. Tan and X. Ruan, "Equivalence relations of resonant tanks: A new perspective for selection and design of resonant converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 2111–2123, Apr. 2016.

[17] J.-H. Jung, H.-S. Kim, M.-H. Ryu, and J.-W. Baek, "Design methodology of bidirectional CLLC resonant converter for high-frequency isolation of DC distribution systems," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1741–1755, Apr. 2013
[18] C. Liu *et al.*, "Magnetic-coupling current-balancing cells based input-parallel output-parallel LLC resonant converter modules for high-frequency isolation of DC distribution systems," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 6968–6979, Dec. 2015.
[19] G. Ortiz, M. G. Leibl, J. Huber, and J. W. Kolar, "Design and experimental testing of a resonant DC-DC converter for soli-state transformer," *IEEE Power Electron*., vol. 32, no. 10, pp. 7534–7542, Oct. 2017.
[20] M. N. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance characterization of a high-power dual active bridge DC-to-DC converter," *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1294–1301, Nov./Dec. 1992.
[21] Y. Xie, J. Sun, and J. S. Freudenberg, "Power flow characterization of a bidirectional galvanically isolated high-power DC/DC converter over a wide operating range," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 54–66, Jan. 2010.
[22] N. H. Baars, J. Everts, H. Huisman, and J. L. Duarte, "A 80-kW isolated DC–DC converter for railway applications," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6639–6647, Dec. 2015.
[23] C. Liu, H. Y. Liu, G. W. Cai, S. Cui, H. Liu, and H. Yao, "Novel hybrid LLC resonant and DAB linear DC–DC converter: Average model and experimental verification," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 6970–6978, Sep. 2017.
[24] J. H. Feng, W. Q. Chu, Z. X. Zhang, and Z. Q. Zhu, "Power electronic transformer-based railway traction systems: Challenges and opportunities," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 3, pp. 1237–1253, Sep. 2017.
[25] B. Zhao, Q. Song, J. Li, W. Liu, G. Liu, and Y. Zhao, "High-frequency-link DC transformer based on switched capacitor for medium-voltage DC power distribution application," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4766–4777, Jul. 2016.
[26] Y. Chen, S. S. Zhao, Z. Y. Li, X. Wei, and Y. Kang, "Modeling and control of the isolated DC–DC modular multilevel converter for electric ship medium voltage direct current power system," *IEEE Trans. Power Electron.*, vol. 5, no. 1, pp. 124–139, Mar. 2017.
[27] B. Zhao, Q. Song, J. G. Li, X. Xu, and W. Liu, "Comparative analysis of multilevel-high-frequency-link and multilevel-DC-link DC–DC transformers based on MMC and dual-active bridge for MVDC application," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2035–2049, Mar. 2018.
[28] J. Z. Xu, P. H. Zhao, and C. Y. Zhao, "Reliability analysis and redundancy configuration of MMC with hybrid sub-module topologies," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2720–2729, Apr. 2016.
[29] A. Lesnicar and R. Marquart, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bologna Power Tech Conf.*, Jun. 2003, pp. 23–26.
[30] Z. Yao *et al.*, "Research on fault diagnosis for MMC-HVDC systems," *Protection Control Modern Power Syst.*, vol. 1, no. 1, pp. 71–77, Jan. 2016.
[31] W. Mcmurray, "The thyristor electronic transformer: A power converter using a high-frequency link," *IEEE Ind. General Appl.*, vol. 7, no. 4, pp. 451–457, Jul./Aug. 1971.
[32] H. Qin and J. W. Kimball, "Solid-state transformer architecture using ac-ac dual-active-bridge converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3720–3730, Sep. 2013.
[33] M. R. Islam, Y. Guo, and J. Zhu, "A high-frequency link multilevel cascaded medium-voltage converter for direct grid integration of renewable energy systems," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4167–4182, Aug. 2014.
[34] S. Essakiappan, H. S. Krishnamoorthy, P. Enjeti, R. S. Balog, and S. Ahmed, "Multilevel medium frequency link inverter for utility scale photovoltaic integration," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3674–3684, Jul. 2015.
[35] K. V. Iyer, R. Baranwal, and N. Mohan, "A high-frequency AC-link single-stage asymmetrical multilevel converter for grid integration of renewable energy systems," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5087–5108, Jul. 2017.
[36] H. Chen, A. Prasai, and D. Divan, "Dyna-C: A minimal topology for bidirectional solid state transformers," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 995–1005, Feb. 2017.
[37] H. Chen and D. Divan, "Soft-switching solid-state transformer (S4T)," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 5087–5108, Apr. 2018.
[38] H. Akagi, "Multilevel converters: Fundamental circuits and systems," *IEEE Proc.*, vol. 105, no. 11, pp. 2048–2065, Nov. 2017.
[39] T. Shimizu, Y. Jin, and G. Kimura, "DC ripple current reduction on a single-phase PWM voltage-source rectifier," *IEEE Trans. Ind. Appl.*, vol. 36, no. 5, pp. 1419–1429, Sep./Oct. 2000.

**Chuang Liu** (M'12) received the M.S. degree in electrical engineering from Northeast Electric Power University, Jilin, China, in 2009, and the Ph.D. degree in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2013. From 2010 to 2012, he was a Visiting Ph.D. Student at the Future Energy Electronics Center, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, supported by the Chinese Scholarship Council.

In 2013, he became an Associate Professor with the School of Electrical Engineering, Northeast Electric Power University, where, since 2016, he has been a Professor. His research interests include power electronics based on ac and dc transformers for future hybrid ac–dc power grids, flexible operation and control of power grid based on ac–ac transformation, and power-electronics-based power system stability analysis and control.

**Chao Liu** was born in Heilongjiang, China, in 1994. He received the B.S. degree in electronic and information engineering in 2016 from Northeast Electric Power University, Jilin, China, where he is currently working toward the M.S. degree in electrical engineering.

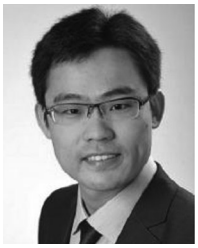
His current research interests include solid-state transformer (SST) and hybrid MVdc/ac power grids.

**Guowei Cai** was born in Jilin, China, in 1968. He received the B.S. and M.S. degrees in electrical engineering from Northeast Electric Power University, Jilin, China, in 1990 and 1993, respectively, and the Ph.D. degree in electrical engineering from Harbin Institute of Technology, Harbin, China, in 1999.

Since 2004, he has been a Professor with the School of Electrical Engineering, Northeast Electric Power University. His current research interests include power system transient stability analysis and smart grid with renewable power generation.

**Hong Ying** was born in Zhejiang, China, in 1972. He received the B.S. degree and the M.S. degree from Northeast Electric Power University, Jilin, China, in 1993 and 1996, respectively.

He is currently a Senior Engineer with Zhejiang Huayun Clean Energy Co. Ltd., Hangzhou, China. His current research interests include renewable energy and distributed generation systems.



**Zhenbin Zhang** (S'13–M'16–SM'18) was born in Shandong, China, in 1984. He received the B.S. degree in electrical engineering and automation from Harbin Engineering University, Harbin, China, in 2008, the M.S. degree in control theory and engineering from Shandong University, Jinan, China, in 2011, and the Ph.D. degree from the Institute for Electrical Drive Systems and Power Electronics (EAL), Technical University of Munich (TUM), Munich, Germany, in 2016, with *summa cum laude*.

From 2016 to 2017, he was a Research Fellow and the Team Leader with "Modern control strategies for electrical drives" group, EAL, TUM. Since 2017, he has been a Full Professor of electrical engineering with Shandong University, Jinan, China. Since 2018, he has been a Guest Professor with TUM. In 2019, he was appointed as a National Distinguished Expert (supported by the Youth Talent Program) of China. His research interests include power electronics and electrical drives, sustainable energy systems, and smart grid.

Dr. Zhang is a recipient of the VDE-Award, Germany, in 2017. He is currently an Associate Editor for IEEE TRANSACTION IN INDUSTRIAL ELECTRONICS.

**Renzhong Shan** was born in Zhejiang, China, in 1982. He received the B.S. degree from Zhejiang University of Science and Technology, Hangzhou, China, in 2004, the M.S. degree from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2007, and the Ph.D. degree from North China Electric Power University, Beijing, China, in 2010. From 2011 to 2014, he was engaged in postdoctoral research at the Department of Electrical Machinery, Tsinghua University, Beijing, China.

From 2018, he has been an Associate Professor with School of Electrical Engineering, Northeast Electric Power University, Jilin, China. His research interests include power quality analysis and control power, and application of power electronic technology in power system.

**Zhongchen Pei** was born in Liaoning, China, in 1994. He received the B.S. degree in smart grid information engineering from Changchun Institute of Technology, Changchun, China, in 2017. He is currently working toward the M.S. degree in electrical engineering at Northeast Electric Power University, Jilin, China.

His current research interests include SST and hybrid MVdc/ac power grids.

**Xiaomin Song** was born in Shandong, China, in 1993. He received the B.S. degree in electrical engineering in 2018 from Northeast Electric Power University, Jilin, China, where he is currently working toward the M.S. degree in electrical engineering.

His current research interests include SST and hybrid MVdc/ac power grids.