Active Magnetizing Current Splitting ZVS Modulation of a 7 kV/400 V DC Transformer

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***Abstract*—The LLC series resonant converter (SRC) is one of the most popular galvanically isolated dc–dc converters since it provides zero voltage switching (ZVS), reduces rms currents, and tightly couples the input and output voltages, when it is operated at (or below) the resonance frequency, and, therefore, acts as a dc transformer (DCX) without requiring closed-loop voltage control. Hence, this topology is of particular importance for the dc–dc converter stage of high power medium voltage to low voltage solid-state transformers (SSTs). This paper first highlights the limitations of passive and synchronous rectification (e.g., oscillations, current distortion, load-dependent voltage transfer ratio) for bridges employing semiconductors with large output capacitances. Afterward, a magnetizing current splitting ZVS (MCS-ZVS) modulation scheme, which allows an active sharing of the magnetizing current between the primary side and secondary side metal oxide semiconductor field effect transistor (MOSFET)-based bridges, is analyzed. It is shown that the ZVS mechanism is acting equivalent to a controller, allowing for a robust open-loop operation of the converter. The proposed modulation scheme features a load-independent voltage transfer ratio, load-independent ZVS for both bridges, and quasi-sinusoidal currents. Finally, the phase shift modulation scheme is experimentally verified for the SiC MOSFET-based dc–dc converter of a 25 kW ac–dc SST, which operates at 48 kHz between a 7 kV and a 400 V dc bus with an efficiency of 99.0%.**

***Index Terms*—Dual active, dc–dc power converters, dc transformer, LLC converter, medium-voltage (MV) converter, phase shift modulation, resonant inverters, series resonant converter (SRC), solid-state transformer (SST), zero voltage switching (ZVS).**

I. Introduction

SOLID-STATE transformers (SSTs) can be used to directly interface the low-voltage (LV) dc bus of datacenters to the ac medium-voltage (MV) grid [1], [2]. The reduction of the number of conversion stages of the supply chain (no low-frequency transformer, no LV ac grid, and no LV ac–dc rectifiers) [3], [4] and the usage of a medium-frequency transformer, result into higher efficiencies and lower construction volumes [4]–[6].

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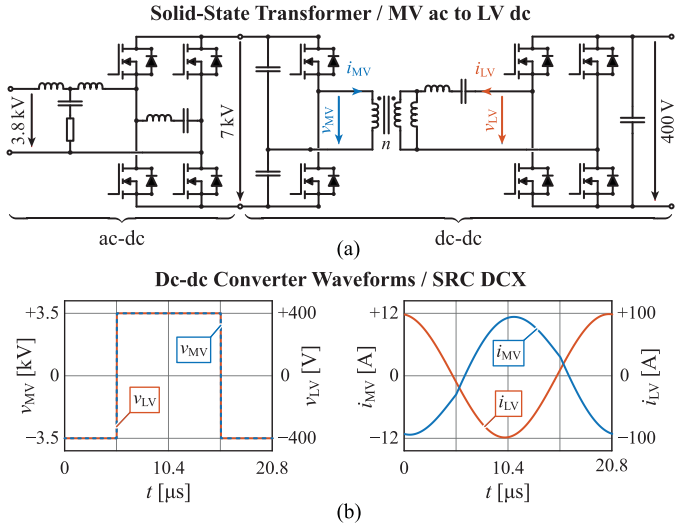

Fig. 1. (a) Considered SST consisting of an ac–dc converter and an isolated dc–dc converter. (b) Schematic view of the current and voltage waveforms of the SRC operated as DCX.

Fig. 1(a) shows the internal structure of the considered SST, consisting of an ac–dc converter with sinusoidal input current and an isolated dc–dc converter output stage. The ac–dc converter interfaces an ac grid (3.8 kV, phase-to-neutral rms voltage) to an MV bus (7 kV) [5]. The dc–dc stage provides galvanic isolation and the voltage step down from the MV (7 kV) to the LV dc bus (400 V), which is used to connect the loads (server racks) and back-up batteries (uninterruptible power supply) [6]. The complete converter structure is bidirectional in order to also allow for the batteries to offer grid energy storage (smart grid) [7], [8].

For increasing the reliability of the power supply chain, each server rack is supplied from an individual SST module featuring a rated power of 25 kW. For the complete datacenter, the single-phase SSTs are assigned to different phases in order to ensure a symmetrical loading of the MV ac three-phase grid. Another advantage of this modular power supply structure is the absence of long LV cables, which would require large copper cross sections and/or cause relatively high losses. The 25 kW power rating and the distributed single-phase architecture have also been chosen for the industrial system described in [4].

The bidirectional dc–dc converter, which is the focus of this paper, employs 10 kV SiC metal oxide semiconductor field effect transistors (MOSFETs), which allow for the realization

with a single-cell structure [9]–[11]. Two main circuit topologies have emerged for such applications—the dual-active bridge (DAB) [12]–[14] and the LLC series resonant converter (SRC) [10], [15]–[19].

1) *DAB:* The DAB features extended voltage and power flow control capabilities [13]. Zero voltage switching (ZVS) and/or zero current switching (ZCS) can be achieved [13]. However, the trapezoidal currents in a DAB exhibit large harmonic contents and the semiconductors have to switch the full load current. Furthermore, a closed-loop voltage control of the converter is required [12]–[14].
2) *SRC:* The SRC features several advantages, such as quasi-sinusoidal currents and the ability to achieve ZVS and/or ZCS [10], [11], [17], [19], [20]. Nevertheless, the control of power flow and voltages require frequency and/or duty cycle modulation in a wide range [16], [21], [22]. However, the SRC, operated at (or below) the resonance frequency, i.e., in half-cycle discontinuous current mode, provides a constant voltage transfer ratio without requiring any closed-loop voltage control. Therefore, this operating mode of the SRC is sometimes referred to as dc transformer (DCX) and is widely used for MV high-power dc–dc converters [17]–[20], [23], [24].

For the considered dc–dc converter, power flow, and voltage control are not required as these functionalities are provided by the input-side ac–dc stage. Therefore, the SRC topology operated as a DCX has been selected for the dc–dc converter stage. The DCX is realized with SiC MOSFETs and commutated at 48 kHz, as shown in Fig. 1(b). Due to the high switching frequency (considering the high input voltage), complete ZVS should be achieved for all semiconductors for all load conditions [25], [26].

In the literature, the modulation of insulated-gate bipolar-transistor (IGBT)-based SRC-DCXs, which feature ZCS has been analyzed in detail [17], [19], [24]. Several MOSFET-based SRC-DCXs, which feature ZVS have also been presented [10], [11], [18], [20], [21], [27]. However, to the knowledge of the authors, no detailed and comprehensive analysis of the ZVS mechanism (considering non-ideal switching transitions) has been published for MOSFET-based SRC-DCXs. The consideration of non-instantaneous switching transitions is especially critical for converters using the newly available MV SiC MOSFETs, which feature large semiconductor output capacitances. Therefore, this paper analyzes the ZVS of SRC-DCXs, including the impact of the parasitic semiconductor capacitances of the inverter and rectifier bridges.

The paper is organized as follows. Section II defines the parameters of the considered SRC-DCX. Section III presents the standard modulation scheme of SRC-DCXs, where the rectifier bridge is operated as passive (or synchronous) rectifier. The limitations of this modulation scheme (e.g., oscillations, current distortion, load-dependent voltage transfer ratio) are highlighted for bridges with large semiconductor output capacitances. Therefore, Section IV introduces an alternative magnetizing current splitting ZVS (MCS-ZVS) modulation scheme, which is based on an active phase shift modulation between the bridges. Section V verifies the stability and robustness of the MCS-ZVS modulation scheme. Finally, Section VI presents experimental results obtained with the aforementioned system (see Fig. 1).

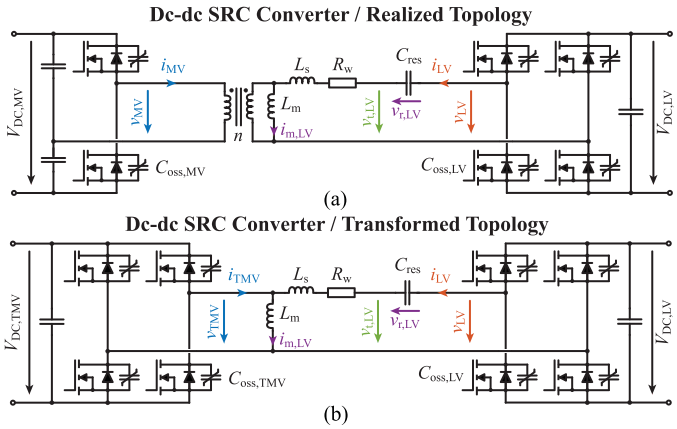

Fig. 2. (a) SRC-DCX operated at the resonance frequency, acting as a bidirectional DCX. (b) SRC-DCX topology with scaled voltages. The MV half bridge is transformed into a full bridge and the complete circuit is referred to the LV side with the voltage transfer ratio of the transformer (n).

TABLE I
PARAMETERS OF THE CONSIDERED SRC-DCX

Variable	Value	Variable	Value
$V_{DC,MV}$	7 kV	$V_{DC,LV}$	400 V
P	25 kW	f_s	48 kHz
R_w	30 mΩ	L_s	2.9 µH
L_m	50.0 µH	n	8.8
C_{res}	3.8 µF	f_{res}	48 kHz
$C_{oss,MV}$	150 pF	$C_{oss,LV}$	1700 pF

II. CONSIDERED SRC-DCX

Fig. 2(a) shows the considered SRC-DCX and Table I shows the corresponding parameters. This all-SiC 25 kW converter operates between a 7 kV and a 400 V dc bus at 48 kHz. In order to reduce the number of switches and for reducing the voltage transfer ratio of the transformer, the combination of a half bridge on the MV side and a full bridge on the LV side is used [17], [24]. However, the presented results also apply for any combinations of full bridges and half bridges. The output capacitance (per switch) of the SiC MOSFETs is represented with a linearized charge-equivalent capacitance ($C_{oss,MV}$ and $C_{oss,LV}$) [26], [28]. The dc-bus ripples, which are small, have no impact on the modulation scheme and are neglected [6], [24].

The transformer equivalent circuit is described with an ideal transformer, a magnetizing inductance, and a leakage inductance (n, L_m, and L_s) [29]. The stray capacitances of the transformer, which slightly reduce the current available for ZVS, are neglected [30], [31]. The capacitor (C_{res}) is placed in series with the transformer on the LV side, which simplifies the electrical insulation design. Additionally, LV ceramic capacitors with high energy density and low losses can be used.

The resonant capacitor (C_{res}) and the leakage inductance of the transformer (L_s) are chosen such that the desired resonance frequency (f_{res}) is achieved. The transformer voltage transfer

ratio (n) is chosen considering the desired voltage transfer ratio between the dc buses. The magnetizing inductance of the transformer (L_{m}) is selected with respect to the MOSFET output capacitances ($C_{\mathrm{oss,MV}}$ and $C_{\mathrm{oss,LV}}$) in order to obtain a sufficiently large magnetizing current (and stored energy) to achieve ZVS within a reasonable time interval [25], [26].

It should be noted that different equivalent circuits can be chosen for the transformer [29]. The equivalent circuit with an ideal transformer and series-parallel inductors (referred to the LV side) has been selected since it allows for a simplified analysis of the circuit. The magnetizing current is a virtual current which does not feature a unique definition and physical interpretation [29]. However, for transformers with high magnetic coupling factors (97% for the considered design), the magnetizing current (related to the LV side) can be described with $i_{\mathrm{m,LV}}$ [29].

The load-dependent losses of the converter are represented by a single series resistance (R_{w}). This resistance represents the conduction losses of the MOSFETs (MV and LV bridges) and the winding losses of the transformer (at the switching frequency). The load-independent losses (i.e., switching losses of the MOSFET and the core losses) could be represented by a parallel resistor. However, the current flowing in this resistor would be negligible compared to the magnetizing current. Therefore, the parallel resistor is neglected for the analysis of the modulation scheme.

In order to simplify the circuit and to allow for a direct comparison between the MV and LV sides, the following transformations are made: The MV half bridge is transformed into a full bridge and the complete circuit is referred to the LV side with the voltage transfer ratio of the ideal transformer (n). The obtained circuit is shown in Fig. 2(b) and the transformed MV (TMV) parameters can be expressed as

$$V_{\mathrm{DC,TMV}} = \frac{V_{\mathrm{DC,MV}}}{2n} \tag{1}$$

$$v_{\mathrm{TMV}} = \frac{v_{\mathrm{MV}}}{n} \tag{2}$$

$$i_{\mathrm{TMV}} = n i_{\mathrm{MV}} \tag{3}$$

$$C_{\mathrm{oss,TMV}} = 2n^2 C_{\mathrm{oss,MV}}. \tag{4}$$

It can be observed that the transformed capacitance of the MV MOSFETs is more than ten times larger than the capacitance of the LV MOSFETs ($C_{\mathrm{oss,TMV}} \gg C_{\mathrm{oss,LV}}$, see Table I).

With the defined parameters, the modulation scheme of the SRC can be examined aiming for the following properties: Load-independent voltage transfer ratio, load-independent ZVS (and quasi-ZCS) for both bridges, quasi-sinusoidal currents (low distortion), DCX behavior in open loop, and robustness against model non-idealities and production tolerances. Moreover, the modulation scheme should work at partial load for both power flow directions.

III. Passive Rectifier

In this section, the standard modulation scheme for SRC-DCXs is examined [17]–[20], [24]. The SRC is operated at (or below) the resonance frequency with an active inverter bridge (50% duty cycle) and a passive rectifier bridge (diode rectifier). The power flow is directed from the active to the passive bridge. Alternatively, synchronous rectification can be used for reducing the losses of the rectifier bridge [10], [11], [18], [21], [27].

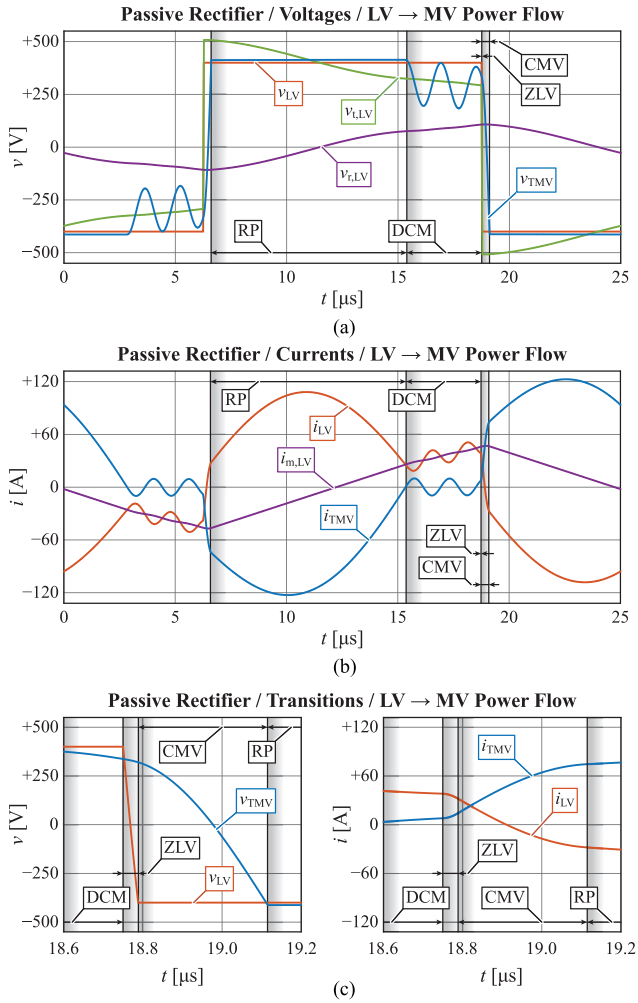

Fig. 3. Simulated (a) voltages and (b) currents with an active LV bridge and a passive MV rectifier ($f_{\mathrm{s}} = 40$ kHz, $P = 25$ kW, and power flow from the LV to the MV side). (c) Voltages and currents during the ZVS switching transition. The different operating modes (time intervals) occurring in one switching cycle are indicated.

A. Operating Principle

For explaining the operating principle of SRC-DCXs, the switching frequency is first set to $f_{\mathrm{s}} = 40$ kHz (instead of $f_{\mathrm{s}} = 48$ kHz) in order to operate the converter below the resonance frequency ($f_{\mathrm{res}} = 48$ kHz). The converter is operated with an active LV bridge and a passive MV rectifier. As shown later, this power flow direction and switching frequency represent the critical case, which includes all the non-idealities.

Fig. 3 shows the simulated waveforms. The switching period can be decomposed in several operating modes and/or time intervals and the corresponding equivalent circuits are shown in Fig. 4. The operation of the converter can be explained as follows.

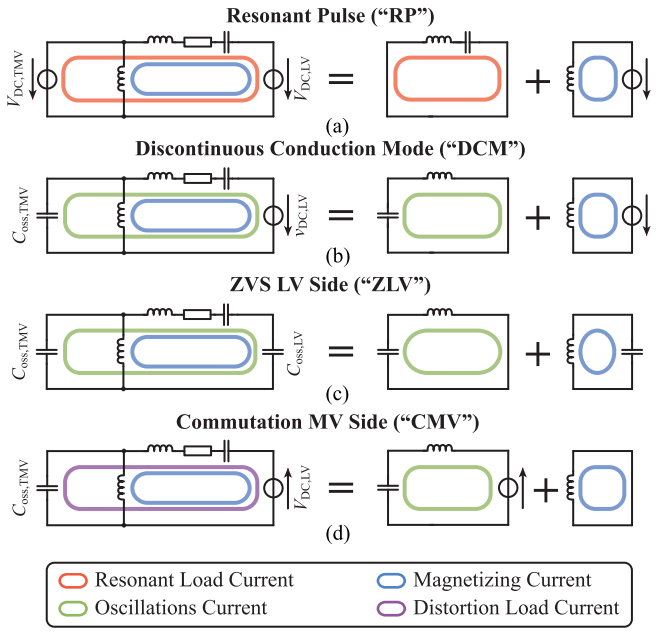

Fig. 4. Equivalent circuits during the different operating modes (time intervals occurring in one switching cycle, see Fig. 3). (a) Resonant Pulse (RP). (b) Discontinuous Conduction Mode (DCM). (c) ZVS LV-Side (ZLV). (d) Commutation MV-Side (CMV).

1) *Resonant Pulse (RP)*—The MV and LV bridge voltages cancel each other and the resonant tank (between L_s and C_{res}) is excited by the initial resonant capacitor voltage (C_{res}). This results in a sinusoidal resonant current flowing between the bridges at the resonance frequency (f_{res}). Simultaneously, the active bridge (LV side) is providing the triangular current flowing in the magnetizing inductance (L_m).
2) *Discontinuous Conduction Mode (DCM)*—As soon as the resonant current returns to zero (on the MV side), the diode rectifier stops conducting. However, the semiconductor output capacitances of the rectifier ($C_{oss,TMV}$) oscillate with the leakage inductance of the transformer (L_s). Simultaneously, the active bridge (LV side) is still providing the magnetizing current of the transformer (L_m) and the voltage of the resonant capacitor voltage (C_{res}) remains approximately unchanged.
3) *ZVS LV Side (ZLV)*—The switches of the active bridge (LV side) are turned off (dead time) and the magnetizing inductance (L_m) is providing current for obtaining a fast ZVS transition, i.e., charging and discharging the MOSFET output capacitances ($C_{oss,LV}$). During this very short interval, the oscillation current (between L_s and $C_{oss,TMV}$) continues to flow, but remains approximately unchanged.
4) *Commutation MV Side (CMV)*—The difference between the MV and LV bridge voltages is applied to the leakage inductance (L_s) causing a rapid change of the current, which distorts the sinusoidal resonant current. This current is charging the semiconductor output capacitances of the rectifier bridge ($C_{oss,TMV}$), which slowly commutates the diodes (resonance between $C_{oss,TMV}$ and L_s). During this short interval, the current in the magnetizing inductance (L_m) continues to flow, but remains approximately unchanged.

Ideally, the SRC-DCX would only feature the resonant (load dependent) current, which is transferring the energy from the active bridge to the passive bridge. This current is flowing at the resonance frequency (f_{res}), which cancels the series impedance (except R_w) between the bridges. This implies that, ideally, the voltage transfer ratio of the SRC-DCX is almost load-independent.

However, in addition to the resonant current, a magnetizing (load-independent) current is required to achieve ZVS of the active bridge [10], [20], [27]. With a passive rectifier, the magnetizing current exclusively flows in the active bridge [19]. The magnetizing current cannot flow in the rectifier bridge due to the unidirectional nature of the diodes. Moreover, a passive rectifier is not able to provide reactive power.

The amplitude of the voltage oscillation, occurring during the discontinuous conduction interval, is related to the peak-to-peak voltage of the resonant capacitor (C_{res}). The amplitude of the current oscillation is proportional to the output capacitances of the rectifier bridge ($C_{oss,TMV}$). These oscillations produce additional losses (conduction losses and switching losses) [11], [19], [25]. Moreover, the oscillations can disturb the initial condition of the next resonant pulse.

The commutation of the passive rectifier would ideally occur instantaneously as soon as the next resonant pulse is starting, i.e., after the ZVS transition of the active bridge. However, due to the semiconductor output capacitances of the rectifier bridge ($C_{oss,TMV}$), the voltage of the diodes cannot change instantaneously. The mismatch between the MV and LV bridge voltages is applied to L_s, causing a rapid change of the currents. This distorts the ideal sinusoidal current shape and also contributes to the energy transfer (as known for SRCs operated above the resonance frequency) [16], [21]. One has to note that during this time interval, the SRC is shortly operated as a DAB [12], [13]. Additionally, as shown in [21], the reverse recovery of the diodes (or body diodes) can create further distortions during the commutation of the rectifier bridge.

The amplitude of the oscillations can be reduced by a proper choice of the impedance of the resonant tank (ratio between L_s and C_{res}), i.e., a design with a small leakage inductance and a large resonant capacitor. On the other hand, a reduction of the leakage inductance (L_s) will increase the current distortion occurring during the commutation of the passive rectifier. For a rectifier bridge realized with diodes or IGBTs, the semiconductor output capacitances are small and the current distortion is often negligible [17], [24]. However, if the semiconductor output capacitances are large (e.g., synchronous rectifier realized with MOSFETs), the current distortion is critical and the leakage inductance cannot be further reduced [25]. Additionally, the leakage inductance of the transformer cannot be reduced below a certain threshold, especially for an MV design (due to geometrical, electric, and magnetic constraints).

B. Simulated Waveforms

From the aforementioned example, the appropriate modulation scheme of SRC-DCXs can be derived. SRC-DCXs using

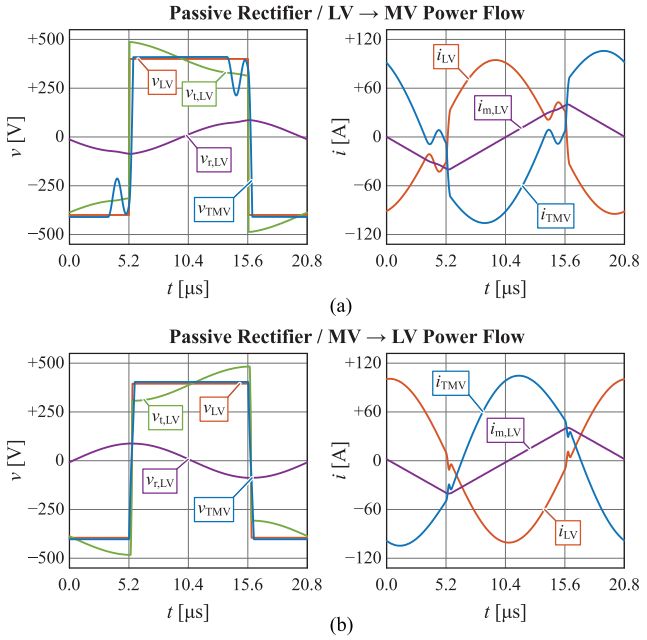

Fig. 5. Simulated voltages and currents with a passive rectifier bridge ($f_s = 48$ kHz and $P = 25$ kW). (a) The power flow is directed from the LV bridge (active) to the MV bridge (passive). (b) The power flow is directed from the MV bridge (active) to the LV bridge (passive).

bipolar semiconductors (e.g., IGBT) are typically operated with a discontinuous conduction interval, i.e., below the resonance frequency, for achieving ZCS. A small magnetizing current can be added for facilitating the recombination of the charge carriers and reducing the switching losses [17], [19], [24]. For SRC-DCXs using unipolar semiconductors (e.g., MOSFET), the usage of a discontinuous conduction interval is not necessary and would only increase the rms currents and, therefore, the losses [24]. Hence, such SRC-DCXs are operated at the resonance frequency with a significant magnetizing current in order to achieve ZVS [10], [20], [27]. Therefore, the considered converter, which is MOSFET based, is operated at the resonance frequency ($f_s = f_{res} = 48$ kHz).

Fig. 5(a) shows the obtained waveforms for a power flow directed from the LV to the MV side. The magnetizing current is flowing on the LV side and significant oscillations and distortions are observed. The current distortion during the commutation of the passive MV rectifier (see Fig. 4) is considerable since the output capacitance of the MV MOSFETs is large ($C_{oss,TMV} \gg C_{oss,LV}$, see Table I). This current distortion is contributing to the energy transfer and, therefore, is impacting the shape and the amplitude of the resonant current. This implies that, even if the converter is operated at the resonance frequency ($f_s = f_{res}$), a discontinuous conduction interval exists and oscillations can be observed. An increased switching frequency ($f_s > f_{res}$) would suppress the oscillations, but the current distortions due to the parasitic DAB operation would become larger.

Fig. 5(b) shows the obtained waveforms for a power flow directed from the MV to the LV side. The currents are almost sinusoidal, the magnetizing current is flowing on the MV side, and no significant oscillations or distortions occur. The current

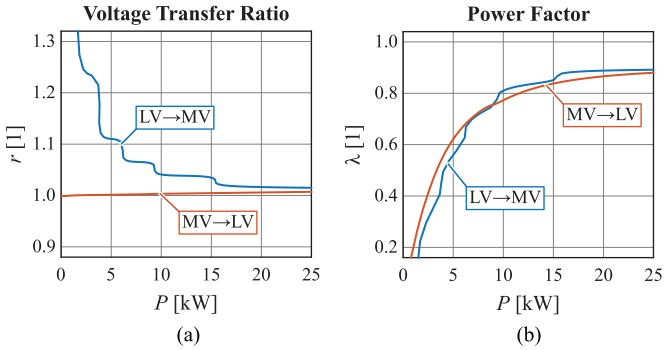

Fig. 6. (a) Voltage transfer ratio [see (5)] and (b) power factor [see (6)]. The SRC-DCX is operated with a passive rectifier bridge ($f_s = 48$ kHz) at different load conditions and for both power flow directions.

distortion during the commutation of the passive LV rectifier (see Fig. 4) is extremely small since the output capacitance of the LV MOSFETs is small ($C_{oss,TMV} \gg C_{oss,LV}$, see Table I) and allows for a fast commutation of the rectifier. The oscillations are not present since the converter is operated at the resonance frequency (no discontinuous conduction interval).

C. Partial-Load Operation

The modulation scheme should also work for partial-load operation. In order to evaluate the achieved performance, different figures of merit are introduced. The voltage transfer ratio (r) is defined as

$$r = \frac{V_{DC,TMV}}{V_{DC,LV}} \tag{5}$$

where the dc-bus voltages ($V_{DC,TMV}$ and $V_{DC,LV}$) are considered. Ideally, the voltage transfer ratio should be load-independent and approximately equal to $r \approx 1$, given that the voltage transformation is only provided by the transformer and by the combination between the half bridge and the full bridge [see (1)]. As a second figure of merit, the power factor (λ) is defined as

$$\lambda = \frac{|P|}{\frac{1}{2}\left(V_{LV} I_{LV} + V_{TMV} I_{TMV}\right)} \tag{6}$$

where the rms currents and voltages of the bridges (V_{LV}, I_{LV}, V_{TMV}, and I_{TMV}), and the transferred power (P) are considered. For an ideal SRC-DCX operated at the resonance frequency with a purely sinusoidal current (no oscillations, no distortions, and no magnetizing current), the obtained power factor is $\lambda = \sqrt{8}/\pi \approx 0.90$, which represents the theoretical maximum [24].

Fig. 6(a) shows the obtained voltage transfer ratio for different load conditions and power flow directions. For a power flow directed from the MV to the LV side, the voltage transfer ratio is, as expected, load-independent. For the reverse power flow direction, i.e., from the LV to the MV side, the voltage transfer ratio is not load-independent and is increasing as the load is reduced.

Fig. 7 shows this last case with a power flow of 5 kW, where the MV dc-bus voltage reaches 7.8 kV (instead of 7 kV). This increased voltage transfer ratio can be explained by the distortion of the resonant current occurring during the commutation of

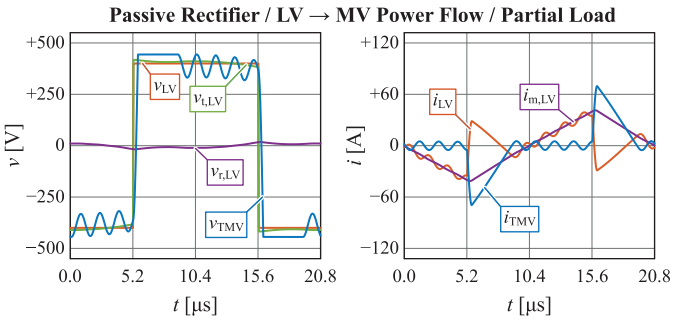

Fig. 7. Simulated voltages and currents at partial load with a passive rectifier bridge ($f_s = 48$ kHz and $P = 5$ kW). The power flow is directed from the LV bridge (active) to the MV bridge (passive).

the MV diodes (see Fig. 3). This current distortion transfers additional energy to the MV dc bus during partial-load operation and, therefore, causes a drift of the MV dc bus voltage until the transferred current matches the load current.

Fig. 6(b) shows the obtained power factor for different load conditions and power flow directions. The power factor at the nominal load (0.88) is close to the theoretical maximum (0.90) of the SRC-DCX. At partial load, the power factor is dropping, mostly due to the constant magnetizing current. Hence, complete ZVS of the active bridge is achieved for all load conditions.

For a power flow directed from the LV to the MV side, the curves shown in Fig. 6 are not smooth in function of the power flow. This is explained by the oscillations occurring during the discontinuous conduction interval which lead to varying initial conditions for the resonant pulses.

It can be concluded that the operation of the SRC-DCX with a passive (or synchronous) rectifier is problematic with a rectifier bridge with large semiconductor output capacitances and/or large mismatches between the semiconductor output capacitances of both bridges ($C_{\text{oss,TMV}}$ and $C_{\text{oss,LV}}$). Oscillations, current distortions, and a load-dependent voltage transfer ratio are occurring. The load-dependent voltage transfer ratio could be eliminated with duty cycle and frequency modulation of the active bridge, at the cost of an increased control complexity [16], [21], [22]. Furthermore, with a closed-loop voltage control, the SRC cannot be anymore considered as a DCX. Another solution is to switch actively the rectifier bridge in order to share the magnetizing current, used for ZVS, between the bridges.

IV. Active Rectifier/Analytical Model

In this section, both bridges are actively operated. This solution has already been examined in order to extend the power flow and voltage control capabilities of SRCs [22], [32], [33]. However, these results cannot be directly used since the goal of this paper is to examine the DCX operating mode, which should not require any closed-loop voltage control. Therefore, the proposed MCS-ZVS modulation scheme offers a DCX behavior with an active phase shift modulation between the bridges. In this section, the power flow is exclusively directed from the LV to the MV side since this has been identified as the critical case (see Section III). However, all the presented results are valid for both power flow directions.

A. Considered Model

Both bridges are actively operated with a duty cycle of 50% and a constant phase shift is actively applied between bridge voltages. For the analytical model, the switching transition durations of the MV and LV bridge are neglected and perfect rectangular voltages are considered. The SRC-DCX is operated at the resonance frequency for achieving sinusoidal currents

$$f_s \approx f_{\text{res}} = \frac{1}{2\pi}\frac{1}{\sqrt{L_s C_{\text{res}}}}. \tag{7}$$

The rectangular PWM voltages produced by the MV and LV bridge can be described by the following functions:

$$v_{\text{TMV}} = -V_{\text{DC,TMV}}\ \text{sgn}\left(\cos\left(2\pi f_s\left(t + t_p\right)\right)\right) \tag{8}$$

$$v_{\text{LV}} = -V_{\text{DC,LV}}\ \text{sgn}\left(\cos\left(2\pi f_s t\right)\right) \tag{9}$$

where t_p represents the phase shift between the bridges. The mismatch between the dc-bus voltages (ΔV_{LV}) can be defined as

$$\Delta V_{\text{LV}} = V_{\text{DC,LV}} - V_{\text{DC,TMV}}. \tag{10}$$

Fig. 8(a) shows the resulting equivalent circuit, the applied voltages, and the obtained currents, which can be decomposed into three distinct parts: The resonant current, the circulating current, and the magnetizing current.

B. Resonant Current

The equivalent circuit for the resonant current is shown in Fig. 8(b). Only the fundamental frequency of the voltages (first Fourier harmonic) is considered. The other harmonics are filtered out by the band-pass characteristic of the series resonant circuit. The phase shift (t_p) is neglected, but the mismatch (ΔV_{LV}) between the dc-bus voltages is considered

$$v_{\text{I,TMV}} = -\frac{4}{\pi}V_{\text{DC,TMV}}\ \cos\left(2\pi f_s t\right) \tag{11}$$

$$v_{\text{I,LV}} = -\frac{4}{\pi}V_{\text{DC,LV}}\ \cos\left(2\pi f_s t\right). \tag{12}$$

The magnetizing inductance (L_m) is neglected and, at the resonance frequency, the impedances of the leakage inductance (L_s) and the resonance capacitor (C_{res}) cancel each other out. Accordingly, only the resistance (R_w) remains. The currents in the equivalent circuit can be expressed as

$$I_{\text{I,pk}} = \frac{4}{\pi}\frac{\Delta V_{\text{LV}}}{R_w} \tag{13}$$

$$i_{\text{I,TMV}} = +I_{\text{I,pk}}\ \cos\left(2\pi f_s t\right) \tag{14}$$

$$i_{\text{I,LV}} = -I_{\text{I,pk}}\ \cos\left(2\pi f_s t\right). \tag{15}$$

As expected, the resonant current is sinusoidal and is created by the mismatch (ΔV_{LV}) between the dc-bus voltages required due to the losses (R_w). The transferred power (positive for the considered power flow) can be expressed as

$$P = \frac{8}{\pi^2}\frac{V_{\text{DC,LV}}\Delta V_{\text{LV}}}{R_w}. \tag{16}$$

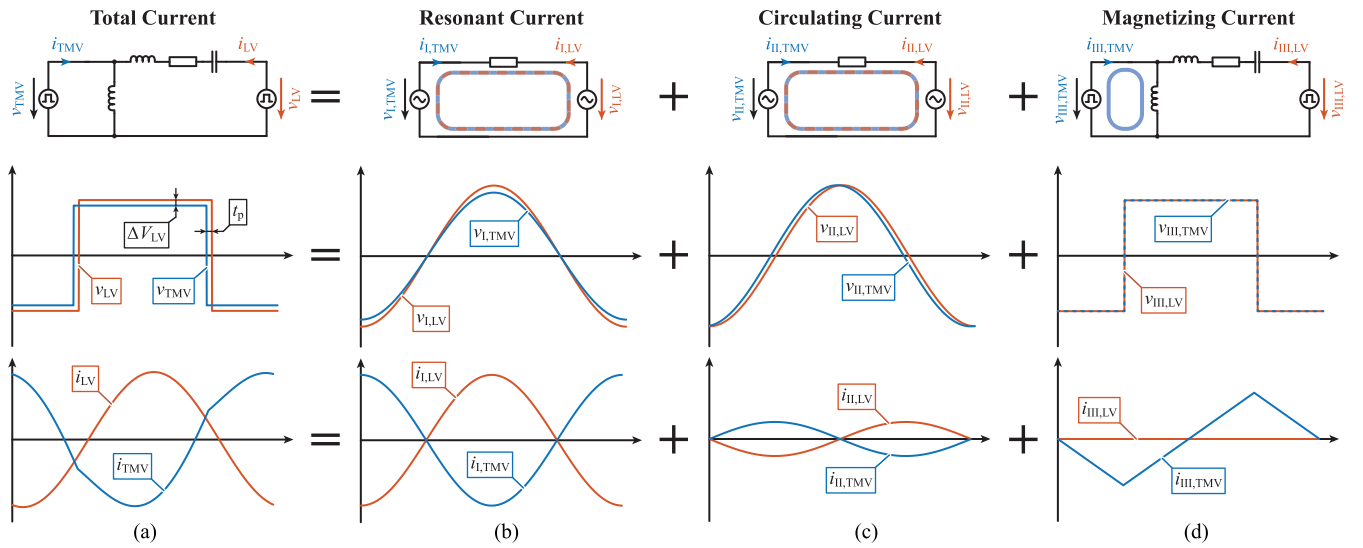

Fig. 8. (a) Equivalent circuit of the SRC-DCX (with a schematic view of the waveforms) operated with MCS-ZVS modulation (phase shifted PWM voltages with 50% duty cycle). The total current in the SRC-DCX can be decomposed into three parts. (b) Resonant current. (c) Circulating current. (d) Magnetizing current. A power flow from the LV to the MV side is considered.

Since R_w is small, both bridges are operated in a quasi-short circuit, resulting in a nearly load-independent voltage transfer ratio. This implies that a small mismatch (ΔV_LV) between the dc-bus voltages will create a large power flow, given that the side where the source is located (LV side) features a slightly higher voltage than the side where the load is located (MV side).

C. Circulating Current

The equivalent circuit for the reactive circulating current is shown in Fig. 8(c). Again, only the fundamental frequency of the voltages (first Fourier harmonic) is considered. The other harmonics are filtered out by the resonant tank. The mismatch (ΔV_LV) between the dc-bus voltages is neglected, but the phase shift (t_p) is considered

$$v_\mathrm{II,TMV} = -\frac{4}{\pi} V_\mathrm{DC,LV} \cos\left(2\pi f_\mathrm{s}\left(t + t_\mathrm{p}\right)\right) \tag{17}$$

$$v_\mathrm{II,LV} = -\frac{4}{\pi} V_\mathrm{DC,LV} \cos\left(2\pi f_\mathrm{s} t\right). \tag{18}$$

The magnetizing inductance (L_m) is neglected and, due to the operation at the resonance frequency, only the resistance (R_w) has to be considered. The currents in the equivalent circuit can be then expressed as

$$I_\mathrm{II,pk} = 8 f_\mathrm{s} \frac{t_\mathrm{p}}{R_\mathrm{w}} \tag{19}$$

$$i_\mathrm{II,TMV} = +I_\mathrm{I,LV,pk} \sin\left(2\pi f_\mathrm{s} t\right) \tag{20}$$

$$i_\mathrm{II,LV} = -I_\mathrm{I,LV,pk} \sin\left(2\pi f_\mathrm{s} t\right). \tag{21}$$

The phase shift between the bridges creates a circulating current, which is also sinusoidal. This current is orthogonal (90° phase shift) to the resonant current and, therefore, purely reactive.

D. Magnetizing Current

The equivalent circuit for the magnetizing current is shown in Fig. 8(d). The rectangular voltages formed by the bridges are considered, but the phase shift (t_p) and the mismatch between the dc-bus voltages (ΔV_LV) are neglected

$$v_\mathrm{III,TMV} = -V_\mathrm{DC,LV} \operatorname{sgn}\left(\cos\left(2\pi f_\mathrm{s} t\right)\right) \tag{22}$$

$$v_\mathrm{III,LV} = -V_\mathrm{DC,LV} \operatorname{sgn}\left(\cos\left(2\pi f_\mathrm{s} t\right)\right). \tag{23}$$

With this operating condition, no voltage is applied to the series elements (L_s, C_res, and R_w) and, therefore, no current is flowing between the bridges. Hence, the current flowing in the magnetizing inductance (L_m) is provided by the MV bridge

$$I_\mathrm{III,pk} = \frac{V_\mathrm{DC,LV}}{4 f_\mathrm{s} L_\mathrm{m}} \tag{24}$$

$$i_\mathrm{III,TMV} = -I_\mathrm{III,pk} \frac{2}{\pi} \arcsin\left(\sin\left(2\pi f_\mathrm{s} t\right)\right) \tag{25}$$

$$i_\mathrm{III,LV} = 0. \tag{26}$$

As expected, the magnetizing current is triangular (integral of the applied rectangular voltage). This current is also orthogonal to the resonant current and, therefore, purely reactive.

E. Choice of the Equivalent Circuit

The considered equivalent circuit features an important assumption: The series resistance of the transformer and of the MOSFETs (R_w) is placed on the LV side. In reality, this resistance would be shared between the MV and LV sides. The choice of a lumped resistance on the LV side has been made to simplify the model. Moreover, in the considered SRC-DCX, the resonant capacitor (C_res) is placed on the LV side. However, the resonant capacitor could be also placed on the MV side and be shared between both sides.

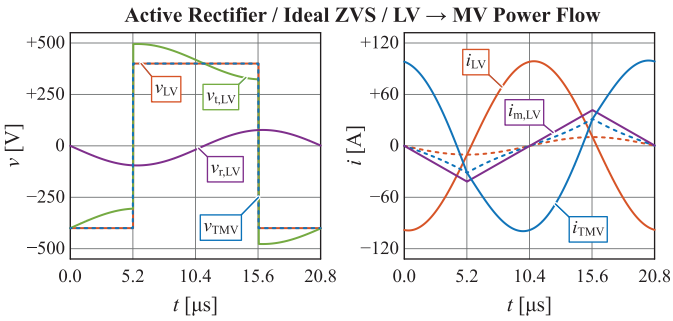

Fig. 9. Calculated voltages and currents with MCS-ZVS modulation ($f_s = 48$ kHz, $t_p = +2$ns, $P = 25$ kW, and power flow from the LV to the MV side). The reactive currents ($i_{TMV} - i_{I,TMV}$ and $i_{LV} - i_{I,LV}$) are indicated with dashed lines for both bridges. For the calculation, the semiconductor output capacitances of the bridges are neglected and perfect switching transitions are considered.

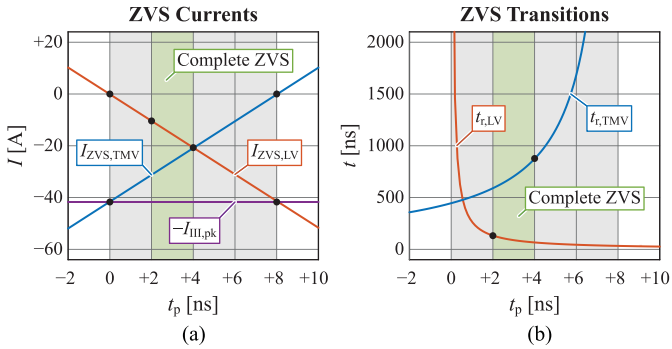

Fig. 10. Calculated (a) ZVS currents and (b) ZVS transition durations obtained for the SRC-DCX operated with MCS-ZVS modulation ($f_s = 48$ kHz, $t_p \in [-2, +10]$ ns). Complete ZVS is calculated as achievable within a reasonable dead time for $I_{ZVS,LV} < -10$ A and $I_{ZVS,TMV} < -20$ A. For the calculation of the currents, the semiconductor output capacitances of the bridges are neglected and ideal instantaneous switching transitions are considered.

The fact that the magnetizing current is solely provided by the MV bridge results from the positions of the resonant capacitor (C_{res}) and the series resistance (R_w). In reality, the magnetizing current will be shared between the bridges [29]. However, the presented model, which features a simple analytical interpretation, is sufficient for explaining the fundamental working principle of the SRC-DCX with MCS-ZVS modulation.

F. Current Waveforms

The three currents shown in Figs. 8(b)–(d) can be superimposed in order to obtain an approximation of the total current shown in Fig. 8(a). This approximation is extremely accurate, i.e., shows less than 8% rms error for the current waveforms for the complete operating range.

The resonant current is only dependent on the mismatch between the dc-bus voltages (ΔV_{LV}), which is, therefore, determining the power flow. The circulating current is only dependent on the phase shift (t_p) and is purely reactive. The magnetizing current is independent of both the mismatch between the dc-bus voltages (ΔV_{LV}) and the phase shift (t_p). This implies that the active and reactive power flow can be controlled independently.

Fig. 9 shows the obtained waveforms. Since both bridges are operated at the resonance frequency with a duty cycle of 50%, no discontinuous conduction interval can be observed. The superposition of the resonant current and the reactive currents is highlighted.

G. ZVS Currents

Without loss of generality, only the switching transitions near $t \approx 1/(4f_s)$ are considered (half-wave symmetry of the waveforms). At the switching instant, the resonant current is zero and only the circulating and magnetizing currents are contributing to ZVS (see Fig. 8). The ZVS currents in the LV bridge ($I_{ZVS,LV}$) and MV bridge ($I_{ZVS,TMV}$) can be computed as

$$I_{ZVS,TMV} = +I_{II,pk} - I_{III,pk} \tag{27}$$

$$I_{ZVS,LV} = -I_{II,pk}. \tag{28}$$

The signs are chosen such that ZVS is achieved for negative $I_{ZVS,LV}$ and $I_{ZVS,TMV}$. The applied phase shift introduces the reactive circulating current ($I_{II,pk}$), which effectively is equivalent to a sharing of the magnetizing current ($I_{III,pk}$) between both bridges. However, the total current available for ZVS for both bridges is limited by the magnetizing current ($I_{III,pk}$). The switching durations of the LV bridge ($t_{r,LV}$) and MV bridge ($t_{r,TMV}$) can be computed as

$$t_{r,TMV} = -C_{oss,TMV}\frac{2V_{DC,TMV}}{I_{ZVS,TMV}} \tag{29}$$

$$t_{r,LV} = -C_{oss,LV}\frac{2V_{DC,LV}}{I_{ZVS,LV}}. \tag{30}$$

These expressions are only valid if complete ZVS is achieved (negative $I_{ZVS,LV}$ and $I_{ZVS,TMV}$). It should again be noted, that the impact of the ZVS transition durations on the currents is not considered with the presented analytical model since the currents are derived with perfect rectangular PWM voltages.

Fig. 10 shows the ZVS currents and the ZVS transition durations for different phase shifts. As expected, for all phase shifts, the sum of both ZVS currents ($I_{ZVS,TMV}$ and $I_{ZVS,LV}$) is limited by the magnetizing current ($I_{III,pk}$). The ZVS transitions are much faster for the LV bridge than for the MV bridge ($C_{oss,TMV} \gg C_{oss,LV}$, see Table I).

The ZVS currents are negative for both bridges for $t_p \in [0, +8]$ ns. However, the ZVS currents should be sufficiently negative for obtaining complete ZVS within a reasonable dead time [26], [28]. Complete ZVS is calculated as achievable within a reasonable dead time for $I_{ZVS,TMV} < -20$ A and $I_{ZVS,LV} < -10$ A. The phase shift window, where complete ZVS is achievable, is reduced to $t_p \in [+2, +4]$ ns. In Fig. 9, a phase shift of $t_p = +2$ ns (minimum value) has been chosen to minimize the mismatch between the switching transition durations of both bridges. The phase shift window, where complete ZVS is achievable, is so small that the robustness of the modulation scheme should be further analyzed with a more detailed ZVS model.

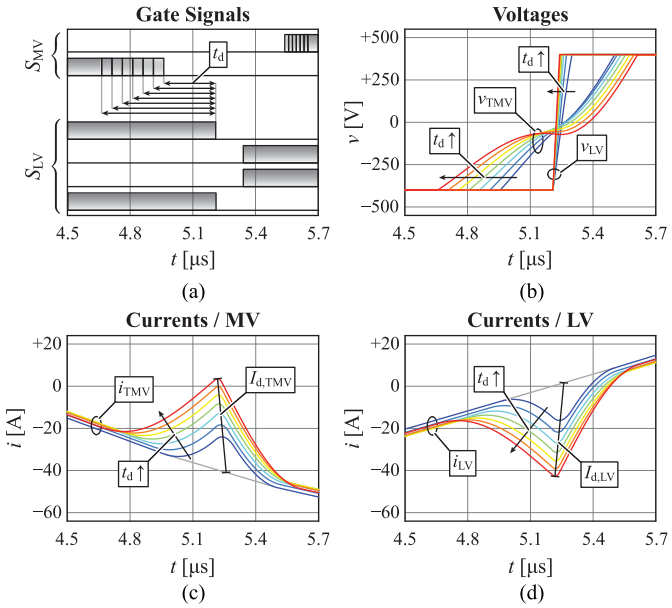

Fig. 11. Simulated ZVS transition with MCS-ZVS modulation for different time delays ($f_s = 48$ kHz, $P = 25$ kW, $t_d \in [+250, +550]$ ns, and power flow from the LV to the MV side). (a) Applied gate signals. (b) Bridge voltages. (c) LV currents. (d) MV currents.

V. Active Rectifier/Simulations

In this section, both bridges are actively operated with a duty cycle of 50% and a constant delay (t_d) is actively applied between the gate signals of the MV and LV bridges, resulting in a phase shift (t_p) between the bridge voltages (see Section IV). The ZVS transitions are now simulated with the output capacitances of the MOSFETs, which implies that the coupling between the ZVS currents and the ZVS transition durations is considered [26], [28]. For the following analysis, the power flow is exclusively directed from the LV to the MV side since this has been identified as the critical case (see Section III). However, all the presented results are valid for both power flow directions.

A. Phase Shift Operation

The obtained phase shift (t_p) between the bridge voltages depends on the applied delay (t_d) between the gating of the bridges and the ZVS switching transition durations ($t_{r,TMV}$ and $t_{r,LV}$), which are determined by the ZVS currents ($I_{ZVS,TMV}$ and $I_{ZVS,LV}$). The coupling between the ZVS currents and the ZVS transition durations implies that only an indirect relation exists between t_p and t_d.

This effect is shown in Fig. 11, where the voltages and the currents are simulated for different time delays. It can be seen that the complete ZVS is achieved for both bridges in a wide range of time delays ($t_d \in [+250, +550]$ ns). This is astonishing, considering the results obtained in Fig. 10, where the switching transitions have been assumed as infinitely fast and ZVS could only be achieved in a very narrow range of time delays (t_d). This difference between the analytical model and the simulations is due to the ZVS mechanism, which is automatically aligning the voltages, such that the phase shift (t_p) between the bridge voltages is always close to zero. The aforementioned analytical model (see Section IV) can be used for explaining this alignment effect for a fixed time delay (t_d)

$$t_p \uparrow \Rightarrow\ I_{ZVS,TMV} \uparrow\ \wedge\ I_{ZVS,LV} \downarrow \tag{31}$$

$$I_{ZVS,TMV} \uparrow\ \wedge\ I_{ZVS,LV} \downarrow \Rightarrow\ t_{r,TMV} \uparrow\ \wedge\ t_{r,LV} \downarrow \tag{32}$$

$$t_{r,TMV} \uparrow\ \wedge\ t_{r,LV} \downarrow \Rightarrow\ t_p \downarrow . \tag{33}$$

This self-alignment effect is stabilizing the modulation scheme, ensuring that large tolerances are acceptable for the time delay between the gating of the bridges (t_d). It appears that, as expected, the ZVS currents and the ZVS transition durations can be controlled by adjusting the time delay (t_d). The following approximations can be made (assuming $C_{oss,TMV} \gg C_{oss,LV}$, see Table I):

$$t_{r,TMV} \approx 2t_d \tag{34}$$

$$t_{r,LV} \approx 0 \tag{35}$$

$$t_p \approx 0. \tag{36}$$

Due to the mismatch of the switching transition durations of the MV and LV bridges, the SRC is shortly operated as a DAB causing a current distortion during the switching transitions, as explained in Section III. The amplitude of the current spikes ($I_{d,TMV}$ and $I_{d,LV}$) can be expressed as (see Fig. 11)

$$I_{d,TMV} \approx +\frac{V_{DC,TMV} t_d}{2L_s} \tag{37}$$

$$I_{d,LV} \approx -\frac{V_{DC,LV} t_d}{2L_s}. \tag{38}$$

Since the phase shift between the bridge voltages is almost zero, these spikes are only causing local distortions and are not changing the global shape of the currents. Nevertheless, these current distortions have an impact on the ZVS currents [see (28) and (27)]. The current $I_{d,LV}$ is negative and increases the LV-ZVS current. The current $I_{d,TMV}$ is positive and decreases the MV-ZVS current, slowing down the switching speed of the MV bridge, especially in the middle of the switching transition (see Fig. 11).

For large time delays ($t_d > +550$ ns), the MV-ZVS current becomes positive and the MV bridge starts to oscillate back in the middle of the transition. For small time delays ($t_d < +250$ ns), the LV-ZVS current is not sufficient to obtain complete ZVS, implying that matching the switching transition durations of both bridges ($t_{r,TMV} = t_{r,LV}$) is not achievable.

The choice of the time delay should be done with two objectives in mind—the minimization of the mismatch between the switching transition durations of both bridges and the mitigation of the switching speed. For the considered converter, a phase shift of $t_d = +270$ ns, which is close to the minimum value, has been chosen in order to minimize the mismatch between the switching transition durations. With this choice, the switching speed is still moderate (below 15 kV/µs), due to the achieved ZVS with quasi-ZCS.

Fig. 12 shows the obtained waveforms. The currents and voltages are very similar to the results obtained with the analytical

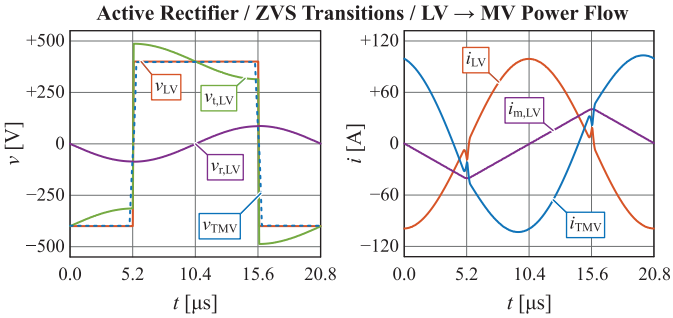

Fig. 12. Simulated voltages and currents with MCS-ZVS modulation ($f_s = 48$ kHz, $t_d = +270$ ns, and $P = 25$ kW, and power flow from the LV to the MV side). The reactive currents (circulating current and magnetizing current) are almost exclusively flowing in the MV bridge [see (27)] and the LV bridge is switched with the current distortion [see (38)].

model (see Fig. 9), except for the aforementioned small current spikes occurring during the switching transition. With the chosen time delay, the reactive currents (circulating current and magnetizing current) are almost exclusively flowing in the MV bridge [see (29)] and the LV bridge is switched with the current distortion [see (38)]. Therefore, the maximum possible current (the magnetizing current) is switched by the MV bridge, which exhibits the larger semiconductor output capacitances ($C_{\text{oss,TMV}} \gg C_{\text{oss,LV}}$, see Table I).

B. Robustness of the Modulation Scheme

With the aforementioned results, it appears that the modulation scheme is highly robust with respect to the delay (t_d) between the gating of the bridges. However, the robustness of the modulation scheme should be further examined, particularly with respect to the operating frequency (f_s). Due to model non-idealities (e.g., non-modeled parasitics) and production tolerances (e.g., transformer parameters and capacitor values), the operating frequency (f_s) might not exactly match the resonance frequency (f_{res}) [29], [34].

Fig. 13 shows the voltage transfer ratio, the phase shift between the bridge voltages (computed between the first Fourier harmonics), and the ZVS transition durations for different time delays (t_d) and operating frequencies (f_s). The voltage transfer ratio is almost constant and ZVS is achieved for the complete range. The time delay, as already shown in Fig. 11, allows for the sharing of the magnetizing current and, therefore, to choose the ZVS switching durations. If the converter is operated at the resonance frequency, the phase shift between the bridge voltages is almost zero (see Fig. 11). For other operating frequencies, a phase shift is automatically introduced by the ZVS mechanism and compensates the mismatch between the resonant capacitor (C_{res}) and the leakage inductance (L_s).

Therefore, it can be concluded that the proposed modulation scheme is robust in a wide range of time delays and operating frequencies. Model non-idealities or production tolerances will only marginally affect the obtained waveforms and complete ZVS can still be achieved.

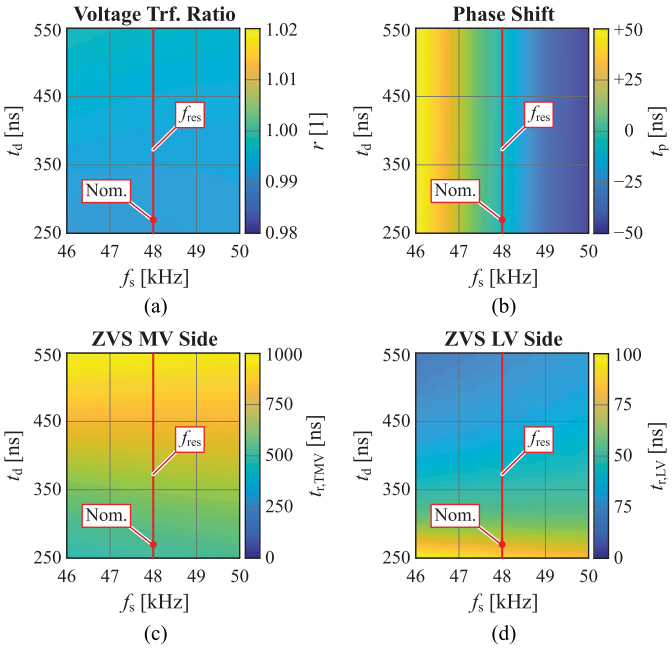

Fig. 13. Simulated (a) voltage transfer ratio [see (5)], (b) phase shift between the bridge voltages (computed between the first Fourier harmonics), (c) MV-ZVS switching durations, and (d) LV-ZVS switching durations. The SRC-DCX is operated with MCS-ZVS modulation ($P = 25$ kW and power flow from the LV to the MV side). Different time delays (t_d) and operating frequencies (f_s) are considered. The nominal operating point ($f_s = 48$ kHz, $t_d = +270$ ns) is indicated.

C. Partial-Load Operation

The modulation scheme should also work for partial-load operation. Fig. 14 shows the obtained voltage transfer ratio, power factor, ZVS currents, ZVS switching transition durations, and the phase shift between the bridge voltages. The voltage transfer ratio is almost constant (less than 0.5% deviation) since no oscillations and no current distortions occur. The power factor at the nominal load (0.88) is close to the theoretical maximum (0.90) of the SRC-DCX. Complete ZVS is achieved for the complete load range. The variation of the ZVS currents (average during the switching transitions) and ZVS switching transition durations is also small (less than 25% deviation). The phase shift between the bridge voltages is always close to zero, proving that the self-alignment of the PWM signal works for all load conditions without requiring a dynamic regulation of the phase shift.

Therefore, the goals defined in Section II are achieved. A robust modulation scheme, featuring a load-independent voltage transfer ratio, bidirectional power flow, load-independent ZVS (and quasi-ZCS), and quasi-sinusoidal currents, has been found. The converter will act as a DCX for the complete load range without requiring measurements or closed-loop voltage control.

VI. Measurements

The considered converter (see Fig. 2(a) and Table I) has been constructed. Fig. 15 shows the realized prototype, which features the following power density: 3.8 kW/l, 62 W/in^3, 2.9 kW/kg,

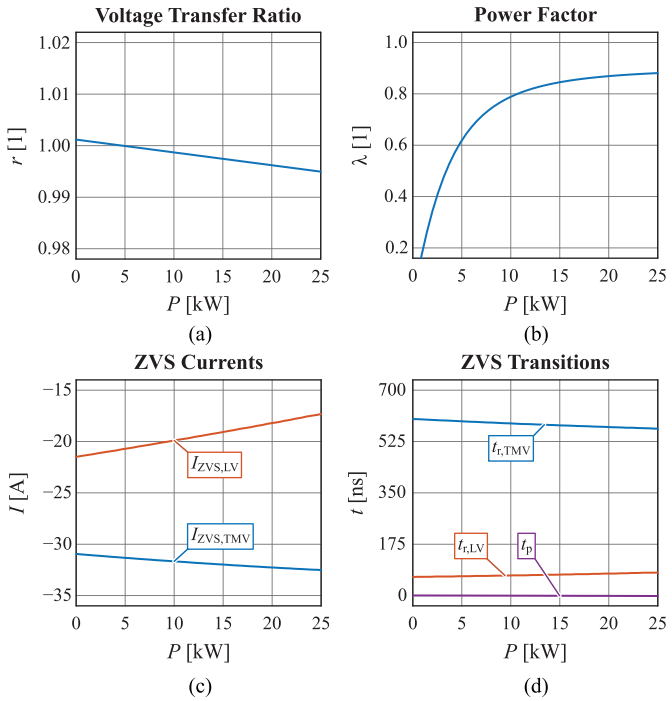

Fig. 14. Simulated (a) voltage transfer ratio [see (5)], (b) power factor [see (6)], (c) ZVS currents (average over the switching durations), and (d) ZVS transition durations. The phase shift between the bridge voltages is also shown (computed between the first Fourier harmonics). The SRC-DCX is operated with MCS-ZVS modulation ($f_s = 48$ kHz, $t_d = +270$ ns, $P = 25$ kW, and power flow from the LV to the MV side) at different load conditions.

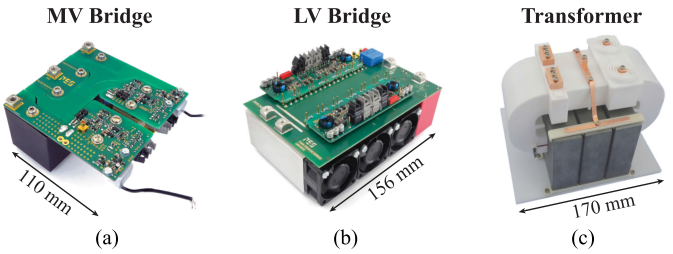

Fig. 15. Considered 25 kW SRC-DCX operated at 48 kHz between a 7 kV and a 400 V dc bus (see Fig. 2(a) and Table I). (a) MV bridge based on 10 kV SiC MOSFETs. (b) LV bridge based on 1200 V SiC MOSFETs. (c) Medium-frequency transformer.

and 1.3 kW/lb. The MV half bridge is realized with "Cree QPM3-10000-0300" 10 kV SiC MOSFETs [35]. The LV full bridge employs "Cree C2M0025120D" 1200 V SiC MOSFETs, where three devices are placed in parallel per switch [36]. The transformer (7.4 kW/l, 121 kW/in^3, 4.0 kW/kg, and 1.8 kW/lb) is constructed with litz wire windings, a ferrite core, and silicone insulation. More details on the realized prototype can be found in [6].

A. Modulation Scheme

The proposed MCS-ZVS modulation scheme is applied. Fig. 16 shows the obtained measurements at 25.3 kW (power flow from the LV to the MV side). The measured waveforms are in very good agreement with the simulations (see Fig. 12). This implies that the accepted assumptions are valid—linearized

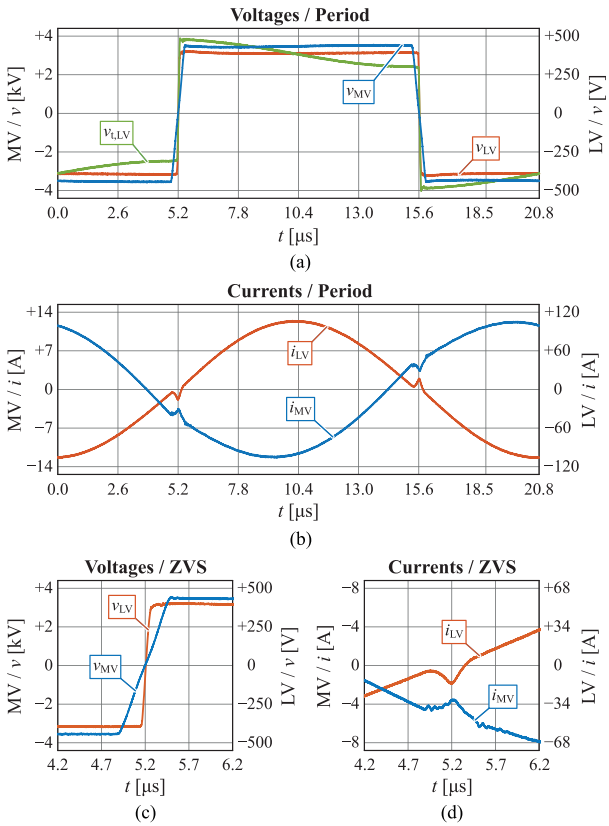

Fig. 16. Measured (a) voltages and (b) currents for a complete switching period. Measured (c) voltages and (d) currents during the ZVS transitions. The MCS-ZVS modulation ($f_s = 48$ kHz, $t_p = +270$ ns, $P = 25.3$ kW, and power flow from the LV to the MV side) is used.

charge-equivalent semiconductor output capacitances ($C_{oss,TMV}$ and $C_{oss,LV}$), lumped series resistance placed on the LV side (R_w), neglected dc-bus ripples, and neglected stray capacitances of the transformer.

The measured currents are almost perfectly sinusoidal (no oscillations or significant distortions) and ZVS is achieved for both bridges. As expected (see Fig. 11), the phase shift between the bridge voltages is very small. The time delay between the gates is chosen such that (see Fig. 12) the magnetizing current is almost exclusively flowing in the MV bridge [see (29)] and the LV bridge is switched with the current distortion [see (38)]. However, the magnetizing current, which is a virtual current, cannot directly be measured in a prototype, and therefore, is not shown [29]. At full-load operation, the measured power factor (0.87) is close to the theoretical maximum (0.90) of the SRC-DCX.

The converter has been tested for $P \in [0{,}25]$ kW with a power flow from the LV to the MV side. In the complete range, ZVS is achieved, no oscillations are observed, and the voltage transfer ratio is almost constant (less than 0.8% deviation). Therefore, it can be concluded that the proposed MCS-ZVS modulation scheme is working as expected from the simulation model.

For the sake of completeness, the converter has also been successfully tested with a power flow from the MV to the LV side. In this case (see. Section III), the converter can be operated with the typical synchronous rectification modulation scheme

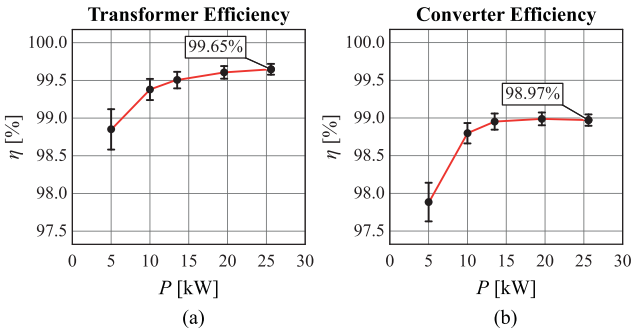

Fig. 17. (a) Measured efficiency of the transformer and (b) dc–dc converter with the corresponding measurement tolerance. More details on the measurement of the losses can be found in [6].

or with the proposed MCS-ZVS modulation scheme. The MCS-ZVS modulation scheme has been preferred since it does not require a zero-crossing detection of the current.

B. Efficiency Measurements

The comparatively low rms currents (high power factor), associated with the quasi-sinusoidal shapes, allow for an efficient operation of the transformer. Fig. 17(a) shows the calorimetrically measured efficiency of the transformer (including core, winding, dielectric, and fan losses) [6]. The full-load efficiency of the transformer reaches $99.65 \pm 0.07\%$.

The achieved complete ZVS with quasi-ZCS leads to reduced semiconductor losses, even for the comparatively high switching frequency (48 kHz) for an MV converter [25]. Fig. 17(b) shows the calorimetrically measured efficiency of the converter (including transformer, LV MOSFETs, MV MOSFETs, capacitors, fans, and auxiliary circuit losses) [6]. The complete converter achieves a full-load efficiency of $98.97 \pm 0.08\%$ [6].

Moreover, the converter reaches an efficiency close to 99.0% between 13 and 25 kW. Therefore, it can be concluded that the converter, despite the additional magnetizing current required for achieving ZVS, achieves extremely high full-load and partial-load efficiencies.

VII. Conclusion

This paper studies the operation of a 25 kW bidirectional dc–dc converter operating at 48 kHz between a 7 kV and a 400 V dc bus. The converter is implemented as a SiC MOSFET-based SRC-DCX topology operating at the resonance frequency. This converter behaves as a DCX and features a load-independent voltage transfer ratio in open-loop, quasi-sinusoidal currents, and achieve ZVS with the magnetizing current.

First, the converter operation is analyzed with a passive (or synchronous) rectifier. It is shown that, for rectifier bridges implemented with semiconductors exhibiting large output capacitances (e.g., 10 kV SiC MOSFETs), oscillations, current distortions, and a load-dependent voltage transfer ratio occur. Therefore, the system does not show a DCX behavior and passive (or synchronous) rectification cannot be used.

These problems can be solved with the proposed MCS-ZVS modulation scheme, where a small phase shift is introduced between the gating of the MV and LV bridges. This modulation scheme is analyzed with analytical and numerical models. The magnetizing current, which is available for ZVS, can be actively shared between both bridges with proper phase shift. It is found that the ZVS mechanism is effectively acting as a controller, which is automatically stabilizing the modulation scheme. All in all, the proposed modulation scheme features the following characteristics: Load-independent voltage transfer ratio, load-independent ZVS (and quasi-ZCS) for both bridges, quasi-sinusoidal currents (low distortion), and robustness against model non-idealities and tolerances. Therefore, the converter will act as a bidirectional DCX for the complete load range without requiring measurements or closed-loop voltage control.

Finally, the described modulation scheme is experimentally verified with an SiC MOSFET-based SRC-DCX with the following ratings: 7 kV to 400 V, 48 kHz, 25 kW, 3.8 kW/l, and 2.9 kW/kg. The measured waveforms are in good agreement with the simulations. Due to the achieved complete ZVS and the quasi-sinusoidal currents, a full-load efficiency of 99.0% is achieved. Moreover, the peak efficiency of 99.0% is maintained between 50% and 100% load.

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