Accurate Temperature Estimation of SiC Power MOSFETs Under Extreme Operating Conditions

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***Abstract*—Electrothermal modeling of silicon carbide (SiC) power devices is frequently performed to estimate the device temperature in operation, typically assuming a constant thermal conductivity and/or heat capacity of the SiC material. Whether and by how much the accuracy of the resulting device temperature prediction under these assumptions is compromised has not been investigated so far. Focusing on high-temperature operating conditions as found under short circuit (SC), this paper presents a comprehensive analysis of thermal material properties determining the temperature distribution inside SiC power MOSFETs. Using a calibrated technology computer-aided design (TCAD) electrothermal model, it is demonstrated that the temperature prediction of SiC power devices under SC operation when neglecting either the top metallization or the temperature dependence of the heat capacity is inaccurate by as high as 25%. The presented analysis enables to optimize compact electrothermal models in terms of accuracy and computational time, which can be used to assess the maximum temperature of SiC power MOSFETs in both discrete packages and multichip power modules exposed to fast thermal transients. A one-dimensional thermal network of a SiC power MOSFET is proposed based on the thermal material properties, the size of the active area of the device, and its thickness.**

***Index Terms*—Electrothermal (ET) modeling, short circuit (SC), silicon carbide (SiC), TCAD, thermal conductivity.**

I. Introduction

With the ever-increasing requirements for energy saving, the adoption of silicon carbide (SiC) power transistors has been following a growing trend across different power electronic (PE) applications, including electrical vehicles (EVs), EV charging infrastructure, power factor correction, power supply, photovoltaics, uninterruptible power supplies, motor drives, wind, and rail [1]. Increasing the acceptance of the emerging SiC technology in the field of high-frequency, high-temperature, and/or high-power applications needs to be supported by a comprehensive understanding of SiC material properties and their influence on the system performance. Nowadays, multiphysics modeling tools based on the underlying physics of the SiC material are widely employed both in academia and industry to assess the benefits of SiC power devices in PE systems and to optimize the system performance. Besides a careful electromagnetic design, thermal design increases in importance especially with the wide operational temperature range enabled by SiC. As the switching elements of PE systems, power devices can experience high-temperature transients during, e.g., short-circuit (SC) events or the overvoltages caused by unclamped inductive switching (UIS). Under these operating conditions, the temperature of SiC power devices can reach significantly higher levels than it is the case for silicon (Si) power devices. Due to thinner gate oxides and higher electric field in the SiC MOSFETs compared to Si MOSFETs and insulated-gate bipolar transistors (IGBTs), the gate oxide of the SiC MOSFET is more vulnerable to thermal effects [2]. Additionally, the gate and source contact in SiC MOSFETs is exposed to high-temperature transients. Therefore, the heat handling capability of the device as a whole needs to be carefully assessed. An accurate prediction of the temperature evolution inside the semiconductor volume, oxide-semiconductor interface, gate oxide, and top metallization is highly useful in terms of preventing device failure, hence enhancing the reliability of the whole system.

In practice, temperature measurements based on direct [3], [4] and indirect methods [5], [6] are performed to evaluate the temperature of power devices in the operation. These measurements provide either a single average junction temperature or a surface temperature distribution; additionally, the temperature calibration has to be performed in advance and sets the limits for the maximum measurable temperature levels [7]. For the measurements of fast temperature transients, which occur, e.g., during the SC or avalanche operation, rather complicated custom-made temperature measurement setups, as, e.g., [3], are necessary. Accordingly, electrothermal (ET) simulations are performed to estimate the temperature of power devices and modules, which cannot be easily approached in thermal measurements. Besides the geometry data input, thermal material properties, namely, thermal conductivity and heat capacity, are required for an accurate temperature evaluation in ET simulations. Thermal conductivity k and heat capacity c_{v} of semiconductors such as Si and SiC are temperature and doping dependent; furthermore, k of 4H-SiC, the semiconductor material used in commercially available SiC power devices, is anisotropic. The tradeoff between the accuracy and the simulation time when neglecting the temperature dependence and anisotropy of SiC thermal properties is still not well understood. This can be evidently observed in a number of publications, e.g., [8]–[13], assuming constant thermal

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conductivity and/or heat capacity of SiC in the ET simulations of power devices operating at high temperatures without a detailed analysis.

Accordingly, the main aim of this paper is to show the influence of these parameters on the device temperature prediction for high-temperature operation of SiC power MOSFETs in a comprehensive way. This is specifically shown with the first complete two-dimensional (2-D) TCAD simulations, taking into account adequate temperature dependence of material parameters as well as the entire device structure including top metallization. The findings are then implemented in a compact RC thermal model with full temperature dependence for the SiC MOSFET.

The rest of this paper is organized as follows. In Section II, an extensive literature overview on the available SiC material data and the ET modeling of SiC power MOSFETs is presented explaining the main motivation behind the research conducted in this paper. Section III investigates the impact of SiC thermal characteristics on the temperature estimation using the SC operation as an example, based on comprehensive TCAD simulations, which considers both the temperature-dependent thermal properties and k-anisotropy. In Section IV, a compact RC thermal model of a SiC power MOSFET including temperature dependence of both thermal conductivity and heat capacity implemented in the circuit simulator LTSpice is compared to the existing RC thermal networks proposed in the literature.

II. Literature Overview

ET modeling is used to gain transient and steady-state temperature development inside power devices and modules under given operating conditions. A study on nonlinear compact thermal models of Si power modules presented in [14] showed that the influence of temperature-dependent thermal capacitance is negligible, while the temperature-dependent thermal conductivity has to be modeled for temperature amplitudes higher than 80 K in order to have a more accurate temperature prediction, i.e., aiming for a relative error, $\epsilon < 10\%$. During the temperature transients shorter than $\tau \approx 100\ \mu$s, the temperature gradient ΔT builds up mainly across the semiconductor die, and the temperature below the die remains unchanged. In field operation, such fast transients can occur under SC and UIS. The maximum temperature of SiC power MOSFETs during these events can reach levels above 1000 K, which is significantly higher than in their counterparts, Si-IGBTs [15]. Moreover, the temperature variation is typically significantly higher than 80 K, and the temperature dependence of the heat capacitance should not be automatically neglected without physical justifications.

A. SiC Thermal Properties

Today's commercially available SiC power devices are based on the 4H polytype [16]. However, the data on thermal conductivity and heat capacity of 4H-SiC in the literature are limited, especially for the high-temperature range above 600 K. Based on differential scanning calorimetry, measurements of the 4H-SiC heat capacity were performed up to 770 K in [17] and then extrapolated up to 2200 K. Using the time-domain thermoreflectance (TDTR) method, the anisotropic thermal conductivity of n-doped and unintentionally doped semi-insulating 4H-SiC was experimentally determined up to 600 K in [18]; the one of V-doped bulk semi-insulating 4H-SiC in the temperature range up to 850 K in [19]. In the TDTR method, a prior known temperature-dependent volumetric heat capacity $c_{\mathrm{v}}(T)$ is needed to extract the temperature-dependent thermal conductivity of the material, $k(T)$, by solving the heat conduction equation. Accordingly, the accuracy of $c_{\mathrm{v}}(T)$ impacts the accuracy of the extracted $k(T)$. In [18] $c_{\mathrm{v,6HSiC}}(T)$ from the literature was used, while, in [19], a theoretical estimation of $c_{\mathrm{v,4HSiC}}(T)$ close to $c_{\mathrm{v,6HSiC}}(T)$ was employed to calculate $k_{\mathrm{4HSiC}}(T)$. According to the experimental results presented in [17], $c_{\mathrm{v,4HSiC}}(T)$ is close to $c_{\mathrm{v,6HSiC}}(T)$ at room temperature and about 10% higher at elevated temperatures above 1000 K. Due to the lack of the available data for 4H-SiC at higher temperatures, the thermal parameters of 4H-SiC are approximated by the experimentally extracted properties of 6H-SiC as suggested in [20] or of 3C-SiC as shown in [21]. The thermophysical experimental data for 6H-SiC in the temperature range up to 2700 K were shown in [22]–[24] and for 3C-SiC in [25]. Recent research [18] has shown that 4H-SiC has an approximately 10% higher thermal conductivity than 6H-SiC in the measurement range up to 450 K. Furthermore, experimental results from [18] and [26] and from first principle calculations [27] demonstrated that the in-plane thermal conductivity, k_{r}, is $\approx$ 30–40% higher than the out-plane thermal conductivity, k_{c}, i.e., $k_{\mathrm{r}}/k_{\mathrm{c}} \approx 1.3$, for both 6H-SiC and 4H-SiC around 400 K.

B. ET Modeling of 4H-SiC Power Devices

The analysis of SiC power devices at the high-temperature levels is typically performed by the aid of finite-element method (FEM) and/or the finite-volume method (FVM) ET simulations [3], [28], [29], which simultaneously solve the drift-diffusion and heat transport equations. The TCAD modeling presented in the literature so far typically did not take into account the source metallization and effects such as phase transitions of materials experiencing melting or oxide leakage currents, which, in turn, occur in SiC power MOSFETs during the SC transition. The main reason is a very high computational cost, i.e., convergence problems, and the limited available calibration dataset for SiC. As a result, the temperatures extracted from the TCAD simulations presented in the literature have to be understood with a certain inaccuracy margin. As FEM simulations are computationally demanding for the circuit-level modeling in PE, there is a need for ET modeling approaches, which enable computationally efficient coupling between the circuit and thermal domains. A more simplified ET modeling exploits the electrical analogy of heat conduction by calculating the heat distribution employing equivalent electrical circuits. The equivalent circuits can then be solved together with compact device models using available circuit simulators. The computational time and complexity of parameterizing and/or solving equivalent networks increases by taking into account heat spreading, anisotropy, and temperature dependence of material properties. The three-dimensional (3-D) equivalent thermal networks consisting of resistors R and capacitors C developed to model primarily the nominal operation of power devices, as, e.g., [30]–[32], neglect the temperature dependence of material parameters. On the other hand, the 3-D

thermal networks that can take into account the temperature-dependent material thermal properties, e.g., [33], [34], imply a higher computational cost due to the need to update the system matrix in each simulation step, which is less attractive for the multiphysics modeling in PE. A special 3-D nonlinear thermal network of SiC power MOSFETs parameterized using FEM simulations was described in [10] taking into account temperature-dependent thermal conductivity and assuming constant heat capacitance. An SC simulation was used to demonstrate the coupling between the proposed thermal network and a compact model of a SiC power MOSFET, assuming, however, constant heat capacitance. In PE, the one-dimensional (1-D) heat transfer approximation with its limits to represent heat spreading and thermal coupling accurately is typically selected over more complex modeling techniques when a shorter simulation time is required, i.e., as for optimization and virtual prototyping at system level. The 1-D thermal modeling can be used to estimate the maximum temperature of power devices in discrete packages and multichip power modules during fast temperature transients [35], when the temperature gradient is mainly located across the die. The work presented here (see Section IV) uses a Cauer RC network for a commercial SiC power MOSFET, specifically including top metallization, volume heat generation, and temperature dependence of the thermal conductivity and the heat capacity with the aim to investigate the error made by assuming temperature insensitive RC cells for modeling SiC power MOSFETs under the extreme operating conditions.

III. Effects of SiC Thermal Properties

The effect of temperature-dependent thermal conductivity at high temperatures was demonstrated for Si-IGBTs in, e.g., [36]. With the capability of SiC power devices to operate in a wider temperature range, this effect can be expected to be even higher than in Si power devices, as described in [37]. Therefore, the temperature dependence of thermal conductivity and heat capacity should be properly addressed for high-temperature operation of commercially available SiC power devices. This section demonstrates the impact of SiC thermal properties on the temperature development internal to SiC power MOSFETs under extreme operating conditions by using SC operation as an example. The investigation is based on TCAD simulations of vertical MOSFET structures representing a commercial 1.2 kV Second Gen Cree SiC power MOSFET (C2M0080120D) [38] using Sentaurus Device (S-Device) [39].

A. 4H-SiC Thermal Parameters Used in the TCAD Simulations

TCAD simulators typically include temperature-independent material parameters as a default option. S-Device provides temperature-dependent material parameters for various materials in the Advanced Calibration (Adv. Cal.) [39], a guide containing vendor-recommended material parameters and device models mainly based on literature data. The data from Adv. Cal. is limited for some materials in the way that the temperature dependence of thermal material parameters is either not available, e.g., for aluminum, or that it is fitted in a narrow temperature range. For example, the cubic expression for $c_{\mathrm{v}}(T)$ of 4H-SiC in Adv. Cal. was fitted to the 6H-SiC experimental data from [23] for $T < 800$ K, which leads to a strong overestimation of c_{v} for the temperatures above 1000 K, as shown in Fig. 1. In this paper, the $c_{\mathrm{v,4H-SiC}}$ from [17] is used, and c_{v} fitting parameters are selected to extend the applicability of c_{v} formula in a wider temperature range. The error between this improved cubic fit and the measured c_{v} data is less than 10% in the whole range from 300 to 2700 K, as shown in Fig. 1. Additionally, the $c_{\mathrm{v,4H-SiC}}$ formula from [17] was implemented in the S-Device using the physical model interface and led to ET simulation results very similar to ET simulations with the improved cubic fit.

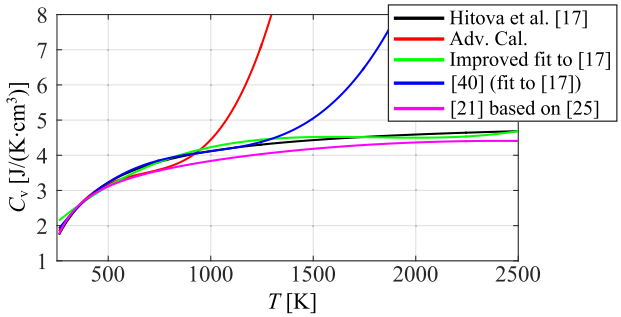

Fig. 1. Comparison of the 4H-SiC volume-specific heat capacitance, $c_{\mathrm{v}}(T)$, measured by Hitova *et al.* [17] with simulated $c_{\mathrm{v}}(T)$ using the parameters given in the Adv. Cal. of S-Device, the new proposed parameters (see Table II), and the $c_{\mathrm{v}}(T)$ from [21] and [40].

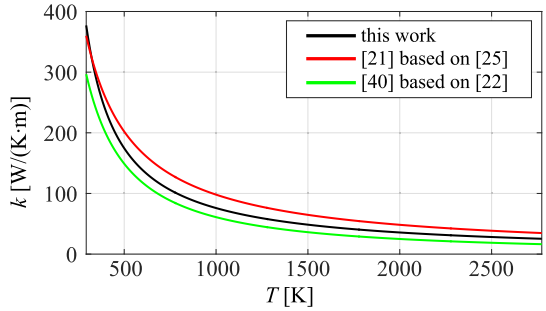

Fig. 2. Comparison of the 4H-SiC thermal conductivity used in [21] and [40] with the thermal conductivity for $k_{\mathrm{c}}(T)$ used in this paper.

To account for the difference between the thermal conductivity of 6H- and 4H-SiC [18], $k_{\mathrm{c,4H-SiC}}(T)$ was set 10% larger than the thermal conductivity expression from the Adv. Cal. file, which, in turn, corresponds to the $k_{\mathrm{c,6H-SiC}}(T)$ data from [23]. The $k_{\mathrm{r}}/k_{\mathrm{c}}$ ratio of 1.35 [18], [26], [27] is used to model the anisotropic thermal conductivity of 4H-SiC material in the whole temperature range. The comparison of the $k_{\mathrm{c,4H-SiC}}(T)$ values used in this paper to the thermal conductivity from the literature [21], [40] is shown in Fig. 2. The parameters for the temperature-dependent $c_{\mathrm{v}}(T)$ and $k(T)$ used in the proposed S-Device simulations are summarized in Tables I and II, respectively. The temperature dependence of the mass density for 4H-SiC, as well as for gate oxide and top metal, is very small and, hence, neglected in the TCAD ET simulations.

B. ET TCAD Simulations of the SiC Power MOSFET

Two structures of the SiC power MOSFET (C2M0080120D) modeling one half of a symmetric active cell with 180-μm SiC

TABLE I
PARAMETERS OF TEMPERATURE-DEPENDENT THERMAL CONDUCTIVITY $k(T)$ [W/(K·cm)] OR RESISTIVITY $r(T)$ USED IN THE TCAD ET SIMULATIONS: $k(T) = k_1 + k_2 \cdot T + k_3 \cdot T^2$, $r(T) = k_1 + k_2 \cdot T + k_3 \cdot T^2$

Material	k_1	k_2	k_3	Ref.
4H-SiC c-axis	-0.171	$1.488 \cdot 10^{-3}$	0	$r(T)$
4H-SiC a-axis	-0.127	$1.102 \cdot 10^{-3}$	0	$r(T)$
Aluminum	2.38	0	0	$k(T)$ [41]
SiO_2 (amorph.)	0.014	0	0	$k(T)$ [42]
Polysilicon	$-3.93 \cdot 10^{-2}$	$1.55 \cdot 10^{-3}$	$1.82 \cdot 10^{-6}$	$r(T)$ [24]
Polyimide	$1.2 \cdot 10^{-3}$	0	0	$k(T)$ [43]

TABLE II
PARAMETERS OF TEMPERATURE-DEPENDENT VOLUME-SPECIFIC HEAT CAPACITY $c_v(T)$ [J/(K·cm^3)] AS USED IN THE TCAD ET SIMULATIONS: $c_v(T) = c_{va} + c_{vb} \cdot T + c_{vc} \cdot T^2 + c_{vd} \cdot T^3$

Material	c_{va}	c_{vb}	c_{vc}	c_{vd}	Ref.
4H-SiC	0.676	$6.565 \cdot 10^{-3}$	$-3.697 \cdot 10^{-6}$	$6.852 \cdot 10^{-10}$	[17]
Aluminum	2.1	$0.96 \cdot 10^{-3}$	$0.35 \cdot 10^{-6}$	0	[44]
SiO_2 (amorph.)	0.435	$5.106 \cdot 10^{-3}$	$-4.086 \cdot 10^{-6}$	$1.132 \cdot 10^{-9}$	[45]
Polysilicon	1.083	$2.493 \cdot 10^{-3}$	$-1.945 \cdot 10^{-6}$	$5.638 \cdot 10^{-10}$	[44]
Polyimide	1.548	0	0	0	[43]

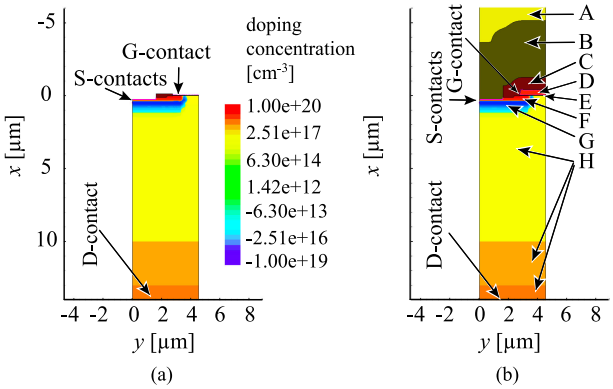

Fig. 3. TCAD modeling of MOSFET structure (an active cell). (a) $M1$ model, a simplified 2-D structure without overlayers. (b) $M2$ model, a 2-D structure with overlayers. Layers are marked from top to down: 50-μm-thick insulator plastic (A), 3.9-μm-thick aluminum (B), 0.84-μm-thick PMD oxide (C), 0.37-μm-thick n+ doped polysilicon gate (D), 50-nm-thick gate oxide (E), 180-μm 4H-SiC consisting of an n+ source contact region (F), the p-well (G), and n- (drift layer) and n epitaxial layers and the n+ substrate (H).

substrate were generated in the Sentaurus Process simulator, S-Process, following an assumed fabrication process flow taking into account the actual device active area and internal dimensions, such as, e.g., gate length, pitch size, thickness of the epitaxial (drift) layer, and metallization. The first structure, $M1$, shown in Fig. 3(a) is simplified and typically used to simulate the nominal operation of power MOSFETs, while the second structure, $M2$, shown in Fig. 3(b) includes top metal overlayers. MOSFET structures without metallization similar to $M1$ were used to estimate the temperature during SC for the same device under test (DUT), C2M0080120D, by means of TCAD simulations in, e.g., [3], [28], and [29]. Additionally, the value of half pitch size used in [3] is approximately 1.9 higher than the half pitch size of 4.55 μm used in this paper (obtained by internal analysis; not shown here), while, in [29], the dimensions of the simulated 2-D planar structure are not specified. The transient mixed-mode (device-circuit coupled) simulations of both $M1$ and $M2$ MOSFET structures are performed using the S-Device to assess the impact of top metallization on the temperature distribution inside the SiC power MOSFET and to show how the assumption of constant heat capacitance can compromise the modeling accuracy when simulating SC operation. Furthermore, the influence of the anisotropy of the thermal conductivity of 4H-SiC and its importance for the heat transfer within SiC power MOSFETs are determined.

The vertical (x-)axis was set as an anisotropy axis (c-axis) of 4H-SiC neglecting the 4° miscut. The 2-D ET device simulation assumes translational symmetry normal to the simulation plain (along the z-axis) and periodicity of active cells in the y-direction. This corresponds to zero-heat-flux boundary conditions in both y- and z-directions. During fast SC transients, lateral heat spreading is not pronounced in most of the active area, as the heat diffusion length for the SC duration is significantly smaller than the size of the active area and the thickness of the SiC substrate. The heat spreading affects the active cells located close to the border of device active area stronger (accounting for less than 10% of active area) due to the change of heat transfer conditions. These thermal effects at the border are mitigated by the negative temperature dependence of the current after reaching the SC current peak and prior to reaching the thermal runaway temperature. Accordingly, 2-D TCAD modeling can be used to predict the temperature distribution of 3-D SiC power MOSFETs during SC without compromising accuracy significantly.

The developed device model accounts for self-heating, incomplete dopant ionization, interface mobility degradation, doping- and temperature-dependent mobility, and anisotropic high-field mobility saturation. The anisotropy was fully accounted for in mobility, impact ionization coefficients, permittivity, and thermal conductivity. For the simulation, three ohmic contacts are set: the gate contact around the polysilicon region, the source contact to n+ 4H-SiC at the border with aluminum and to the p-well on the left side, and the drain contact at the bottom of the 4H-SiC substrate. The drain contact also serves as a single thermal contact with an ambient temperature of 300 K. This thermal contact is modeled by a surface thermal resistance of 32.6×10^{-3} (K·cm^2)/W, corresponding to the junction-to-case thermal resistance as specified in the datasheet, $R_{th,j-c} = 0.6$ K/W, reduced by a thermal resistance of the 180-μm 4H-SiC die at room temperature. The thermal conductivity of the plastic overlayer (marked in Fig. 3) used in the device model is very small, which results in a large thermal resistance and, hence, a negligible heat flux density on the top. Therefore, zero-flux boundary conditions are assumed on the top side.

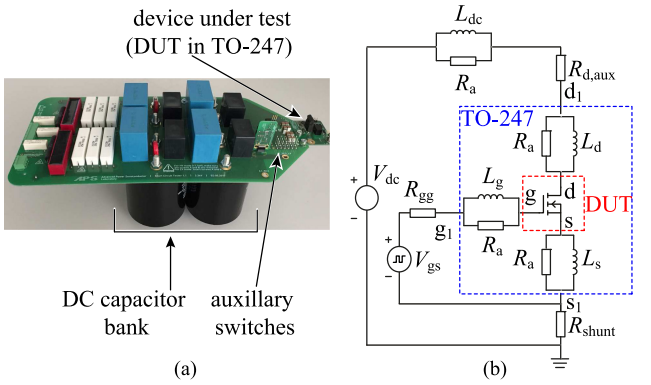

Fig. 4. SC measurement setup. (a) Photo showing the capacitor bank, the auxiliary switch comprising six parallel IGBTs, and the DUT (1.2 kV Second Gen. Cree SiC power MOSFET, C2M0080120D). (b) Circuit used in the mixed-mode TCAD 2-D ET simulations for SC.

For longer SC test times and/or higher V_{dc}, the temperature of the source metallization reaches the Al melting temperature. To estimate the device temperature with a higher precision under these operating conditions, physical effects such as melting solidification of aluminum and phase transitions in the plastic overlayer and silica should be considered in the TCAD modeling; however, these physical effects are beyond the scope of this paper and not included in the TCAD simulations. Additionally, electrical boundary conditions assumed to be constant across the active area are violated in the case of the strong gate leakage, which becomes prominent for certain dc voltages after the source metallization starts to melt. The TCAD modeling in this paper does not take into account gate leakage currents. Accordingly, the developed TCAD model cannot be used for an accurate estimation of the maximum SiC temperature during the SC event if these conditions are met; however, it can be used to estimate the time required for the source metallization to start melting t_M accurately. Prior to this time point, a SiC power MOSFET under the SC operation does not experience any degradation, and hence, t_M guarantees the safe turn-OFF time, which can be, in turn, used by system engineers as a reference for the design of an adequate SC protection circuit.

A photo of the measurement setup and the simulated electrical circuit are shown in Fig. 4(a) and (b), respectively. The DUT in Fig. 4(b) represents one of the device structures shown in Fig. 3. The gate drive external resistance, $R_g = 2.5\ \Omega$, and the internal gate resistance of 4.6 Ω are included. An inductance $L_{dc} = 180$ nH, modeling the capacitor bank of the SC experimental setup, is set to reproduce the measured drain–source voltage drop V_{ds} at the onset of the $V_{gs} = 20$ V. The resistors $R_a = 10\ \Omega$ are added to control the simulation stability. The coaxial shunt resistor used for the current measurements in the experimental setup is modeled by $R_{shunt} = 25\ m\Omega$, while the auxiliary switch comprising six parallel IGBTs (IXBK55N300) is modeled by the resistor $R_{d,aux} = 25\ m\Omega$.

As the $M2$ structure in Fig. 3(b) includes the effect of top overlayers existing in an actual device in comparison to the $M1$ structure in Fig. 3(a), $M2$ was used to calibrate the TCAD modeling in order to match the measured C–V and I–V characteristics and the SC experimental results of the actual power MOSFETs. For the

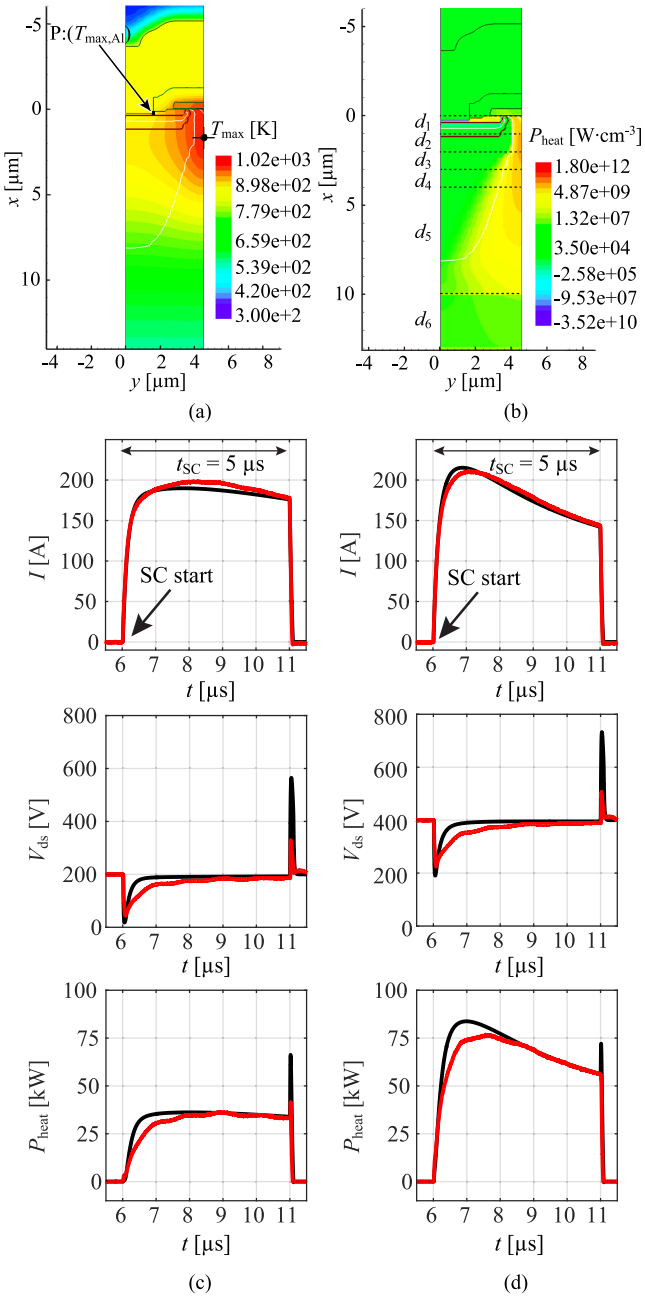

Fig. 5. SC test verification: the 2-D TCAD simulation (TCAD-SIMREF) of (a) the lattice temperature and (b) the volume heat distribution inside the power MOSFET structure at the end of the SC time ($t = 11\ \mu s$). A comparison between the simulated (black) and measured (red) current I, voltage V_{DS}, and power losses P_{heat} for the SC test at (c) $V_{dc} = 200$ V and (d) $V_{dc} = 400$ V and $t_{sc} = 5\ \mu s$.

TCAD calibration of SC experiments, temperature dependence of phonon-related components of both interface and bulk low-field electron mobility was set to T^{-3}, considering the research presented in [46]. For the calibration, the material properties, $c_v(T)$, $k(T)$, and the anisotropy of k based on the formulas from Tables I and II are implemented. A good matching between the TCAD simulations and the SC experimental results is shown in Fig. 5(c) and (d) for the dc voltages of $V_{dc} = 200$ V and 400 V, respectively, and the SC time of $t_{sc} = 5\ \mu s$. This TCAD simulation marked as TCAD-SIMREF is used as the reference

TABLE III
SUMMARY OF TCAD SIMULATIONS PRESENTED IN THIS PAPER

TCAD-	$c_{\mathrm{v}}(T)$	$k(T)$	MOSFET Structure	Purpose
SIM-REF	[17]	$k_{\mathrm{c/a}}(T)$ from Table I	$M2$	reference TCAD simulation
SIM1	[17]	$k_{\mathrm{c/a}}(T)$ from Table I	$M1$	to evaluate the effect of source metallization
SIM2	$c_{\mathrm{v}}(T) = const.$	$k_{\mathrm{c/a}}(T)$ from Table I	$M1$	to evaluate the effect of const. heat capacitance
SIM3	[17]	$k_{\mathrm{c}}(T)$ from Table I	$M2$	to evaluate the effect of anisotropy in thermal conductivity of 4H-SiC
SIM4	[21]	$k_{\mathrm{c/a}}(T)$ from Table I	$M2$	to evaluate the sensitivity to heat capacity variation
SIM5	[17]	$k_{\mathrm{c}}(T)$ from [40]	$M2$	to evaluate the sensitivity to thermal conductivity variation
SIM6	[17]	$k_{\mathrm{c}}(T)$ from [40]	$M1$	to evaluate the T-estimation using material data and MOSFET structure from [40]
SIM7	[21]	$k_{\mathrm{c}}(T)$ from [21]	$M1$	to evaluate the T-estimation using material data and MOSFET structure from [21]

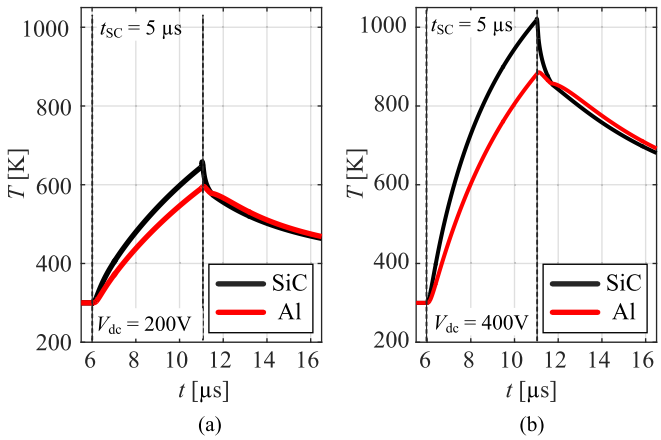

Fig. 6. TCAD simulation (TCAD-SIMREF) results for the maximum temperature inside SiC and Al during the SC time of $t_{\mathrm{SC}} = 5\,\mu$s for (a) $V_{\mathrm{dc}} = 200$ V and (b) $V_{\mathrm{dc}} = 400$ V.

simulation in the further analysis. Besides TCAD-SIMREF, seven more TCAD simulations are performed to demonstrate the effects of thermal material properties and source metallization in SiC power MOSFETs, as summarized in Table III.

The evolution of the maximum temperature in the Al metallization together with the maximum temperature in the SiC die extracted from the TCAD-SIMREF simulation is plotted in Fig. 6. The temperature of Al metallization reaches the maximum value of 888 K at $V_{\mathrm{dc}} = 400$ V with a small delay after the end of the SC time (5 μs), which is below the Al melting

TABLE IV
PREDICTION OF THE TIME-TO-START-AL-MELTING, $t_{\mathrm{M,P}}[\mu\mathrm{s}]$, AT THE LOCATION P OF THE PLANAR SiC POWER MOSFET (C2M0080120D) USING DIFFERENT TCAD SIMULATIONS

$t_{\mathrm{M,P}}$	200 V	400 V	600 V	800 V
[47]	–	5.7 μs	–	2.4 μs
TCAD-SIMREF	19.3 μs	5.84 μs	3.45 μs	2.48 μs
TCAD-SIM1	14.5 μs	3.71 μs	2.04 μs	1.42 μs
TCAD-SIM2	6.4 μs	1.69 μs	0.97 μs	0.7 μs
TCAD-SIM3	19.9 μs	6.09 μs	3.64 μs	2.64 μs
TCAD-SIM4	18.06 μs	5.52 μs	3.27 μs	2.36 μs
TCAD-SIM5	21.9 μs	6.27 μs	3.60 μs	2.54 μs
TCAD-SIM6	15.63 μs	3.81 μs	2.02 μs	1.38 μs
TCAD-SIM7	13.26 μs	3.59 μs	2.05 μs	1.46 μs

$t_{\mathrm{M,P}}$ is calculated from the start of the SC event.

temperature (933 K). The temperature of the top metallization can reach the melting temperature for longer SC test times and/or $V_{\mathrm{dc}} > 400$ V. Here, the physics of phase change transitions would have to be included in the TCAD simulation to estimate the temperature evolution with a higher accuracy (not the scope of this paper). The melting temperature in the source metallization is first reached in the point P that is marked in Fig. 5(a). Clearly, the presented TCAD modeling can be used to accurately estimate the time needed for the temperature at the point P to reach the melting temperature of aluminum, with a time reference at the start of the SC event, $t_{\mathrm{M,P}}$, for $V_{\mathrm{dc}} = 200$ V and 400 V as well as for typically operating dc voltages of 600 and 800 V, as summarized in Table IV. The estimation of $t_{\mathrm{M,P}}$ for 400 and 800 V in TCAD-SIMREF is close to the experimental results from [47] obtained using a high-speed camera.

SC failure of SiC power MOSFETs is typically ascribed in the literature to either oxide degradation or semiconductor failure at temperatures above 1000 K [48]. To prevent system failure, the SC protection has to be designed to safely turn OFF the device before any degradation starts. For example, the short-circuit withstand time (SCWT) of the investigated SiC power MOSFET for $V_{\mathrm{dc}} = 800$ V is in the range from 3.5 to 4.5 μs, showing an actual spread for the commercially available devices. The $t_{\mathrm{M,P}}$ (not to be mistaken with SCWT) estimated here for $V_{\mathrm{dc}} = 800$ V is around 2.48 μs. This time guarantees that the device can be safely turned OFF without any degradation.

The effects of SiC thermal properties are further demonstrated in detail for the SC test at $V_{\mathrm{dc}} = 400$ V and an SC time of $t_{\mathrm{sc}} = 5\,\mu$s.

1) Impact of Top Overlayers: TCAD device modeling of power MOSFETs is typically based on MOSFET structures similar to $M1$, as shown in Fig. 3(a). Such a MOSFET structure, including only SiC, gate oxide, and gate contact, can correctly reproduce device behavior at constant temperature or its quasi-stationary behavior. However, it cannot accurately reproduce device self-heating during fast transients as it is presented in this section. The overlayers serve mostly as a heat capacitor on top of the SiC die, where heat generation is small, and are, therefore, neglected in the developed 2-D ET simulation. In addition, there are six thick aluminum bond wires ($d_{\mathrm{w}} \approx 150\,\mu$m) attached to

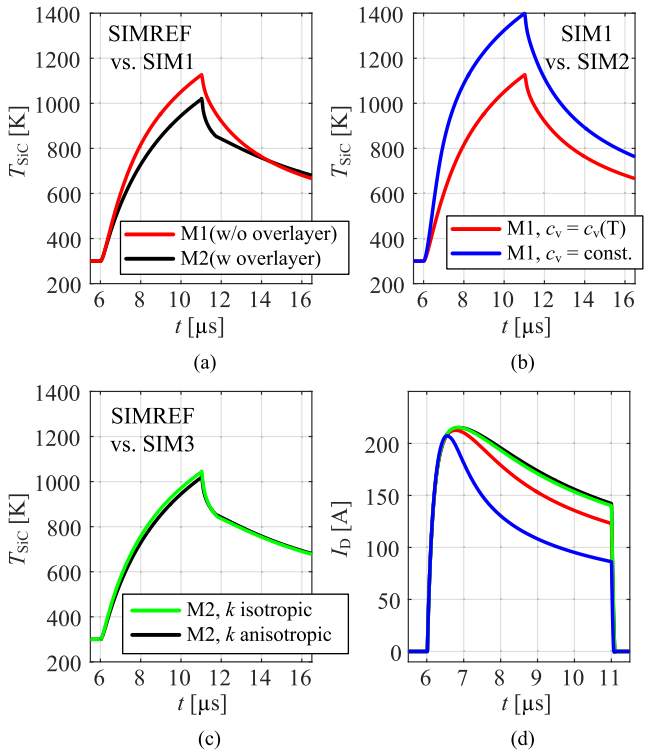

Fig. 7. Comparison between the maximum temperatures inside SiC as calculated in the presented TCAD simulations (cf., Table III). (a) TCAD-SIMREF versus TCAD-SIM1. (b) TCAD-SIM1 versus TCAD-SIM2. (c) TCAD-SIMREF versus TCAD-SIM3. (d) Corresponding current profiles: (black) TCAD-SIMREF, (red) TCAD-SIM1, (blue) TCAD-SIM2, and (green) TCAD-SIM3. $k(T)$ and $c_v(T)$ are based on the formulas given in Tables I and II, respectively.

the source contact pads in the actual MOSFET. The presence of an Al bond wire (with high thermal conductivity) changes thermal conditions in its vicinity providing additional heat capacitance, which, in turn, results in a lower temperature in the active cells below the wires. As most of the contact pad area is not in direct thermal contact with the bond wires, the bond wires were not included in the simulations. Accordingly, the developed TCAD simulations correspond to the die active area away from the bond wires, leading to a small overestimation of the average temperature in the aluminum metallization.

In the first analysis, the TCAD mixed-mode SC simulations of the $M1$ and $M2$ structures, TCAD-SIM1 and TCAD-SIMREF, respectively, taking into account $c_v(T)$, $k(T)$, and the anisotropy of k based on the formulas given in Tables I and II are compared. As shown in Fig. 7(a), $T_{\max,SiC}$ without taking into account the top overlayers overestimates the maximum temperature by $\Delta T \approx 100\,^{\circ}$C, i.e., 10%. The estimated $t_{M,P}$ in TCAD-SIM1 and TCAD-SIMREF are 3.71 and 5.84 μs, respectively. Accordingly, the top metallization of MOSFET structures has a nonnegligible influence on both the maximum temperature of SiC-MOSFET and the time when melting of the top metallization starts during the SC transients.

2) Impact of Heat Capacitance: To evaluate the accuracy of temperature prediction when using the assumption of $c_{v,4H-SiC}(T) = \text{const}$, as in, e.g., [8]–[10], the second analysis is performed by comparing two SC simulations, TCAD -SIM1 and TCAD-SIM2, using the $M1$ structure with $c_v(T)$ and $c_v = \text{const}$, respectively, at 300 K based on the formulas given in Table II. Both simulations take into account $k(T)$ and the anisotropy of k from Table I. The simulation results are shown in Fig. 7(b). The maximum temperature in SiC when using physically more accurate material properties (TCAD-SIM1) differs from the temperature prediction when using $c_{v,SiC} = \text{const}$ (TCAD-SIM2) by $\Delta T \approx 240\,^{\circ}$C, i.e., 22%. The estimated $t_{M,P}$ in TCAD-SIM1 and TCAD-SIM2 are 3.71 and 1.69 μs, respectively. These results point out that the temperature dependence of $c_{v,4H-SiC}$ should be considered when simulating the SC operation of SiC power MOSFETs.

3) Impact of Anisotropy of Thermal Conductivity: The third analysis is conducted to evaluate the effect of the anisotropy of 4H-SiC thermal conductivity, $k_{SiC}(T)$. Two SC simulations, TCAD-SIMREF and TCAD-SIM3, using the $M2$ structure with isotropic $k = k_c(T)$ and anisotropic $k(T)$ given in Table I, and taking into account $c_v(T)$ from Table II, are compared. According to the comparison in Fig. 7(c), the anisotropic thermal conductivity (TCAD-SIMREF) shows $T_{\max,SiC}$ reduced by $\Delta T \approx 20\,^{\circ}$C, i.e., 2%, in comparison to the TCAD simulation with the isotropic thermal conductivity (TCAD-SIM3). This small difference can be explained by the relatively high thermal conductivity of 4H-SiC and the small characteristic distance in lateral direction equal to the half pitch length of 4.55 μm. The estimated $t_{M,P}$ in TCAD-SIMREF and TCAD-SIM3 are 5.84 and 6.09 μs, respectively. Therefore, the anisotropy of 4H-SiC thermal conductivity can be neglected to simplify the modeling complexity.

The simulated SC current waveforms, I_D, from these four TCAD simulations (TCAD-SIMREF, TCAD-SIM1, 2, and 3) are shown in Fig. 7(d). The simulation with the simplified MOSFET structure and assuming temperature-independent heat capacitance of SiC (c_v at 300 K), TCAD-SIM2, returns the lowest device current. However, the simulated temperature under these assumptions is significantly higher than the maximum temperature calculated in the simulation with the more accurate model of material properties. In the actual SC experiment, this high temperature would trigger the melting of metallization and, eventually, device failure before the actual SC endurance time for $V_{dc} = 400$ V. Accordingly, a proper set of thermal material data is needed for an accurate temperature prediction of SiC power MOSFETs, which is, in turn, needed to avoid overcalibration of temperature-dependent device models.

C. Sensitivity Analysis

To demonstrate the sensitivity of temperature estimation to the variations of thermal material parameters, two additional TCAD simulations using the MOSFET structure $M2$, TCAD-SIM4 and TCAD-SIM5, are performed (Table III). Comparing the TCAD-SIM4 and TCAD-SIMREF, the sensitivity of temperature estimation to the input data for 4H-SiC heat capacitance is determined. The $c_{v,4H-SiC}(T)$ from [21] used in TCAD-SIM4 is shown in Fig. 1 together with the reference $c_{v,4H-SiC}(T)$ from [17] used in TCAD-SIMREF. The estimation of the maximum SiC temperature T_{SiC} for $V_{dc} = 400$ V at the SC time of $t_{sc} = 5$ μs returned by TCAD-SIMREF and TCAD-SIM4 is 1017 and 1039 K, respectively. The estimated $t_{M,P(SIMREF)}$ and

$t_{\mathrm{M,P(SIM4)}}$ for $V_{\mathrm{dc}} = 400$ V are 5.84 and 5.52 μs. This shows that 6% lower thermal capacitance at higher temperatures above 1000 K leads to 2% higher temperature estimation and 5.5% shorter $t_{\mathrm{M,P}}$ estimation.

Similarly, using TCAD-SIMREF and TCAD-SIM5, the sensitivity of temperature estimation to a variation in thermal conductivity is calculated. The $k_{4\mathrm{H-SiC}}(T)$ curve from [21] was used in TCAD-SIM5, while the reference $k_{4\mathrm{H-SiC}}(T)$ curve from Table I was used in TCAD-SIMREF (Fig. 2), keeping all other material properties the same. The estimation of the SiC temperature T_{SiC} for $V_{\mathrm{dc}} = 400$ V at the SC time of $t_{\mathrm{sc}} = 5$ μs returned by TCAD-SIMREF and TCAD-SIM5 is 1017 and 994.3 K, respectively. The estimated $t_{\mathrm{M,P(SIMREF)}}$ and $t_{\mathrm{M,P(SIM5)}}$ for $V_{\mathrm{dc}} = 400$ V are 5.84 and 6.27 μs. This demonstrates that 35% higher thermal conductivity at the temperatures above 1000 K leads to 2.2% lower temperature estimation and 7.4% higher $t_{\mathrm{M,P}}$ estimation.

D. Comparison to the Temperature Estimation From the Literature

Two TCAD simulations are performed using the MOSFET structure without the source metallization, $M1$, and SiC material parameters as employed in [40] (TCAD-SIM6) and [21] (TCAD-SIM7). Particularly, in [21], a 1-D ET model of SiC power MOSFETs, including the die, the die attachment, and the case, was numerically solved taking into account the temperature dependence of the thermal conductivity and the specific heat of SiC based on 3C-SiC from [25]. In [40], the temperature is estimated based on a 1-D R-C thermal model, without considering the top metallization and using the thermal conductivity properties of 6H-SiC from [22] and the heat capacity properties of 4H-SiC from [17]. The estimated $t_{\mathrm{M,P(SIM6)}}$ and $t_{\mathrm{M,P(SIM7)}}$ for $V_{\mathrm{dc}} = 800$ V are 1.46 and 1.38 μs, while the estimated $t_{\mathrm{M,P(SIMREF)}}$ using the reference TCAD simulation is 2.48 μs. The estimation of the SiC temperature T_{SiC} for $V_{\mathrm{dc}} = 400$ V at the SC time of $t_{\mathrm{sc}} = 5$ μs, returned by TCAD-SIM6 and TCAD-SIM7 is 1114 and 1202 K, respectively, in comparison to the reference estimation from TCAD-SIMREF of 1017 K. Accordingly, using the thermal material data and the MOSFET structure without source metallization, as it has been done so far in the TCAD simulations as presented in the literature, leads to an overestimation of the temperature from 10% up to 19% and an underestimation of $t_{\mathrm{M,P}}$ estimation by $\approx$40%.

In [48], the temperature of SiC power MOSFETs during SC transients was estimated by a 1-D thermal model implemented in COMSOL taking into account the phase-transition energy of the aluminum top metal and the temperature dependence of 4H-SiC from [25]. The authors in [48] noted that the proposed thermal model was not calibrated, and hence, the accuracy of their temperature estimation was not specified. To the best of our knowledge, in the state-of-the-art literature, 2-D TCAD ET simulations of SiC power MOSFET are performed neglecting the effects of source metallization.

IV. 1-D Thermal Network for the SiC Power MOSFET

The temperature-dependent material properties can be included in 1-D thermal modeling by Foster- and/or Cauer-type RC thermal networks. The nonphysical Foster thermal networks consist of RC cells depending on the level of power losses. The R and C elements are calculated from the device transient thermal impedance in a wide range of the dissipated power extracted either from thermal transient measurements or extensive numerical simulations, as shown in, e.g., [12], [49], and [50]. This approach can be feasible for nominal device operation and highly challenging for high-temperature variations. The physics-based Cauer-type networks with temperature-dependent R and C elements are more suitable for thermal modeling of power devices experiencing fast temperature transients and high-temperature amplitudes. This section presents a 1-D Cauer network with temperature-dependent R and C elements developed by using the TCAD SC simulation results and implemented in the LTSpice circuit simulator.

The developed 1-D thermal network allows engineers to estimate the maximum temperature in SiC planar power MOSFETs when a specific power loss profile is applied to the device. The 1-D Cauer-type networks model the heat transfer by representing the device and/or module geometry as a set of layers described by the corresponding material characteristics. The thickness of layers have to be selected properly in order to capture the temperature development under both short- and long-term temperature transients accurately. The 1-D Cauer-type thermal networks used to calculate the device temperature under SC operating conditions without considering the variation of material properties with temperature were shown in [8], [9], [11], [13], and [37]. On the other hand, temperature-dependent R-C Cauer thermal networks were proposed in, e.g., [40], [51], and [52]. The authors in [51] showed that the effect of heat volume generation and top metallization should be considered and included in 1-D models to estimate the temperature distribution during the fast transients occurring under UIS tests physically more accurately; however, they used temperature-dependent thermal resistors and constant thermal capacitors analyzing silicon CoolMOS devices. The analysis presented in [52] was focused only on the nominal operation of SiC power devices, and not on fast temperature transients. The thermal model of a SiC power MOSFET developed in [40] for estimating the device temperature during the SC operation was not shown; it does not model the top metallization, and the source of power losses was placed at the first node of the thermal network, assuming surface heat generation.

A. Implementation of the 1-D Cauer-Type Thermal Network

The thermal network with $n = 9$ RC stages is developed [cf., Fig. 8(c)], where $k(T)$ and $c_{\mathrm{v}}(T)$ are modeled by the voltage-dependent resistors $R_i(T)$ and capacitors $C_i(T)$ $i = 1, \ldots n$, respectively, by setting the voltage dependencies according to $k_{\mathrm{c}}(T)$ and $c_{\mathrm{v}}(T)$ of 4H-SiC (see Tables I and II). Particularly, the die thickness (180 μm) is divided into n layers. The R_i and C_i are calculated using the thickness of the layers, k, c_{v}, and the chip active area A_{chip}, as described in [9]; however, in comparison to [9], the temperature dependence of k and c_{v} is taken into account. The Al metallization of the die is modeled with a single RC cell, considering the $k(T)$ and $c_{\mathrm{v}}(T)$ of aluminum, as given in Tables I and II, respectively. The thickness of the layers determining the RC cells are selected, as shown in Fig. 8, and

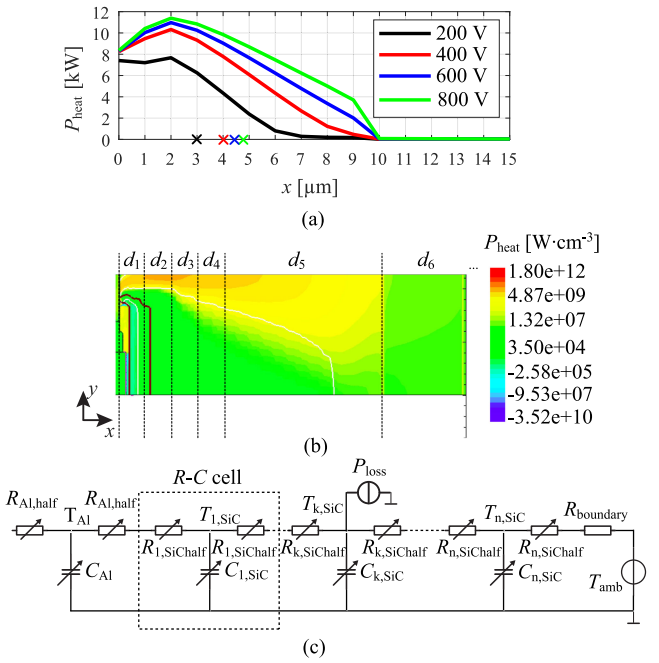

Fig. 8. 2-D TCAD simulation of the volume heat distribution, P_{heat}, inside SiC of a planar power MOSFET at the end of the SC time ($t = 11\ \mu$s). (a) Average P_{heat} in the layers along the x-direction for $V_{\mathrm{dc}} = \{200\ \mathrm{V}, 400\ \mathrm{V}, 600\ \mathrm{V}, 800\ \mathrm{V}\}$. (b) 2-D P_{heat} distribution for $V_{\mathrm{dc}} = 400\ \mathrm{V}$. The colored points mark the corresponding average distances for the power loss distribution along the x-direction. The SiC die is divided in $n = 9$ layers with thickness: $d_{1-4} = 1\ \mu$m, $d_5 = 6\ \mu$m, $d_6 = 24\ \mu$m, $d_7 = 32\ \mu$m, $d_8 = 64\ \mu$m, and $d_9 = 50\ \mu$m. (c) Developed RC thermal network.

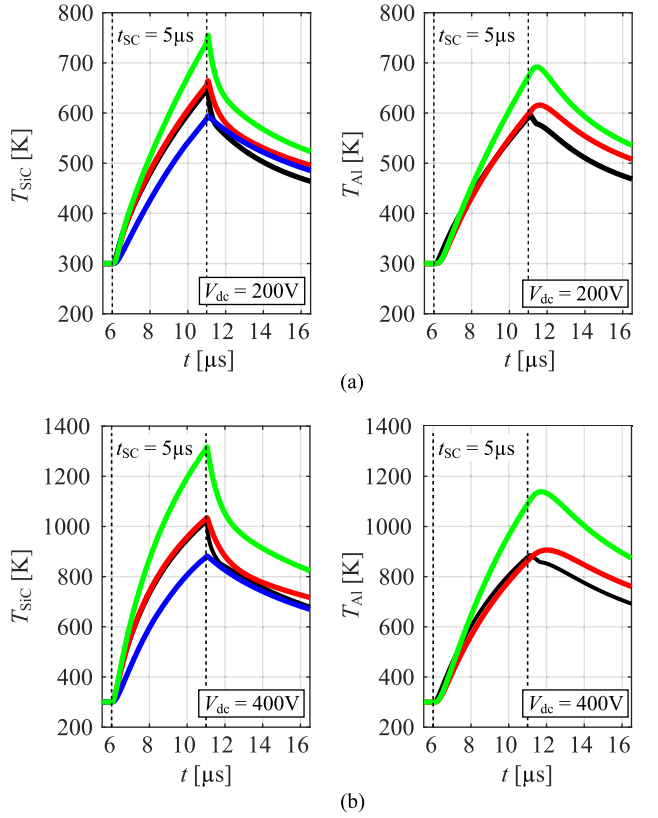

Fig. 9. Comparison of LTSpice simulations with the TCAD simulation (TCAD-SIMREF) results for the maximum temperature inside of SiC and Al during the SC time of $t_{\mathrm{SC}} = 5\ \mu$s for (a) $V_{\mathrm{dc}} = 200\ \mathrm{V}$ and (b) $V_{\mathrm{dc}} = 400\ \mathrm{V}$. TCAD-SIMREF (black), the proposed 1-D thermal network with temperature-dependent RC cells (red), the 1-D thermal network with temperature-independent RC cells provided by the manufacturer [38] (blue), and the proposed 1-D thermal network with temperature-dependent R elements and temperature-independent C elements (green).

are based on the TCAD simulation of heat distribution inside the SiC power MOSFET at the end of the SC event. For fast thermal transients, such as SC and UIS events, the first five layers modeling the 10 μm of the SiC die under the SiC-oxide interface (d_{1-5}) are responsible for the temperature development during the heating phase, while the last three layers (d_{6-9}) mainly determine the cooling behavior, together with the boundary condition RC cells. The generated heat is modeled by a current source, P_{loss}, where the input waveform can be defined externally.

To simulate the SC temperature transients, P_{loss} is placed at the fifth node ($k = 5$) of the developed 1-D thermal network, which can be correlated with the calculated average distance for the power loss distribution along the vertical direction of heat transport in the device, as marked in Fig. 8(a) for $V_{\mathrm{dc}} = 400\ \mathrm{V}$. At the beginning of the SC event, the maximum heat generation is located in the channel as the channel resistance dominates over the drift layer resistance at lower temperatures. As the temperature increases, the drift layer resistance becomes higher, and the maximum heat generation is shifted from the channel to the volume toward the drain, as shown in Fig. 5(b). Accordingly, at higher V_{dc} (e.g., $V_{\mathrm{dc}} \geq 400\ \mathrm{V}$ for the investigated SiC power MOSFET), the maximum temperature T_{max} in the SiC MOSFET occurs at the end of the SC time within the volume of the device [cf., Fig. 5(a)], in comparison to the nominal operation where the heat is mostly generated near the surface inside the channel. On the other hand, for lower V_{dc} ($< 400\ \mathrm{V}$), the maximum heat generation stays in the channel, and the heat distribution at the end of SC time is slightly changed in comparison to the heat distribution for $V_{\mathrm{dc}} \geq 400\ \mathrm{V}$, which is illustrated in Fig. 8(a) for $V_{\mathrm{dc}} = 200\ \mathrm{V}$.

The comparison of the maximum temperatures calculated by the developed 1-D thermal model ($T_{\mathrm{max,1Dtd}}$), the developed 1-D thermal model with constant thermal capacitances, the temperature-independent 1-D thermal model from [38] ($T_{\mathrm{max,1Dtid}}$), and the TCAD ET simulations TCAD-SIMREF ($T_{\mathrm{max,TCAD}}$) is shown in Fig. 9 for $V_{\mathrm{dc}} = 200\ \mathrm{V}$ and 400 V. The inputs, P_{loss} of the 1-D thermal networks, are the power loss waveforms as calculated in the TCAD ET simulations with the same V_{dc} and $t_{\mathrm{SC}} = 5\ \mu$s. The boundary condition is set similar to the one in the TCAD ET simulations.

The matching with less than 10% relative error between $T_{\mathrm{max,1Dtd}}$ and $T_{\mathrm{max,TCAD}}$ in both aluminum and SiC shows that the proposed 1-D thermal network can be used to estimate the critical device temperatures. By using the temperature-independent 1-D thermal model provided in datasheets [38] as in [8], the temperature is underestimated by $\Delta T = 146\ ^{\circ}\mathrm{C}$, i.e., 14%, in comparison to the TCAD ET device simulation. Similarly, as observed in Fig. 7(b), assuming a constant heat volume capacitance for SiC leads to an overestimation of the temperature by $\Delta T \approx 270\ ^{\circ}\mathrm{C}$, i.e., 25%, compared to the fully

TABLE V
PREDICTION OF THE TIME-TO-START-AL-MELTING, $t_{\mathrm{M,P}}[\mu\mathrm{s}]$, AT THE LOCATION P OF THE PLANAR SIC POWER MOSFET (C2M0080120D) USING THE TCAD SIMULATION TCAD-SIMREF AND THE PROPOSED 1-D TEMPERATURE-DEPENDENT RC NETWORK (WITH TEMPERATURE-DEPENDENT RC CELLS AND TEMPERATURE-DEPENDENT R ELEMENTS AND TEMPERATURE-INDEPENDENT C ELEMENTS, RESPECTIVELY)

$t_{\mathrm{M,P}}$	200 V	400 V	600 V	800 V
TCAD-SIMREF	19.37 μs	5.84 μs	3.45 μs	2.48 μs
1-D proposed R-C network	16.72 μs	6.01 μs	3.19 μs	2.87 μs
1-D proposed R-C network (C const.)	9.98 μs	3.77 μs	2.46 μs	1.95 μs

temperature-dependent 1-D thermal model. For higher V_{dc} or longer SC time, the proposed 1-D thermal network can be used to estimate the time point when the melting of top metallization starts. The comparison of $t_{\mathrm{M,P}}$ estimations using the TCAD-SIMREF simulation and the proposed 1-D temperature-dependent RC thermal network is summarized in Table V for $V_{\mathrm{dc}} = \{200\,\mathrm{V}, 400\,\mathrm{V}, 600\,\mathrm{V}, 800\,\mathrm{V}\}$. The best matching is achieved for $V_{\mathrm{dc}} = 400\,\mathrm{V}$, since the power loss distribution along the x-axis for $V_{\mathrm{dc}} = 400\,\mathrm{V}$ is used to calibrate the RC cells. These results show that the proposed 1-D thermal network can be used to provide an estimate of the time-to-start-melting of the source metallization in planar SiC power MOSFETs.

In comparison to the temperature-independent RC thermal networks, the modeling accuracy is increased by introducing voltage-dependent resistors and capacitors at the cost of potential convergence problems in the circuit simulators as, e.g., the Spice-based simulators and the simulators dedicated for PEs as PLECS [37]. However, the proposed RC model consists of a significantly lower number of RC cells in comparison to the vectorized RC network shown in [37]. The RC network proposed here was coupled to the Spice-based model of C2M0080120D provided by the manufacturer, and no convergence problems were observed in a LTSpice simulation. The modeling principle can be extended to other SiC MOSFET structures as, e.g., trench design.

V. CONCLUSION

This paper serves to improve the modeling accuracy and engineering confidence in the ET modeling of SiC-power MOSFETs operating at high temperatures. Using the example of SC operation, the modeling accuracy when neglecting the temperature dependence of the SiC heat capacity and the top metallization is determined. The dominating effects that have to be considered for simulating the operation of SiC power MOSFETs as accurately as possible are identified. A temperature-dependent 1-D RC thermal network of a 1.2 kV SiC planar power MOSFET is proposed, allowing the temperature estimation of the thermally critical device regions during SC events, the drift layer, the oxide-SiC interface, and the top metallization, while still maintaining its usefulness for design and optimization of reliable SiC-based power electronic systems.

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