

A Lithium-Ion Battery Balancing Circuit Based on Synchronous Rectification

Yunlong Shang , *Member, IEEE*, Shuofeng Zhao , Yuhong Fu , Bing Han, Panpan Hu, and Chunting Chris Mi , *Fellow, IEEE*

Abstract—In this paper, a battery balancing circuit is proposed for the series-connected lithium-ion battery cells based on the principle of synchronous rectification. The proposed balancing circuit, also referred to as an equalizer, mainly includes a buck–boost converter (BBC), a multiport half-bridge converter (MHBC), and a driving circuit. The MHBC is coupled with a multiwinding transformer. Compared with the conventional congeneric methods, the number of transformer windings is almost reduced by half, leading to a more compact size and lower cost. Moreover, the secondary MOSFETs of the MHBC are synchronously driven by the primary half-bridge converter (HBC) without the need of additional isolated MOSFET gate drivers and power supplies, dramatically reducing the circuit cost and complexity. In addition, the proposed equalizer can realize the module-to-multi-cell (M2MC) equalization under severe imbalance conditions to improve the balancing speed, and work at the any-cell-to-any-cell (AC2AC) self-balancing mode under slight imbalance conditions to improve the balancing efficiency and effectiveness, which achieves a good trade-off between balancing speed and effectiveness. The expressions of the equalization current and efficiency are derived and verified by experimental results. The proposed equalizer is experimentally evaluated for a string with 12 series-connected lithium-ion cells.

Index Terms—Electric vehicles, equalizers, half-bridge converters, lithium-ion batteries, multiwinding transformers, synchronous rectification.

I. INTRODUCTION

LITHIUM-ION batteries are widely used in electric vehicles, laptop computers, and medical equipment, which are connected in series to meet the voltage and power requirements.

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Y. Shang is with the School of Control Science and Engineering, Shandong University, Shandong 250061, China, and also with the Department of Electrical and Computer Engineering, San Diego State University, San Diego, CA 92182 USA (e-mail: yshang@sdu.edu.cn).

S. Zhao and Y. Fu are with the Department of Electrical and Computer Engineering, San Diego State University, San Diego, CA 92182 USA (e-mail: SFZhao.frankivc@gmail.com; fuyuhong@gmail.com).

B. Han and P. Hu are with the BMS R&D Department, Hefei Guoxuan High-Tech Power Energy Co., Ltd., Anhui 230012, China (e-mail: hanbing@gotion.com.cn; hupanpan@gotion.com.cn).

C. C. Mi is with the Department of Electrical and Computer Engineering, San Diego State University, San Diego, CA 92182 USA (e-mail: cmi@sdsu.edu).

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However, no two battery cells are entirely identical [1]. In other words, battery cells always have slight differences in capacity, impedance, self-discharge rate, etc. [1]–[2]. These differences lead to a divergence of the cells' voltages over time and significantly reduce the available battery capacity and accelerate battery degradation. Therefore, many battery balancing methods have been proposed to extend battery run time as well as battery life [2], which are generally divided into passive and active balancing types.

The passive solution employs one bleeding resistor for each cell to dissipate the excessive energy when the cell has a higher voltage [3], [4]. Due to the compact size, this structure can be easily integrated into the integrated circuit (IC), which is favorable in low-cost applications [3]. However, the passive method cannot be used during battery discharging since the energy loss by the balancing resistors will dramatically shorten the battery run time and, at the same time, create additional heat that has to be dissipated from the battery pack.

Active balancing method utilizes capacitors [5]–[9], inductors [10]–[12], LC resonance circuits [13]–[15], transformers [16]–[24], or their combination [25], [26] to transfer energy to where it is needed. Therefore, this solution is significantly more efficient, but needs more components with a higher cost and larger size. Apparently, the active balancing method is preferable in efficiency-conscious system applications.

Ye *et al.* [7] proposed a switched-capacitor (SC)-based cell balancing circuit, which can automatically and simultaneously balance all cells with a fast speed and high efficiency. However, two MOSFETs and corresponding isolated gate drivers are required for each cell, contributing to a large size and high cost. Mestrallet *et al.* [10] introduced an any-cell-to-any-cell (AC2AC) equalizer using buck–boost converters (BBCs), which achieves a fast equalization speed. However, its size and cost are also high because $m - 1$ inductors, $2m - 2$ MOSFETs, and corresponding gate drivers are needed for m series-connected cells. Moreover, the $m - 1$ BBCs need $m - 1$ independent pulsewidth modulations (PWMs) with different duty cycles to realize the multiphase equalization, resulting in a complex control and low reliability. Lee *et al.* [15] proposed an LC -based balancing topology [16], which can directly deliver energy from one cell to another cell regardless of the cell position, resulting in a high efficiency. However, the equalization speed is still lower for a larger battery string because only two cells are balanced at the same time. Moreover, this method has the key disadvantages of large circuit size and complex control because it needs four

MOSFETs for each cell and voltage sensors to find the highest and lowest voltage cells.

Chen *et al.* [18] introduced a direct cell-to-cell (DC2C) balancing topology based on forward or flyback operation. However, it employs $2m$ MOSFETs and m windings for m series-connected battery cells with a large volume and high price. Further, Park *et al.* [19] improved the DC2C equalizer with the need of $m/2$ windings based on buck–boost and flyback conversions, reducing the size and cost of the equalizer. However, it still requires two MOSFETs and two corresponding isolated gate drivers for each cell. Imtiaz and Khan [20] introduced a cell-to-module (C2M) balancing topology based on time-shared flyback conversion. Nonetheless, this equalizer uses many MOSFETs and diodes and requires cell voltage monitoring to identify the highest voltage cell and, therefore, has the disadvantages of bulky size, sophisticated control, and low reliability.

In order to reduce the quantities of MOSFETs and isolated drivers, Uno and Kukita [9] proposed the simultaneous module-to-multi-cell (M2MC) equalizer based on voltage multiplier only using two MOSFET switches. However, this approach uses two diodes for each cell to achieve the automatic equalization, which causes a low equalization efficiency because of the voltage drop across the diodes. Analogously, Gottwald *et al.* [22] proposed a charging equalizer based on a ramp converter with fewer MOSFETs. Soft switching is realized to reduce switching losses, increase the switching frequency, and minimize the size of the heatsinks and reactive components. Particularly, the number of the secondary windings of the transformer is reduced by 50%, which provides an important circuit simplification. However, this topology is based on the passive rectification using diodes, which is appropriate for the series-connected battery strings with high cell voltages, e.g., 11.5–15.5 V. When this equalizer is applied to a low-cell-voltage battery string, e.g., 2–4.2 V, the balancing efficiency will become very low because of the higher voltage drop across the diodes, i.e., 0.4–0.8 V. In addition, the ramp equalizer [22] can only realize charging equalization, it cannot achieve battery self-equalization due to the unidirectional converter used. In addition, Shang *et al.* [23] proposed an automatic AC2AC balancing topology based on forward-flyback conversion with a high efficiency. The design highlight is that only one MOSFET and one isolated gate driver are required for each cell, reducing circuit cost and size.

In summary, most of the existing active equalizers have the essential problems of high circuit cost, large size, complex control, and low reliability due to the requirement of a large number of MOSFETs and isolated gate drivers. Besides, the automatic equalizer [23] has a slow balancing speed due to the limited balancing current that entirely relies on the cell voltage difference.

Driven by the purpose of reducing the numbers of MOSFETs and gate drivers, and improving the balancing speed and efficiency, this paper proposes an automatic equalizer with a reduced number of driving circuits based on synchronous rectification. Specifically, three original contributions are made in this paper. First, a multiport half-bridge converter (MHBC) based on synchronous rectification is proposed to significantly reduce the number of automotive-grade isolated gate drivers for the MOSFETs and simplify the control. Second, the proposed equalizer can realize M2MC equalization for a larger cell voltage

difference to improve the balancing speed, and achieve AC2AC self-equalization for a smaller cell voltage difference to improve the balancing efficiency and effectiveness. Therefore, the proposed equalizer achieves a good trade-off between balancing speed and effectiveness. Finally, the mathematical models of the balancing current, magnetic current, and efficiency are derived and verified by experimental results.

II. PROPOSED EQUALIZER

A. Circuit Configuration and Operation Principles

Fig. 1(a) illustrates the proposed automatic equalizer based on synchronous rectification for 12 series-connected cells, which consists of a BBC, a MHBC, and one driving circuit.

The MHBC is coupled with a multiwinding transformer (i.e., T_1) with one primary winding and six secondary windings. The primary HBC is connected to the BBC, and the secondary HBCs are connected to the cells, which forms the M2MC balancing topology. Moreover, the total balancing current can be adjusted by controlling the BBC according to the cell voltage difference, which provides the potential to improve the balancing speed. It is important to note that the secondary windings should have the same turns number to achieve balancing among the odd/even cells. The turns ratio of the primary winding to the secondary winding, i.e., n_1 , is determined by the output voltage of the BBC and the cell voltage.

It is important to note that the proposed MHBC should be synchronously driven by a pair of complementary PWM signals, but this requires one isolated gate driver and one isolated power supply for each MOSFET, leading to a very high cost. Fortunately, under the control of a pair of complementary PWM signals, the primary HBC can also generate an ac square-wave voltage, which can be easily used to synchronously drive the secondary HBCs. Therefore, one driving transformer (i.e., T_2) with one primary winding and twelve secondary windings is used to connect the primary HBC with the gates and sources of the secondary MOSFETs, as shown in the blue line in Fig. 1(a). It is worth mentioning that in order to alternately drive the odd and even MOSFETs, the odd and even windings should have opposite polarities. The detailed driving circuit is presented in Fig. 1(b) [27].

The proposed equalizer needs two pairs of complementary PWM signals to drive the MHBC and BBC, respectively. As shown in Fig. 2, the proposed MHBC has two working states within one switching period. For ease of illustrations, the cell voltages are assumed to be $V_{B1} > V_{B2} > \dots > V_{B11} > V_{B12}$. However, the cell voltages can be in any order in real applications, which does not affect the operations of the proposed circuit. Fig. 3 presents the corresponding operating principles of the proposed driving circuit in the two working states. Fig. 4 presents the key waveforms of the proposed equalizer, including the ac voltage of the primary HBC V_{TP} , the driving voltage of MOSFETs V_{GS} , the primary current i_P , the secondary current i_S , and the magnetic current i_{Lm} .

State I: As shown in Fig. 2(a), MOSFET Q_{h1} is turned ON. The dotted terminals of the balancing and driving transformers are positive (See V_{TP} in Fig. 4). As shown in Fig. 3(a), the transistors of the odd cells are turned OFF and the ones for even cells are turned ON, charging the gate-source capacitors of the

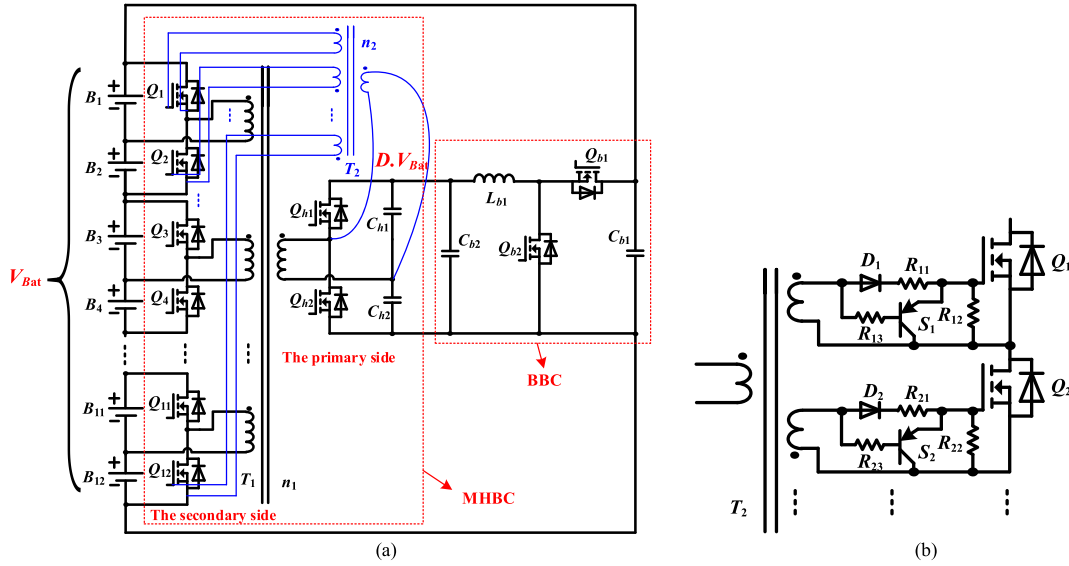


Fig. 1. Proposed automatic equalizer based on synchronous rectification for 12 series-connected cells. (a) Balancing topology. (b) Driving circuits for even and odd MOSFETs.

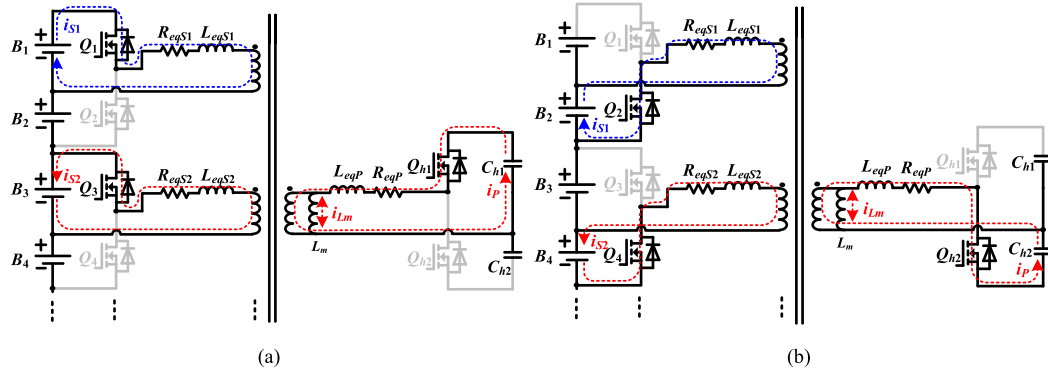


Fig. 2. Operational principles of the proposed MHBC under the assumption of $V_{B1} > V_{B2} > \dots > V_{B11} > V_{B12}$. (a) State I. (b) State II.

odd MOSFETs and discharging the gate-source capacitors of the even MOSFETs (see $V_{GS(Q1)}$ and $V_{GS(Q2)}$ in Fig. 4). As a result, the odd MOSFETs are turned ON and the even MOSFETs are turned OFF. Energy is transferred from C_{h1} to the odd cells based on forward conversion (see the primary current i_P in Fig. 4). If the cell voltage is higher than the voltage of the secondary windings, the balancing current will flow from the cell to the secondary winding, e.g., i_{S1} (see i_{S1} in Fig. 4). The higher the cell voltage, the larger the balancing current. If the cell voltage is lower than the voltage of the secondary windings, the balancing current will flow from the secondary winding to the cell, e.g., i_{S2} (see i_{S2} in Fig. 4). The lower the cell voltage, the larger the balancing current. It is worth mentioning that the magnetic current i_{Lm} is a triangle waveform due to the large magnetic inductance, as shown in Fig. 4.

State II: As shown in Fig. 2(b), MOSFET Q_{h2} is turned ON. The dotted terminals of the balancing and driving transformers are negative. As shown in Fig. 3(b), the gate-source capacitors of the even MOSFETs are charged and those of the odd MOSFETs are discharged, turning ON the even MOSFETs and turning OFF the odd MOSFETs. Energy is transferred from C_{h2} to the even cells based on forward conversion.

It can be seen that the secondary MOSFETs can be directly driven by the primary HBC, which achieves the synchronous rectification. In addition, the equalization between the odd and even cells can be achieved based on the buck–boost and flyback conversions through the two complementary states. Therefore, the proposed equalizer realizes the M2MC balancing for the battery string. It should be noted that if the voltages of the capacitors C_{h1} and C_{h2} are not equal, the voltage equalization between the odd and even cells will not be achieved. In fact, according to the working principle of the half-bridge converter, the voltages of C_{h1} and C_{h2} are mainly dependent on the duty cycle of the half-bridge converter. Therefore, the duty cycle of the half-bridge converter should be optimally set as $D = 50\%$ to achieve $V_{Ch1} = V_{Ch2}$.

In summary, the proposed equalizer based on synchronous rectification has the unique characteristics as follows:

- 1) One cell only needs one MOSFET and two cells share one transformer winding. Compared with the conventional congeneric methods, the proposed topology only requires almost half of the transformer windings, significantly reducing the circuit volume and cost.

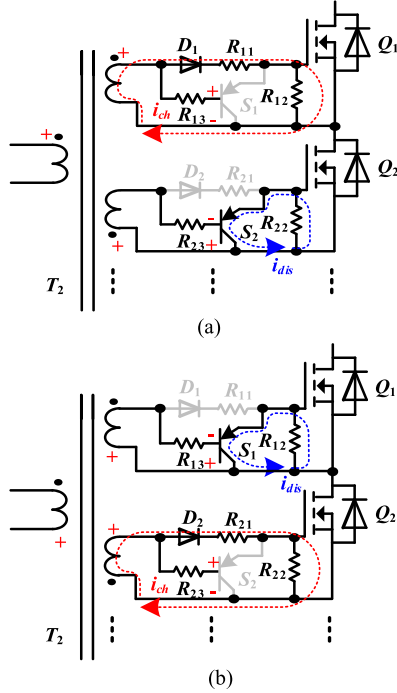


Fig. 3. Operating principles of the proposed gate driving circuits. (a) State I. (b) State II.

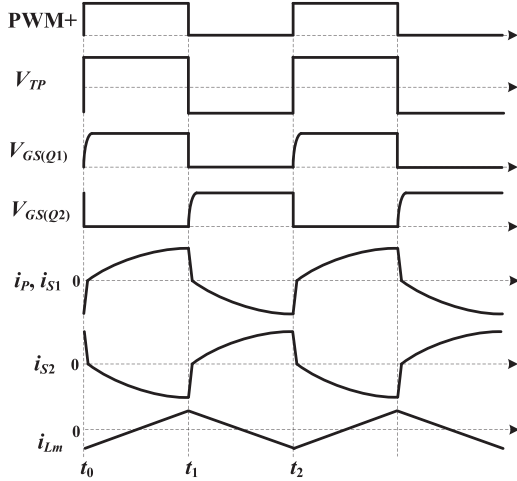


Fig. 4. Key waveforms of the proposed equalizer.

- 2) The secondary MOSFETs of the MHBC are synchronously driven by the primary HBC without the need of additional isolated gate drivers and power supplies, contributing to a low cost and ease of control.
- 3) The balancing current can be adjusted by controlling the BBC according to the cell voltage difference, which achieves a good trade-off between balancing speed and effectiveness. Particularly, when the cell voltage difference is small, the proposed equalizer can also operate at the AC2AC self-equalization mode without energy transferred from the battery module to the cells, achieving a high efficiency and good effectiveness.

B. Modeling and Analysis of the Primary and Secondary Balancing Currents

According to the forward conversion and Kirchhoff's voltage law (KVL), the voltage across the magnetic inductor is equal to the average value of the input voltages of the MHBC [24], i.e.

$$\begin{cases} V_{Lm} = \frac{n_1 \cdot \sum_{j=1}^{12} V_{Bj} + 2 \cdot \frac{D \cdot V_{Bat}}{2}}{14} = \frac{(n_1 + D) \cdot V_{Bat}}{14}, & 0 < t < \frac{T}{2} \\ V_{Lm} = -\frac{(n_1 + D) \cdot V_{Bat}}{14}, & \frac{T}{2} < t < T \end{cases} \quad (1)$$

where V_{Bj} is the voltage of cell B_j , n_1 is the turns ratio of the primary winding to the secondary winding of the balancing transformer. $D \cdot V_{Bat}$ is the output voltage the BBC. V_{Bat} is the total voltage of the battery module, i.e., $V_{Bat} = \sum_{j=1}^{12} V_{Bj}$. D is the duty cycle of the BBC. It can be seen that the average magnetic voltage is zero in a switching period, which ensures the energy balance of the transformer.

Based on Kirchhoff's current law (KCL), the magnetic current during one switching period can be expressed as

$$\begin{cases} \frac{di_{Lm}}{dt} = -\frac{R_{Lm}}{L_{Lm}} \cdot i_{Lm} + \frac{V_{Lm}}{L_{Lm}}, & 0 < t < \frac{T}{2} \\ \frac{di_{Lm}}{dt} = \frac{R_{Lm}}{L_{Lm}} \cdot i_{Lm} - \frac{V_{Lm}}{L_{Lm}}, & \frac{T}{2} < t < T \end{cases} \quad (2)$$

where L_{Lm} is the magnetic inductance, T is the switching period, and R_{Lm} is the equivalent resistance of the primary winding.

The positive and negative peak values of the magnetic current are equal, i.e.

$$i_{Lm}(0) = -i_{Lm}\left(\frac{T}{2}\right). \quad (3)$$

According to (2) and (3), the magnetic current during one switching period can be derived as

$$\begin{cases} i_{Lm}(t) = \frac{V_{Lm}}{R_{Lm}} \cdot \left(1 - \frac{2}{1 + e^{-\frac{R_{Lm}}{2L_{Lm}f}}} e^{-\frac{R_{Lm}}{L_{Lm}}t}\right), & 0 < t < \frac{T}{2} \\ i_{Lm}(t) = \frac{V_{Lm}}{R_{Lm}} \cdot \left(\frac{2}{1 + e^{-\frac{R_{Lm}}{2L_{Lm}f}}} e^{-\frac{R_{Lm}}{L_{Lm}}(t-\frac{T}{2})} - 1\right), & \frac{T}{2} < t < T \end{cases} \quad (4)$$

where f is the switching frequency, which can be expressed as $f = 1/T$.

At $t = T/2$, the maximum magnetic current can be given by

$$I_{Lm(\max)} = i_{Lm}\left(\frac{T}{2}\right) = \frac{V_{Lm}}{R_{Lm}} \cdot \left(\frac{2}{e^{-\frac{R_{Lm}}{2L_{Lm}f}} + 1} - 1\right). \quad (5)$$

It can be seen that the magnetic current is directly proportional to the voltage across the magnetic inductance but in inverse proportion to the equivalent resistance and the magnetic inductance. Particularly, decreasing the switching frequency can improve the amplitude of the magnetic current.

According to KVL, the primary and secondary balancing currents during the first half period can be expressed, respectively,

as

$$\begin{cases} L_{eqP} \cdot \frac{di_P}{dt} + i_P \cdot R_{eqP} \\ = \frac{D \cdot V_{Bat}}{2} - \frac{(n_1+D) \cdot V_{Bat}}{14} \\ L_{eqS} \cdot \frac{di_{S_k}}{dt} + i_{S_k} \cdot R_{eqS} \\ = \frac{(n_1+D) \cdot V_{Bat}}{14n_1} - V_{B_{2k-1}} \end{cases}, 0 < t < \frac{T}{2} \quad (6)$$

where i_P is the primary balancing current. i_{S_k} is the secondary balancing current of the k th winding. k is the winding number, i.e., 1, 2, ..., 6. $V_{B_{2k-1}}$ is the voltage of the odd cell B_{2k-1} . R_{eqP} represents the primary equivalent resistance, including the on resistance of one MOSFET, the connecting resistance, and the winding resistance. R_{eqS} represents the secondary equivalent resistance. L_{eqP} is the primary leakage inductance. L_{eqS} is the secondary leakage inductance.

Analogously, the balancing currents during the second half period can be expressed, respectively, as

$$\begin{cases} L_{eqP} \cdot \frac{di_P}{dt} + i_P \cdot R_{eqP} \\ = \frac{(n_1+D) \cdot V_{Bat}}{14} - \frac{D \cdot V_{Bat}}{2} \\ L_{eqS} \cdot \frac{di_{S_k}}{dt} + i_{S_k} \cdot R_{eqS} \\ = V_{B_{2k}} - \frac{(n_1+D) \cdot V_{Bat}}{14n_1} \end{cases}, \frac{T}{2} < t < T \quad (7)$$

where $V_{B_{2k}}$ is the voltage of the even cell B_{2k} .

Because the proposed equalizer mainly works at forward conversion, the initial balancing currents at each half period are approximately zero, i.e.

$$i_P(0) = i_P\left(\frac{T}{2}\right) \approx 0 \quad (8)$$

$$i_{S_k}(0) = i_{S_k}\left(\frac{T}{2}\right) \approx 0. \quad (9)$$

By solving (2)–(5), the primary and secondary equalization currents can be solved, respectively, as

$$\begin{cases} i_P(t) = \frac{(6D-n_1) \cdot V_{Bat}}{14R_{eqP}} \cdot \left(1 - e^{-\frac{R_{eqP}}{L_{eqP}}t}\right), & 0 < t < \frac{T}{2} \\ i_P(t) = \frac{(n_1-6D) \cdot V_{Bat}}{14R_{eqP}} \cdot \left(1 - e^{-\frac{R_{eqP}}{L_{eqP}}t}\right), & \frac{T}{2} < t < T \end{cases} \quad (10)$$

$$\begin{cases} i_{S_k}(t) = \frac{(n_1+D) \cdot V_{Bat} - 14n_1 \cdot V_{B_{2k-1}}}{14n_1 \cdot R_{eqS}} \\ \cdot \left(1 - e^{-\frac{R_{eqS}}{L_{eqS}}t}\right), & 0 < t < \frac{T}{2} \\ i_{S_k}(t) = \frac{14n_1 \cdot V_{B_{2k}} - (n_1+D) \cdot V_{Bat}}{14n_1 \cdot R_{eqS}} \\ \cdot \left(1 - e^{-\frac{R_{eqS}}{L_{eqS}}t}\right), & \frac{T}{2} < t < T. \end{cases} \quad (11)$$

Based on (10) and (11), the average primary current I_P and the average cell current I_{B_j} can be expressed, respectively, as

$$\begin{cases} I_P = \frac{|(6D-n_1) \cdot V_{Bat}|}{14R_{eqP}} \cdot \left[1 - \frac{2L_{eqP}}{T \cdot R_{eqP}} \left(1 - e^{-\frac{R_{eqP}}{L_{eqP}} \cdot \frac{T}{2}}\right)\right] \\ I_{B_j} = \frac{|(n_1+D) \cdot V_{Bat} - 14n_1 \cdot V_{B_j}|}{14n_1 \cdot R_{eqS}} \cdot \left[1 - \frac{2L_{eqS}}{T \cdot R_{eqS}} \left(1 - e^{-\frac{R_{eqS}}{L_{eqS}} \cdot \frac{T}{2}}\right)\right] \end{cases} \quad (12)$$

where j is the cell number, i.e., 1, 2, ..., 12.

From (10) to (12), it can be observed that the primary current I_P is in inverse proportion to the primary equivalent resistance R_{eqP} . The secondary cell current I_{B_j} is in inverse proportion to the secondary equivalent resistance R_{eqS} and the turns ratio. The cell current is also dependent on the cell voltage. Particularly, decreasing the switching frequency or leakage inductance can improve the average equalization currents, nevertheless which are independent of the magnetic inductance.

C. Analysis of the Balancing Loss

The balancing loss mainly consists of four parts, i.e., the conduction loss, the core loss of the balancing transformer, the gate driver circuit loss, and the switching loss.

The conduction loss owing to the equivalent resistance in circuits can be expressed as

$$P_R = I_P^2 \cdot R_{eqP} + \sum_{j=1}^{12} I_{B_j}^2 \cdot R_{eqS}. \quad (13)$$

It can be seen that the conduction loss will increase with the decrease of switching frequency due to the increased balancing current according to (12). However, due to the skin effect, the equivalent resistance will also increase with the increase of switching frequency, resulting in an increasing of conduction loss.

The core loss of the balancing transformer can be calculated using Steinmetz equation [28], [29], i.e.

$$P_B = k_1 \cdot f^{a_1} \cdot \Delta B_1^{b_1} = k_1 \cdot f^{a_1} \cdot \left(\frac{L_{m1}}{A_{S1} \cdot N_{P1}} \cdot \Delta I_{Lm1}\right)^{b_1} \quad (14)$$

where f is the switching frequency, i.e., $1/T$. ΔB_1 is the peak-to-peak flux density of the balancing transformer. k_1 , a_1 , and b_1 are the Steinmetz coefficients, which can be determined from the manufacturers. A_{S1} is the cross-sectional area of the magnetic core. L_{m1} is the magnetic inductance of the balancing transformer. N_{P1} is the turns number of the primary winding. ΔI_{Lm1} is the peak-to-peak magnetizing current, which can be achieved according to (1)

$$\Delta I_{Lm1} = \frac{(n_1+D) \cdot V_{Bat}}{28L_m \cdot f}. \quad (15)$$

Substituting (15) into (14) yields a further core loss expression as follows:

$$P_B = k_1 \cdot f^{a_1-b_1} \cdot \left(\frac{(n_1+D) \cdot V_{Bat}}{28A_{S1} \cdot N_{P1}}\right)^{b_1}. \quad (16)$$

Normally, we have $a_1 < b_1$; thus, a higher switching frequency leads to a lower core loss. The core loss will also decrease with the increase in the cross-section area and the turns number. However, the cross-section area is limited by the size of the transformer; therefore, the turns number should be as large as possible to get a lower core loss.

The gate driver circuit loss mainly includes the core loss of the driving transformer and the charging loss for the gate-source capacitors of the MOSFETs, which can be given by

$$P_D = k_2 \cdot f^{a_2 - b_2} \cdot \left(\frac{D \cdot V_{\text{Bat}}}{4A_{s2} \cdot N_{P2}} \right)^{b_2} + \sum_{i=1}^{12} \left(\frac{1}{2} f \cdot C_{GS} \cdot \left(\frac{D \cdot V_{\text{Bat}}}{2n_2} \right)^2 \right) \quad (17)$$

where k_2 , a_2 , and b_2 are the Steinmetz coefficients of the driving transformer. N_{P2} is the turns number of the primary winding of the driving transformer. n_2 is the turns ratio. A_{s2} is the cross-section area of the magnetic core. C_{GS} is the MOSFET gate-source capacitance.

It can be seen that a large turns number N_{P2} is favorable to decrease the core loss of the driving transformer. Decreasing the switching frequency or increasing the turns ratio n_2 will decrease the charging loss for the drain-source capacitors.

The switching loss of the MOSFETs can be represented as [30], [31]

$$P_S = \sum_{j=1}^{12} \left(\frac{1}{2} f \cdot C_{DS} \cdot V_{Bj}^2 + \frac{1}{2} f \cdot V_{Bj} \cdot I_{Bj} \cdot t_f \right) \quad (18)$$

where C_{DS} is the MOSFET drain-source capacitance. t_f is the MOSFET fall time. Apparently, a lower switching frequency leads to lower switching loss.

Based on (13) to (18), the overall balancing efficiency can be expressed as

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_R + P_B + P_D + P_S} \times 100\% \quad (19)$$

where P_{out} is the output balancing power. To summarize, a higher switching frequency leads to lower conduction loss and core losses, while a lower switching frequency leads to lower driving loss and switching loss. Therefore, the switching frequency should be optimized to achieve a lower overall loss.

D. Design Consideration of the Balancing and Driving Transformers

According to the analysis in Section II-C, there are six key design parameters, namely, the switching frequency, the turns ratio, the turns number, the cross-section area of the wire, the core size, and the air gap of the balancing and driving transformers.

1) *Switching Frequency*: Because the secondary MOSFETs are driven by the primary HBC, the secondary driving signals lag slightly behind the primary ones. Therefore, in order to achieve a good synchronization of the primary and secondary HBCs, the switching frequency cannot be too high. However, a lower switching frequency will lead to a larger transformer.

2) *Turns Ratio*: The turns ratio of the transformers is a crucial design factor, which is governed by the output voltage of the BBC. The total voltage of a 12-cell battery module is about 30–44 V. Due to the buck conversion, the dc voltage should be less than 30 V. Therefore, the turns ratio of the balancing transformer should be 3–4 to achieve a large current and high efficiency. The turns ratio of the driving transformer should be 1–2 to achieve 7–15 V driving voltages.

3) *Turns Number*: According to (16), the core loss can be significantly reduced by increasing the turns number. Moreover, the larger the turns number, the better the consistency of the transformer windings. However, a large turns number will cause a higher copper loss and a larger transformer size.

4) *Cross-Section Area of the Wire*: The cross-section area of the wire is determined by the wire resistance, which limits the power of the transformer. On the one hand, the resistance of the windings will cause the secondary winding voltages to drop at higher balancing currents. On the other hand, the ohmic loss of the windings will heat up the transformer. Therefore, the resistance of the windings must be kept as low as possible to make the transformer with a high-power rating and efficiency. As a result, the thicker wires can be chosen to reduce resistance, nevertheless, which will result in an increase of the core size. In summary, the cross-section area of the wire can be reasonably designed to achieve a good trade-off between the power loss and the core size.

5) *Core Size*: The core size only limits the number of the windings and the cross-section area of the wire, but does not determine the power of the transformer. A large core gives more space for the windings with thicker wires to reduce the resistance. Moreover, a larger core area can increase the flux by reducing the number of turns and can better dissipate the heat caused by the power loss. Generally, 2.5–3 times the calculated core size should be chosen to do with the wire insulation, air between the turns, and a coil former.

6) *Air Gap Length*: Because the power of the balancing transformer is large, and the equalization works partially at the buck–boost and flyback conversions, the balancing transformer needs a certain air gap to store energy. However, the power of the driving transformer is lower. Therefore, in order to reduce the leakage inductance and delay in the secondary driving signals, the air gap of the driving transformer is better to be 0.

III. EXPERIMENTAL RESULTS

In order to verify the proposed balancing method, an experimental prototype was built for 12 series-connected LiFePO₄ batteries with 1100-mAh capacity. According to the forward and flyback operations, the secondary windings should have the same turns number (or turns ratio) to achieve the fine voltage equalization among cells. Nevertheless, the consistency of the battery internal resistance, the MOSFET ON-resistance, the parasitic capacitance, and the leakage inductance only affect the balancing current, not the final balanced cell voltage. Therefore, in order to achieve a good consistency of the transformer, twisted multi-strand magnet copper wires are used to make the multiple windings. Table I presents the parameters of the balancing

TABLE I
PARAMETERS OF THE BALANCING CIRCUIT

Symbol	Parameter
Q_1 - Q_{12}	MOSFETs, BUK7K8R7-40EX, $R_{DS(on)} \leq 8.5 \text{ m}\Omega$
Q_{b1} - Q_{b2}	MOSFETs, BUK7K8R7-40EX, $R_{DS(on)} \leq 8.5 \text{ m}\Omega$
C_{h1} - C_{h2}	Electrolytic capacitors, 220 μF
C_{b2}	Film capacitors, 3.3 μF
L_{b1}	Inductors, 100 μH
Q_{b1} - Q_{b2}	MOSFETs, BUK9Y12-100E,115, $R_{DS(on)} \leq 12 \text{ m}\Omega$
C_{b1}	Film capacitors, 1 μF
S_1 - S_{12}	Transistors, NMB2227AF, PNP, $V_{CEO} \leq 40\text{V}$, $I_C \leq 600 \text{ mA}$
D_1 - D_{12}	Diodes, BAT54GWJ
R_{11} - $R_{12,1}$	Resistors, 100 Ω
R_{12} - $R_{12,2}$	Resistors, 10 k Ω
R_{13} - $R_{12,3}$	Resistors, 1 k Ω

Note: $R_{DS(on)}$: Static drain-source on resistance of MOSFETs. V_{CEO} : collector-emitter voltage of transistors. I_C : collector current of transistors.

TABLE II
PARAMETERS OF THE BALANCING TRANSFORMERS WITH DIFFERENT TURNS NUMBERS

N_{P1}	N_{S1}	L_{m1} (μH)	L_{eqP} (μH)	L_{eqS} (μH)	R_{wP} (m Ω)	R_{wS} (m Ω)
20	5	985.4	15.3	1.0	113	24
32	8	2524	16.1	1.0	116	24
40	10	3939	34.7	2.1	119	24
60	15	8798	23.0	0.9	172	26

Note: N_P and N_S are the primary and secondary turns numbers, respectively. L_{eqP} and L_{eqS} are the primary and secondary leakage inductances, respectively. R_{wP} and R_{wS} are the primary and secondary winding resistances, respectively.

TABLE III
PARAMETERS OF THE DRIVING TRANSFORMERS WITH DIFFERENT TURNS NUMBERS

N_{P2}	N_{S2}	L_{m2} (μH)	L_{eqP} (μH)	L_{eqS} (μH)	R_{wP} (m Ω)	R_{wS} (m Ω)
33	33	2793	0.6	0.6	615	615
45	30	5340	4.9	2.2	980	194
66	33	11608	1.9	0.6	1510	598

circuit. Tables II and III present the parameters of the balancing and driving transformers with different turns numbers and air gaps, respectively.

Fig. 5 presents the experimental waveforms of the driving voltage, the driving current, and the magnetizing current of the driving transformer with the MHBC working at 10 kHz. It can be seen that the driving voltage for the odd cells follows the ac voltage of the primary HBC in the first half period. Due to the leakage inductance of the driving transformer and the series-connected resistor R_{11} , the driving voltage lags slightly behind the ac voltage. When the ac voltage jumps from negative to positive, the peak charging current for the drain-source capacitor of the MOSFET is about 0.24 A, which is limited by the series-connected resistor R_{11} . When the ac voltage jumps from positive to negative, the peak discharging current of the drain-source

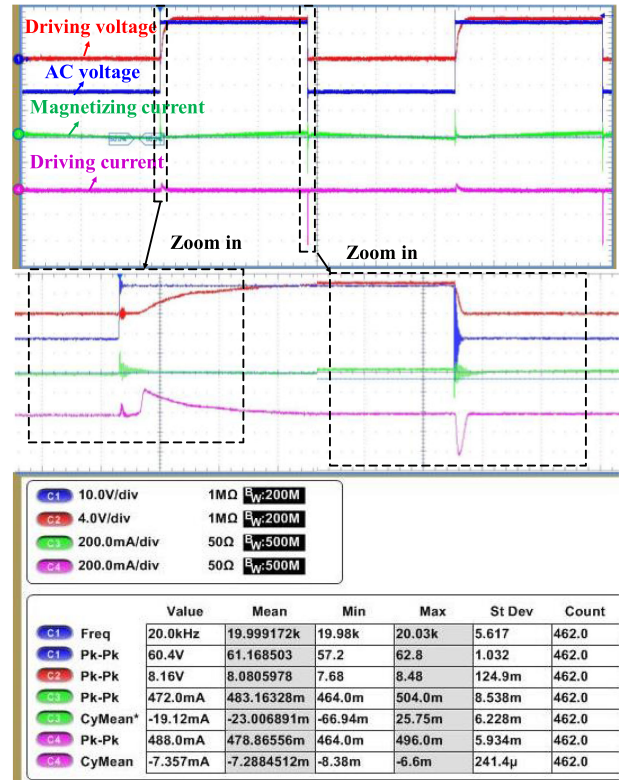


Fig. 5. Experimental waveforms of the driving voltage, current, and magnetizing current of the driving transformer with the MHBC working at 10 kHz.

capacitor is up to 0.4 A because of the short circuit of the drain-source capacitor. It is worth mentioning that the magnetizing current is approximately a triangle waveform. However, due to the charging of the drain-source capacitors, a 0.2-A spike is added in the magnetizing current when the ac voltage jumps.

Fig. 6 further presents the experimental waveforms of the winding currents and the magnetic current with the MHBC working at 10 kHz. It can be observed that because the balancing is mainly based on the forward conversion, the balancing

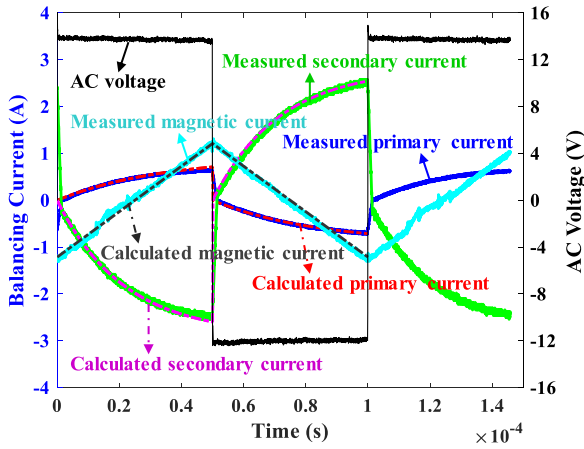
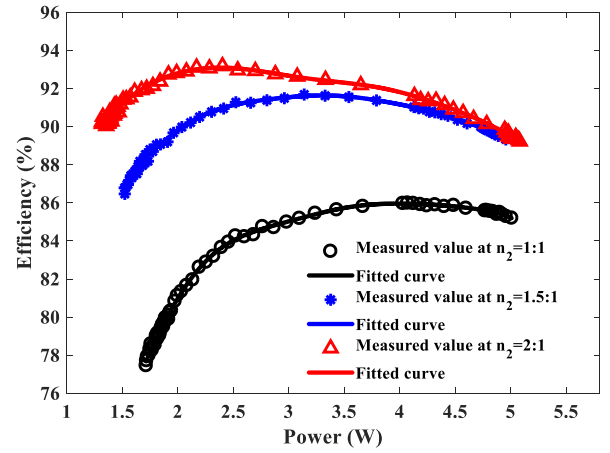


Fig. 6. Experimental and theoretical waveforms of the winding currents and the magnetic current at 10 kHz.

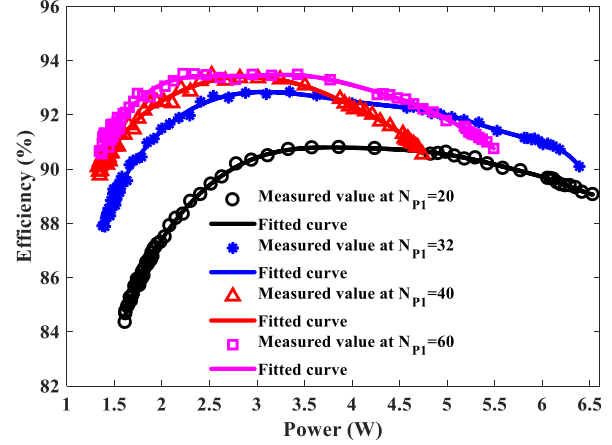
currents exponentially increase from near zero during each one half period due to the effect of the leakage inductance and the equivalent resistance. The peak primary and secondary balancing currents are 0.7 and 2.56 A, respectively. In addition, the measured magnetic current is approximately a triangular waveform with an amplitude of 1.2 A due to the larger magnetic inductance and smaller equivalent resistance. It is important to note that the calculated primary/secondary currents and the magnetic current match well with the experimental ones, which verifies the effectiveness of (4), (10), and (11).

Fig. 7 illustrates the measured efficiencies of the MHBC with different driving and balancing transformers. As shown in Fig. 7(a), the efficiency can be dramatically improved by increasing the turns ratio of the driving transformer. On the one hand, a higher turns ratio leads to a lower driving voltage, decreasing the driving loss. On the other hand, the core loss of the driving transformer is reduced by increasing the primary turns number. As shown in Fig. 7(b), when the primary turns number of the balancing transformer increases from 20 to 32, the efficiency increases dramatically due to the reduced core loss of the balancing transformer. However, when the turns number increases from 32 to 60, the efficiency increases slightly due to almost the same core loss. From Fig. 7(c), we can observe that the peak efficiency, i.e., 93%, is achieved at 10 kHz. When the switching frequency is lower, the efficiency at lower power dramatically decreases because of the increasing core loss of the transformer, but the efficiency increases instead at higher power. When the switching frequency is higher, the efficiency decreases significantly, particularly at higher power because of the larger switching loss and copper loss of the transformer.

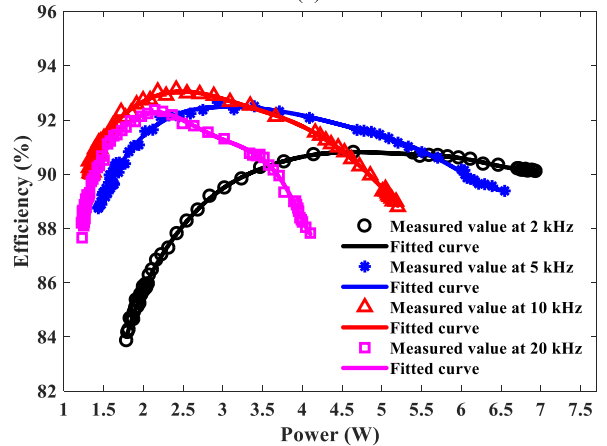
Fig. 8 shows the balancing results with the fixed duty cycle of the BBC for 12 series-connected cells at 10 kHz. It can be observed from Fig. 8(a) that all the cells are balanced toward the average cell voltage. The higher voltage cells are balanced by discharging and the lower voltage cells are balanced by charging. As shown in Fig. 8(b), the cell balancing currents have a similar evolution tendency. The cell current is dependent on the cell voltage. At the beginning of balancing, the maximum cell current



(a)



(b)



(c)

Fig. 7. Measured efficiencies of the MHBC with different balancing and driving transformers. (a) With different turns ratios of the driving transformer. (b) With different turns numbers of the balancing transformer. (c) At different switching frequencies.

is about 1.3 A and the total balancing current is about 6 A for 12 cells. After about 800 s, the cell voltages are balanced to about 3 V. As shown in Fig. 8(b), it is important to note that when the cells are balanced at 800 s, the cells still have a 0.35-A charging current, which is the loop current caused by the M2MC equalization.

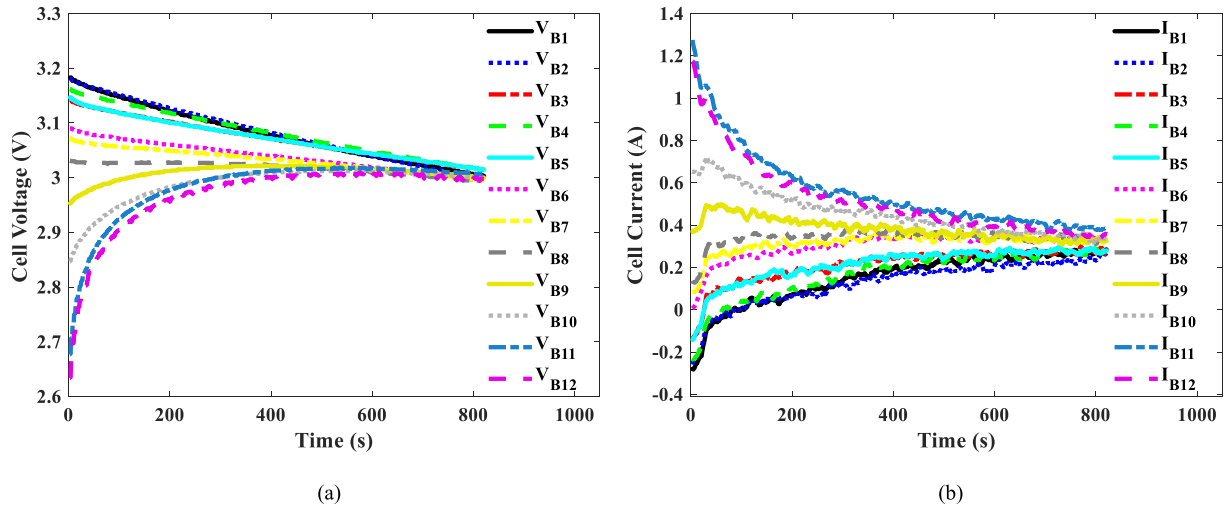


Fig. 8. Balancing results with the fixed duty cycle of the BBC for 12 series-connected cells at 10 kHz. (a) Cell voltage evolution. (b) Cell current evolution.

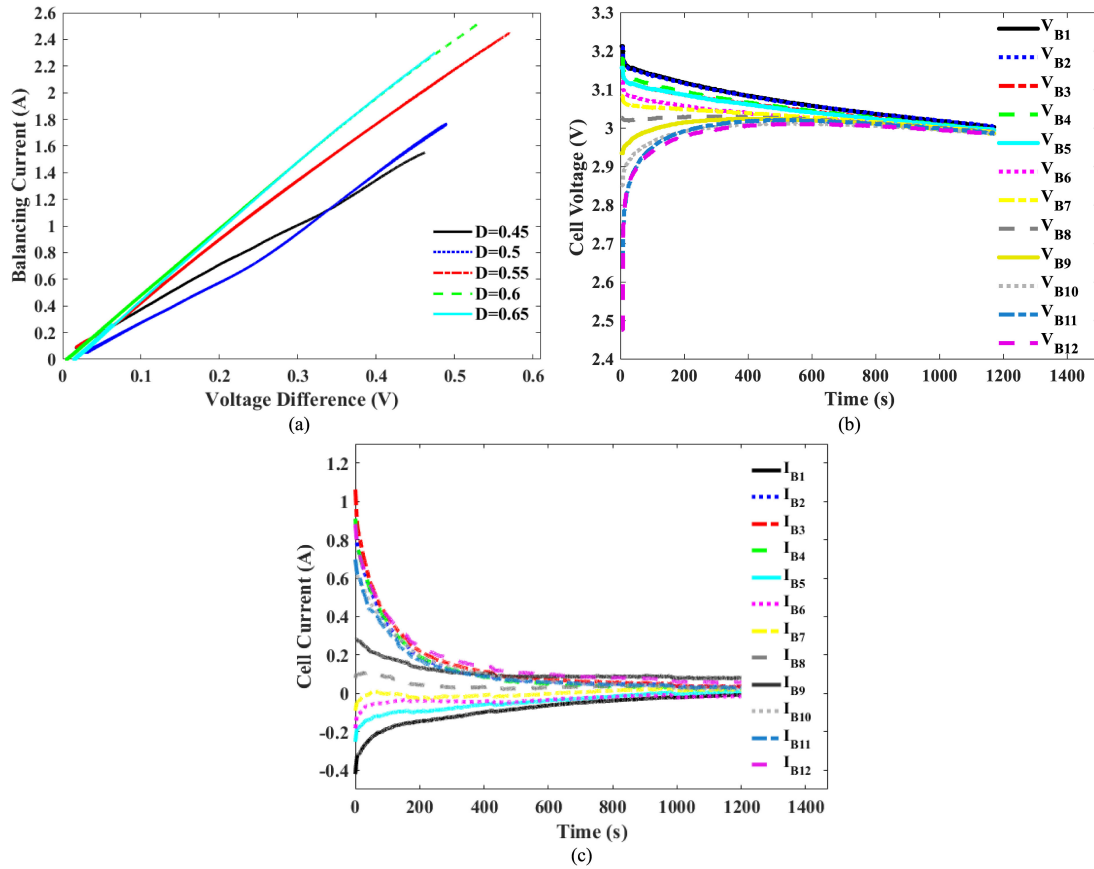


Fig. 9. Balancing results with varying balancing currents for 12 series-connected cells at 10 kHz. (a) Balancing current versus the cell voltage difference at different duty cycles of the BBC. (b) Cell voltage evolution. (c) Cell current evolution.

Fig. 9(a) presents the balancing current versus the cell voltage difference at different duty cycles of the BBC. It can be noted that the larger the cell voltage difference, the larger the balancing current. Particularly, the balancing current can be significantly improved by increasing the duty cycle D at larger cell

voltage differences. However, the effect of the duty cycle on the balancing current becomes less and less with the decrease of the cell voltage difference. Therefore, in order to reduce the loop current flowing from module to cells, the duty cycle of the BBC should be reduced with the decrease of the cell voltage

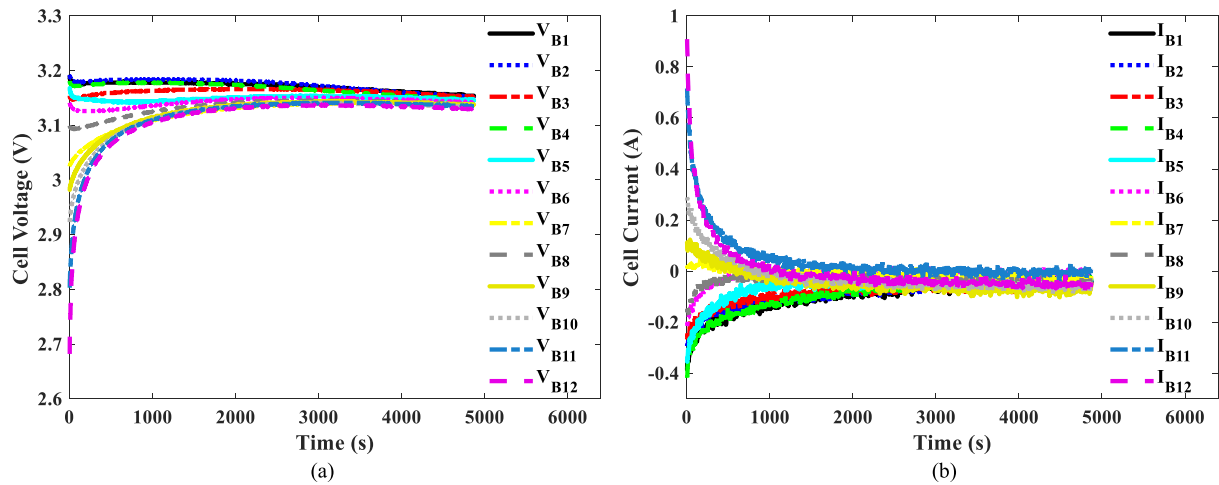


Fig. 10. Self-balancing results for 12 series-connected cells at 10 kHz. (a) Cell voltage evolution. (b) Cell current evolution.

TABLE IV
A COMPARISON OF THE PROPOSED EQUALIZER WITH THE CONVENTIONAL ANALOGOUS SOLUTIONS [22], [23]

Topologies	Winding number	Diode number	MOSFET or driver number	Balancing mode	Balancing Speed	Efficiency
Ramp equalizer [22]	$m/2+1$	m	2	M2MC balancing	Low Adjustable	$\leq 75\%$
Forward-flyback equalizer [23]	m	0	m	AC2AC self-balancing	Low Non-adjustable	89%
Proposed equalizer	$m/2+1$	0	4	M2MC balancing and AC2AC self-balancing	High Adjustable	88%

difference. Fig. 9(b) shows the balancing results with the varying duty cycle of the BBC according to the cell voltage difference. It can be seen from Fig. 9(c) that the cell currents decrease continuously with the decrease of the cell voltage difference. All the cell currents almost decrease to zero when the cells are balanced. However, the total equalization time increases to 1200 s because of the reduced balancing current.

Fig. 10 shows the AC2AC self-balancing results for 12 series-connected cells when no energy is transferred from module to cells. As shown in Fig. 10(a), because the balancing current is dependent on the cell voltage difference, the equalization time increases significantly, which is up to 5000 s. As shown in Fig. 10(b), the maximum balancing current for the lowest-voltage cell is 0.9 A. It is important to note that the cell currents gradually decrease to 0 with the decrease in the cell voltage difference without loop current.

Table IV presents a comparison of the proposed equalizer with the conventional methods in terms of the numbers of components, balancing speed, and efficiency.

The ramp equalizer [22] is based on the passive rectification using diodes, which uses fewer MOSFETs and isolated gate drivers, leading to a small size and low cost. However, its efficiency will become very low, i.e., lower than 75%, for low-voltage cells, e.g., 2–3.65 V, due to the higher voltage drop across diodes, e.g., 0.4–0.8 V. Moreover, because the ramp equalizer [22] is a unidirectional converter, it only works at the M2MC

balancing mode and has a low balancing speed due to the voltage drop across diodes.

The forward-flyback equalizer [23] uses m MOSFETs and m transformer windings to achieve the AC2AC self-equalization with a balancing efficiency of 89%. However, the balancing current is nonadjustable and completely dependent on the cell voltage difference, leading to a slow equalization speed for a large battery string.

In fact, the proposed equalizer is an improvement of the forward-flyback conversion [23], which reduces the number of windings by half based on buck–boost and forward operations, significantly reducing circuit volume and cost. Moreover, the secondary MOSFETs are directly driven by the primary HBC without the need of additional isolated gate drivers and power supplies, contributing to a low cost and ease of control. The proposed equalizer works at two modes, i.e., the M2MC balancing for larger cell voltage differences and AC2AC self-balancing for smaller cell voltage differences. Particularly, the balancing current can be adjusted by controlling the BBC according to the cell voltage differences, effectively improving the equalization speed and effectiveness. Considering the loss of the BBC, the total efficiency of the M2MC balancing is approximately 88%, which is comparable to the forward-flyback equalizer [23].

In order to show the advantages of the proposed driving scheme based on synchronous rectification, Table V further presents a cost comparison of the proposed driving method with

TABLE V
COST COMPARISON OF THE PROPOSED DRIVING METHOD WITH THE CONVENTIONAL SOLUTION FOR 12 SERIES-CONNECTED CELLS

Driving method	Component	Parameter	Unit price (\$)	Quantity	Cost (\$)	Total cost (\$)
Proposed method	Transformer core	E20/10/11 Ferrite	0.283	1	0.283	1.413
	Transformer skeleton	E20/10/11 Skeleton	0.5	1	0.5	
	Transistor	NMB2227AF	0.05	7	0.35	
	Diode	BAT54GWJ	0.02	14	0.28	
Traditional method [23]	Driver IC (pair)	UCC21520QDWRQ1	3.31	6	19.86	22.74
	Bootstrap diode for driver	PMEG40T30EPX	0.129	12	1.548	
	Blocking diode for driver	SBR1A20T5	0.111	12	1.332	

the conventional solution [23] for 12 series-connected cells. It can be seen that the total cost for the proposed driving scheme is only \$1.413, which is much lower than the conventional solution [23], i.e., \$22.74.

IV. CONCLUSION

This paper proposed a battery balancing circuit based on synchronous rectification with a reduced number of gate driver circuits. On the one hand, the number of transformer windings is almost reduced by half, and thus, the circuit cost is significantly lowered. On the other hand, the secondary MOSFETs are directly driven by the primary HBC, significantly reducing the cost of the MOSFETs and isolated gate drivers. It is worth mentioning that the equalization current can be adjusted by controlling the BBC, which makes the proposed equalizer capable of working in either M2MC or AC2AC balancing modes according to the cell voltage differences. The analytical expressions of the balancing currents and efficiency were derived. The design considerations of the proposed equalizer are discussed. An experimental prototype for 12 series-connected cells was built. Through detailed analyses of the experimental results for 12 series-connected Li-ion batteries, some conclusions can be obtained.

- 1) The balancing current is mainly determined by the input voltage of the BBC, the equivalent resistance, the leakage inductance, and the switching frequency, but independent of the magnetic inductance.
- 2) The balancing efficiency can be improved by increasing the primary turns number of the balancing transformer.
- 3) The loss of the gate driver circuit can be reduced by increasing the turns ratio of the driving transformer.
- 4) In order to achieve a higher efficiency, a higher switching frequency is favorable at lower balancing power while a lower switching frequency is favorable at higher balancing power.

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Yunlong Shang (S'14–M'18) received the B.S. degree in automation from Hefei University of Technology, Hefei, China, in 2008, and the Ph.D. degree in control theory and control engineering from Shandong University, Shandong, China, in 2017.

In 2019, he joined Shandong University, where he is currently a Full Professor and Qilu Youth Talent Scholar with the School of Control Science and Engineering. Between September 2015 and October 2017, he conducted scientific research as a joint Ph.D. student with the Department of Electrical and Computer

Engineering, San Diego State University, San Diego, CA, USA, where between December 2017 and January 2019, he was a Postdoctoral Research Fellow. His current research interests include battery balancing, self-heating for low-temperature batteries, battery modeling and states estimation, and design of battery management systems (BMS).

Prof. Shang won the Excellent Doctoral Dissertation Award of the Chinese Association of Automation (CAA) in 2018.



Shuofeng Zhao received the B.E. and Ph.D. degrees, both in electrical engineering from Zhejiang University, Hangzhou, China, in 2013 and 2018, respectively.

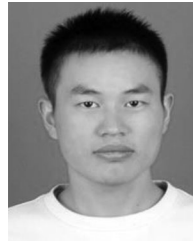
Since December 2018, he has been a Postdoctoral Researcher with the Department of Electrical and Computer Engineering, San Diego State University, San Diego, CA, USA. His current research interests include power electronics and machine in e-transportation and clean energy applications.



Yuhong Fu received the M.S. degree in automotive systems engineering from the University of Michigan-Dearborn, Dearborn, MI, USA, in 2011.

She is currently with San Diego State University, San Diego, CA, USA.

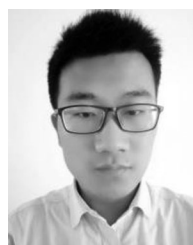
Her current research interests include battery modeling and management for electric drive vehicle applications.



Bing Han received the B.S. degree in electronic and information engineering from Hefei University, Hefei, China, in 2012.

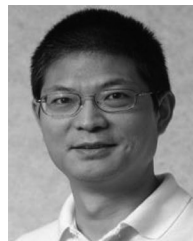
He is currently an Electronic Engineer in the R&D Department of Battery Management System (BMS), Hefei Guoxuan High-Tech Power Energy Co. Ltd., Anhui, China. He is mainly engaged in the design of active balancing BMS based on a national major project. Additionally, he worked at the transmission business unit of Continental Corporation in Shanghai for two years. His current research inter-

ests include several switching mode power supply topologies such as buck, boost, fly-back and forward, especially the analysis of their electromagnetic compatibility issues.



Panpan Hu received the Undergraduate degree from the Nanchang Institute of Technology, Nanchang, China, in 2008.

He has been engaged in the research and development of BMS technology for about ten years. In 2014, he joined Hefei Guoxuan High-Tech Power Energy Co. Ltd., Anhui, China, to conduct BMS research on electric vehicles. His current research interests include electric commercial vehicles, passenger vehicles, energy storage, and other fields.



Chunting Chris Mi (S'00–A'01–M'01–SM'03–F'12) received the B.S.E.E. and M.S.E.E. degrees in electrical engineering from Northwestern Polytechnical University, Xi'an, China, in 1985 and 1988, respectively, and the Ph.D. degree in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2001.

He is currently a Professor and Chair of Electrical and Computer Engineering and the Director of the Department of Energy (DOE)-funded Graduate Automotive Technology Education (GATE) Center for Electric Drive Transportation, San Diego State University (SDSU), San Diego, CA, USA. Prior to joining SDSU, he was with the University of Michigan, Dearborn, MI, USA, from 2001 to 2015. His current research interests include electric drives, power electronics, electric machines, renewable-energy systems, and electric and hybrid vehicles.