A Four-Switch Three-Phase AC–DC Converter With Galvanic Isolation

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***Abstract*—A new single stage three-phase ac–dc converter with four switches and galvanic isolation is proposed in this paper. The new converter is simple and uses fewer switches than previously proposed ac–dc converters of the same type. It is a bridgeless converter that can operate with continuous input current and with any pulsewidth modulated method suitable for a standard three-phase six-switch voltage source rectifier. In this paper, the operation, control, analysis, and design of the proposed converter are explained and its features are discussed. Experimental results obtained from a prototype that confirm the feasibility of the converter are presented as well.**

***Index Terms*—AC–DC converter, pulsewidth modulated (PWM) power converters, single-stage power factor corrected (SSPFC), transformers.**

I. Introduction

THREE-PHASE ac–dc converters that have galvanic isolation are widely used in industrial applications. The harmonic content of these converters are restricted to the limits placed by the harmonic standards of regulatory agencies; the converters are thus implemented with some form of the input power factor correction (PFC). Typical converters are two-stage converters with an input three-phase ac–dc stage followed by a dc–dc stage that includes an isolation transformer.

There are different options for the ac–dc stage implementation. Boost-type continuous conduction mode (CCM) converters are an attractive option for the PFC stage because they have low input current distortion and an input power factor around unity. Among boost type CCM converters, pulsewidth modulated (PWM) voltage source rectifiers (VSRs) are one of the most simple and common choices for ac–dc converters [1]. A typical three-phase PWM-VSR uses six switches to perform ac–dc conversion. The operation, design, and control of PWM-VSRs are comprehensively studied in the literature and they are used widely in industry [2]–[4]. For the second stage, the dc–dc converter full bridge (FB) zero-voltage switching (ZVS)-PWM converters are an attractive option [5]–[7]. FB-ZVS-PWM converters are well-known and widely used in industrial applications; such converters use four switches for the dc–dc conversion. Fig. 1 shows a typical two-stage ac–dc converter; it can be seen that two-stage converters need a significant number of switches and, consequently, are expensive and bulky.

Simpler, lighter, and cheaper single-stage ac–dc converters that can convert a three-phase ac voltage into an isolated dc voltage have thus been proposed in the literature. These converters perform three-phase ac–dc conversion and dc–dc conversion using just a single converter. Previously proposed single-stage converters have at least one of the following drawbacks.

1) The input currents of the converter are discontinuous with very high current peaks as the converter input section is left uncontrolled. By operating the converter with a fixed duty-cycle and designing the converter so that its input currents are discontinuous the input currents are a set of triangular current pulses whose amplitudes are bounded by a sinusoidal envelope. These current waveforms are problematic because their high current peaks create high peak current stresses in components, high turn-off losses, and high electromagnetic interference (EMI) noise. These current peaks limit the amount of power that three-phase single-stage ac–dc converters can operate at to about 2–3 kW at most (i.e., [8], [9]).
2) They require a large number of switches so that the benefit of cost-reduction that single-stage converters have is minimized. This is especially true of matrix-type converters that can require at least six pairs of back-to-back switches (12 switches) such as those proposed in [10]–[13] for example.
3) The converters have an input diode bridge, which can contribute to conduction losses for higher power converters where there is more current flowing in the converter (i.e., [14]–[16]).
4) Sophisticated, non-standard, converter specific control methods must be used to operate the converter. This is especially the case for 12-switch single-stage converters and for resonant-type converters that are operated with a combination of variable-switching frequency control and PWM [11], [17]).

A six-switch, three-phase, single-switch converter that had a three-phase transformer in its topology and that did not have any of these drawbacks was proposed by Khodabakhsh and Moschopoulos [18]. That paper briefly explained the operation

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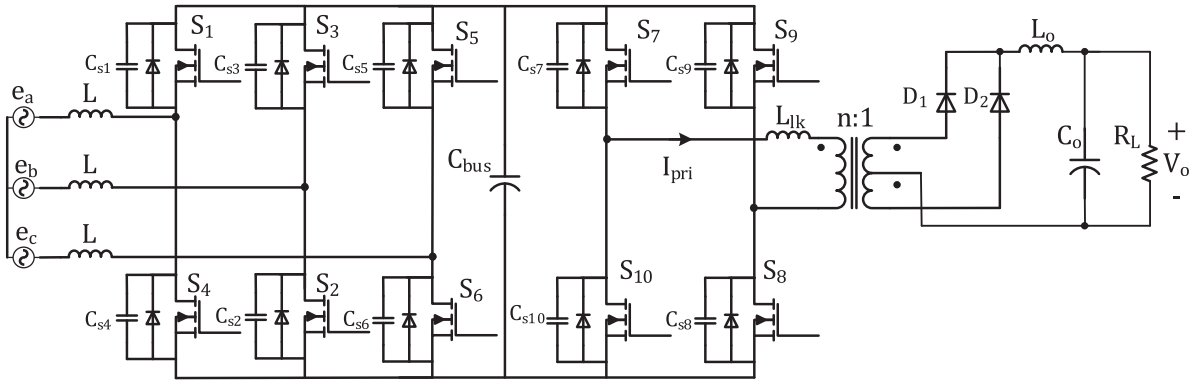

Fig. 1. Typical two-stage converter.

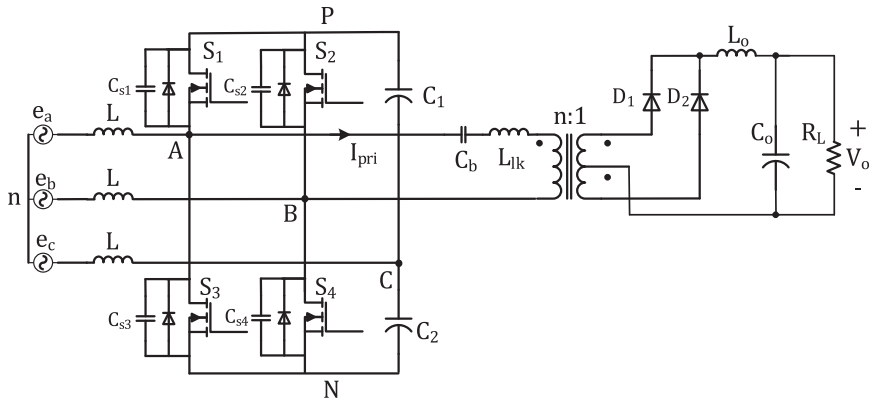

Fig. 2. Proposed three-phase ac–dc single-stage converter.

of the converter and presented some simulation results, but did not present any analysis, design, or experimental work. A version of the converter that was designed for aerospace applications where three-phase 400 Hz input voltage sources are used was proposed in [19]. That paper presented a six-switch, three-phase, single-switch converter that had a single-phase transformer in its topology; the feasibility of the converter was confirmed with experimental results.

In this paper, a new single-stage power factor corrected (SSPFC) ac–dc is proposed. The outstanding features of the proposed converter are that it has only four switches in its topology, it is bridgeless, its input currents are continuous, and it can be implemented with any control method used in standard three-phase, six-switch VSRs. In this paper, the converter's general operation and its modes of operation are explained in Section II, its features are stated in Section III. A steady-state mathematical model of the converter is developed in Section IV, a design procedure of the converter is developed and demonstrated with a design example in Section V, and experimental results from a simple proof-of-concept prototype are presented in Section VI. The main points of the paper are summarized and conclusions are made in Section VII.

II. Converter Operation

The proposed three phase ac–dc converter is shown in Fig. 2. The converter consists of three input inductors *L*j with internal resistance equal to *R*, a four-switch three-phase rectifier with switches S_1–S_4 and capacitors C_1 and C_2, a dc blocking capacitor C_b, an isolation transformer with n:1 turns ratio and leakage inductance L_{lk}, two output rectifying diodes $D_1 - D_2$, an output filter inductor L_o, and an output capacitor C_o.

The converter is a combination of a four-switch three-phase ac–dc rectifier and an FB-ZVS-PWM dc–dc converter in its topology. Fig. 3 shows the circuit diagram of the two sub-converters; the operation of each sub-converter is explained in this section. The following should be noted.

1) The operation of the proposed converter is based on three-phase PWM theory and thus differs from that of a number of other, previously proposed ac–dc converters where the converter is made to operate with a fixed duty-cycle and the input currents are made to be discontinuous with high current peaks. Information about the operation of three-phase, six-switch VSrs/inverters and three-phase PWM can be found in standard textbooks such as [20]–[22].
2) More information about the operation of the three-phase, four-switch sub-converter can be found in papers such as [4], [23]. What is presented here is a brief explanation of how a six-switch converter can be transformed into a four-switch converter. It should be especially noted that the transformation alters just the phase relationships between the gating signals of two legs and not the PWM pattern; any PWM method that can be in a six-switch converter can be

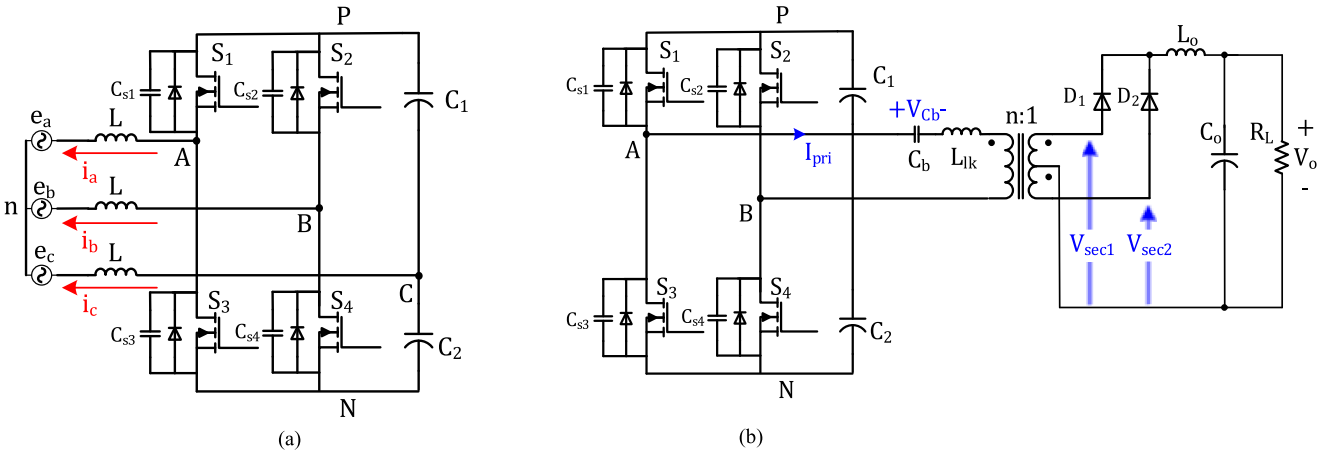

Fig. 3. AC–DC converter stages. (a) AC–DC stage. (b) DC–DC stage.

used in a four-switch converter. In a balanced three-phase system, if two of the input currents are controlled by two phase legs, then the third input current will automatically be such that when the three input current waveforms are added up, the sum is zero.

3) During steady-state operation, switches S_1 and S_3 turn ON and OFF so that the voltage at point A in the circuit diagram shown in Fig. 2 is either the bus voltage V_{PN} or 0 at any instant of a switching cycle. Likewise, switches S_2 and S_4 turn ON and OFF so that the voltage at point B in the circuit diagram is either the bus voltage V_{PN} or 0 at any instant of a switching cycle. As a result, voltage V_{AB} will either be $+V_{PN}$, $-V_{PN}$, or 0 at any instant of a switching cycle. As there is a transformer between points A and B, switches S_1, S_3, S_2, and S_4 are indeed like a dc–dc full-bridge converter where $+V_{PN}$, $-V_{PN}$, or 0 are also impressed across its transformer's primary, with one key difference—the duty-cycle of this full-bridge is not fixed, but varies throughout an ac input line cycle. The four converter switches are operated in accordance with a PWM method to ensure that the three input currents are sinusoidal and in phase with the three-phase input voltages, and the dc–dc conversion part of the converter is just tapped off points A and B with the transformer. Blocking capacitor C_b has been added to prevent transformer saturation.

A. AC–DC Converter

The ac–dc converter stage [see Fig. 3(a)] is a four switch PWM VSR. This converter should perform PFC and absorb the required active power from the grid to supply the load and store it in the two capacitors (C_1 and C_2) at the intermediate dc bus. To perform these operations, the four-switch converter should apply a proper three phase balanced voltage at the converter terminals A, B, and C and since only two legs of the converter have active switches, the phase difference between the voltages of the two active legs (phase A and B) is 60° instead of 120°.

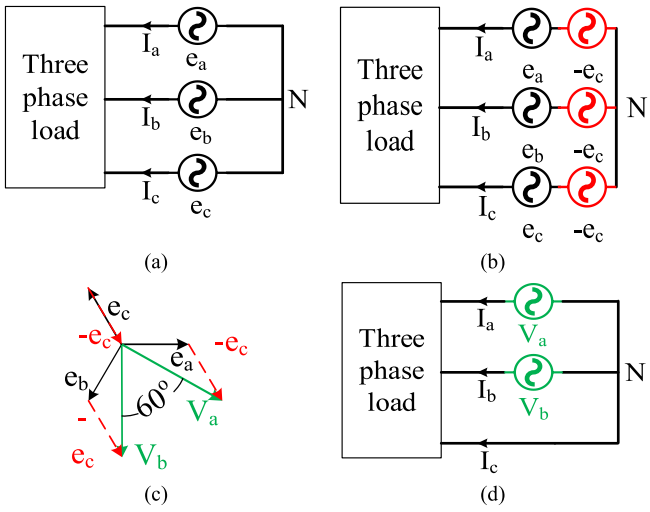

Fig. 4. Three phase load supply by two voltage sources.

The aforementioned operation method can be explained based on the phasor diagram of phase voltages shown in Fig. 4. Fig. 4(a) shows a three-phase star connected voltage source that is connected to a three-phase load. In Fig. 4(b), three voltage sources having the same amplitude and 180° phase shift with phase "C" voltage are connected in series to each phase voltage source. The new system phasor diagram is shown in Fig. 4(c). In phase "C," the overall voltage is zero; for phases "A" and "B" the voltages become V_a and V_b, respectively. The current that flows in the leg with split capacitors, phase "C," is the sum of the current in phases "A" and "B;" as a result, current flows in phase "C" without any voltage source.

Fig. 5 shows some typical control signals of phases "A" and "B" within a line cycle (note the 60° phase shift in modulation signals). Since any PWM method that can be used for six-switch voltage source converters can be used in the proposed ac–dc converter to generate the switching signals, sinusoidal PWM (SPWM) was used in this work at it is one of the simplest PWM methods.

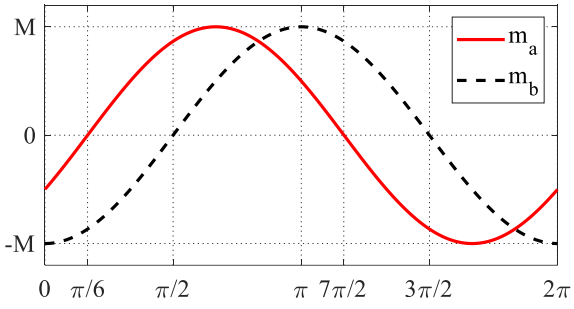

Fig. 5. Modulation signals in line frequency.

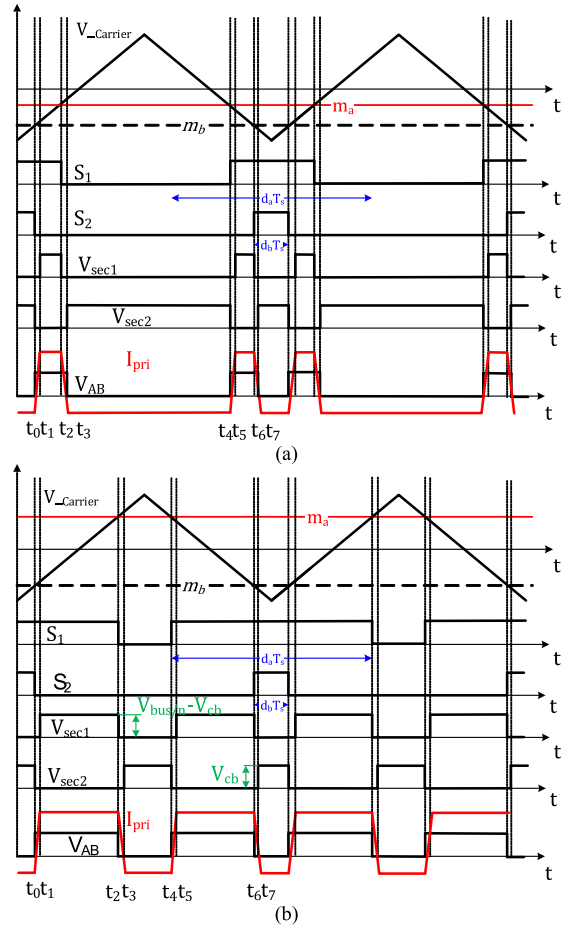

Fig. 6. Modulation signals in switching frequency scale, gate signals, secondary voltages, primary voltage, and current. (a) $0 \leq \omega t \leq \frac{\pi}{6}$. (b) $\frac{\pi}{6} \leq \omega t \leq \frac{\pi}{2}$.

B. DC–DC Converter

The dc–dc sub-converter is shown in Fig. 3(b). The converter is a conventional FB-ZVS-PWM converter, but with its gating signals generated with an SPWM pattern. Consequently, the modes of operation of the dc–dc stage can be explained with respect to the SPWM switching sequence. The gating pulses are generated with comparison of the modulation signals, as shown in Fig. 5 with a triangular carrier.

Fig. 6 shows some typical gating signal waveforms for a switching cycle with respect to the modulation signals within the range of $\pi/6 < \omega.t < \pi/2$. The gate pulses for the upper switches of the legs (S_1 and S_2) are shown, with the carrier and modulating signals of the SPWM pattern, voltage V_{AB} and primary current $I_{\rm pri}$. It should be noted that S_3 and S_4 are complementary to S_1 and S_2, respectively.

The four switches of the converter act as an FB-ZVS-PWM converter and V_{AB} is a square wave PWM waveform with varying duty cycle. The voltage of V_{AB} has a dc component in the switching cycle and a blocking capacitor C_b is used to prevent this component from saturating the transformer.

The modes of operation of the dc–dc sub-converter with respect to the gate pulses that is shown in Fig. 6 are explained for each switching cycle. Also, an equivalent circuit for each mode shown in Fig. 7. it is assumed that S_1 and S_2 are on and that there is a dead-time between switching transitions.

1) *Mode 1 ($t_0 < t < t_1$):* At the start of this mode, S_2 turns OFF and the transformer primary current ($I_{\rm pri}$) starts to flow through the body diode of S_4. $V_{\rm AB}$ is equal to dc-bus voltage (V_{PN}), and $I_{\rm pri}$ increases linearly. Sometime during this mode, S_4 can be turned on with ZVS before $I_{\rm pri}$ reaches zero. During this mode, both $V_{\rm sec1}$ and $V_{\rm sec2}$ are zero and the output inductor current circulates through the secondary side diodes. This is a freewheeling mode and no energy is transferred from the primary side to the output.
2) *Mode 2 ($t_1 < t < t_2$):* At the start of this mode, $I_{\rm pri}$ becomes positive and it flows through S_1 and S_4. V_{AB} is equal to the dc-bus voltage. The transformer primary voltage is positive and energy from the dc-bus capacitors is transferred to the output as the $V_{\rm sec1}$ is positive and diode D_1 is conducting.
3) *Mode 3 ($t_2 < t < t_3$):* At the start of this mode, S_1 turns OFF and $I_{\rm pri}$ flows through the anti-parallel diode of S_3. The voltage across V_{AB} is zero; as a result, blocking capacitor voltage (V_{Cb}) is applied to the transformer primary winding and $I_{\rm pri}$ decreases linearly. In this mode, energy is not transferred from the primary side to the secondary side and output current circulates through the secondary rectifier diodes. S_3 can be turned on with ZVS sometime during this mode.
4) *Mode 4 ($t_3 < t < t_4$):* At the start of this mode, $I_{\rm pri}$ becomes negative and it flows through S_3 and the anti-parallel body diode of S_4. A voltage $-V_{Cb}$ is applied to the transformer primary winding. During this mode, $V_{\rm sec2}$ is positive and equal to the reflected value of V_{Cb}, diode D_2 is conducting, and the output inductor current (I_{Lo}) increases. The energy is transferred from the C_b to the output during this mode.
5) *Mode 5 ($t_4 < t < t_5$):* At the start of this mode, S_1 turns ON. This mode is the same as mode 1.
6) *Mode 6 ($t_5 < t < t_6$):* At the start of this mode, the direction of $I_{\rm pri}$ changes. This mode is the same as mode 2. At the end of this mode S_4 turns OFF and $I_{\rm pri}$ flows through the anti-parallel body diode of S_2.
7) *Mode 7 ($t_6 < t < t_7$):* At the start of this mode, S_2 turns ON with ZVS. The voltage across the V_{AB} is zero; as a result, blocking capacitor voltage (V_{Cb}) is applied to the transformer primary winding and $I_{\rm pri}$ and decreases linearly. In this mode, energy is not transferred from input

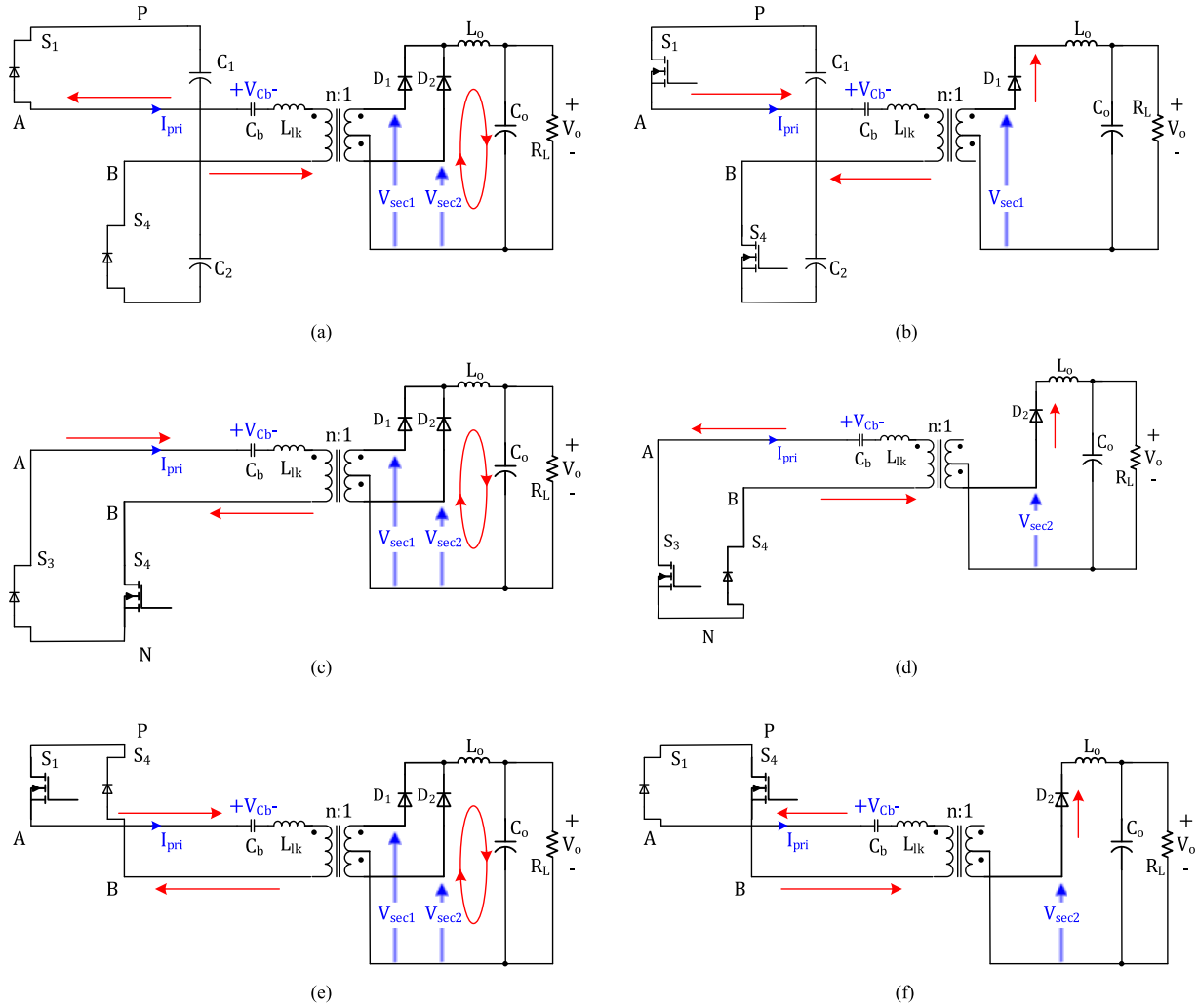

Fig. 7. Modes of operation. (a) Mode 1 ($t_0 < t < t_1$) and Mode 5 ($t_4 < t < t_5$). (b) Mode 2 ($t_1 < t < t_2$) and Mode 6 ($t_5 < t < t_6$). (c) Mode 3 ($t_2 < t < t_3$). (d) Mode 4 ($t_3 < t < t_4$). (e) Mode 7 ($t_6 < t < t_7$). (f) Mode 8 ($t_7 < t < t_8$).

to output and output current circulates through the secondary rectifier diodes.

8) *Mode 8 ($t_7 < t < t_8$):* At the start of this mode, $I_{\rm pri}$ becomes negative and it flows through S_1 and S_3. A voltage of $-V_{Cb}$ is applied to the transformer primary winding. The voltages and currents in the transformer and secondary are the same as in mode 4.

III. Converter Features

The proposed converter has the following features.

1) Any control method used for three phase rectifiers/inverters can be used to operate the proposed converter. Decoupled power control and PWM used in this paper were selected because of their straightforwardness. Other, more complex methods that may result in better performance can be used as well.
2) Only four active switches are used for three-phase ac–dc power conversion with galvanic isolation.
3) The converter can be operated with near unity input power factor.
4) The input current is continuous; thus, the peak current stress of components is not excessive.
5) The converter switches can operate with ZVS.

IV. Converter Control

In the control system used to control the converter, measured line voltages and currents are transformed to the *dq* frame and, because the rotating reference frame is synchronized with the grid frequency, measured parameters are transformed to dc values so that the controller deals with dc values. Current mode control is used; current mode control of four switch inverters in the *dq* frame is comprehensively explained in the literature [23], [24]. The block diagram of the control system is shown in Fig. 8.

Two decoupled loops are used to control the converter input current. A controller is used to control the *d*-axis current based on the load value and another controller sets the *q*-axis current equal to zero to ensure PFC in the converter. Both these current control loops have the same structure. The measured current value is transformed to a synchronous reference frame. The transformed value is compared with a reference value and an error signal is

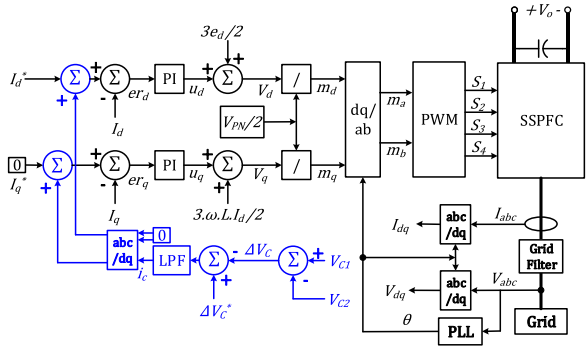

Fig. 8. Control system (voltage balancing control system is in blue).

fed to a proportional integral (PI) controller. Decoupling terms are added to the PI controller output and reference voltages are generated. A *dq*-transformation is then performed according to (13) and a modulation signal is used to generate the switching sequence as shown in Fig. 8 [25]–[32].

As shown in (12) and (13), the dynamics of the current control loop of the proposed converter is the same as conventional four-switch voltage rectifier and the controllers are designed with same procedure; thus, the current controllers can be designed with the same procedure as that shown in [33].

A control loop, shown in blue in the control system block diagram (see Fig. 8), was used to balance the voltages of the dc capacitors; capacitor voltage balancing is discussed in detail in [33]. As a result, the dc component of the voltage of the capacitors is assumed to be identical ($\frac{V_{PN}}{2} = V_{C1} = V_{C2}$) in the modeling process.

It should be noted that there is no novelty in the design of the control in the proposed converter as conventional schemes can be used. This has been confirmed by simulation.

V. Converter Design

In this section, a procedure for the design of the converter is shown and an example is used to demonstrate the design procedure. The example converter is designed based on the following specifications: input voltage $V_{LL} = 120$ V, output voltage $V_o = 48$ V, maximum output power $P_{o,\max} = 1$ kW, and switching frequency $f_{\rm sw} = 50$ kHz. The key parameters values in the design of the converter are dc-bus voltage (V_{PN}), dc blocking capacitor (C_b), switches rms current ($I_{\rm SW\text{-}RMS}$), and transformer turns ratio (n). The values of the dc-bus capacitors and input inductor can be selected based on the procedure that is presented in [4]. The following should be considered in the selection of the abovementioned components.

A. DC Blocking Capacitor C_b

The dc blocking capacitor prevents the transformer from saturation. The value of C_b should be large enough to keep its voltage constant when the direction of the transformer primary current changes because the capacitor should supply the output load during some operation modes. The variation in the voltage across C_b can be expressed as

$$\Delta V_{Cb} = \frac{I_o}{2 \cdot nC_bF_{\rm sw}} \tag{1}$$

where I_o is output current, n is the transformer turns ratio, and $F_{\rm sw}$ is switching frequency. In order to limit ΔV_{Cb} to 10% of dc-bus voltage, a value of $C_b = 1$ μF is chosen.

B. Root Mean Square (RMS) Current of the Switches

The switch rms current consists of two components—ac–dc stage rms current and dc–dc stage rms current. The total rms current can be expressed as

$$I_{\rm rms} = \sqrt{\left(I_{\rm rmsAC-DC}\right)^2 + \left(I_{\rm rmsDC-DC}\right)^2}. \tag{2}$$

The ac–dc converter current is calculated based on the fact that power factor of converter output voltage and current is almost 1 and by applying the method introduced in [34], using

$$I_{\rm rmsAC-DC} = \frac{I_l}{\sqrt{2}} \tag{3}$$

where I_l is the input line current.

The dc–dc converter current component can be calculated based on power transferred to the load. The averaging method can be used to calculate the low frequency component of $I_{\rm pri}$. The secondary current is transferred as a constant current over a switching period to the primary. The transferred current is modulated by the PWM pattern and flows through the converter leg; therefore, the low-frequency component of the current is a sinusoidal current. The reflected current from the secondary is equal to $\frac{I_o}{n}$. The average value of the switch duty cycle for a line cycle can be expressed as

$$D_{\rm av} = \frac{1}{T}\int_0^T \left| M \cdot \sin\left(\omega.\tau + \frac{\pi}{6} + \varphi\right)\right| d\tau = \frac{2M}{\pi}. \tag{4}$$

The rms value of the current can be calculated from (4)

$$I_{\rm rmsDC-DC} = \frac{1}{T_s}\int_0^{D_{\rm av}T_s} \sqrt{\left(\frac{I_o}{n}\right)^2} dt = \sqrt{\frac{2M}{\pi}}\frac{I_o}{n}. \tag{5}$$

The total $I_{\rm rms}$ for the switches is equal to 7.5 A. It should be noted that this is an initial approximation.

A good approximation of switch peak current is when the ac–dc sub-converter and dc–dc sub-converter operates at maximum current and both the current are added up. The switch current stress can be expressed as

$$I_{\rm sw-max} = |I_{\rm AC-DC} + I_{\rm DC-DC}| = P_{\rm out}\left(\frac{2}{3\hat{e}} + \frac{1}{nV_o}\right) \tag{6}$$

where $\hat{e}$ is the peak input line-to-neutral voltage. The switch current stress from (6) is 15.13 A.

C. Transformer Turns Ratio (n)

Under steady-state conditions, the power delivered by the input should match the power absorbed by the output. In the proposed converter, the input power is controlled by the control variable I_d that is associated with the magnitude of the input current and output power is associated with the output voltage.

The output voltage is a function of the duty cycle of the switches, dc-bus voltage, and n. In single stage converters, the dc-bus voltage is a function of duty cycle and n; thus, it cannot be used as an independent control variable to balance the energy in

the converter. In the proposed converter, *n* should be selected as a coarse-tuning control parameter and modulation index should be used as a fine-tuning control parameter for the output voltage and thus the output power.

In this section, the output voltage relation is developed as a function of transformer turns ratio (n) and the load resistance (R_L). A value of *n* is selected based on the range of output voltage and load resistance variations. The value of *n* must be such that it can ensure that the converter's input power can be made equal to the output power for a particular modulation index. Since the same modulation index is applied to both the ac–dc and the dc–dc converter sections, a value of *n* should be selected such that V_o is equal to 48 V.

Based on this explanation

$$P_{\text{in}} = \frac{3}{2} e I_d = \frac{V_o^2}{R_L} = P_{\text{out}}. \tag{7}$$

To determine the transformer turns ratio, a relationship between V_o and V_{PN} needs to be determined. A state-space equation of the converter can be written and a steady-state model for the converter can be developed with the following considerations.

Remark 1: The converter components are assumed ideal. For the purpose of modeling the converter at the line frequency, high switching frequency components are ignored. The loading effect of the dc–dc power conversion is modeled as a constant load in the dc bus.

Remark 2: The grid voltages are defined as follows:

$$\begin{bmatrix} e_a(t) \\ e_b(t) \\ e_c(t) \end{bmatrix} = \begin{bmatrix} \hat{e} \cdot \cos(\omega t) \\ \hat{e} \cdot \cos\left(\omega t - \frac{2.\pi}{3}\right) \\ \hat{e} \cdot \cos\left(\omega t + \frac{2.\pi}{3}\right) \end{bmatrix}. \tag{8}$$

Remark 3: The power transfers from the grid to the converter occurs at power system frequency so that ac–dc converter operation is explained based on the low-frequency model.

As demonstrated in [4], assuming balanced voltage and current operation, converter, the following state-space equations can be written:

$$\frac{di_a}{dt} = -\frac{R}{L} i_a + \left(\frac{-2S_a + S_b}{3L}\right) v_{C1} + \left(\frac{-2S_a + S_b + 1}{3L}\right) v_{C2} + \frac{e_a(t)}{L} \tag{9}$$

$$\frac{di_b}{dt} = -\frac{R}{L} i_b + \left(\frac{S_a - 2S_b}{3L}\right) v_{C1} + \left(\frac{S_a - 2S_b + 1}{3L}\right) v_{C2} + \frac{e_b(t)}{L} \tag{10}$$

$$\frac{di_c}{dt} = -\frac{R}{L} i_c + \frac{2S_a}{3L} v_{C1} + \left(\frac{S_a + S_b - 2}{3L}\right) v_{C2} + \frac{e_c(t)}{L} \tag{11}$$

$$C\frac{dv_{PN}}{dt} = 2S_a i_a + 2S_b i_b + i_c - \frac{2P_{\text{out}}}{V_{PN}^2} \tag{12}$$

where R is the inductor resistance, P_{out} is the output power, and S_a and S_b are the switching functions of the legs that are connected to phase "A" and "B," respectively, and defined as

$$S_j = \begin{cases} 1 & \text{Upper switch is close} \\ 0 & \text{Lower switch is close} \end{cases} \quad j \in a,\ b.$$

Applying averaging method shown in [35] to (8) to (11) and using the Park transformation, the average state space equations for currents of the ac–dc converter can be written in the *dq* frame as

$$L\frac{di_d}{dt} = -Ri_d - L\omega i_q - \frac{V_{PN}}{3} m_d + e_d \tag{13}$$

$$L\frac{di_q}{dt} = -Ri_q + \omega L i_d - \frac{V_{PN}}{3} m_q \tag{14}$$

where m_d and m_q are the average values of S_a and S_b that are transferred to *dq* frame.

The ac–dc converter works as an ideal rectifier so that current and voltage should be in phase; if the *d*-axis is aligned with the phase "A" voltage, then the current and voltage at the *q*-axis is zero and $e_d = \hat{e}$, the peak input line-to-neutral voltage. Considering this condition, the steady-state converter state-space equations can be expressed as

$$\hat{e} = -RI_d - \frac{V_{PN}}{3} m_d \tag{15}$$

$$\omega I_d = \frac{V_{PN}}{3L} m_q. \tag{16}$$

The value of the modulation indices in the *dq* reference frame (M_d and M_q) from the (7) and (8) results in

$$m_d = \frac{3(\hat{e} - R \cdot I_d)}{V_{PN}} \tag{17}$$

$$m_q = \frac{3 \cdot \omega \cdot L \cdot I_d}{V_{PN}}. \tag{18}$$

The modulation signals for the legs are calculated by using an inverse reduced Park transform that is an upper-left 2 by 2 Park transform matrix T_R^{-1} as shown here

$$T_R^{-1} = \frac{2}{\sqrt{3}} \begin{bmatrix} -\cos\left(\omega t + \frac{\pi}{3}\right) & \sin\left(\omega t + \frac{\pi}{3}\right) \\ -\cos(\omega t) & \sin(\omega t) \end{bmatrix} \tag{19}$$

$$\begin{bmatrix} m_a \\ m_b \end{bmatrix} = T_R^{-1} \cdot \begin{bmatrix} m_d \\ m_q \end{bmatrix}. \tag{20}$$

The modulation signals for the legs can be expressed as

$$\begin{bmatrix} m_a \\ m_b \end{bmatrix} = \begin{bmatrix} M\cos\left(\omega.t - \frac{\pi}{6} + \varphi\right) \\ M\cos\left(\omega.t - \frac{\pi}{2} + \varphi\right) \end{bmatrix} \tag{21}$$

and the modulation signal parameters, including modulation index *M* and phase shift φ can be expressed as

$$M = \frac{2\sqrt{3}}{V_{PN}} \sqrt{(\hat{e} - R.I_d)^2 + (\omega L I_d)^2} \tag{22}$$

$$\varphi = \tan^{-1} \frac{\omega L I_d}{\hat{e} - R.I_d}. \tag{23}$$

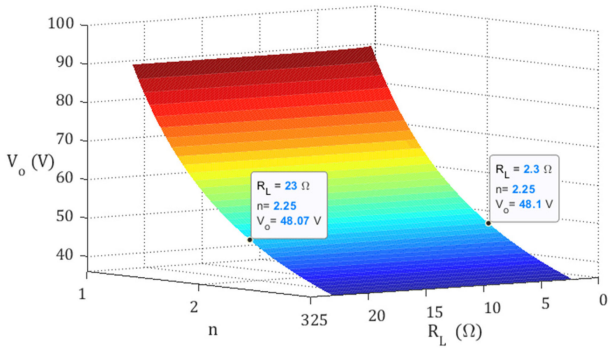

Fig. 9. Output voltage variation with respect to the R_L (x-axis) and transformers turns ratio (y-axis).

Since the dc–dc stage operates with same PWM pattern that is generated with respect to (16), the output voltage of the proposed converter can be expressed as

$$V_o = \frac{V_{PN}\cdot\omega}{2\cdot n\cdot\pi}\int_T^{T+\frac{\pi}{\omega}} \left|m_a(\tau) - m_b(\tau)\right| d\tau = \frac{V_{PN}\cdot M}{n\cdot\pi}. \tag{24}$$

Combining (17) and (19), the output voltage can be expressed as a function of I_d as follows:

$$V_o = \frac{2\sqrt{3}\cdot\sqrt{(\hat{e} - R.I_d)^2 + (\omega L I_d)^2}}{n.\pi} \tag{25}$$

where n is the transformer turns ratio.

By calculating I_d from (25) and plugging in (22), the value of V_o for steady-state operation can be expressed as

$$V_o = \frac{\sqrt{3}\hat{e}\sqrt{2(R_L n\pi)^2 - 2\sqrt{(R_L n\pi)^4 - 256(R_L\omega L)^2}}}{8\omega L} \tag{26}$$

n can be then selected based on (26). It should be mentioned that R, which is the internal resistance of an input inductor, is neglected in (26). Fig. 9 shows the variation of output voltage with respect to R_L and n. As shown in Fig. 11 the value of $n = 2.25$ and the load variation from 10% to 100% does not change the energy equilibrium point considerably.

D. DC-Bus Voltage

The dc-bus voltage should be sufficiently large to ensure that there is sufficient output voltage when the converter operates at full load condition [36]. The minimum value of the dc-bus voltage for a four-switch rectifier in general should be

$$2\sqrt{3}\hat{e} < V_{PN} \tag{27}$$

where $\hat{e}$ represents the peak value of the grid line-to-neutral voltage.

The intermediate dc-bus voltage in SSPFCs is not controlled and is dependent on the energy balance between power from the input and power transferred to the output under steady-state conditions. The maximum value of the intermediate dc-bus voltage is thus used to determine the voltage rating of dc-bus capacitors. The dc-bus voltage equation for the low-frequency model is shown in (3). In this part, the constant power model is replaced by a more precise model for the dc–dc stage to calculate the intermediate dc-bus current and voltage.

Power transfer from the intermediate dc-bus capacitors to the output occurs during a switching cycle, and the switches' duty ratio varies with a low frequency (60 Hz) so that the conventional averaging method cannot be used. A method presented in [19] is used instead in this paper to determine dc-bus voltage variations based on output power variations. The method is based on the multi-frequency averaging method that was introduced in [37] that considers the variation of the switches' duty ratio and can be used in this paper to calculate the power transfer in the dc–dc stage.

The power that is transferred to the output can be expressed as

$$P_{\text{out}} = \frac{V_o^2}{R_L} = \langle v_{AB}\rangle_1 \langle I_{\text{pri}}\rangle_1 \tag{28}$$

where $\langle x\rangle_k$ shows the kth coefficient of Fourier series of parameter x as defined in [37]. It should be mentioned that blocking capacitor (C_b) blocks the dc component (index-0) of the current. Since the ac component of V_{PN} is much smaller than the dc component of V_{PN}, (28) can be simplified to be

$$P_{\text{out}} = \frac{V_o^2}{R_L} = V_{PN}\langle S_a - S_b\rangle_1 \langle I_{\text{pri}}\rangle_1. \tag{29}$$

Considering (29) and (12), the first coefficient of Fourier series for the intermediate dc bus can be expressed as

$$\left\langle C\frac{dV_{PN}}{dt}\right\rangle_1 = \langle 2S_a - 1\rangle_1 i_a + \langle 2S_b - 1\rangle_1 i_b + 2\langle S_b - S_a\rangle_0 \langle I_{\text{pri}}\rangle_1. \tag{30}$$

$\langle I_{\text{pri}}\rangle_1$ for a typical switching period can be determined to be

$$\langle I_{pri}\rangle_1 = \frac{\langle 2S_a - 1\rangle_1 i_a + \langle 2S_b - 1\rangle_1 i_b - \left\langle C\frac{\Delta\times V_{PN}}{T_s}\right\rangle_1}{-2(d_b - d_a)} \tag{31}$$

where $\Delta \times V_{PN}$ is the variation of the dc-bus voltage in each switching cycle due to current that passes through the capacitors; d_b and d_a are the duty-ratios of S_1 and S_2 as shown in Fig. 6. Substituting (31) into (29), the equation of steady-state operation for intermediate dc-bus voltage can be written as

$$V_{PN}^2\frac{\Delta\langle S_a - S_b\rangle_1}{-2T_s(d_b - d_a)} + V_{PN}\frac{\langle 2S_a - 1\rangle_1 i_a + \langle 2S_b - 1\rangle_1 i_b}{-2(d_b - d_a)} - P_{\text{out}} = 0. \tag{32}$$

The first Fourier series coefficient of the switching functions can be determined from the complex Fourier transform definition in [37] and can be written as

$$\langle S_i\rangle_1 = \frac{1}{T}\int_{t-T}^{t} S_i(\tau)\, e^{-j\omega_s\tau} d\tau \quad i \in a, b. \tag{33}$$

The switching functions are shown in Fig. 6. Considering the integration period from one of the positive peaks of the carrier

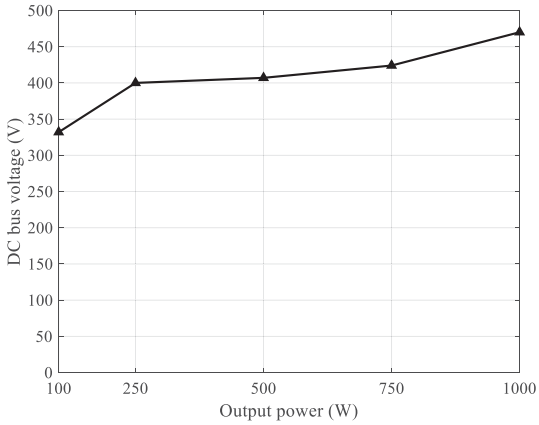

Fig. 10. Maximum dc-bus voltage.

waveform up to the next positive peak, (33) can be solved and the result can be expressed as

$$\langle S_i \rangle_1 = \frac{-1}{\pi} \sin(d_i \pi) \qquad i \in a, b \tag{34}$$

with the value of $\langle S_i \rangle_1$ beings a real value. By replacing (34) in (32), a second-order linear equation can be derived in terms of V_{PN} and then used to plot the dc-bus voltage variation as shown in Fig. 10. i_a and i_b are the phase current magnitudes and d_a and d_b are limited between 0 and 1.

The dc-bus voltage in the proposed converter is not fixed as it is in a two-stage converter because the converter is a single-stage converter that has just a single controller that is used to regulate the output voltage. This voltage is dependent on the energy equilibrium that exists between the energy that is fed to the dc bus from the input and the energy that is transferred from the dc bus to the output.

The proposed converter has the characteristic that its dc-bus voltage rises as its load increases; the converter presented in [19] has the same characteristic. This characteristic differs from what is typically found in most other single-controller, single-stage ac–dc converters. This is because for both the proposed converter and the converter in [19], the difference in the PWM pattern that produces V_A and V_B at both ends of the transformer, V_{AB}, becomes smaller so that V_{AB} is zero more often, which results in less opportunity for energy to be transferred from the dc bus to the output, which affects the dc bus energy equilibrium so that the dc-bus voltage is increased. This characteristic is actually advantageous because issues with high dc-bus voltage are only encountered during heavy load operation and the load can be limited, whereas in most other single-stage converters, these issues are encountered when the converter operates with light loads, which is generally unavoidable unless the load is fixed.

It should be noted that the dc-bus voltage is the peak switch voltage stress.

E. ZVS Range

To achieve ZVS in the converter switches as discussed in Section II-B, the magnitude of the dc–dc converter current

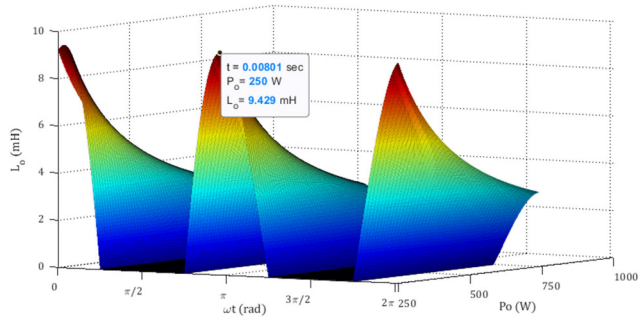

Fig. 11. Minimum value of L to achieve ZVS.

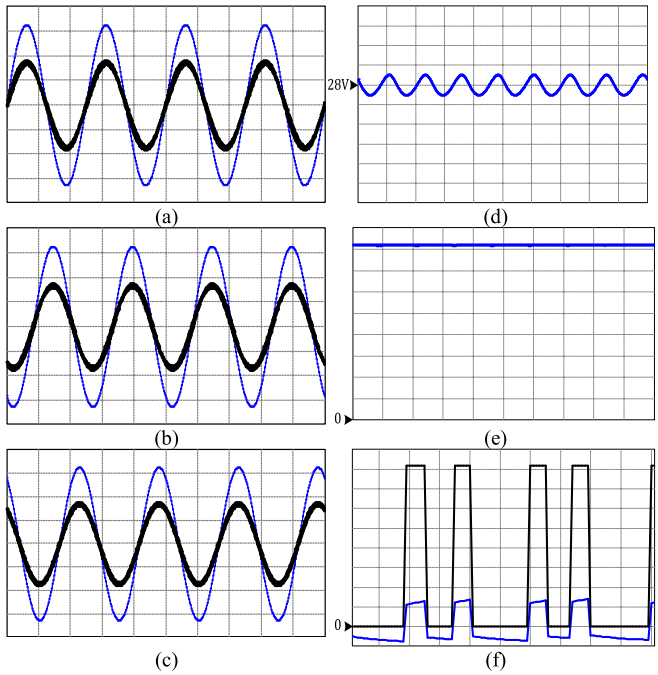

Fig. 12. Simulated converter waveforms. (a) Phase A voltage and current (I: 10 A/div., V: 100 V/div., t: 1 ms/div.). (b) Phase B voltage and current (I: 10 A/div., V: 100 V/div., t: 1 ms/div.). (c) Phase C voltage and current (I: 10 A/div., V: 100 V/div., t: 1 ms/div.). (d) Output voltage (V: 0.5 V/div., t: 1 ms/div.). (e) V_{PN} (V: 100 V/div., t: 1 ms/div.). (f) V_{AB} and $I_{\rm pri}$ (V: 100 V/div., I:10 A/div., t: 5 μs/div.)

component should be larger than the ac–dc converter current component over the ac line cycle

$$|I_{\rm DC-DC}| > |I_{\rm AC-DC}|. \tag{35}$$

The magnitude of the dc–dc converter can be expressed as

$$|I_{\rm DC-DC}| = \frac{I_{LO}}{n} \tag{36}$$

so that the magnitude of the primary current of the dc–dc converter is equal to I_{LO}. I_{LO} can be approximated by a dc current that is the sum of the load current and a component with double frequency (120 Hz). Neglecting the voltage drop across the input filter at line frequency, I_{LO} can be expressed as [22]

$$I_{LO} = \frac{P_o}{V_o} - \frac{\sqrt{3} e_a}{3\pi\omega L_O} \cos(2\omega t) \tag{37}$$

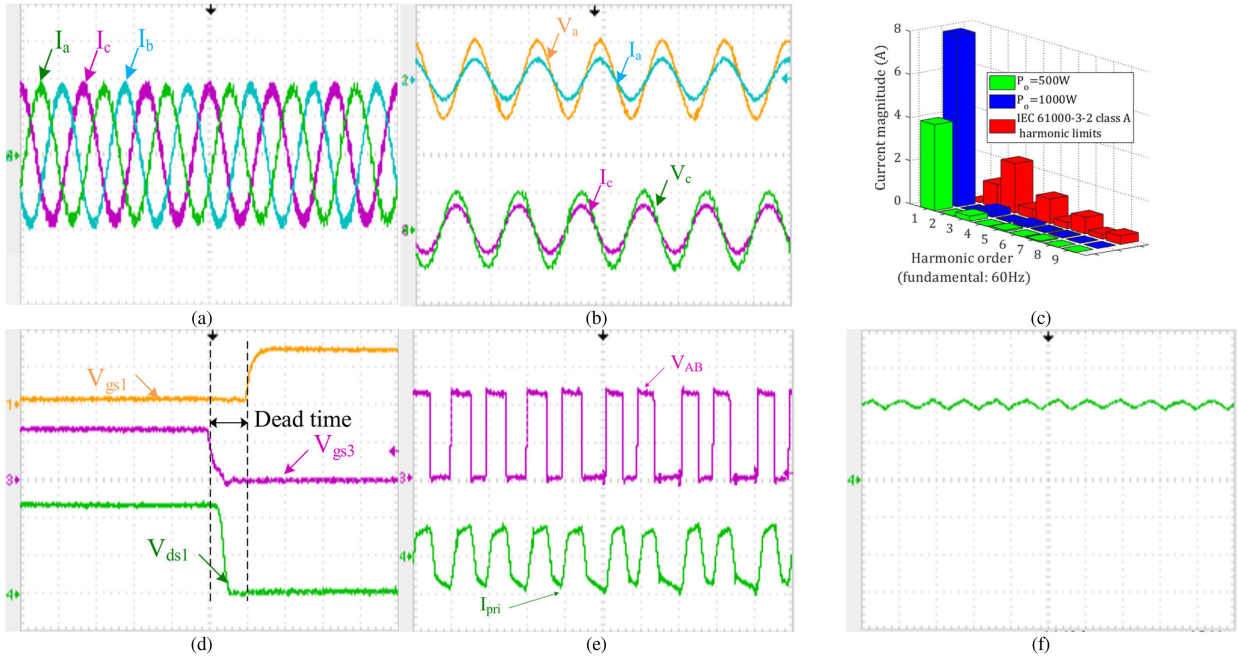

Fig. 13. Typical converter waveforms. (a) Three phase input currents (*I*: 5 A/div, *t*: 10 ms/div.). (b) Phases A and C voltage and current (*I*: 10 A/div., *V*: 100 V/div., *t*: 10 ms/div.) (c) Harmonic contents of phase A at full load and current and IEC61000-3-2 harmonic limits for class A equipment. (d) S_1 and S_2 gate source voltage (*V*: 10 V/div., *t*: 500 ns/div.), and S_1 drain source voltage (*V*: 200 V/div., *t*: 500 ns/div.). (e) V_{AB} and *I*pri (*V*: 200 V/div., *I*: 10 A/div, *t*:10 μs/div.). (f) Output current (*I*: 10 A/div., *t*: 10 ms/div.)

where $\omega = 2\pi 60$, and P_o is the output power. The ac–dc sub-converter current can be calculated as

$$I_{\mathrm{AC-DC}} = \frac{\sqrt{2}P_o/\eta}{3e_a}\sin(\omega t)\,. \tag{38}$$

Combining (35) and (38) and rearranging the result results in

$$L_o \geq -\frac{\sqrt{3}e_a^2\cos(2\omega t)\,V_o}{\pi P_o\omega\left(\sqrt{2}\sin(\omega t)\;\; V_o\eta n - 3e_a\right)} \tag{39}$$

where $0 \leq t \leq 1/f_{\mathrm{line}}$.

The positive part of the right-hand side of (39) is plotted in Fig. 11 with respect to time and output power. As shown in Fig. 11, the upper limit of the right side of (39) occurs at minimum output power. The value of L_o needed to achieve ZVS in the proposed converter can then be selected based on the upper limit. It means such other converters the minimum load is the key factor to select L_o. In order to achieve ZVS in the converter switches for at least 25% of the nominal full load, the value of L_o is chosen to be 9.4 mH.

VI. Simulation and Experimental Results

The output inductor value that was derived in the following section is generally considered to be very high for most applications. This inductor has a high value because of the converter has a large low-frequency component (2×60 Hz $= 120$ Hz) at its output as the transformer primary voltage varies with the input line cycle. This makes the proposed converter most suitable for applications, such as aerospace like the converter proposed in [19] where the input line frequency is 400 Hz, which results in less current ripple and thus less inductance at the output or for applications where the converter's output is connected to a battery, such as a battery charger or a telecom power system with battery backup.

In order to see how the proposed converter would work with a 400 Hz input voltage supply, computer simulations were performed using PSIM software. The converter was simulated with the following parameters, which were almost the same as those used in [19]: Input voltage $V_{LL} = 115$ V, $f = 400$ Hz, output voltage $V_o = 28$ V, maximum output power $P_{o,\max} = 2$ kW and switching frequency $f_{\mathrm{sw}} = 50$ kHz. The input inductors were 1.2 mH, $C_b = 180$ nF and $L_r = 2$ μH, and the transformer turns ratio was 8:1, The values of L_o and C_o values were $L_o = 800$ μH, and $C_o = 3000$ μF. It should be noted that the value of L_o is much smaller than it would be if the converter was implemented with 60 Hz input frequency.

Fig. 12 shows typical waveforms of the simulated converter. The phase currents and phase voltages for phases A, B, and C are shown in Fig. 12(a)–(c). It can be seen that the input current is continuous and in phase with input voltage for all phases. Fig. 12(d) shows the output voltage; it can be seen that output voltage is 28 V with an 800 Hz (twice the line frequency) ripple. Voltage V_{PN} is shown in Fig. 12(e); it is an 800 V dc voltage. Fig. 12(f) shows V_{AB}, the voltage across the transformer primary and blocking capacitor, and the primary current I_{pri}; it can be seen that they are square waveforms that are similar to what can be found in a typical dc–dc PWM full-bridge converter. The dc component of the voltage waveform can be removed by the blocking capacitor.

A simple proof-of-concept prototype of the proposed converter was built to verify its feasibility. The following specifications are used to build the prototype: Input voltage $V_{LL} =$

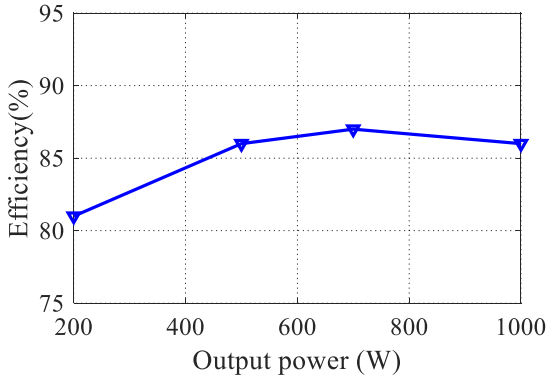

Fig. 14. Converter efficiency.

120 V, output voltage $V_o = 48$ V, maximum output power $P_{o,\max} = 1$ kW and switching frequency $f_{\rm sw} = 50$ kHz. The devices used for switches S_1–S_4 were FCA20N60 MOSFETs, D_1–D_2 and RURG3060 devices were used for the output rectifying diodes. The input inductors were 1.2 mH, $C_b = 1$ μF and $L_r = 5.5$ μH, and the transformer turns ratio was 2:1, L_o and C_o values were $L_o = 9$ mH, and $C_o = 4700$ μF. The converter was implemented with the decoupled power flow control method and with conventional SPWM, using a TMS320F28069M DSP.

Fig. 13 shows typical converter waveforms at full load. The three phase input currents are shown in Fig. 13(a) and two phase currents and voltages (phases A and C in Fig. 2) are shown in Fig. 13(b). As can be seen, the three-phase input currents are all sinusoidal and in phase with the input voltage. The harmonic contents of the input current for a typical phase (phase A) is shown in Fig. 13(c) for full load and half load. It can be seen that the harmonics are lower than the limits specified by the IEC61000-3-2 Class A standard; moreover, the power factor was about 0.99 for full load and half load. A typical waveform of the voltage across a switch (S_1) is shown along with its gate source voltage and complementary switch gate source voltage in Fig. 13(d). It can be seen that it is similar to a switch voltage waveform commonly seen in a dc–dc full-bridge converter; also, after S_3 turns OFF, the primary current discharges the output capacitance of S_1 during the dead-time and S_1 turns ON with ZVS. Voltage V_{AB}, the voltage across the transformer primary and blocking capacitor, and $I_{\rm pri}$ are shown in Fig. 13(e). It can be seen that the waveforms are similar to what can be found in a typical dc–dc PWM full-bridge converter. The output rectifier current is shown in Fig. 13(f); it can be seen that it is a dc current with a 120 Hz ripple. The 120 Hz ripple is due to the change in duty cycle over a line cycle; however, C_b attenuates the low-frequency components of the voltage that is applied to the transformer primary winding so that the transformer does not saturate.

Fig. 14 shows a graph of curves of efficiency versus output load for the proposed converter. A maximum efficiency of about 87% was obtained for the converter prototype. It should be noted that an efficiency of 98% was reported for the three-phase six-switch single-stage converter in [19], which used SiC devices and output synchronous rectifiers. A higher efficiency can be obtained for the proposed converter if a similar implementation is used.

VII. Conclusion

A new three-phase, four-switch ac–dc converter with transformer isolation was proposed in this paper. In this paper, the converter's general operation and its modes of the operation were explained in detail, a steady-state mathematical model of the converter was derived, a design procedure of the converter was developed and demonstrated with a design example, and experimental results from a simple proof-of-concept prototype were presented in Section V.

The outstanding features of the proposed converter are that it has only four switches in its topology, it is bridgeless, its input currents are continuous, and it can be implemented with any control method used in standard three-phase, six-switch VSRs. Its main drawbacks are that it has a significant low-frequency ripple and a dc-bus voltage that increases as its load increases. The first drawback is not an issue if the converter is used in aerospace applications where three-phase 400 Hz ac voltage supplies are used or in applications where the converter's output is connected to a battery, such as a battery charger or a telecom power system with battery backup. The second drawback is more significant as it increases component stress and limits the load range of the converter to 2–3 kW if 1200 V devices are used, a load range that is the maximum on most other three-phase single-stage converters.

In essence, the proposed converter does away with issues caused by discontinuous input currents with high peaks, such as high current stresses, turn-OFF losses, and noise that typically place limitations on three-phase single-stage converters, but places high voltage stress on its components. Nonetheless, the proposed converter has fewer semiconductors than any other topology of its kind and is thus the simplest and least expensive three-phase single-stage ac–dc converters with galvanic isolation in existence.

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