Single-Phase Split-Inductor Differential Boost Inverters

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***Abstract*—In this paper, two single-phase single-stage split-inductor buck–boost inverters are proposed: type-I and II. The proposed type-I is unity power factor inverter, while the proposed type-II inverter is suitable for any power factor. Both topologies remove the shoot-through problem. Furthermore, the reverse recovery issues for all switches are eliminated; therefore, MOSFETs are used to obtain higher efficiencies. The proposed inverters operated at higher switching frequencies confer the additional benefit of smaller passive components. The current stresses of the two switches in the proposed type-I and II inverters are lower of the conventional boost inverter. The dead time can be eliminated at both the high and line switching frequencies. In addition, the inductor conduction loss is minimized to improve efficiency. Moreover, the voltage stresses of the two switches in the type-I inverter can be much lower of its counterpart boost inverter. Most importantly, unlike the conventional high-reliability inverters, the magnetic volume of the proposed high-reliability type-I and II inverters is same of its counterpart boost inverter. The experimental results obtained for 500 W, 110 Vrms, 60 Hz hardware prototypes verify the analysis.**

***Index Terms*—Buck–boost inverter, efficiency, low current stress, low-voltage stress, magnetic volume, reliability, single stage, split inductor.**

I. Introduction

APPLICATIONS such as photovoltaic, uninterruptible power supplies and small wind turbines need buck–boost inverters (BBI). A typical BBI has two-stage power conversion, a boost dc–dc and buck dc–ac. They are time tested and work well. The disadvantage of the multistage BBIs is that more power components are required. BBIs providing buck–boost operation in a single stage can obtain higher power density [1], [2].

The Z-source [3] and quasi-Z-source inverters [4] containing impedance network (*LC*) provide buck–boost function by

Manuscript received November 9, 2018; revised February 11, 2019; accepted March 31, 2019. Date of publication April 28, 2019; date of current version October 18, 2019. This work was supported by the Natural Sciences and Engineering Research Council of Canada. Recommended for publication by Associate Editor Y. Xing. *(Corresponding author: Ashraf Ali Khan.)*

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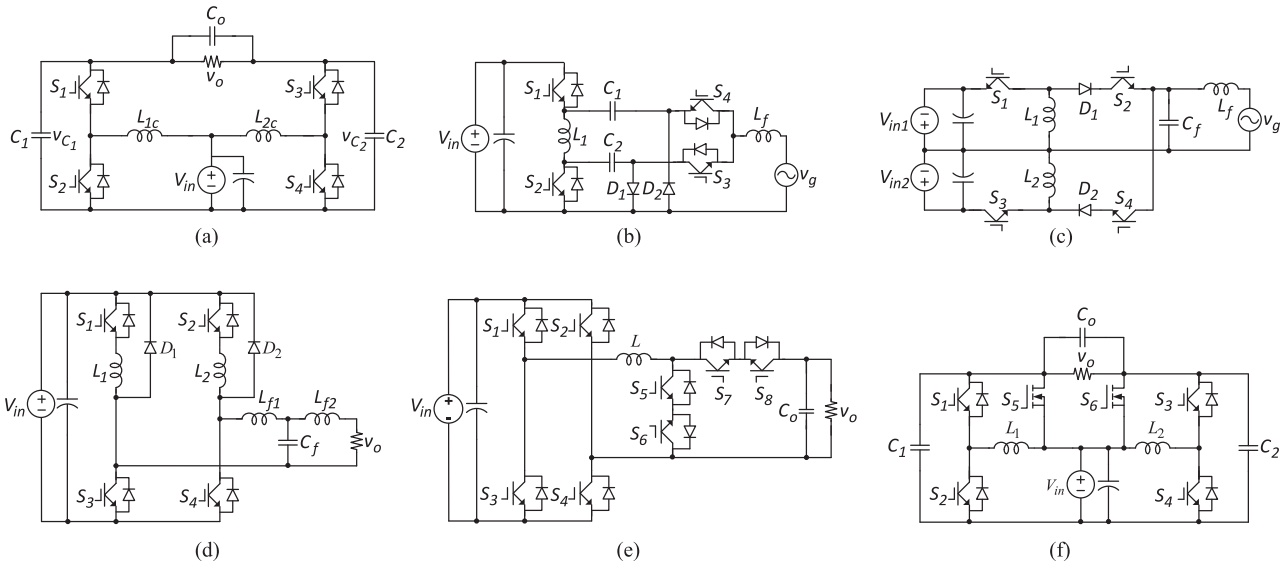

Fig. 1. Conventional single-stage buck–boost inverters. (a) [7]. (b) [8]. (c) [9]. (d) [10]. (e) [5] and [6]. (f) [12].

the conventional DBI. In [13] and [14], single-stage inverters with common ground are presented to decrease the common mode leakage current.

Each of the aforementioned inverters has its own advantages and disadvantages, but the following issues are common to most of them.

1) Shoot-through problem, which is a major reliability issue. To avoid it, dead time is set in the switching signals. For example, the inverter in Fig. 1(f) has shoot-through risk of C_1, C_2, and C_o. To avoid the shoot through, dead time should be inserted between S_1 and S_2, S_3 and S_4, and S_5 and S_6. The dead time reduces voltage gain and causes waveforms distortion and less energy transfer. This drawback becomes more severe as the inverter switching and fundamental frequencies are increased.
2) The high-frequency switches of single-stage BBIs cannot be simply implemented with power MOSFETs because of slow reverse recovery features of MOSFET body diode. The slow reverse recovery induces large turn ON loss and leads to reliability and EMI concerns [15]–[17]. To minimize the reverse recovery issues, insulated gate bipolar junction transistors (IGBTs) can be used. However, compared to IGBT, MOSFET has fast switching, low switching loss, and resistive conduction voltage drop features. The resistive voltage drop becomes lower as the power level decreases.

The single-phase dual-buck inverters [18]– [22], [32], three-phase buck inverter [23], cascaded inverters [24], [25], BBI [26], single-phase ac–ac converters [27], [28], three-phase ac–ac converters [29], cascaded ac–ac converters [30], and neutral point clamped inverter (NPCI) [31] are proposed to realize high reliability and efficiency. All these converters have no shoot-through problem and they use MOSFETs without reverse recovery issues to improve efficiency and increase switching frequencies. However, they have a major drawback of high magnetic volume compared to their counterpart traditional converters. The magnetic volumes of the dual-buck inverter [19], dual-paralleled-buck inverter [32], and inverters in [21] and [23] can be as high as twice of their counterpart H-bridge inverter. The magnetic volume of the split inductor NPCI [31] is twice of its counterpart traditional NPCI.

The BBI in [26] has no shoot-through problem. However, it requires six inductors and its magnetic volume is higher of the proposed inverter. In addition, it requires more diodes, and the voltage stress of its switches is higher than the proposed type-I inverter. Furthermore, its inductor conduction loss is higher and efficiency is lower than the proposed inverter. Moreover, its circuit layout is complex and requires more footprints. In summary, the aforementioned inverters [18]–[32] provide high reliability and efficiency at the cost of high magnetic volume.

In this paper, type-I and II single-phase single-stage split-inductor BBIs are introduced. They completely remove the shoot-through problem experienced by the BBIs in Fig. 1. Furthermore, MOSFETs can be utilized in the proposed inverters to boost efficiency since the topologies inherently eliminate the reverse recovery loss of the body diodes. The proposed inverters can operate at higher switching frequencies, which allows the reduction of passive components.

In addition, the proposed type-I inverter has the following advantages.

1) Two switches are line frequency.
2) Dead time can be eliminated.
3) The voltage stresses of the two switches S_1 and S_3 can be much lower.
4) The current stresses of the two switches S_1 and S_3 can be much lower.
5) The inductor conduction loss is lower.
6) The magnetic volume is same of its counterpart as DBI.

The proposed type-II inverter has many advantages of the type-I inverter such as no shoot-through issue, no dead-time requirements, lower current stress of two switches and same

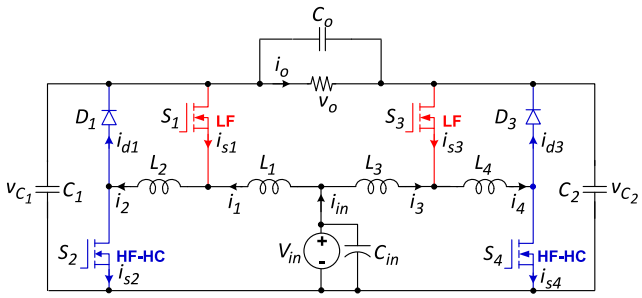

Fig. 2. Proposed type-I inverter.

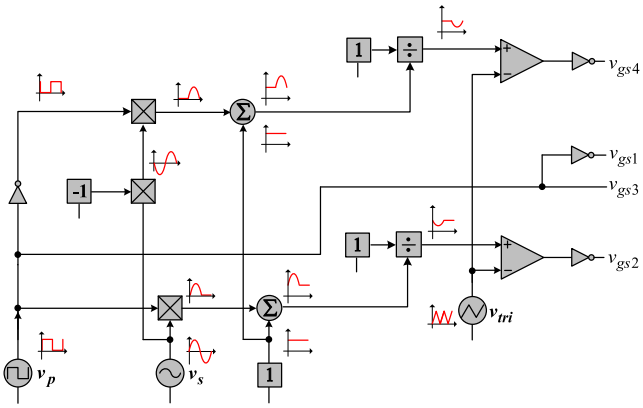

Fig. 3. Control signals generation of the type-I inverter.

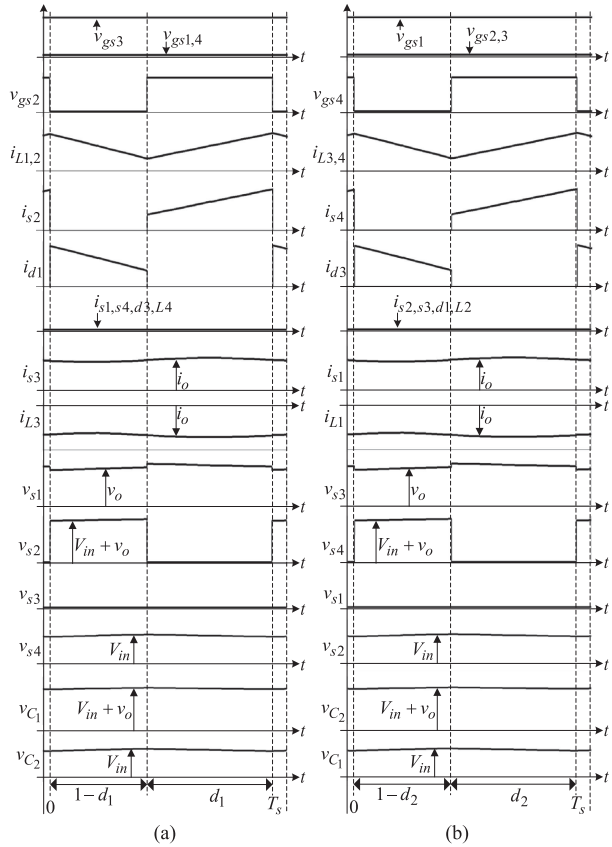

Fig. 4. Waveforms of the proposed type-I inverter. (a) $v_o > 0$. (b) $v_o < 0$.

magnetic volume as of its counterpart DBI. In addition, it offers reactive power flow operation.

II. Proposed Topologies and Operation Analysis

A. Type-I Inverter

Fig. 2 shows the proposed type-I inverter for unity power factor operation. It has four inductors $L_1 - L_4$, two diodes D_1, D_3, four switches $S_1 - S_4$, and two capacitors C_1 and C_2. An input capacitor $C_{\rm in}$ can be used to alleviate the input current ripple. The inductors are configured to prevent the shoot through and work as boosting inductors. The main switches are S_2 and S_4, and S_1 and S_3 are added to freewheel output current i_o. The body diodes of MOSFETs in the type-I inverter never conduct, thus, inherently eliminating their reverse recovery issues.

The control signals generation of the type-I inverter is shown in Fig. 3. To obtain the control signal of S_2, a sinusoidal signal $v_s = G\sin(2\pi ft)$ is multiplied with in-phase line-frequency rectangular signal v_p. v_p has an amplitude 1, dc offset 0.5, duty cycle 0.5, and frequency f. G is the output voltage gain of the inverter and f is line frequency. The resulting half-sinusoidal signal is then added with a constant of a value of 1. Finally, the inverse of the dc-biased-half-sinusoidal signal is compared with a triangular carrier signal $v_{\rm tri}$. Similarly, to generate v_{gs4}, $-v_s$ is multiplied with an inverted v_p. The half-sinusoidal signal is summed with a constant 1. The inverse of the dc-biased-half-sinusoidal signal is compared with $v_{\rm tri}$. The switch S_1 and S_3 operate at line frequency.

B. Operation of the Type-I Inverter

Dead times in the switching signals of the type-I inverter can be completely removed. Theoretical waveforms of the type-I inverter are given in Fig. 4. d_1 and d_2 are the duty cycles of S_2 and S_4, respectively. $i_{d1,d3}$, i_{s1-s4}, and i_{L1-L4} are the diode, switch and inductor currents defined in Fig. 2. v_{C_1} and v_{C_2} are the voltages of C_1 and C_2, respectively.

For $v_o > 0$, S_3 is ON, S_1 and S_4 are OFF, D_3 is reverse biased, L_4 does not conduct and L_3 freewheels i_o. In a switching period, the inverter has two states.

1) *Active state:* As shown in Fig. 5(a), S_2 is ON and L_1 and L_2 store energy.
2) *Freewheeling state:* As shown in Fig. 5(b), S_2 is OFF, D_1 is forward biased and L_1 and L_2 release the stored energy.

For $v_o < 0$, S_1 is ON, S_2 and S_3 are OFF, D_1 is reverse biased, L_2 does not conduct and L_1 freewheels i_o. The switching states are as follows.

1) *Active state:* As shown in Fig. 6(a), S_4 is ON, D_3 is reverse biased and L_3 and L_4 store energy.
2) *Freewheeling state:* As shown in Fig. 6(b), S_4 is OFF, D_3 is forward biased and L_3 and L_4 release the stored energy.

C. Type-II Inverter

Fig. 7 shows the proposed type-II inverter. It can provide reactive power. Compared to the type-I inverter, the type-II inverter requires two more diodes D_2 and D_4.

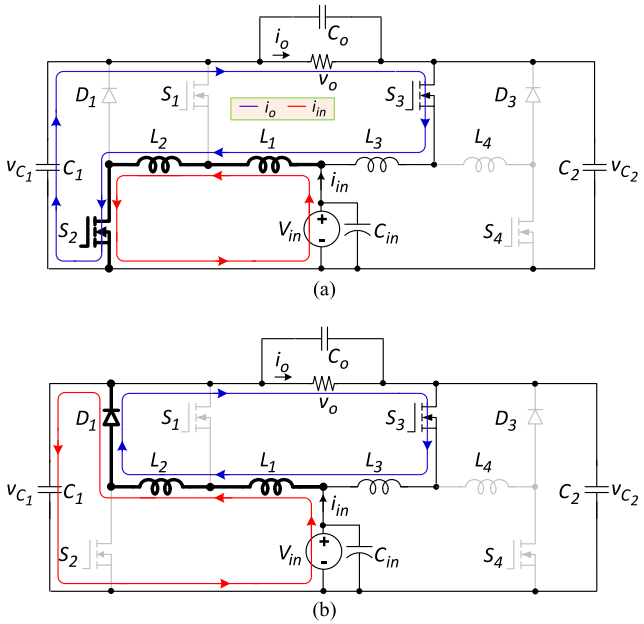

Fig. 5. Switching states of the type-I inverter for $v_o > 0$. (a) Active state. (b) Freewheeling state.

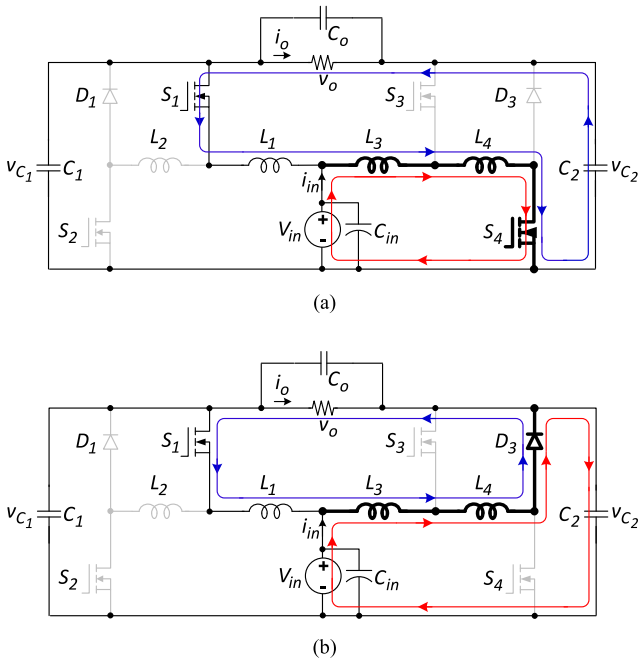

Fig. 6. Switching states of the type-I inverter for $v_o < 0$. (a) Active state. (b) Freewheeling state.

The gate signals of S_2 and S_4 of the type-II inverter are the same as of the type-I inverter (see Fig. 8). However, S_1 and S_3 of the type-II inverter receive complementary switching signals of S_2 and S_4, respectively.

D. Operation of the Type-II Inverter

As the converter has no shoot-through problem, the dead time in the switching signals of the type-II inverter can also be eliminated. However, the high-frequency switching of S_1 and

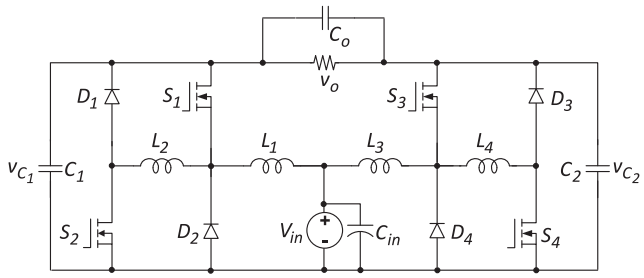

Fig. 7. Type-II inverter.

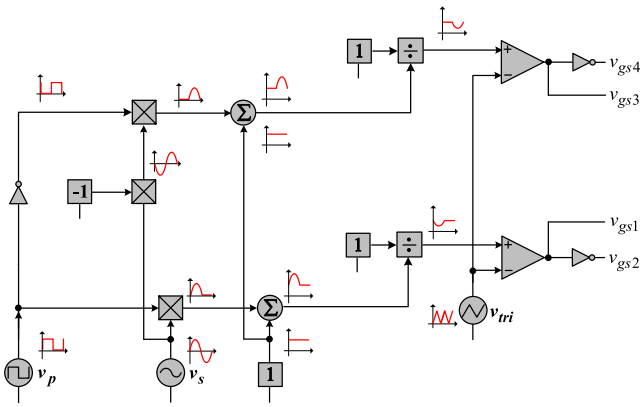

Fig. 8. Control signals generation of the type-II inverter.

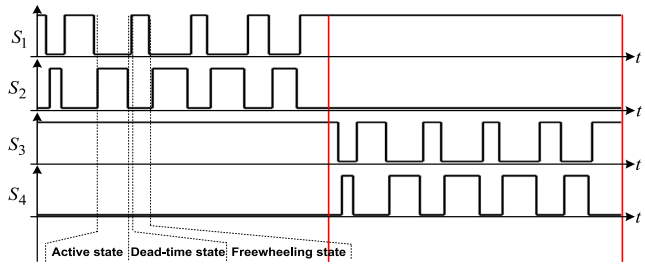

Fig. 9. Switching strategy of the type-II inverter.

S_3 generates circulating currents in the type-II inverter. In order to limit the circulating currents small dead time between S_1 and S_2, and S_3 and S_4 can be used. In a switching cycle, the inverter has three states as shown in Fig. 9. The four-quadrant ac operation of the type-II inverter is shown in Fig. 10. It has four cases: ($v_o > 0$, $i_o < 0$), ($v_o > 0$, $i_o > 0$), ($v_o \langle 0$, $i_o \rangle 0$), and ($v_o < 0$, $i_o < 0$).

The operation of the type-II inverter for $v_o > 0$, $i_o < 0$ is discussed below. Similar analysis can be extended for the other three cases.

1) *Active state:* As shown in Fig. 11(a), S_2 is ON and S_1 is OFF. However, S_2 does not conduct.
2) *Dead-time state:* As shown in Fig. 11(b), S_1 and S_2 are OFF and D_2 is forward biased.
3) *Freewheeling state:* The switch S_2 is ON and S_1 is OFF, however S_2 does not conduct as shown in Fig. 11(b).

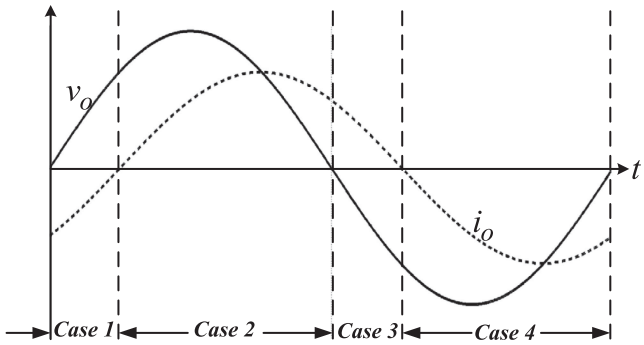

Fig. 10. Four-quadrant ac operation of the type-II inverter.

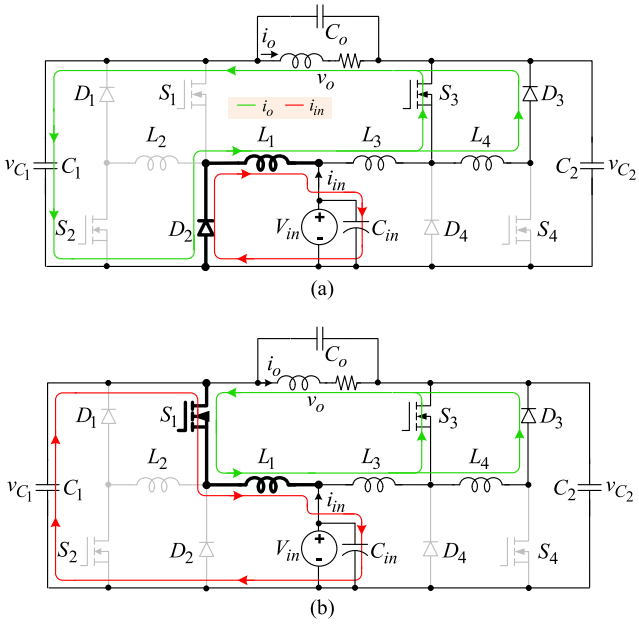

Fig. 11. Topological states of the type-II inverter for $v_o > 0$ and $i_o < 0$. (a) Active state. (b) Freewheeling and dead-time states.

The body diodes of switches in the type-II inverter do not conduct under the unity power factor operation. The S_1 and S_3 of the type-II inverter can conduct in reverse direction when v_o and i_o are not in-phase. The body diodes' conduction of S_1 and S_3 is dependent on their voltage drops. However, S_1 and S_3 conduct in reverse direction only when they are switching at line frequency and v_o and i_o are not in-phase (see Fig. 11). Therefore, their switching loss and reverse recovery issues are negligible.

In all operations, regardless of operation modes the following relations are always valid.

For $v_o > 0$

$$\begin{cases} d_1(t) = \frac{V_o \mathrm{Sin}(\omega t)}{V_{\mathrm{in}} + V_o \mathrm{Sin}(\omega t)} \\ d_2(t) = 0 \\ v_{C_1} = \frac{V_{\mathrm{in}}}{1-d_1(t)} = V_{\mathrm{in}} + V_o \mathrm{Sin}(\omega t) \\ v_{C_2} = \frac{V_{\mathrm{in}}}{1-d_2(t)} = V_{\mathrm{in}}. \end{cases} \tag{1}$$

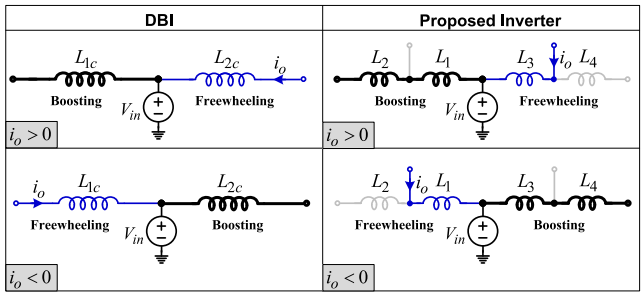

Fig. 12. Inductor volume and conduction loss comparison.

For $v_o < 0$

$$\begin{cases} d_1(t) = 0 \\ d_2(t) = \frac{V_o \mathrm{Sin}(\omega t - \pi)}{V_{\mathrm{in}} + V_o \mathrm{Sin}(\omega t - \pi)} \\ v_{C_1} = \frac{V_{\mathrm{in}}}{1-d_1(t)} = V_{\mathrm{in}} \\ v_{C_2} = \frac{V_{\mathrm{in}}}{1-d_2(t)} = V_{\mathrm{in}} + V_o \mathrm{Sin}(\omega t - \pi). \end{cases} \tag{2}$$

From Fig. 2, $v_o = v_{C_1} - v_{C_2}$. Using (1) and (2), $v_o = V_o \sin(\omega t)$. From (1) and (2), the output voltage gain is obtained as $G = \frac{V_o}{V_{\mathrm{in}}} = \frac{D_{\max}}{1-D_{\max}}$. Where $D_{\max}$ is the maximum value of d_1 and d_2 which occurs at the peak of v_o.

III. Design Considerations of the Inverters

A. Magnetic Volume

As depicted in Fig. 12, for $i_o > 0$, L_1 and L_2 of the proposed inverters are in series and they work as boosting inductors. The sum of L_1 and L_2 of the proposed inverters is same as L_{1c} of the DBI. Similarly, for $i_o < 0$, L_3 and L_4 of the proposed inverters are in series and they work as boosting inductors. The sum of L_3 and L_4 of the proposed inverters is same as L_{2c} of the DBI. Therefore, the magnetic volumes and total inductances of the proposed and conventional boost inverters are equivalent.

B. Inductor Conduction Loss of the Type-I Inverter

The DBI requires two inductors L_{1c} and L_{2c}. For $i_o > 0$, L_{1c} is a boosting inductor and L_{2c} freewheels i_o. For $i_o < 0$, L_{2c} is a boosting inductor and L_{1c} freewheels i_o. In the proposed type-I inverter, for $i_o > 0$, $L_1 + L_2 = L_{1c}$ work as boosting inductors, L_3 freewheels i_o and L_4 does not conduct (see Fig. 12). For $i_o < 0$, $L_3 + L_4 = L_{2c}$ work as boosting inductors, L_1 freewheels i_o and L_2 does not conduct. Thus, in the type-I inverter the inductor conduction loss can be decreased by disabling L_2 and L_4 during the current freewheeling.

In the type-I inverter, $L_2 = L_4$ are designed with 0.3 mH and $L_1 = L_3$ are designed with 0.05 mH. For $i_o > 0$, $L_1 + L_2 = 0.35$ mH limit the inductor current ripple, $L_3 = 0.05$ mH freewheel i_o and $L_4 = 0.3$ mH does not conduct. Similarly, for $i_o < 0$, $L_3 + L_4 = 0.35$ mH limit the inductor current ripple, $L_1 = 0.05$ mH freewheel i_o and $L_2 = 0.3$ mH does not conduct. For the same inductor current ripple, L_{1c} and L_{2c} in the DBI must be designed with 0.35 mH. As illustrated in Fig. 12,

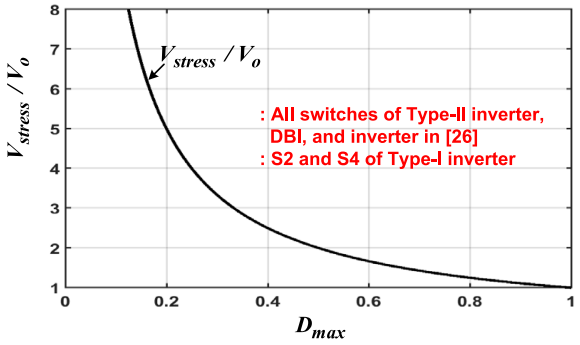

Fig. 13. Voltage stress of $S_1 - S_4$ in the type-II inverter.

for $i_o > 0, L_{1c} = 0.35$ mH limits the inductor current ripple and $L_{2c} = 0.35$ mH freewheels i_o. For $i_o < 0$, $L_{2c} = 0.35$ mH limits the inductor current ripple and $L_{1c} = 0.35$ mH freewheel i_o. Thus, in the proposed type-I inverter, smaller inductors 0.05 mH freewheel i_o, while in the DBI larger inductors 0.35 mH freewheel i_o. Therefore, the inductor conduction loss can be reduced in the type-I inverter.

C. Inductor Conduction Loss of the Type-II Inverter

In the type-II inverter, circulating currents are generated due to high-frequency switching of S_1 and S_3. To limit the circulating currents, L_1 and L_3 should be designed larger. In this paper, L_1 and L_3 of the type-II inverter are designed of 0.3 mH. Compared to the type-I inverter, type-II has higher inductor conduction loss, because in the type-I inverter, $L_1 = L_3 = 0.05$ mH freewheel i_o while in the type-II inverter, $L_1 = L_3 = 0.3$ mH freewheel i_o.

D. Switch Voltage Stress in the Type-II Inverter

The voltage stress of $S_1 - S_4$ of the type-II inverter is obtained as

$$V_{\text{stress}} = V_{C1,2} = \frac{V_o}{D_{\max}}. \tag{3}$$

The voltage stress of all switches of the DBI [7] and inverter in [26] is same as given in (3) and plotted in Fig. 13.

E. Switch Voltage Stress in the Type-I Inverter

S_2, S_4 : Their voltage stress is same as in (3).

S_1, S_3 : As shown in Fig. 14, for $i_o > 0$, S_3 is ON therefore voltage of L_3 is zero. For $i_o < 0$, S_1 is ON and voltage of L_1 is zero. From Fig. 14, maximum voltages of S_1 and S_3 are obtained

$$\begin{cases} V_{s1} = V_{L1} + V_o & i_o > 0 \\ V_{s3} = V_{L3} + V_o & i_o < 0 \end{cases} \tag{4}$$

where V_{L1} and V_{L3} are the maximum voltages of L_1 and L_3. From Fig. 14, V_{L1} and V_{L3} are obtained as

$$V_{L1} = V_{L3} = kV_{\text{in}}\ , \quad k = \frac{L_1}{L_1 + L_2} = \frac{L_3}{L_3 + L_4}. \tag{5}$$

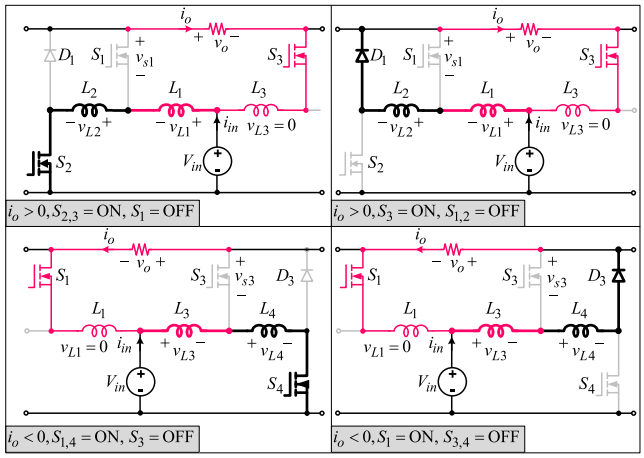

Fig. 14. Voltage stress of S_1 and S_3 in the type-I inverter.

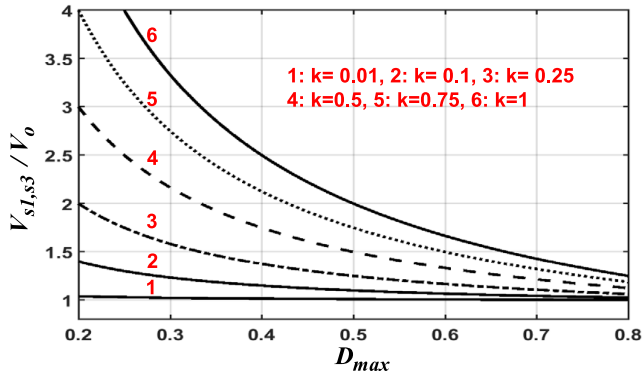

Fig. 15. Voltage stress of S_1 and S_3 in the type-I inverter for different values of k.

TABLE I
VOLTAGE STRESS OF SWITCH S3 IN THE TYPE-I INVERTER

k	$L_3 = kL_{eff}$	$V_{s3}\ (V) = kV_{in} + V_o$
1	L_{eff}	232
0.5	$0.5L_{eff}$	193
0.33	$0.33L_{eff}$	180
0	0	155

In (5), $L_1 + L_2 = L_3 + L_4$ is represented as L_{eff}. By putting (5) in (4) and using the voltage gain relation $V_o/V_{\text{in}} = D_{\max}/(1 - D_{\max})$, the voltage stress of S_1 and S_3 can be expressed as

$$V_{s1,s3} = \frac{V_o\,(k - kD_{\max} + D_{\max})}{D_{\max}}. \tag{6}$$

From (6), $\frac{V_{s1,s3}}{V_o}$ versus $D_{\max}$ is plotted in Fig. 15 for different values of k. It is noted that $V_{s1,s3}$ decrease with k. To further clarify the above-mentioned analysis, simulated voltage waveforms of S_3 for different values of k, $V_{\text{in}} = 77\ V$ and $V_o = 155\ V$ are shown in Fig. 16. The values of k, L_3 and voltage stress V_{s3} of S_3 are given in Table I. As shown in Fig. 16, when k approaches 0, V_{s3} reaches V_o, and when k approaches

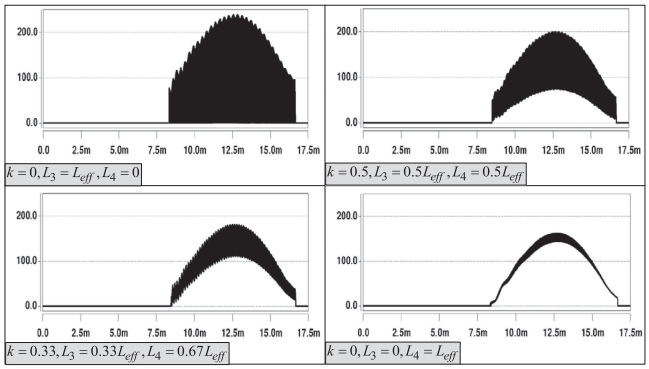

Fig. 16. Voltage of S_3 in the type-I inverter for different inductance values of L_3.

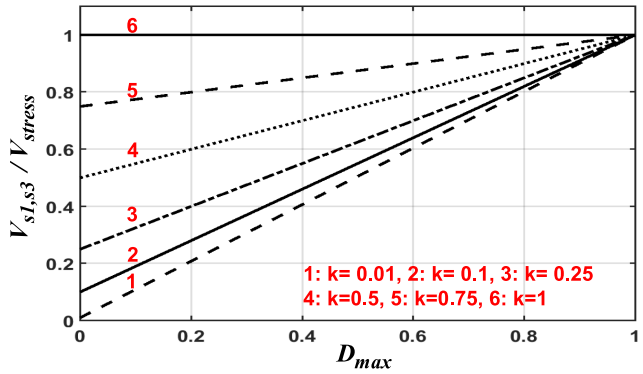

Fig. 17. Comparison of voltage stress of S_1 and S_3.

1, V_{s3} reaches $V_{\text{in}} + V_o$ given in (3). Thus, to keep the inductor conduction loss and voltage stress of S_1 and S_3 lower L_1 and L_3 should be designed smaller.

The voltage stress of S_1 and S_3 in the type-I inverter $V_{s1,s3}$ from (6) is normalized to the voltage stress V_{stress} of the type-II, DBI and inverter in [26] from (3) as

$$\frac{V_{s1,s3}}{V_{\text{stress}}} = (k - kD_{\max} + D_{\max}). \tag{7}$$

The ratio in (7) is plotted in Fig. 17 for different k values. It is noted that for smaller k values the maximum voltage stress of S_1 and S_3 in the type-I inverter is significantly smaller.

F. Switch Current Stress of the Type-I and Type-II Inverters

The switch current stress of the type-I and II inverters are given as

$$I_{s2,s4} = \frac{I_o}{1 - D_{\max}} \tag{8}$$

$$I_{s1,s3} = I_o. \tag{9}$$

From (8) and (9), $I_{s2,s4}/I_o$ and $I_{s1,s3}/I_o$ are plotted in Fig. 18(a). The maximum switch current ($I_{\text{stress.DBI}}$) of all switches of the DBI are same as in (8). $I_{s1,s3}$ of the proposed

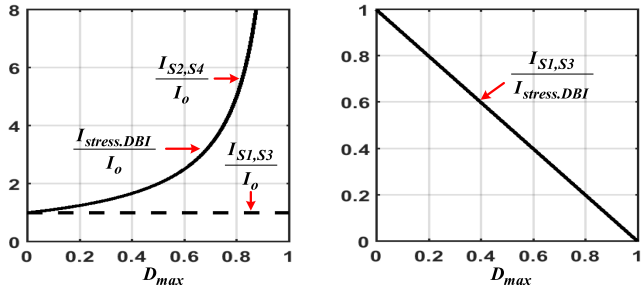

Fig. 18. Switch current stresses. (a) Proposed inverter. (b) Comparison between the proposed inverter and DBI.

inverters from (9) is normalized to $I_{\text{stress.DBI}}$ as

$$\frac{I_{s1,s3}}{I_{\text{stress.DBI}}} = 1 - D_{\max}. \tag{10}$$

The ratio in (10) is plotted in Fig. 18(b). As shown the current stresses of S_1 and S_3 of the proposed inverters are much lower.

G. Inductance and Capacitance

From Figs. 5 and 6, L_{eff} for current ripple $x\%$ of maximum inductor current I_L is obtained as

$$L_{\text{eff}} = \frac{V_o\,(1 - D_{\max})}{f_{sw}\,x\%\,I_L} \tag{11}$$

I_L is same as in (8). Using (8) and (11) we get

$$L_{eq} = \frac{V_o(1 - D_{\max})^2}{f_{sw}\,x\%\,I_o}. \tag{12}$$

From Figs. 5 and 6, the capacitance of C_1 and C_2 for voltage ripple $y\%$ of maximum capacitor voltage $V_{C1,2}$ is obtained as

$$C = \frac{I_o D_{\max}}{f_{sw}\,y V_{C1,2}}. \tag{13}$$

The maximum capacitor voltage $V_{C1,2}$ is given by (3). Using (3) and (13) we get

$$C = \frac{I_o D_{\max}^2}{f_{sw}\,y V_o}. \tag{14}$$

IV. RMS Currents and Conduction Power Loss

In the following analysis, $i_o(t) = I_o\text{Sin}(\omega t)$ and $d_1(t)$ and $d_2(t)$ are used from (1) and (2).

A. RMS Currents

S_1, S_3: Their rms currents are obtained as

$$I_{S1,3.\text{rms}} = \sqrt{\frac{1}{2\pi}\int_{\pi}^{2\pi} i_o(t)^2.d\,(\omega t)} = \frac{I_o}{2}. \tag{15}$$

S_2, S_4: Their rms currents are derived as

$$I_{S2,4.\mathrm{rms}} = \sqrt{\frac{1}{2\pi}\int_0^{\pi}\left(\frac{i_o(t)}{1-d_1(t)}\right)^2 .d_1(t).d(\omega t)} = I_o\frac{\sqrt{32V_oV_{\mathrm{in}}+9\pi V_o^2)}}{4V_{\mathrm{in}}\sqrt{3\pi}}. \quad (16)$$

From (16) $I_{S2,4.\mathrm{rms}}$ in terms of G can be expressed as

$$I_{S2,4.\mathrm{rms}} = I_o\sqrt{\left(\frac{2G}{3\pi}+\frac{3G^2}{16}\right)}. \quad (17)$$

D_1, D_3: Their rms currents are obtained as

$$I_{D1,3.\mathrm{rms}} = \sqrt{\frac{1}{2\pi}\int_0^{\pi}\left(\frac{i_o(t)}{1-d_1(t)}\right)^2 .(1-d_1(t)).d(\omega t)} = \frac{I_o}{2\sqrt{3\pi}}\sqrt{\frac{3\pi V_{\mathrm{in}}+8V_o}{V_{\mathrm{in}}}}. \quad (18)$$

From (18) $I_{D1,3.\mathrm{rms}}$ in terms of G can be expressed as

$$I_{D1,3.\mathrm{rms}} = I_o\sqrt{\frac{1}{4}+\frac{2G}{3\pi}}. \quad (19)$$

L_2, L_4: Their rms currents are obtained as

$$I_{L2,4.\mathrm{rms}} = \sqrt{\frac{1}{2\pi}\int_0^{\pi}\left(\frac{i_o(t)}{1-d_1(t)}\right)^2 .d(\omega t)} = I_o\sqrt{\frac{12\pi V_{\mathrm{in}}^2+64V_oV_{\mathrm{in}}+9\pi V_o^2}{48\pi V_{\mathrm{in}}^2}}. \quad (20)$$

From (20) $I_{L2,4.\mathrm{rms}}$ in terms of G can be expressed as

$$I_{L2,4.\mathrm{rms}} = I_o\sqrt{\frac{1}{4}+\frac{3G^2}{16}+\frac{4G}{3\pi}}. \quad (21)$$

L_1, L_3: Their rms currents are modeled as

$$I_{L1,3.\mathrm{rms}} = \sqrt{\frac{1}{2\pi}\left(\int_0^{\pi}\left(\frac{i_o(t)}{1-d_1(t)}\right)^2 .d(\omega t)+\int_{\pi}^{2\pi}(i_o(t))^2.d(\omega t)\right)} = I_o\sqrt{\frac{64V_oV_{\mathrm{in}}+9\pi V_o^2+24\pi V_{\mathrm{in}}^2}{48\pi V_{\mathrm{in}}^2}}. \quad (22)$$

From (22) $I_{L1,3.\mathrm{rms}}$ in terms of G can be expressed as

$$I_{L1,3.\mathrm{rms}} = I_o\sqrt{\frac{1}{2}+\frac{3G^2}{16}+\frac{4G}{3\pi}}. \quad (23)$$

For close examination of the modeled results, the rms currents of the proposed inverter are simulated using the PSIM software with electrical specifications given in Table II.

The simulated and calculated rms currents are compared in Fig. 19. The calculated results are in very good agreement with the simulated results.

TABLE II
SPECIFICATIONS AND POWER DEVICES

Topology	Parameter	Symbol	Part. No./Value
Type – I and II	Output power	P_o	500 W
	Output voltage	V_o	155 V_{pk}
	Input voltage	V_{in}	$70-200$ V_{dc}
	Line frequency	f	60 Hz
	Switching frequency	f_{sw}	50 kHz
	MOSFET	S_1-S_4	60C7040
	Diode	D_1, D_3	RURG3060
	Capacitor	C_1, C_2	3 μF
	Output capacitor	C_o	6.8 μF
	Input capacitor	C_{in}	0.4 mF
Type – II	Diode	D_2, D_4	RURG3060
	Inductor	L_2, L_4	50 μH
	Inductor	L_1, L_3	0.3 mH
Type – I	Inductor	L_2, L_4	0.3 mH
	Inductor	L_1, L_3	50 μH

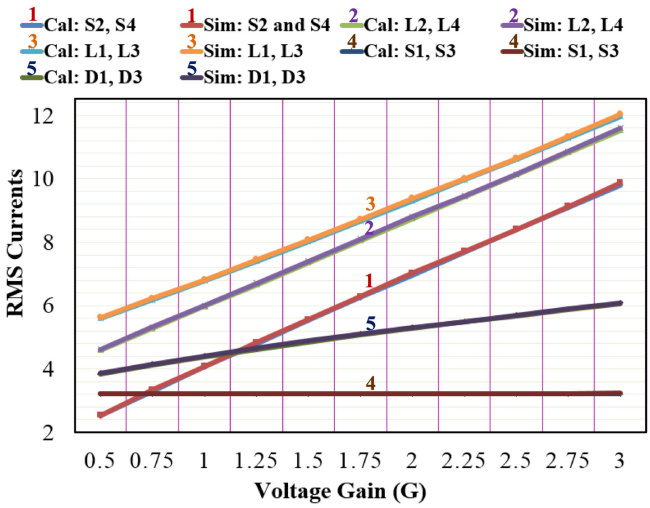

Fig. 19. Comparison of the rms currents for $P_o = 500$ W and $V_o = 155$ V_{pk}.

TABLE III
CONDUCTION LOSS OF POWER COMPONENTS

Power component	Conduction power loss
S_1, S_3	$I^2_{S1,3.rms}R_{ds}$
S_2, S_4	$I^2_{S2,4.rms}R_{ds}$
D_1, D_3	$I^2_{D1,3.rms}R_{ak}+I_{D1,3.FV}V_f$
L_2, L_4	$I^2_{L2,4.rms}R_{L2,4}$
L_1, L_3	$I^2_{L1,3.rms}R_{L1,3}$

B. Average Currents

The average currents of D_1 and D_3 are obtained as

$$I_{D1,3.FV} = \frac{1}{2\pi}\int_0^{\pi} I_o\sin(\omega t).d(\omega t) = \frac{I_o}{\pi}. \quad (24)$$

C. Conduction Loss

The conduction loss of the power devices can be estimated using power loss equations shown in Table III. In Table III, R_{ds} is the channel resistance of MOSFET, V_f is the forward

TABLE IV
COMPARISON OF THE POWER INVERTERS

	Differential-boost inverter [DBI] [7]	Improved differential-boost inverter [12]	Quasi Z-source inverter [4], [33]	Switched-coupled inductor inverter [14]	Buck-boost inverter in [13]	Proposed type-II inverter	Proposed type-I inverter	Buck-Boost Inverter in [26]
Voltage gain $G=\frac{V_o}{V_{in}}$	$\frac{D_{max}}{1-D_{max}}$	$\frac{D_{max}}{1-D_{max}}$	$\frac{(M=1-D_{ZSI})}{1-2D_{ZSI}}$	$\frac{5D-2}{D}$	$\frac{D_{max}}{1-D_{max}}$	$\frac{D_{max}}{1-D_{max}}$	$\frac{D_{max}}{1-D_{max}}$	$\frac{D_{max}}{1-D_{max}}$
Maximum duty cycle	$D_{max}=\frac{G}{1+G}$	$D_{max}=\frac{G}{1+G}$	$D_{ZSI}=\frac{G-1}{2G-1}$	$D=\frac{2}{5-G}$	$D_{max}=\frac{G}{1+G}$	$D_{max}=\frac{G}{1+G}$	$D_{max}=\frac{G}{1+G}$	$D_{max}=\frac{G}{1+G}$
Operation	single-stage symmetrical	single-stage symmetrical	quasi single-stage symmetrical	single-stage symmetrical	single-stage asymmetrical	single-stage symmetrical	single-stage symmetrical	single-stage symmetrical
Total no. of switches	4: (S_1-S_4)	6: (S_1-S_6)	4: (S_1-S_4)	3: (S_1,S_2,S_x)	4: (S_1-S_4)	4: (S_1-S_4)	4: (S_1-S_4)	4: (S_1-S_4)
High frequency switches out of the total switches	4: (S_1-S_4)	4: (S_1-S_4)	4: (S_1-S_4)	3: (S_1,S_2,S_x)	4: (S_1-S_4)	4: (S_1-S_4)	2: (S_2,S_4)	4: (S_1-S_4)
Line frequency switches out of the total switches	0	2: (S_5,S_6)	0	0	0	0	2: (S_1,S_3)	0
Switches at high frequency at a time	4 (S_1-S_4)	2: (S_1,S_2) or (S_3,S_4)	4: (S_1-S_4)	3: (S_1,S_2,S_x)	2: (S_1,S_4) or (S_2,S_3)	2: (S_1,S_2) or (S_3,S_4)	1: (S_2 or S_4)	2: (S_1,S_2) or (S_3,S_4)
Diodes	0	0	1: D_x	0	0	4: (D_1-D_4)	2: (D_1,D_3)	4: (D_1-D_4)
Current stress	S_1-S_4: $(1+G)I_o$	S_1-S_4: $(1+G)I_o$, S_5-S_6: I_o	S_1-S_4: $(2G-1)I_o$ $(boost)$ S_1-S_4: I_o $(buck)$	$S1$: $\frac{(5-G)(G-1)}{3-G}I_o$ $S2$: $\frac{5+G}{2}I_o$, Sx: $\frac{5-G}{3-G}I_o$,	S_1-S_4: $(1+G)I_o$	S_2,S_4: $(1+G)I_o$, S_1,S_3: I_o	S_2,S_4: $(1+G)I_o$, S_1,S_3: I_o	S_2,S_4: $(1+G)I_o$, S_1,S_3: I_o
Voltage stress	S_1-S_4: $(1+\frac{1}{G})V_o$	S_1-S_4: $(1+\frac{1}{G})V_o$ S_5-S_6: V_o	S_1-S_4: $\frac{(2G-1)V_o}{G}$ (bo) S_1-S_4: $\frac{V_o}{M}$ (bu)	$S1$: $\frac{5+G}{2G}V_o$ $S2,x$: $\frac{5+G}{G}V_o$	S_1-S_4: $(1+\frac{1}{G})V_o$	S_1-S_4: $(1+\frac{1}{G})V_o$	S_2,S_4: $(1+\frac{1}{G})V_o$ S_1,S_3: V_o	S_1-S_4: $(1+\frac{1}{G})V_o$
Shoot-through risk	yes	yes	no	yes	yes	no	no	no
PWM dead-time	yes	yes	can be eliminated	yes	yes	no	no	yes
MOSFET body diodes reverse recovery issues	yes	yes	yes	yes	yes	no	no	no
Peak measured efficiency	86.3 % at Fsw= 20 kHz F= 50 Hz Vin= 80 V Vo=110 Vrms Po= 500 W	92.6 % at Fsw= 20 kHz F= 50 Hz Vin= 80 V Vo= 110 Vrms Po= 500 W	90.2 % at Fsw= 10 kHz, F= 50 Hz Vin= 90 V Vo=110 Vrms Po= 300 W	90.5 % at Fsw= 20 kHz F= 60 Hz Vin= 62 V Vo=110 Vrms Po= 280 W	not available	96.5 % at Fsw= 50 kHz F= 60 Hz Vin= 155 V Vo=110 Vrms Po= 500 W	97 % at Fsw= 50 kHz F= 60 Hz Vin= 155 V Vo=110 Vrms Po= 500 W	96.1 % at Fsw= 50 kHz F= 60 Hz Vin= 155 V Vo=110 Vrms Po= 500 W
Common ground	no	no	no	yes	yes	no	no	no
Reactive power operation	yes	yes	yes	yes	yes	yes	no	yes
Magnetic Volume under same electrical specifications	DBI	Same as DBI	NA	NA	Same as DBI	Same as DBI	Same as DBI	Twice of DBI

voltage drop of diode, R_{ak} is the conduction resistance of diode, and $R_{L1,3}$ and $R_{L2,4}$ are the equivalent series resistances of inductors. The conduction and switching loss of the type-I and II inverters were simulated using thermal and device database editor modules in PSIM software. In device database editor module, inductors, MOSFETs, and diodes are modeled using data from the datasheets of the components. The power loss of the type-II inverter is higher than the type-I inverter, because in the type-I inverter, a single high frequency switch is switching and in the type-II inverter two high-frequency switches are switching at a time. In addition, the conduction loss of the type-II inverter is higher than the type-I inverter.

V. COMPARISON OF THE PROPOSED AND CONVENTIONAL INVERTERS

The comparison of the proposed and conventional inverters is given in Table IV. In the DBI, all the switches are switched simultaneously under the high-voltage stress (sum of input and output voltages) and current stress (sum of input and output currents). In addition, it uses IGBTs as switching devices with finite dead time in the switching signals, therefore its efficiency is considerably lower. The inverter in [14] has only three switches but its voltage and current stresses are higher, which results in lower efficiency. The inverters in [7] and [12]–[14] have the shoot-through risk, therefore dead time is used which limits the switching frequency and achievable voltage gain.

As shown, only one switch of the proposed type-I inverter and two switches of the proposed type-II are working under high frequency, which results in lower power loss. In addition, shoot-through issues, PWM dead time and MOSFETs reverse recovery issues can be eliminated. Furthermore, the current stress of the two switches (S_1,S_3) in the proposed type-I and II inverters is I_o and the voltage stress of the two line frequency switches in the proposed type-I inverter can be as low as V_o. Moreover, the inductor conduction loss in the type-I inverter is reduced.

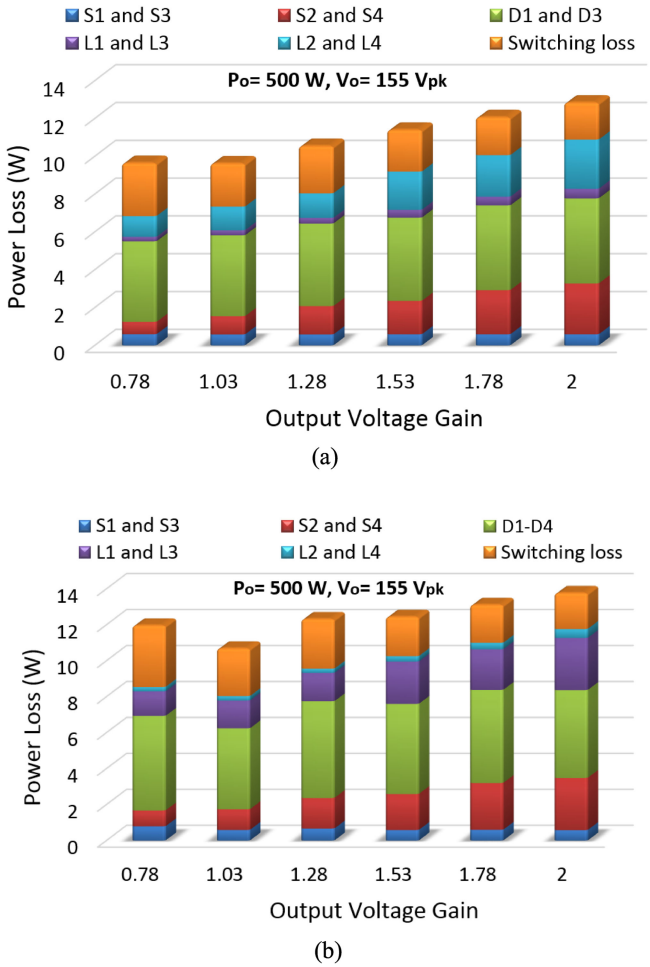

Fig. 20. Comparison of the switching and conduction losses at 50 kHz. (a) Type-I. (b) Type-II.

Due to the advantage of the proposed inverters, higher switching frequencies can be used for the reduction of the passive components. For detailed comparison, see Table IV.

VI. Experimental Results

To verify the theoretical analysis, 500 W hardware prototypes of the proposed inverters were built and tested. The electrical specifications are given in Table II.

A. Type-II Inverter

The experimental waveforms of the type-II inverter are shown in Figs. 21–23. The waveforms in Figs. 21 and 22 are obtained with resistive load $R_L = 24\ \Omega$. Fig. 21(a) shows the waveforms of the input voltage V_{in}, output voltage v_o, and capacitor voltage v_{C_1} and v_{C_2} of C_1 and C_2, respectively, in the boost operation.

Fig. 21(b) shows the waveforms of the drain-source voltage v_{DS_1}, v_{DS_2}, v_{DS_3}, and v_{DS_4} of the switch S_1, S_2, S_3, and S_4, respectively. Fig. 21(c) shows the waveforms of the input current $i_{\rm in}$, current i_1 through the inductor L_1 and current i_2 through the inductor L_2. Fig. 22 shows the waveforms of the type-II inverter in the buck operation. The waveforms in Fig. 23 are obtained

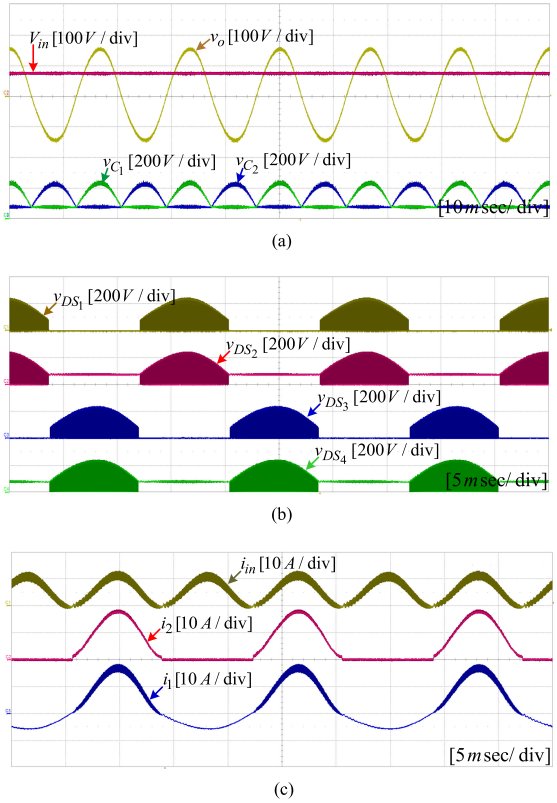

Fig. 21. Boost operation of the type-II inverter (Resistive load, $\mathrm{V_{in}} = 77\ \mathrm{V}$, $\mathrm{V}_o = 155\ \mathrm{V}_{pk}$, $P_o = 500\ \mathrm{W}$).

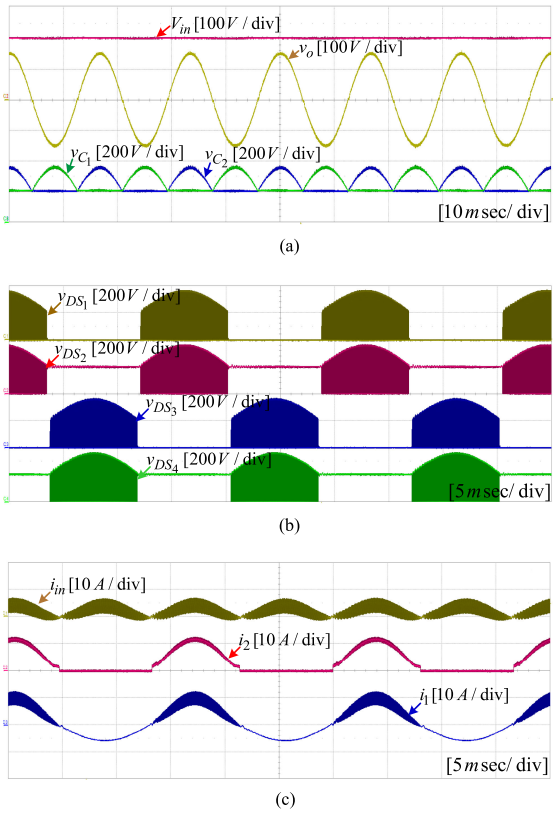

Fig. 22. Buck operation of the type-II inverter (Resistive load, $\mathrm{V_{in}} = 200\ \mathrm{V}$, $\mathrm{V}_o = 155\ \mathrm{V}_{pk}$, $P_o = 500\ \mathrm{W}$).

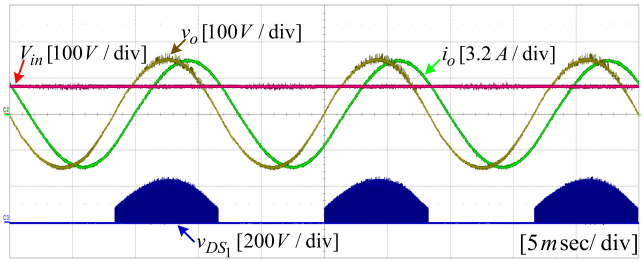

Fig. 23. Boost operation of the type-II inverter (partially inductive load, $\mathrm{V_{in}} = 77$ V, $\mathrm{V}_o = 155$ V_{pk}).

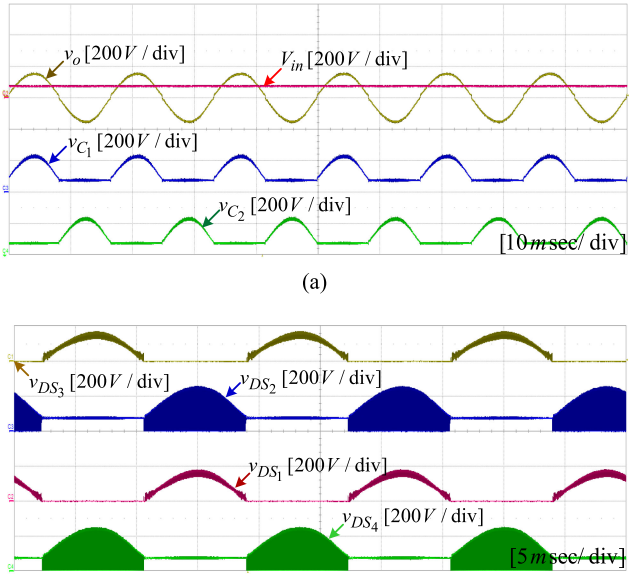

Fig. 24. Boost operation of the type-I inverter (resistive load, $\mathrm{V_{in}} = 77$ V, $\mathrm{V}_o = 155$ V_{pk}, $P_o = 500$ W).

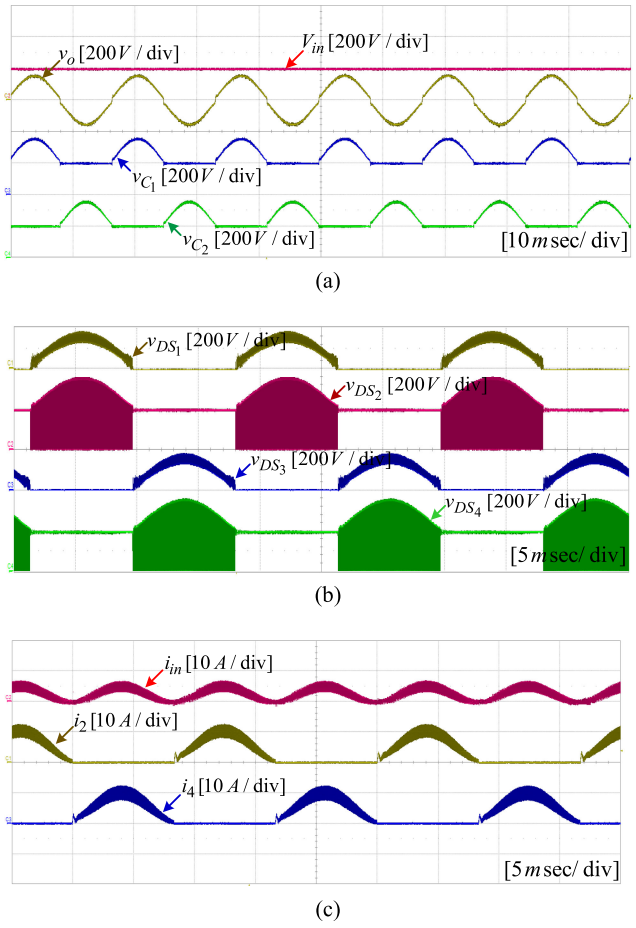

Fig. 25. Buck operation of the type-I inverter (resistive load, $\mathrm{V_{in}} = 200$ V, $\mathrm{V}_o = 155$ V_{pk}, $P_o = 500$ W).

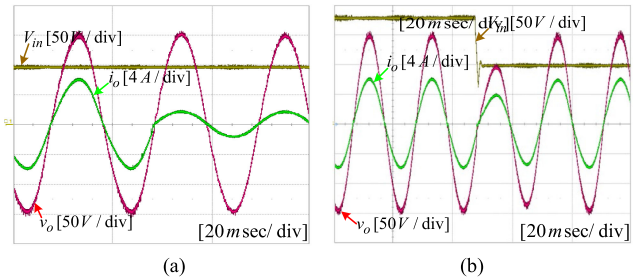

Fig. 26. Dynamic results. (a) Step-load change. (b) Step-input voltage change.

with partially inductive load ($R_L = 24\ \Omega$, $L_L = 50$ mH) in the boost operation.

B. Type-I Inverter

The experimental waveforms of the type-I inverter are given in Figs. 24 and 25.

As shown in Figs. 24(b) and 25(b), the drain source voltage of S_1 and S_3 in the type-I inverter is much lower than the type-II inverter shown in Figs. 21(b) and 22(b). Ideally, for a unity power factor inverter v_o and i_o are in-phase. However, in practical implementation as shown in the waveforms of the type-I inverter, due to the reactive components of the converter, a small phase shift between v_o and i_o can occur, which can lead to a small zero crossing distortion.

The type-II inverter due to its reactive power flow capability does not generate zero crossing distortion even when v_o and i_o are not in-phase (see Fig. 23).

Fig. 26(a) shows the dynamic experimental results for the step load change from 24 to 100 Ω. Fig. 26(b) shows the results for the step input voltage change from 180 to 100 V. Fig. 27 shows the measured efficiencies. Fig. 28 shows total harmonic distortion (THD) of output voltage versus input voltage. Fig. 29 is a photo taken of the prototype. All the experimental results are in good agreement with the theoretical analysis.

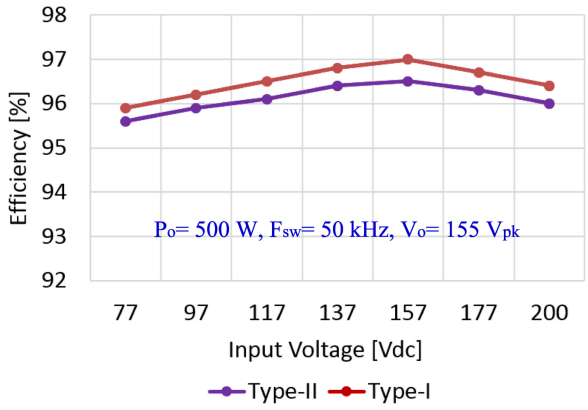

Fig. 27. Measured efficiencies.

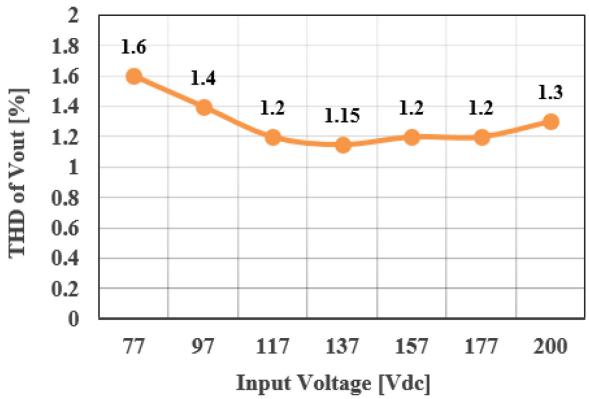

Fig. 28. Measured THD of output voltage versus input voltage.

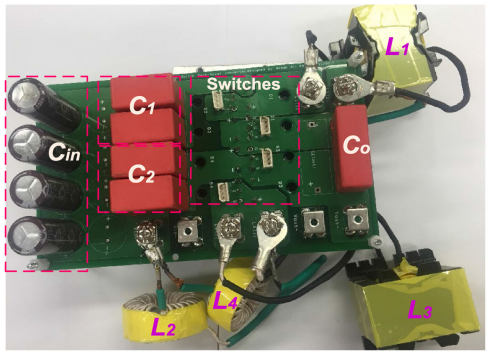

Fig. 29. Prototype picture.

VII. Conclusion

In this paper, type-I and type-II split-inductor differential boost inverters were presented. Compared to the traditional boost inverter, the proposed inverters have more inductors count. However, the total inductance and magnetic volumes of the proposed and traditional boost inverters are equivalent. The type-I inverter requires two extra diodes and the type-II inverter requires four extra diodes compared to the traditional boost inverter. However, the proposed inverters have many benefits given as follows.

1) High efficiency is obtained by using power MOSFETs in conjunction with external fast recovery diodes without reverse recovery issues of the MOSFETs body diodes.
2) High reliability is obtained by eliminating shoot-through issues.
3) Dead time in the type-I inverter is eliminated while in the type-II inverter it is minimized, which improved the efficiency and output voltage quality.
4) High switching frequency of 50 kHz is used to reduce the volume of the passive components while maintaining high efficiency.
5) Current stresses of the two switches in both the type-I and II inverters and voltage stress of the two switches in the type-I inverter are lowered.
6) Inductor conduction loss in minimized.
7) Two switches of the type-I inverter are line frequency, and only one switch of the type-I inverter and two switches of the type-II inverter are operated under the high-frequency switching at a time, which deceased the power loss.

The operation of the proposed inverters was explained and analyzed. The experimental results obtained for 500 W, 110 Vrms hardware prototypes verified the analysis.

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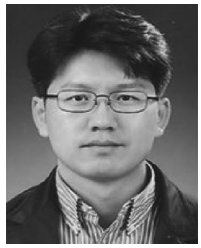

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