Single-Phase AC–DC Converter With Dual-Output Rectifier, Dual-Input DC Transformer, and Voltage-Split/Sigma Principle

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***Abstract*—A single-phase ac–dc converter with dual-output rectifier (DOR) and dual-input dc transformer (DI-DCX) is proposed in this paper. A voltage-split/sigma principle is adopted, that is, the grid voltage is split into two variable dc bus voltages first by the front-stage DOR, and then the two bus voltages are combined into an adjustable output voltage by the downstream DI-DCX. DC output voltage is directly regulated by the front-end rectifier. Therefore, no voltage regulation is required for the dc–dc stage, and a DI-DCX with optimized operation condition is employed to improve the overall efficiency of the ac–dc converter. Moreover, since the DOR has two different output voltages, three-level characteristic is achieved naturally to reduce switching losses of the converter. Zero voltage switching of all the active switches in the DI-DCX is realized as well. Detailed operation principles, control and modulation strategies, and characteristics of the proposed ac–dc converter are analyzed in detail. Experimental results of a 1.5-kW prototype are provided to verify the effectiveness of the proposed converter.**

***Index Terms*—AC–DC converter, dual-input (DI) converter, dual-output rectifier (DOR), power factor correction (PFC), voltage-split/sigma (VSS).**

I. Introduction

Single-phase ac–dc converters are widely employed in electric-vehicles [1], server and telecom power systems [2], and consumer electronics [3] to interface ac grid and various dc loads. In applications such as electric vehicle charging, isolated two-stage ac–dc converters with wide range of output voltage regulation capabilities are usually used [4]–[6], as shown in Fig. 1. A boost power factor correction (PFC) converter is typically used in the front stage to achieve high power factor (PF) and low input current total harmonic distortion to meet harmonic standards, and an isolated dc–dc converter is used in the second stage to regulate the output voltage.

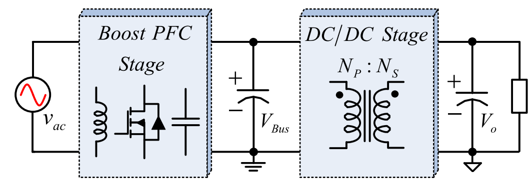

Fig. 1. Conventional two-stage ac–dc converter.

For dc–dc isolated stage, zero voltage switching (ZVS) topologies are preferable to enhance efficiency of the ac–dc converter. *LLC* resonant topology is a good candidate since it can realize soft switching of the primary switches within full load range and has a wide range of voltage regulation capabilities [7]–[9]. However, as the required output voltage range increases, the operating frequency range of the *LLC* converter also increases, which introduces additional reactive power to the *LLC* converter, resulting in reduced power conversion efficiency [10]–[13]. Many efforts were made to solve the contradiction between wide voltage gain and power conversion efficiency of the *LLC* converters. In [11], the switching frequency range of the *LLC* converter is narrowed significantly by changing the configuration of the secondary hybrid rectifier, which reduces the converter's circulating losses and conduction losses. In [12], output voltage regulation is achieved by pulsewidth modulation (PWM) control of the secondary-side auxiliary MOSFET, and the primary switches can operate at resonant frequency. Open-loop delay time control for secondary rectifier switches is proposed in [13], which improves the efficiency of the *LLC* converter. Although these approaches have been proven to improve performance, they increase the cost of circuit or the complexity of control.

The optimal condition of the *LLC* converter is operating its switching frequency the same as the resonant frequency, making it behave like a dc transformer (DCX). The ideal voltage transfer ratio in this scenario is independent of the load, and highest power conversion efficiency can be achieved [14]–[17]. However, the voltage gain of DCX is fixed, leading to an unregulated output voltage. AC–DC converters with variable dc bus voltage were proposed in [18]–[21], the output voltage is regulated by the dc bus and the second-stage *LLC* converter can operate as a

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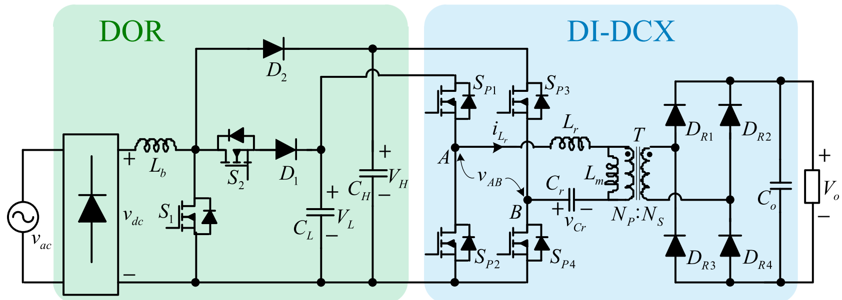

Fig. 2. Circuit topology of the proposed ac–dc converter.

DCX. For the conventional boost PFC converter, the intermediate bus voltage must be higher than the peak value of the grid voltage. In applications where the grid voltage is single-phase 220 VAC, this bus voltage is typically 380–400 V. To make it variable, it is required to increase the bus voltage in the range above 400 V, which will significantly increase the voltage stress of the power devices, resulting in a further increase in switching losses [18], [19]. Although soft switching technology is applied to the PFC converter in [18], the conduction loss and turn-OFF loss are increased, and the modulation method gets complicated.

The major contribution of this paper is to propose a dual-output rectifier (DOR) and a dual-input DCX (DI-DCX) based single-phase ac–dc converter. The output voltage is directly regulated by adjusting the two bus voltages provided by the DOR, and no voltage regulation is required for the dc–dc stage. Therefore, a DI-DCX with optimized operation condition is employed to improve the overall efficiency of the ac–dc converter. This paper is organized as follows. In Section II, the topology, voltage regulation principle, and operation principle of the ac–dc converter will be introduced. Section III presents the control strategy of the converter. The characteristics analysis of the DOR is presented in Section IV. Design considerations of the ac–dc converter are presented in Section V. Experiment results are provided in Section VI. Finally, Section VII concludes this paper.

II. Proposed Single-Phase AC–DC Converter

A. *Topology of the Converter and Voltage-Split/Sigma (VSS) Principle*

The ac–dc converter proposed in this paper is shown in Fig. 2. Dual-output boost converter is employed as the front-end PFC converter. It is composed of a rectifier bridge, an inductor L_b, power switches S_1 and S_2, power diodes D_1 and D_2, capacitors C_1 and C_2, and has two output ports. D_1 and D_2 are followed by low-voltage and high-voltage output ports, respectively. PFC and voltage regulation of V_H and V_L are realized by the DOR. Dual-input *LLC* converter operating as a DCX is used for the second-stage dc–dc converter. It consists of power switches S_{P1}–S_{P4}, power diodes D_{R1}–D_{R4}, capacitor C_o, resonant inductor L_r, resonant capacitor C_r, and transformer *T*. Galvanic isolation is realized by the DI-DCX.

The VSS principle is adopted by the ac–dc converter to achieve output voltage regulation as shown in Fig. 3. The rectified input voltage v_{dc} is split into two bus voltages V_L and V_H

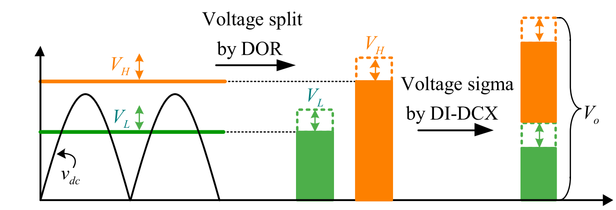

Fig. 3. Illustration of the VSS principle.

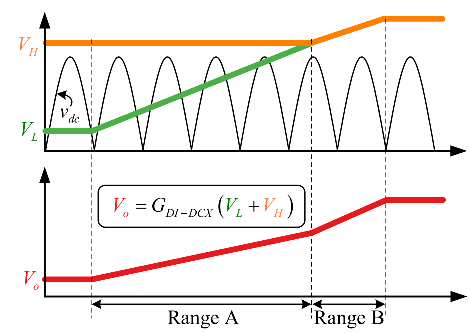

Fig. 4. Voltage regulation principle of the ac–dc converter.

first by the DOR. V_L and V_H are both adjustable. Then, the two bus voltages are added together by the DI-DCX to become output voltage V_o. Since V_L and V_H are both adjustable, V_o can be regulated by directly adjusting their voltages. Therefore, voltage regulation is not required for the DI-DCX, and a DI-DCX with optimized operation condition can be adopted to enhance the overall efficiency of the ac–dc converter.

B. *Voltage Regulation Principle*

The voltage regulation principle of the ac–dc converter is plotted in Fig. 4. It can be observed that the whole output voltage range is divided into two ranges, which are range A and range B. In both ranges, V_H provided by the DOR is always higher than the peak value of the grid voltage, allowing the ac–dc converter to work properly and realize PFC. Different from the conventional boost PFC converter, V_L is a new port voltage that can be either lower or higher than the peak value of the grid voltage. Therefore, compared with the conventional two-stage scheme, the converter proposed in this paper does not increase the voltage stress of the power devices of the front and rear stages.

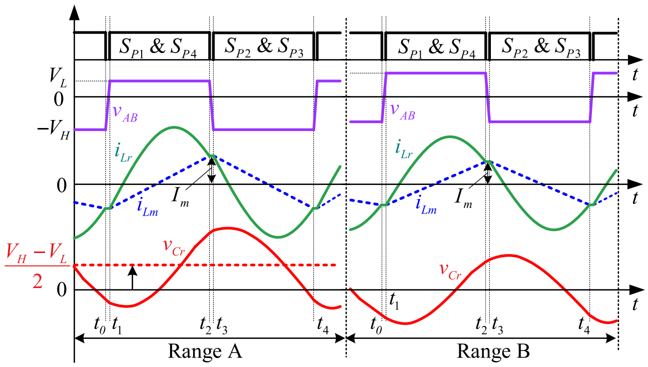

Fig. 5. Main operation waveforms of the DI-DCX.

In range A, V_H is a fixed value, only V_L is adjustable and is lower than V_H. Therefore, V_o is regulated directly by V_L. In range B, V_L and V_H are equal, and they are both flexible, the output voltage is regulated by both V_L and V_H. A wide range regulation of the output voltage can be achieved by adjusting the voltages of V_L and V_H, and the quantitative relationship of V_L, V_H, and V_o can be expressed as

$$V_o = G_{\text{DI-DCX}}\,(V_L + V_H) \tag{1}$$

where $G_{\text{DI-DCX}}$ represents the voltage gain of the DI-DCX. Thus, no voltage regulation is required for the DI-DCX and its high power conversion efficiency can be achieved.

It is worth mentioning that the DOR can output two different voltages, V_L and V_H. This natural multi-level characteristic helps to reduce its switching losses, further improving the overall efficiency of the ac–dc converter.

C. Operation Principle of the DI-DCX

The main waveforms of the DI-DCX corresponding to range A and range B are plotted in Fig. 5. When S_{P1} and S_{P4} are ON, the voltage V_L is employed as the input of the converter. Then, the midpoint voltage $v_{AB} = V_L$. When S_{P2} and S_{P3} are ON, V_H is used as input voltage and $v_{AB} = V_H$. Considering the symmetrical operation of the converter, the average input current from V_L and V_H ports must be equal, and the equivalent input voltage of the DI-DCX is $(V_H + V_L)/2$. It means that the DI-DCX is equivalent to a conventional single-input *LLC* resonant converter with an input voltage of $(V_H + V_L)/2$. Therefore, the basic characteristics, modulation, control, and design of the DI-DCX are still the same as a conventional *LLC* resonant converter. ZVS of all primary switches can be ensured within the entire operation range.

As known, the average voltage applied on the resonant inductor and the transformer must be zero. Then, the relationship among V_L, V_H, and the dc component of v_{Cr}, V_{Cr0}, can be given by

$$V_H - V_{\text{Cr0}} = V_L + V_{\text{Cr0}}. \tag{2}$$

According to (2), $V_{Cr0} = (V_H - V_L)/2$. When the DI-DCX operates in range A and $V_L < V_H$, there will be a dc bias voltage on the resonant capacitor C_r. When the DI-DCX operates in range B and $V_L = V_H$, the dc bias voltage on C_r will be zero. Hence, for the DI-DCX, the dc bias voltage on C_r is the only difference of range A and range B.

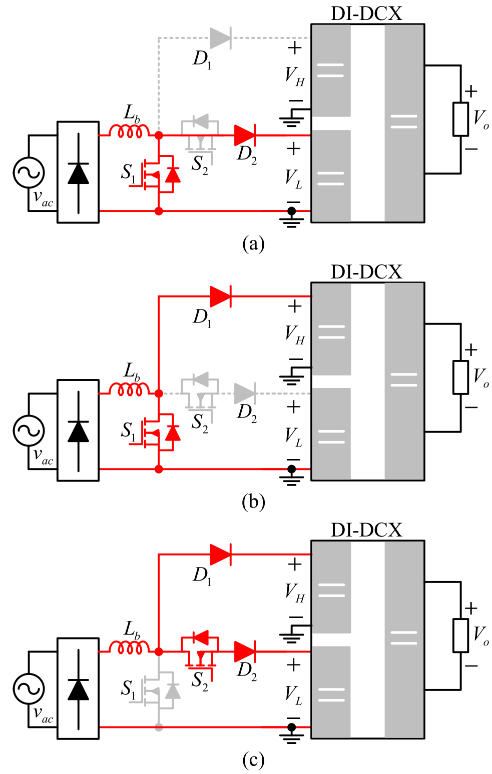

Fig. 6. Equivalent circuits of three operation modes of the DOR in range A. (a) V_L-SOM. (b) V_H-SOM. (c) DOM.

D. Operation Principle of the DOR

The input voltage v_{ac} is rectified by the rectifier bridge and becomes $v_{\text{dc}} = V_m|\sin(\omega t)|$, where V_m is the peak value of v_{dc} and ω is the angular frequency of grid voltage. In range A, the DOR has three possible operation modes within half of the grid voltage cycle whose equivalent circuits are shown in Fig. 6.

1) In V_L single output mode $(V_L - \text{SOM})$, S_2 is always kept ON and D_1 is OFF since $V_H \geq V_L$. All the input power is delivered to the low-voltage port V_L. The duty cycle of S_1 in this mode is

$$d_{1\_V_L-\text{SOM}} = 1 - \frac{V_m\,|\sin\omega t|}{V_L}. \tag{3}$$

2) In V_H single output mode $(V_H - \text{SOM})$, S_2 is always kept OFF and all the input power is delivered to the high-voltage port V_H. The duty cycle of S_1 in this mode is

$$d_{1\_V_H-\text{SOM}} = 1 - \frac{V_m\,|\sin\omega t|}{V_H}. \tag{4}$$

3) In dual-output mode (DOM), S_1 is always kept OFF and S_2 takes effect to control the input power distribution between

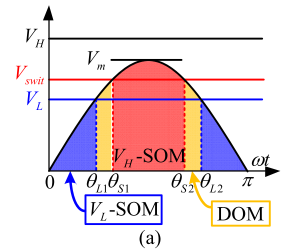

Fig. 7. Sketch diagram of operation modes allocation of the DOR. (a) $V_L < V_{\text{swit}}$. (b) $V_L \geq V_{\text{swit}}$.

the two output ports. The duty cycle of S_2 is

$$d_{2\_\text{DOM}} = 1 - \frac{V_m\,|\sin\omega t| - V_L}{V_H - V_L}. \tag{5}$$

It can be observed that each operation mode corresponds to a boost circuit with different input and output voltages. According to the operating conditions of the boost circuit, $V_H - \text{SOM}$ is always available since $V_H > V_m$, whereas $V_L - \text{SOM}$ and DOM can only exist under certain conditions. θ_{L1} and θ_{L2} are used to represent the two moments corresponding to $V_L = v_{\text{dc}}$ in half of the grid voltage period when $V_L < V_m$. The calculation formulas of θ_{L1} and θ_{L2} are

$$\begin{cases} \theta_{L1} = \arcsin\left(V_L/V_m\right) \\ \theta_{L2} = \pi - \arcsin\left(V_L/V_m\right). \end{cases} \tag{6}$$

The possible operation intervals of $V_L - \text{SOM}$ are [0, θ_{L1}] and [θ_{L2}, π], whereas the possible operation interval of DOM is [θ_{L1}, θ_{L2}]. To reduce switching losses of the DOR, $V_L - \text{SOM}$ and DOM should be selected first when their conditions are satisfied. In addition to that, a switching voltage V_{swit} is introduced to regulate the power distribution of the two output ports, and the value of V_{swit} is between 0 and V_m. The corresponding switching points are

$$\begin{cases} \theta_{S1} = \arcsin\left(V_{\text{swit}}/V_m\right) \\ \theta_{S2} = \pi - \arcsin\left(V_{\text{swit}}/V_m\right). \end{cases} \tag{7}$$

As shown in Fig. 7(a), if $V_L < V_{\text{swit}}$, the DOR switches among $V_L - \text{SOM}$, DOM, and $V_H - \text{SOM}$. If $V_L \geq V_{swit}$ (either higher or lower than V_m), the DOR switches between $V_L - \text{SOM}$ and $V_H - \text{SOM}$ as plotted in Fig. 7(b). By changing the value of V_{swit}, the acting time of different operation modes can be changed, thereby the power transmitted to the two output ports of the DOR can be regulated.

It should be noted that $V_H - \text{SOM}$ must be used to make sure the power distribution between V_L and V_H ports satisfies the requirement of the downstream DI-DCX. For any given values of V_m, V_L, and V_H, there is only one valid V_{swit} value to achieve equal currents of V_L and V_H ports, as required by the DI-DCX. Detailed analysis on the power distribution ratio of the converter with respect to V_{swit} will be given in Section IV.

In range B, the two output voltages of the DOR are equal and the corresponding equivalent circuit is shown in Fig. 8. The duty cycle of S_1 in this range is

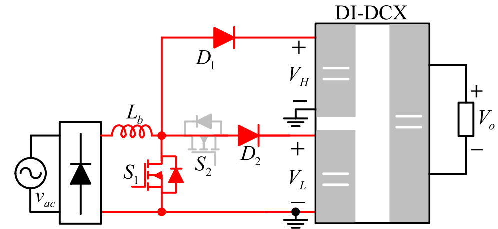

Fig. 8. Equivalent circuit of the DOR in range B.

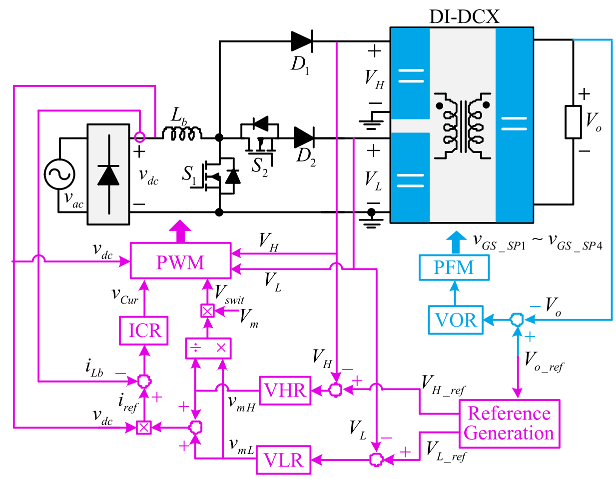

Fig. 9. Control block diagram of the ac–dc converter.

$$d_{1\_\text{range}\_B} = 1 - \frac{V_m\,|\sin\omega t|}{V_H} = 1 - \frac{V_m\,|\sin\omega t|}{V_L}. \tag{8}$$

Since V_L and V_H are equal, the input power is evenly distributed to the two output ports. There is no operation modes switching in range B. The DOR works like a conventional boost PFC converter, except that it has an additional output voltage port.

III. Control Strategy of the AC–DC Converter

A. *Control Scheme of the DOR*

The control block diagram of the DOR is shown in Fig. 9. Similar to the control of a conventional boost PFC converter, outer voltage loop and inner current loop are employed to regulate the inductor current and output voltage of the DOR. However, different from a conventional single output PFC converter, two voltage loops are used to regulate V_L and V_H ports simultaneously.

The voltage reference for the V_L and V_H ports is generated based on the output voltage of the DI-DCX to optimize the operation of the DI-DCX

$$\frac{(V_{L\_\text{ref}} + V_{H\_\text{ref}})}{2} \cdot \frac{N_S}{N_P} = V_{o\_\text{ref}} \tag{9}$$

where N_P and N_S are the number of turns of the primary and secondary sides of the transformer of the DI-DCX. The equivalent gain of the DI-DCX can be regarded as 1 since it operates around the resonant frequency. According to the voltage regulation principle of the converter, in range A, V_{H_ref} is fixed and V_{L_ref} varies with V_{o_ref}. In range B, V_{H_ref} and V_{L_ref} are equal, and they change simultaneously with the change of V_{o_ref}.

VLR and VHR are two voltage regulators, and their outputs are v_{mL} and v_{mH}, respectively. V_{swit} is determined by the quotient of v_{mL} and v_{mH}. Take the V_L port as an example to illustrate the function of V_{swit}. If V_L suddenly decreases, then the output of the VLR, i.e., v_{mL}, will increase, causing V_{swit} to increase. It will be analyzed in Section IV that the increase in V_{swit} will increase the power delivered to the V_L port, and the voltage of V_L rises. A similar analysis can also be done for the V_H port. It can be seen that the voltage of the two ports can be accurately regulated by the generation principle of V_{swit}. In addition, the value of V_{swit} is updated online since v_m is detected online, and v_{mL} and v_{mH} are updated in real time.

ICR is the inner current loop regulator. Since the total power of the converter is determined by both high and low voltage output ports, the sum of v_{mL} and v_{mH} is used to generate the reference i_{ref} of the inductor current. The output of ICR is v_{Cur}.

B. Adaptive PWM Strategy

PWM strategy for the DOR is illustrated in Fig. 10, where Fig. 10(a) shows the case that the DOR switches among $V_L -$ SOM, DOM, and $V_H -$ SOM in range A, Fig. 10(b) shows the case that DOR switches between $V_L -$ SOM and $V_H -$ SOM in range A, and Fig. 10(c) shows the case of range B.

v_{Cur} is directly used to generate the driving signal of S_1 in $V_H -$ SOM, whereas v_{C1} and v_{C2} are derived from v_{Cur}, and they only take effect in $V_L -$ SOM and DOM to generate the driving signals of S_1 and S_2, respectively.

As shown in Fig. 10(a), transition between $V_L -$ SOM and DOM is natural and smooth by employing a dual-carrier modulation strategy. But mode switching between $V_L -$ SOM and $V_H -$ SOM, or between DOM and $V_H -$ SOM, is determined by V_{swit}. When switching between $V_L -$ SOM and $V_H -$ SOM, the duty cycle of S_1 will be changed suddenly, and when switching between DOM and $V_H -$ SOM, the high-frequency operated switch will be changed from S_2 to S_1, or from S_1 to S_2. In order to achieve smooth switching between any of the modes, a basic criterion is to ensure the volt–second balance of the inductor L_b before and after mode switching.

The average voltage at the left end of L_b is always v_{dc}, and the average voltage at the right end, i.e., the average drain–source voltage of S_1 can be calculated by (10) according to the operation principle and PWM strategy of the DOR

$$\bar{v}_{\mathrm{DS}\_S1} = \begin{cases} V_L\left(1-d_{1\_V_L-\mathrm{SOM}}\right) = V_L\left(2-v_{C1}\right) & V_L-\mathrm{SOM} \\ V_L d_{2\_\mathrm{DOM}} + V_H\left(1-d_{2\_\mathrm{DOM}}\right) & \\ = V_L v_{C2} + V_H\left(1-v_{C2}\right) & \mathrm{DOM} \\ V_H\left(1-d_{1\_V_H-\mathrm{SOM}}\right) = V_H\left(2-v_{\mathrm{Cur}}\right) & V_H-\mathrm{SOM}. \end{cases} \tag{10}$$

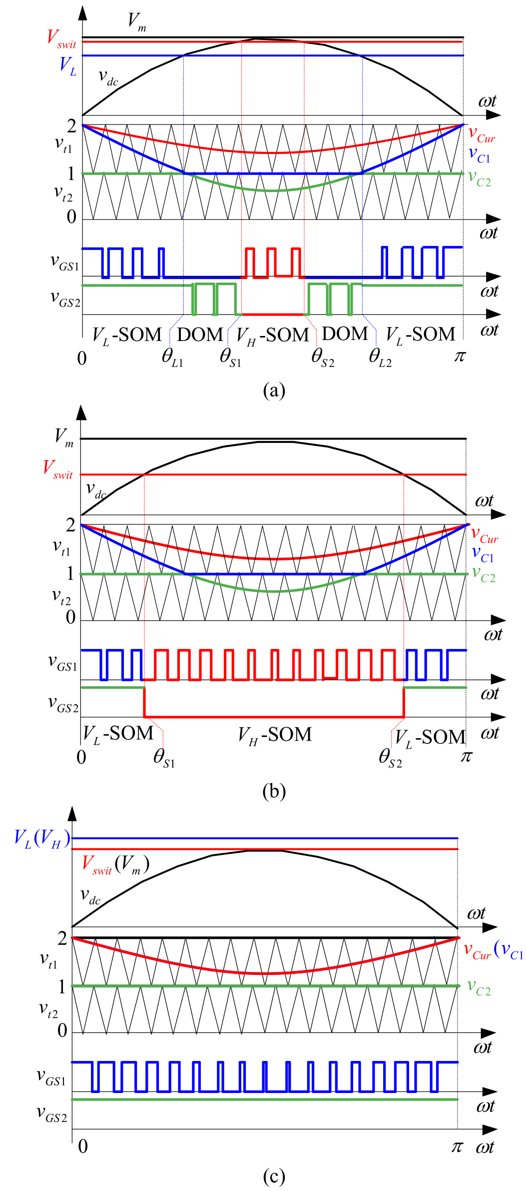

Fig. 10. PWM strategy of the DOR. (a) Switching among $V_L -$ SOM, DOM, and $V_H -$ SOM in range A. (b) Switching between $V_L -$ SOM and $V_H -$ SOM in range A. (c) Case of range B.

Since the average voltage at the right end of L_b is equal in either operation mode, the expressions of v_{C1} and v_{C2} can be derived from (10) as follows:

$$\begin{cases} v_{C1} = \frac{V_H v_{\mathrm{Cur}} - 2(V_H - V_L)}{V_L} \\ v_{C2} = \frac{V_H(v_{\mathrm{Cur}}-1)}{V_H - V_L}. \end{cases} \tag{11}$$

As shown in Fig. 10, the carriers corresponding to v_{C1} and v_{C2} are v_{t1} and v_{t2}, respectively. Since the valley and peak values of carrier v_{t1} are 1 and 2, whereas the valley and peak values of carrier v_{t2} are 0 and 1, the minimum value of v_{C1} and the

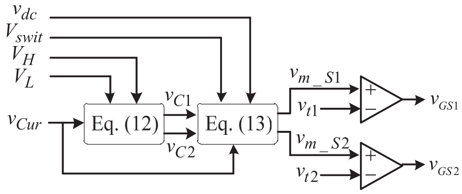

Fig. 11. Implementation of the PWM strategy for the DOR.

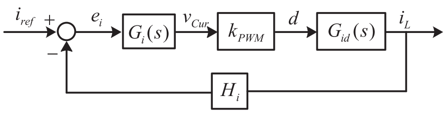

Fig. 12. Simplified control block diagram of the current loop.

maximum value of v_{C2} should be limited

$$\begin{cases} v_{C1} = \max\left[1, \frac{V_H v_{\mathrm{Cur}} - 2(V_H - V_L)}{V_L}\right] \\ v_{C2} = \min\left[1, \frac{V_H(v_{\mathrm{Cur}} - 1)}{V_H - V_L}\right]. \end{cases} \tag{12}$$

As analyzed, v_{Cur} is directly used to generate the driving signal of S_1 in $V_H - \mathrm{SOM}$, whereas v_{C1} and v_{C2} only take effect in $V_L - \mathrm{SOM}$ and DOM. In order to describe this issue clearly, v_{m_S1} and v_{m_S2} are used to represent the modulation waveforms that are ultimately used to generate the driving signals for S_1 and S_2, and the expressions are as follows:

$$\begin{cases} v_{m\_S1} = v_{C1}, \quad v_{m\_S2} = v_{C2} \quad v_{\mathrm{dc}} < V_{\mathrm{swit}} \\ v_{m\_S1} = v_{\mathrm{Cur}}, \quad v_{m\_S2} = 0 \quad\quad v_{\mathrm{dc}} \geq V_{\mathrm{swit}}. \end{cases} \tag{13}$$

Then, the driving signals for S_1 and S_2, i.e., v_{GS1} and v_{GS2}, can be obtained by comparing v_{m_S1} and v_{m_S2} with carrier waveforms v_{t1} and v_{t2}. Complete implementation of the PWM strategy for the DOR is shown in Fig. 11.

The PWM strategy is still effective in range B of the DOR. In range B, V_{swit} reaches its upper limit V_m; therefore, v_{dc} is always lower than V_{swit}. As drawn in Fig. 10(c), there is no mode switching in range B. v_{Cur} and v_{C1} are equal, and the value of v_{C2} is limited to 1. It means that only switch S_1 operates at the PWM state and S_2 is kept ON. Since V_L is equal to V_H, both diodes D_1 and D_2 are ON and the input power is evenly converted to two output ports simultaneously.

C. Analysis of the Current Loop

The simplified control block diagram of the current loop is shown in Fig. 12, where $G_i(s)$ represents the regulator in ICR, k_{PWM} is the gain of the PWM modulator, $G_{id}(s)$ is the transfer function of duty cycle to the inductor current, and H_i is the current sampling coefficient.

As analyzed in [22], $G_{id}(s)$ can be regarded as a first-order inertial element. According to the operation principle of the DOR, the expression of $G_{id}(s)$ in the three operation modes is derived as

$$G_{id}(s) = \begin{cases} \frac{V_L}{sL_b} & V_L - \mathrm{SOM} \\ \frac{V_H - V_L}{sL_b} & \mathrm{DOM} \\ \frac{V_H}{sL_b} & V_H - \mathrm{SOM}. \end{cases} \tag{14}$$

By using the PWM strategy analyzed earlier, the gain of the PWM modulator can be derived

$$k_{\mathrm{PWM}} = \begin{cases} \frac{d(v_{C1} - 1)}{dv_{\mathrm{Cur}}} = \frac{V_H}{V_L} & V_L - \mathrm{SOM} \\ \frac{dv_{C2}}{dv_{\mathrm{Cur}}} = \frac{V_H}{V_H - V_L} & \mathrm{DOM} \\ \frac{d(v_{\mathrm{Cur}} - 1)}{dv_{\mathrm{Cur}}} = 1 & V_H - \mathrm{SOM}. \end{cases} \tag{15}$$

The product of $G_{id}(s)$ and k_{PWM} in the three operation modes can be calculated as

$$G_{id}(s) \cdot k_{\mathrm{PWM}} = \frac{V_H}{sL_b}. \tag{16}$$

According to (16), the gain of k_{PWM} plus $G_{id}(s)$ is fixed in different operation modes. Then, the current loop regulator ICR can be designed using the method of a conventional boost PFC converter [23].

D. Control Strategy of the DI-DCX

In order to suppress the twice grid frequency power ripple of the intermediate ports, the switching frequency of the DI-DCX is regulated within a narrow range around the resonant frequency. Then, pulse frequency modulation is used to generate the driving signals of the DI-DCX.

Since the average input current of the two ports of the DI-DCX is equal, and the equivalent input voltage is $(V_H + V_L)/2$, the DI-DCX can be regarded as a conventional *LLC* converter. The small signal modeling approach discussed in [24] can be referenced to design the regulator for the DI-DCX.

However, unlike the conventional variable-frequency *LLC* converter, the *LLC* converter proposed in this paper only operates around the resonant frequency, and it has two inputs. In order to distinguish it from the conventional *LLC* converter, it is called DI-DCX.

IV. CHARACTERISTICS OF THE DOR

A. Power Distribution Ratio

In order to provide guidance for the design of circuit parameters, the ratio of the power converted to V_L in total input power should be deduced. Assume that the converter has no power loss and has a unit input PF. The instantaneous input power of the grid during the positive half cycle is

$$p_{\mathrm{in}} = \frac{V_m I_m}{2}(1 - \cos 2\omega t) \tag{17}$$

where I_m is the peak value of input current i_{ac}.

Assume that the input current remains constant in one switching cycle and use $p_{L\_VL-\mathrm{SOM}}$ and p_{L_DOM} to represent the instantaneous powers converted to V_L in $V_L - \mathrm{SOM}$ and DOM,

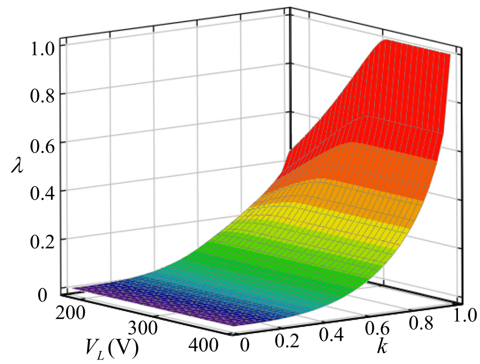

Fig. 13. Relationship of λ and k under different V_L.

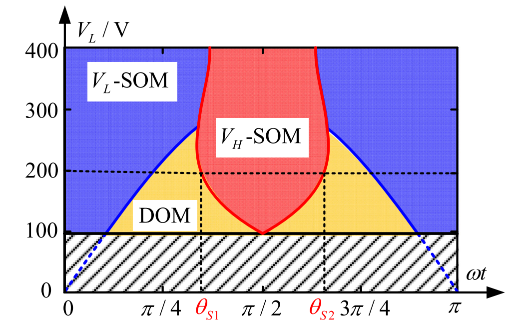

Fig. 14. Operation modes allocation.

respectively. They can be expressed by

$$\begin{cases} p_{L\_V_L\text{-SOM}} = p_{\text{in}} = \frac{V_m I_m}{2}(1-\cos 2\omega t) \\ p_{L\_\text{DOM}} = I_m \sin\omega t \cdot d_{2\_\text{DOM}} \cdot V_L. \end{cases} \tag{18}$$

According to Fig. 7, the power absorbed by the low-voltage port P_L when $V_L < V_{\text{swit}}$ and $V_L \geq V_{\text{swit}}$ can be calculated by integrating $p_{L\_VL\text{-SOM}}$ and p_{L_DOM} over the positive half of the grid voltage period as follows:

$$P_L = \begin{cases} \frac{2}{\pi}\int_0^{\theta_{L1}} p_{L\_V_L\text{-SOM}} d\omega t \\ \quad + \frac{2}{\pi}\int_{\theta_{L1}}^{\theta_{S1}} p_{L\_\text{DOM}} d\omega t & V_L < V_{\text{swit}} \\ \frac{2}{\pi}\int_0^{\theta_{S1}} p_{L\_V_L\text{-SOM}} d\omega t & V_L \geq V_{\text{swit}}. \end{cases} \tag{19}$$

Then, the ratio of the power converted to the low-voltage port in total input power λ can be obtained by (20) shown at the bottom of this page, where $k = V_{\text{swit}}/V_m$.

It should be noted that, for the proposed DOR, V_{swit} is the key to regulate the power distribution of the two output ports, and its value is between 0 and V_m. For the simplicity of the expression, θ_{S1} is used to represent the corresponding switching angle, and $\theta_{S1} = \arcsin(V_{\text{swit}}/V_m) = \arcsin(k)$.

The relationship of λ and k under different V_L is drawn in Fig. 13. It can be observed that λ increases with the increase in k under different V_L, and they show positive correlation characteristics and are monotonous, which confirms that V_{swit} can be used to allocate the power of the two output ports of the DOR. It can also be observed that when $V_L < V_m$, the maximum value of λ increases with the increase in V_L. If $V_L > V_m$, the maximum value of λ can reach 1, which means that all the input power can be transmitted to the low-voltage port.

B. Calculation of Switching Point Angles

Since the two input currents of the DI-DCX are equal, the ratio of the power required by the low-voltage port to the total output power of the DOR can be calculated by

$$\lambda_{\text{load}} = \frac{V_L}{V_L + V_H}. \tag{21}$$

When the DOR works normally, the power transfer ratios obtained from (20) and (21) must be equal, so the switching voltage V_{swit} can be solved. Therefore, the corresponding switching point angles θ_{S1} and θ_{S2} and $k = \sin(\theta_{S1})$ can also be obtained. Fig. 14 shows the operation modes allocation diagram when $V_m = 311$ V and $V_H = 400$ V. The red boundary line refers to the angle corresponding to the switching point. And the blue boundary line refers to the instantaneous grid voltage v_{dc}. The shaded part at the bottom shows that the solution of the switch point is not found.

For example, if $V_L = 200$ V, draw a horizontal line and get the intersection with the red boundary line. Then, draw two vertical lines from these two points. The intersections with the abscissa are the angles θ_{S1} and θ_{S2}. In addition, it can also be found that the DOR switches among $V_L -$ SOM, DOM, and $V_H -$ SOM when $V_L = 200$ V.

C. Voltage Selection Range of the Low-Voltage Port

From Fig. 13, it can be observed that when $k = 1$, λ reaches its maximum value $\lambda_{\max}$. The expression of $\lambda_{\max}$ can be obtained by substituting $k = 1$ (i.e., $\theta_{S1} = \pi/2$) into (20)

$$\lambda_{\max} = \frac{-\pi V_L V_m + 2V_H V_L \cos\theta_{L1} + 2V_H V_m \theta_{L1}}{\pi V_m (V_H - V_L)}. \tag{22}$$

To make the DOR operate normally, $\lambda_{\max} \geq \lambda_{\text{load}}$ must be satisfied. Based on this limitation, the minimum value of V_L can be obtained and is denoted as V_{Lmin1}.

For example, curves of $\lambda_{\max}$ and λ_{load} with respect to V_L when $V_H = 400$ V are depicted in Fig. 15, it is shown that V_{Lmin1} is located at the crossing point of λ_{load} and $\lambda_{\max}$ when $v_{ac} = 240$ VAC. The selectable range of V_L is from V_{Lmin1} to V_H.

$$\lambda = \frac{P_L}{\frac{1}{\pi}\int_0^{\pi} p_{\text{in}} d\omega t} = \begin{cases} \frac{V_L V_m[\sin(2\theta_{S1}) - 2\theta_{S1}] - 4V_H V_L \cos(\theta_{S1}) + 2V_H V_L \cos\theta_{L1} + 2V_H V_m \theta_{L1}}{\pi V_m (V_H - V_L)} & \frac{V_L}{V_m} < k \leq 1 \wedge V_L < V_m \\ \frac{1}{\pi}[2\theta_{S1} - \sin(2\theta_{S1})] & 0 < k \leq \frac{V_L}{V_m} \vee V_L \geq V_m \end{cases} \tag{20}$$

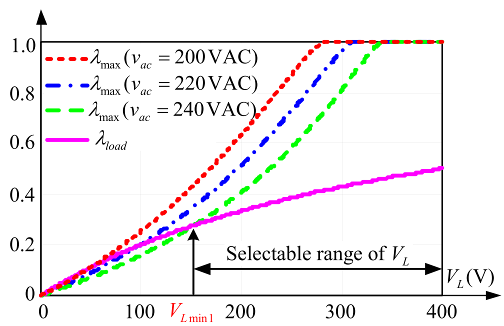

Fig. 15. Curves of $\lambda_{\max}$ and λ_{load} with respect to V_L when $V_H = 400$ V.

TABLE I
SYSTEM SPECIFICATIONS

Grid voltage (v_{ac})	200~240 VAC
DC Output voltage (V_o)	240~360 V
Maximum output power (P_{out})	1.5 kW
Switching frequency of the DOR (f_{DOR})	100 kHz
Resonant frequency of the DI-DCX (f_r)	100 kHz

V. Design Considerations of the AC–DC Converter

A 1.5-kW ac–dc converter is adopted as an example to explore the main design considerations. The system specifications are given in Table I.

A. Selection of VH, VL, and Turns Ratio of the Transformer in the DI-DCX

According to the voltage regulation principle of the converter, the whole output voltage range is divided into range A and range B. In range A, V_H is fixed, and only V_L is adjustable. In range B, V_L and V_H are equal, and they are both flexible.

The turns ratio of the transformer in the DI-DCX is determined by the value of V_H in range A, the selected minimum value of V_L in range A, and the minimum value of V_o. They are denoted as V_{H_RA}, V_{Lmin2}, and $V_{o\_\min}$, respectively.

The voltage of V_H should be as low as possible to reduce the switching loss while ensuring that it is always higher than the peak value of the grid voltage. Referring to the conventional boost PFC converter, its output voltage is generally between 380 and 420 V. Therefore, $V_{H\_\text{RA}} = 400$ V is selected.

As analyzed, the criterion to choose the value of V_L is based on the power distribution ratio of the DOR. V_{Lmin1} is about 160 V as shown in Fig. 15, reserving some voltage margin, the value of V_{Lmin2} is selected as 180 V.

The equivalent input voltage of the DI-DCX is $(V_H + V_L)/2$, and its equivalent gain can be regarded as 1 since it operates around the resonant frequency. Then, the turns ratio of the transformer of the DI-DCX can be derived as

$$\frac{N_P}{N_S} = \frac{V_{H\_\text{RA}} + V_{L\text{min2}}}{2V_{o\_\min}} = \frac{29}{24} \tag{23}$$

where N_P and N_S are the number of turns of the primary and secondary sides of the transformer, respectively.

After the turns ratio is determined, the maximum values of V_H and V_L can be derived according to the maximum value of V_o. When V_L reaches its maximum value of 400 V in range A, the corresponding output voltage of the ac–dc converter is 331 V. Therefore, the maximum values of V_L and V_H in range B are 435 V so that the output voltage reaches 360 V.

B. Selections of the Capacitors and Inductor in the DOR

The design of the capacitors in V_L and V_H is still the same as a conventional boost PFC converter. The voltage ripple on capacitors is the main consideration. The capacitors are designed by setting the peak-to-peak voltages of the capacitors within 5% of its average value. The selected values of C_L and C_H are 940 and 820 μF, respectively.

The inductor current ripple is the main consideration when designing the inductor. According to the operation principle of the DOR, the required inductance value in different modes can be derived as

$$L_b \geq \begin{cases} \frac{V_L d_{1\_V_L\text{-SOM}}(1-d_{1\_V_L\text{-SOM}})}{\Delta i_{Lb\max} f_{\text{DOR}}} & V_L\text{–SOM} \\ \frac{(V_H-V_L) d_{2\_\text{DOM}}(1-d_{2\_\text{DOM}})}{\Delta i_{Lb\max} f_{DORs}} & \text{DOM} \\ \frac{V_H d_{1\_V_H\text{-SOM}}(1-d_{1\_V_H\text{-SOM}})}{\Delta i_{Lb\max} f_{\text{DOR}}} & V_H\text{–SOM.} \end{cases} \tag{24}$$

The maximum inductor current ripple $\Delta i_{Lb\max}$ is designed to be 25% of the maximum input current. As a result, 400 μH is selected for the inductor L_b.

C. Design of the DI-DCX

Since the average input currents of the two ports of the DI-DCX are equal, and the equivalent input voltage is $(V_H + V_L)/2$, the DI-DCX can be designed using the method of a conventional *LLC* converter, considering a variation range of $\pm$2.5% of its input voltage. The design approaches analyzed in [25] are referenced to design the DI-DCX. The selected switching frequency range is from 80 to 120 kHz, and the parameters of the resonant tank are: $L_r = 31.66$ μH, $C_r = 80$ nF, and $L_m = 362$ μH.

VI. Experimental Verification

A 1.5-kW prototype was built to verify the effectiveness and evaluate the performance of the proposed ac–dc converter. The output voltage range is 240–360 V. The voltage ranges of V_L and V_H are 180–435 V and 400–435 V, respectively. When V_L is in the range of 180–400 V, V_H is fixed at 400 V. When V_L is higher than 400 V, V_L and V_H are equal, and they change together in the range of 400–435 V. Referring to the conventional Si device based converter, the switching frequency of DOR and the resonant frequency of DI-DCX are selected as 100 kHz. The turns ratio of the transformer in DI-DCX is set to be 29:24. The model numbers of the power devices are as follows, S_1 and S_2: IPW60R070C6, D_1 and D_2: SCS230AE2, $S_{P1} - S_{P4}$: IPW65R110CFD, and $D_{R1} - D_{R4}$: DSEC30 – 06 A.

Steady-state experimental waveforms of the DOR when $v_{\text{ac}} =$ 220 VAC and $V_o = 240$ V at full load are presented in Fig. 16. In this case, V_L and V_H are 180 and 400 V, respectively. In Fig. 16(a), v_{GS_S1} and v_{GS_S2} are the driving voltages of S_1 and S_2, v_{dc} is the rectified input voltage, and i_{Lb} is the current flowing through the inductor L_b. It can be observed that the DOR switches between the three operation modes of V_L – SOM,

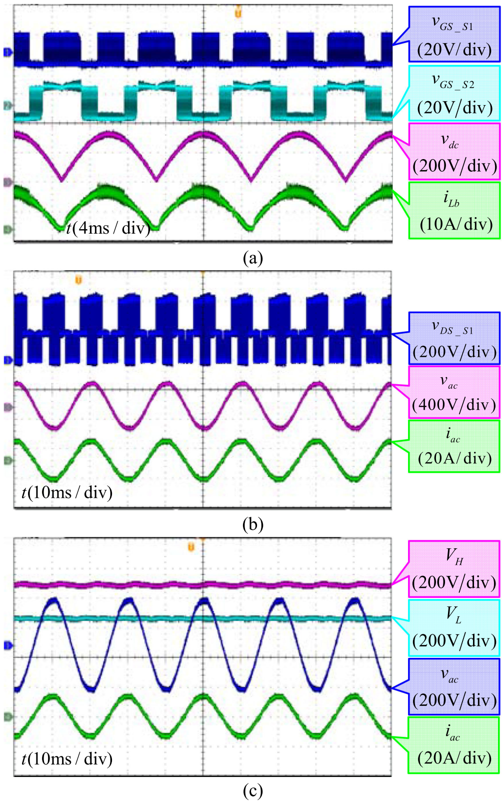

Fig. 16. Steady-state experimental waveforms of the DOR. (a) Waveforms of v_{GS_S1}, v_{GS_S2}, $v_{\rm dc}$, and i_L. (b) Waveforms of v_{DS_S1}, $v_{\rm ac}$, and $i_{\rm ac}$. (c) Waveforms of V_H, V_L, $v_{\rm ac}$, and $i_{\rm ac}$.

DOM, and V_H – SOM, and the input current can track grid voltage well in all these modes. In Fig. 16(b), v_{DS_S1} is the drain–source voltage of S_1, whereas $v_{\rm ac}$, and $i_{\rm ac}$ are the input voltage and current. It is obvious that v_{DS_S1} has three voltage levels of 0, V_L, and V_H. And corresponding to the three operation modes of V_L – SOM, DOM, and V_H – SOM, v_{DS_S1} is switched between 0 and V_L, V_L and V_H, and 0 and V_H, respectively. This three-level feature helps to reduce switching losses of the proposed converter. In Fig. 16(c), the voltage waveforms of V_L, V_H, and $v_{\rm ac}$ are put together to show their relationship. As discussed earlier, V_L is adjustable within a wide voltage range and can be lower than the peak value of $v_{\rm ac}$, whereas V_H is always higher than the peak value of $v_{\rm ac}$.

Steady-state experimental waveforms of the DI-DCX when the output voltage is 300 V at full load are shown in Fig. 17. The waveforms from top to bottom in Fig. 17(a) are resonant capacitor voltage v_{Cr}, resonant inductor current i_{Lr}, driving voltage, and drain–source voltage of S_{P2} respectively. While the driving voltage and drain–source voltage waveforms of S_{P4} are shown in Fig. 17(b). It can be observed that ZVS is achieved by both S_{P2} and S_{P4}. The resonant capacitor voltage contains a positive offset of approximately 40 V. While the positive and negative half cycles of the resonant inductor current waveform are symmetrical. These experimental waveforms are in good agreement with the theoretical analysis.

Fig. 18 shows the experimental waveform when the grid voltage changes from 260 to 100 VAC at half load. The output voltage is 300 V, and the corresponding voltages of V_L and V_H are

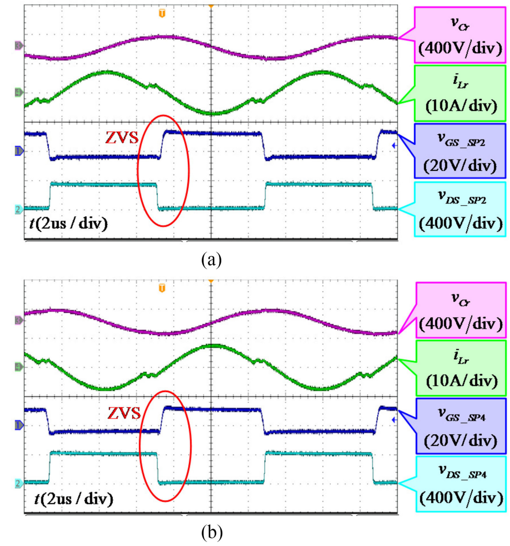

Fig. 17. Steady-state experimental waveforms of the DI-DCX. (a) Waveforms of v_{Cr}, i_{Lr}, v_{GS_SP2}, and v_{DS_SP2}. (b) Waveforms of v_{Cr}, i_{Lr}, v_{GS_SP4}, and v_{DS_SP4}.

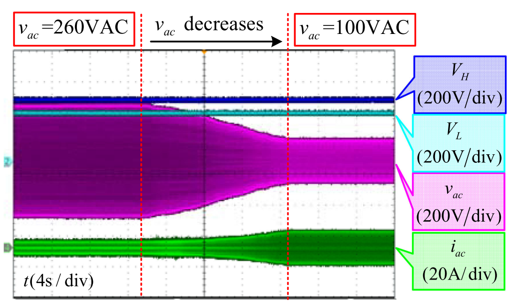

Fig. 18. Experimental waveform when the grid voltage changes from 260 to 100 VAC at half load.

325 and 400 V. It can be seen that both V_L and V_H are regulated well and kept constant during the changing of input voltage.

The waveforms of stepping load between half load and full load are given in Fig. 19. It is shown that the converter can operate well even when the output power is changed.

Efficiency curves of the DOR, DI-DCX, and the whole ac–dc converter when $v_{\rm ac} = 220$ VAC are provided in Fig. 20. Efficiency of the DOR shown in Fig. 20(a) is tested in range A with $V_H = 400$ V. It can be seen that when V_L increases, the efficiency of the DOR decreases. Therefore, if only a narrow range of V_L is required when designing the converter, choosing a lower value of V_L is better for efficiency. The efficiency curves in Fig. 20(b) and (c) are tested over the full output voltage range. As shown in Fig. 20(b), the highest efficiency of DI-DCX is more than 98%. From Fig. 20(c), it can be seen that high power conversion efficiency is also achieved by the proposed ac–dc converter, the measured highest efficiency is about 96.2%.

Fig. 21 shows the tested efficiency of the ac–dc converter when the grid voltage range is 100–260 V and the output voltage is 300 V. It should be noted that, considering the current stress of the devices of the experimental setup, when the grid voltage is lower than 180 VAC, the maximum power has to be degraded

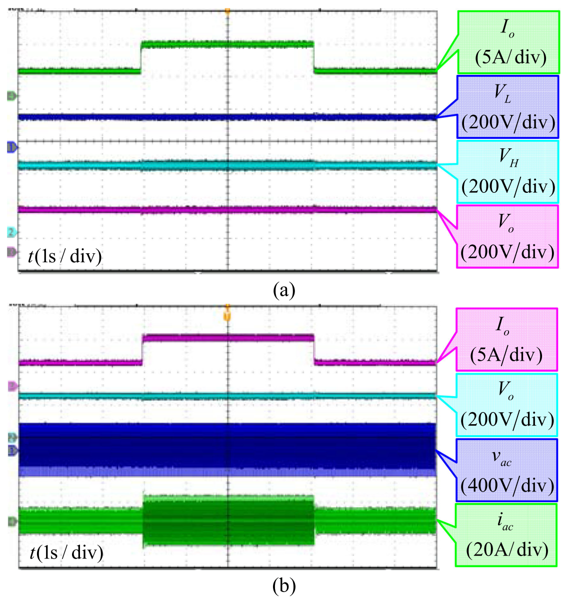

Fig. 19. Experimental waveforms when load steps up and down. (a) Waveforms of I_o, V_L, V_H, and V_o. (b) Waveforms of I_o, V_o, v_{ac}, and i_{ac}.

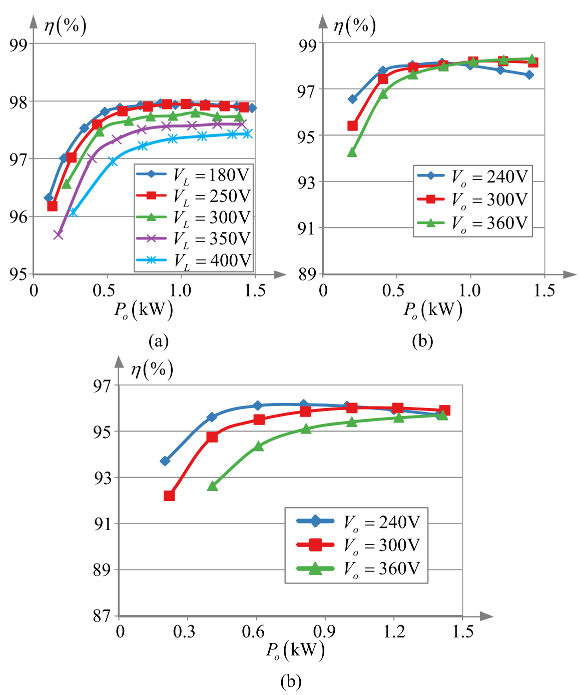

Fig. 20. Tested efficiency curves of the converter. (a) Efficiency of the DOR. (b) Efficiency of the DI-DCX. (c) Efficiency of total ac–dc converter.

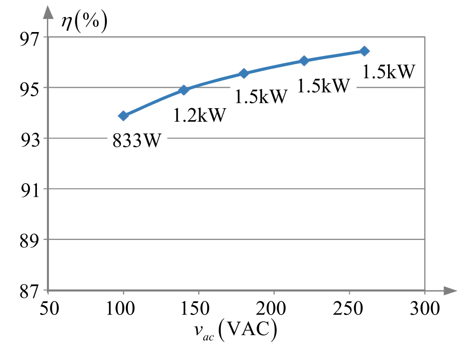

Fig. 21. Tested efficiency of the ac–dc converter when the grid voltage range is 100–260 VAC and the output voltage is 300 V.

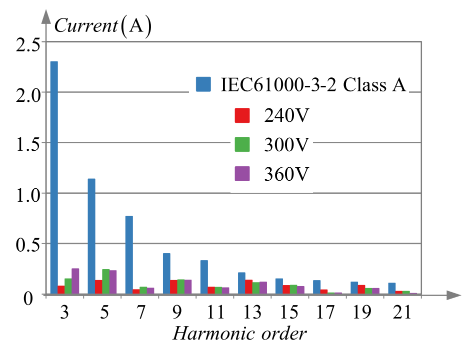

Fig. 22. Tested input current harmonic content under different output voltages.

according to the designed maximum input ac current. It can be observed that as the grid voltage increases, the efficiency of the converter also increases.

Tested input current harmonic content when v_{ac} is 220 VAC at full load is shown in Fig. 22. It can be observed that the magnitude of each harmonic current under different output voltages can all meet the requirements of IEC61000-3-2 Class A limits.

VII. Conclusion

An ac–dc converter composed of a DOR and a DI-DCX is presented in this paper. The ac input voltage is split into two dc bus voltages by the DOR, and then combined by the DI-DCX to form an adjustable output voltage. Output voltage regulation is achieved with the DOR directly regulating the voltages of the two dc buses. Therefore, there is no output voltage regulation requirement for DI-DCX, and it can always run as a high-efficiency DCX. Operation principles and characteristics of both the DOR and DI-DCX are analyzed in detail. It can be found that the DOR has three-level output voltage, and DI-DCX can realize ZVS of the switches within full operating range, which further improves the overall efficiency. Control and modulation strategies with which to regulate the grid current, the two intermediate buses, and the output voltage are illustrated. Experimental results obtained from the prototype are presented to validate the theoretical analysis and show the effectiveness of the proposed ac–dc converter.

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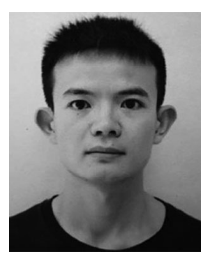

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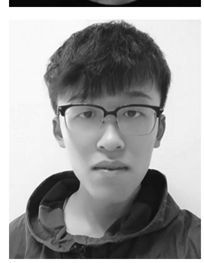

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