Resonant Bridgeless AC/DC Rectifier With High Switching Frequency and Inherent PFC Capability

Hamed Valipour, *Student Member, IEEE*, Mohammad Mahdavi, and Martin Ordonez, *Member, IEEE*

***Abstract*—Boost-based converters are used in a variety of non-isolated step-up applications, such as power factor correctors, because of their simplicity. The power density of these converters can be increased in higher switching frequencies, which reduces the size of the magnetic elements. This increases the switching losses, but that can be solved by soft-switching techniques. This paper proposes a resonant bridgeless power factor correction converter that provides soft switching for all of the semiconductors. The proposed structure can provide zero voltage switching for the switches and zero current switching for the diodes. In the proposed structure, the input current is inherently sinusoidal with low total harmonic distortion, even with small inductances. Therefore, a high input power factor is achieved without requiring a current control loop in the circuit. This reduces the complexity of the control circuit. An experimental prototype has been constructed to investigate the validity of the claims. Experimental results show near-unity power factor, as well as 2% efficiency improvement at full load when compared to a conventional interleaved boost converter with the same components.**

***Index Terms*—AC/DC converter, boost, bridgeless, high frequency, new converter, power factor correction (PFC), resonant, soft switching.**

I. Introduction

IN ORDER to be able to fulfill the requirements of the standards such as IEC61000-3-2, power factor correction (PFC) converters should be employed [1]. Boost converters are traditionally used as the non-isolated PFC structures after a diode bridge rectifier. This topology is widely used because of its simplicity [2]–[4]. This converter has many advantages, including its simplicity, but also has some disadvantages, namely higher control complexity, high conduction losses because of the diode bridge, and switching losses, which restrict the converter's efficiency in higher switching frequencies[5]. The other popular traditional solution is the Flyback converter, which is dominant in isolated applications with very low power [6]–[8]. To solve the aforementioned problems in the traditional boost converter, many techniques have been proposed in the literature. The ideas presented for increasing the efficiency can be divided into three main categories.

Manuscript received October 22, 2018; revised January 26, 2019; accepted April 2, 2019. Date of publication April 10, 2019; date of current version October 18, 2019. This work was supported by the Natural Sciences and Engineering Research Council, Canada. Recommended for publication by Associate Editor T. Shimizu. *(Corresponding author: Hamed Valipour.)*

The authors are with the Department of Electrical and Computer Engineering, The University of British Columbia, Vancouver, BC V6T 1Z4, Canada (e-mail: hamed.valipour.v@ieee.org; mahdavi@ece.ubc.ca; mordonez@ieee.org).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2019.2910755

In the first category, soft-switching techniques are used to reduce the switching losses [9]–[13].

In the second category, conduction losses are reduced by using techniques such as bridgeless, single-stage, parallel PFC, and interleaving structures [11], [14]–[20]. Interleaved PFC is an emerging solution that has become particularly popular in the applications where a strict form factor has to be met, such as in slim notebook adapters, LCD TVs, flat screens, and OLED lighting panels [21]–[23]. Ultra flat converters have recently been proposed in some papers as a solution for providing power to those applications [24], [25]. Interleaving consists of paralleling two small stages in lieu of a bigger one, which may be more difficult to design. This approach has several merits like ease of implementation, use of more but smaller components, and better heat distribution. To further decrease the conduction losses, the input rectifier of the traditional PFC converter can be removed. This results in the bridgeless interleaved PFC converter [26]. With this method, the number of the semiconductor elements is reduced in the current flowing path.

In the third and last category, the first and second approaches are combined to simultaneously provide soft-switching conditions and reduce conduction losses [27]–[32]. There are two types of soft-switching techniques presented in the literature: providing soft switching for the PWM converters with constant switching frequency, and resonant-based approaches with variable switching frequency. Solutions based on constant switching frequencies usually need bigger sizes of inductors at the input [33]. While variable switching frequency converters have smaller inductors as resonant elements not as filter inductances [34]–[39]. So, potentially, the variable switching frequency converters have lower volume and weight. In [34] and [35], isolated resonant converters are studied. They suffer from lower efficiencies than their non-isolated counterparts because of the transformer losses. Therefore, it is better to use a non-isolated converter as a front-end PFC converter. Since a dc/dc converter as the second stage is needed to provide the voltage regulation for the load, this converter can provide the required isolation at the same time. In [36], [37], and [40], a resonant bridgeless PFC converter is proposed based on a resonant single-ended primary-inductor converter (SEPIC) converter. These converters have bridgeless structures, easy control with inherent PFC, and soft-switching capability. However, some of the SEPIC structure's problems still exist like the higher stress of the components, the bulky capacitor in the SEPIC structure, and also limited soft-switching capability. In [38] and [41], the same idea is presented in which soft-switching condition is provided by

using an extra switch. So, the number of the active elements is increased as well as the gate circuit required for the added semiconductor. A bridgeless resonant buck PFC converter is introduced in [39]. This converter provides soft-switching condition for the semiconductor elements and has inherent PFC capability. Therefore, the current loop can be removed in the controller, making the controller circuit very simple. A similar concept has been proposed in [42] for a buck converter with inherent PFC capability. However, in zero crossing points of the input voltage, when the output voltage is higher than the input, the input current is zero for a high fraction of the period. Therefore, it needs large filter elements in order to compensate the lower power factor when the output voltage is high. This converter also draws discontinuous current at the input, increasing total harmonic distortion (THD) and reducing the power factor.

In this paper, a resonant bridgeless boost PFC converter is proposed, shown in Fig. 1(a). The proposed circuit simultaneously provides many benefits: simple bridgeless and symmetrical structure, resonant behavior providing soft switching for all of the semiconductors, intrinsic high power factor capability, continuous input current with low ripples even with small inductors with discontinuous conduction mode (DCM) currents, and simple modulation and control circuit. The input current is continuous and divided equally between two input inductors even in the lower parts of the input voltage in the line cycle. In addition, in the proposed structure, soft switching is provided for all of the semiconductors in the circuit. Zero voltage switching (ZVS) is provided for the MOSFETs at turn-ON, and zero current switching (ZCS) is provided for the diodes at turn-OFF. Moreover, the studied PFC converter has inherent power factor correction capability. In other words, as shown in Fig. 1(a), the converter draws a sinusoidal input current when connected to a sinusoidal input voltage without any current controller loops, making the controller simple and easy to incorporate.

In Section II, the principles of operation for the proposed converter is fully discussed. In Section III, related equations and analysis necessary for the design stage are provided. Design considerations have been provided in Section IV based on the represented equations for a 400 W experimental setup. To show the validity of the theoretical analysis, the prototype is constructed and experimental results are presented in Section V.

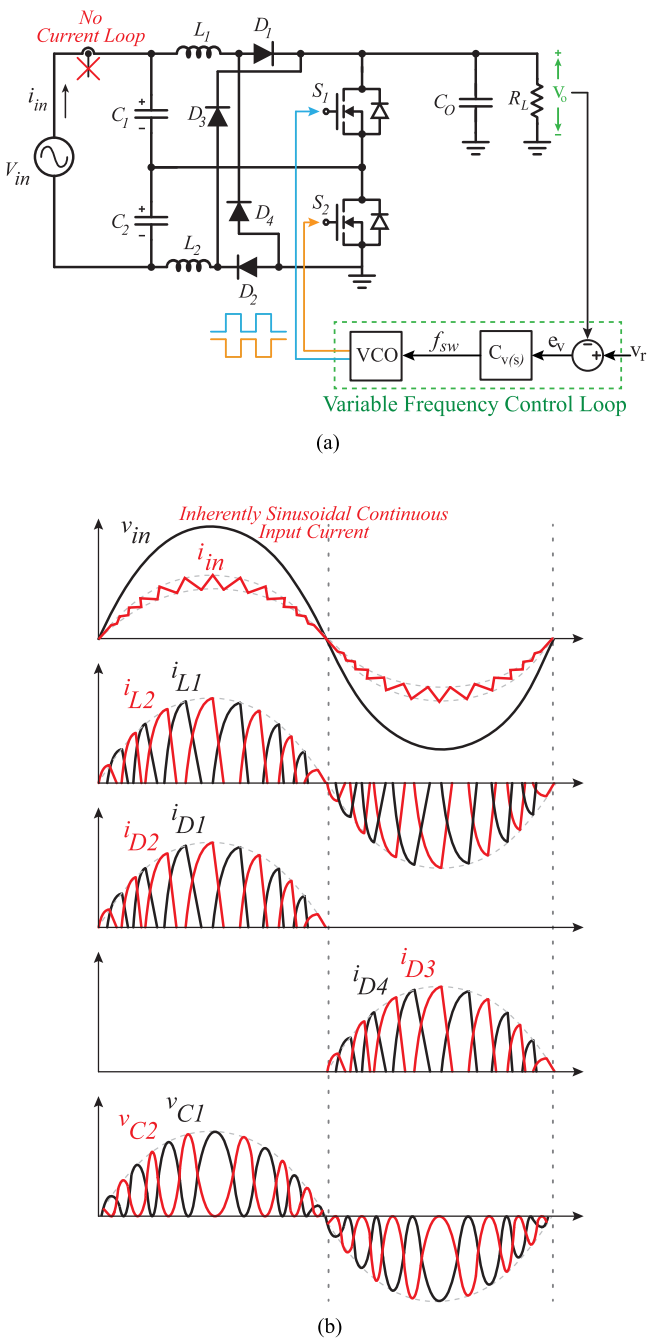


Fig. 1. (a) Proposed resonant bridgeless ac/dc PFC boost converter with inherent sinusoidal and continuous input current without any current loops. (b) Current and voltage waveforms of the circuit in a line-frequency cycle with simple variable switching frequency modulation.

II. Principles of Operation for the Proposed Resonant Bridgeless PFC Rectifier

The principles of operation for the proposed converter is analyzed in this section. The proposed bridgeless PFC rectifier has a resonant behaviour to convert the input ac voltage to the output dc, and also to draw a sinusoidal and continuous input current from the grid. This resonant phenomenon in the circuit is described in this section to show some of the benefits of the proposed converter. In this section, the behaviour of the proposed converter in different intervals of the line cycles and also the switching cycles are investigated. Equivalent circuit of the proposed converter as well as currents' and voltages' waveforms in different intervals are also given in this section. The power stage of the proposed converter is illustrated in Fig. 1(a). The simple control algorithm used in the proposed converter is also shown in Fig. 1(a). The operation of the converter is symmetrical in two half-line cycles. Fig. 1(b) represents the line cycle waveforms of the proposed converter. The equivalent circuit diagrams in the positive and negative half-line cycles are illustrated in Fig. 2. As seen in the figures, one switch leg is used in the circuit with S_1 and S_2. Two series diodes (D_1 and D_2 in the positive half cycle, and D_3 and D_4 in the negative half cycle) are used to prevent

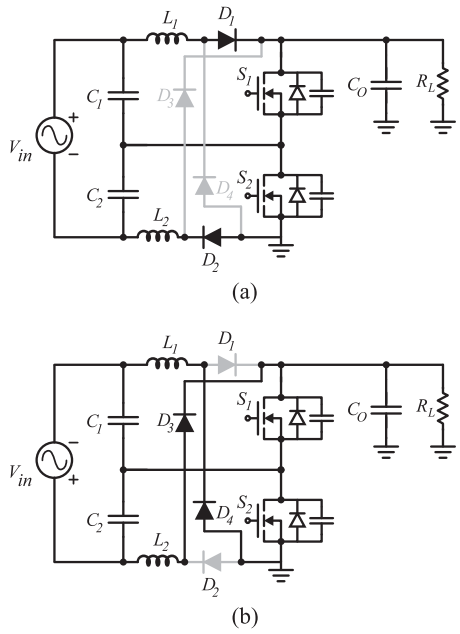


Fig. 2. Equivalent circuit of the proposed converter in (a) positive half-line cycles, and (b) negative half-line cycles.

reverse power from flowing to the input. It will be shown in this section that the input current is continuous during the line frequency period, which is one of the benefits of the proposed converter.

In order to simplify the analysis, it is assumed that all of the circuit elements are ideal except for the MOSFETs. In the MOSFETs, the parasitic drain–source capacitance is not neglected. Considering the output capacitors of the MOSFETs is necessary in order to show the ZVS conditions for the switches. The circuit operates at steady state and the output capacitors are large enough to be considered as an ideal dc voltage source. It is assumed that the inductors L_1 and L_2 are equal, as the input capacitors C_1 and C_2. Thus, each of the inductors and the input capacitors can be shown with L and C, respectively, in the equations. Because of the symmetrical operation in the proposed converter in each of the half-line cycles, the analysis is done during the positive portion of the input voltage. Then, it can be extended to the whole range. Additionally, it is assumed that the input voltage is constant in a switching cycle. This is because of the high switching frequency in comparison with the line frequency. Waveforms of the converter in a line frequency cycle are shown in Fig. 1(b). The equivalent circuit of the converter is given in Fig. 2(a) for the positive half-line cycles, and in Fig. 2(b) for the negative half-line cycles. Moreover, the equivalent active circuit and theoretical key waveforms in a switching cycle scale are shown in Figs. 3 and 4, respectively. These figures are describing the switching frequency operation of the proposed converter in the positive half-line cycles. Since the circuit is symmetrical, the switching operation of the proposed converter is similar in both of the half-line cycles. As seen, there are eight different operational modes for a switching cycle. Since the operation of the converter is symmetrical, only the first four modes are explained in this section. Before the first mode, it is assumed that the drain–source capacitor of the switch S_1 is discharged. So, the parasitic capacitor of the switch S_2 is fully charged to the output voltage. Additionally, it is assumed that the anti parallel diode of the switch S_1 is conducting. At this moment, switch S_1 can be turned ON under the ZVS condition.

Mode I [$t_0 < t < t_1$] shown in Fig. 3(a): This mode is started when the body diode of the switch begins to conduct. Since the body diode of S_1 is conducting, S_1 can be switched ON under ZVS condition. In this mode, i_{S1} is negative and ramping up. This mode ends when i_{S1} reaches zero (at t_1). At this moment, the currents of the input capacitors become zero, and since i_{C1} was positive before that, the voltage of C_1 is at its peak and v_{C2} is at its lowest value in the switching cycle.

Mode II [$t_1 < t < t_2$] shown in Fig. 3(b): The current flowing through D_1 and S_1 is still charging inductor L_1. Simultaneously, L_2 is supplying the load through D_2 and S_1. Nevertheless, after t_1, the net current of L_1 and L_2 is positive flowing from the drain to the source of S_1. During this interval, i_{L1} is increasing and at the same time i_{L2} is decreasing. At t_2, i_{L2} touches zero, which forces the diode D_2 to turn OFF under ZCS condition and consequently stops the inductors from feeding the output capacitor. As seen in Fig. 4, i_{L1} and i_{L2} can be interpreted approximately linearly from t_0 to t_2. During this mode, in order to simplify the equations, the input capacitors' voltages (v_{C1} and v_{C2}) can be considered to be constant as

$$v_{C1}(t) \approx v_{C1}(t_1) = v_{C\max}, v_{C2}(t) \approx v_{\text{in}} - v_{C\max} \quad (1)$$

where $v_{C\max}$ is the maximum voltage of the input capacitors in a switching cycle. As stated, considering the voltage across the input capacitors to be constant during this interval means that the inductors L_1 and L_2 have constant voltages equal to $v_{C\max}$ and $v_{\text{in}} - v_{C\max} - v_o$, respectively. The equations for calculating the inductors' currents are represented as

$$i_{L1}(t) = \frac{v_{C\max}}{L_1}(t - t_0) \quad (2)$$

$$i_{L2}(t) = i_{L_{\max}} - \frac{v_{\text{out}} - v_{\text{in}} + v_{C\max}}{L_2}(t - t_0). \quad (3)$$

Mode III [$t_2 < t < t_3$] shown in Fig. 3(c): Once the diode D_2 turns OFF, this interval begins. During this time, i_{L1} is ramping up through S_1 and D_1, and i_{L2} is zero. At the same time, v_{C1} decreases because of the negative value of i_{C1}. On the other hand, since i_{C2} is positive, v_{C2} is increasing. Turning OFF the switch S_1 by the controller is the end of this interval. Since a resonance between L_1 and the parallel combination of C_1 and C_2 is happening during this mode, v_{C1} and i_{L1} can be expressed with sinusoidal equations given by

$$v_{C1}(t) = v_{C\max}\cos(\omega_{\text{res}}(t - t_2))$$
$$i_{L1} = \frac{v_{C\max}}{Z_r}\sin(\omega_{\text{res}}(t - t_2)). \quad (4)$$

Resonant frequency or ω_{res} is the result of the resonance between each inductor (L_1 or L_2) and the parallel combination of the input capacitors (C_1 and C_2). Therefore, it can be defined as

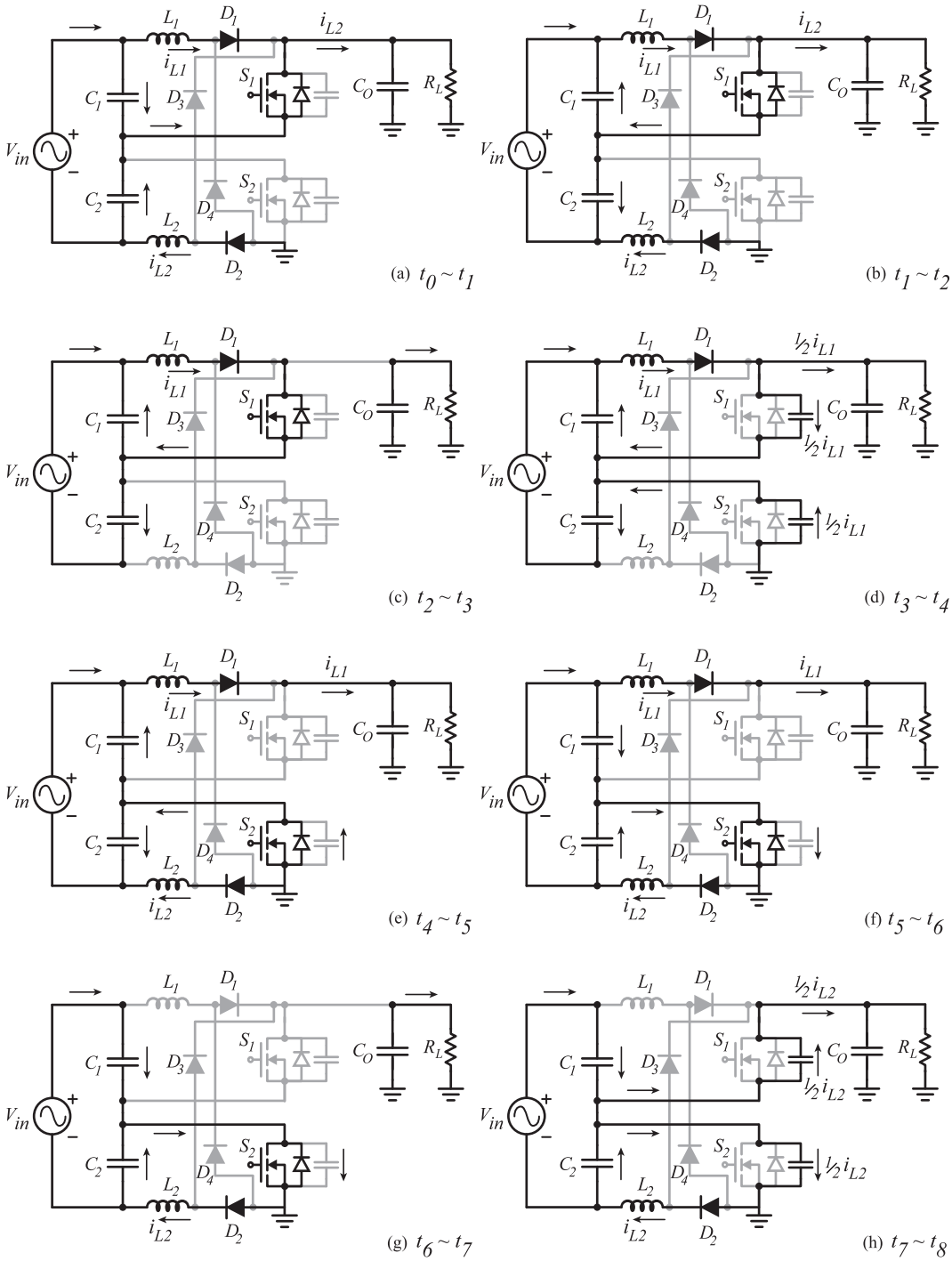


Fig. 3. Proposed resonant boost PFC converter structure in the positive half-line cycle during each switching cycle interval.

(5). In addition, the impedance of the resonant elements is shown with Z_r, and is defined in (6). The resonant tank impedance or Z_r is just a definition that will prove useful in the analysis section of this paper

$$\omega_{\text{res}} = \frac{1}{\sqrt{2LC}} \tag{5}$$

$$Z_r = \sqrt{\frac{L}{2C}}. \tag{6}$$

Moreover, (4) can be used to find a relationship between $i_{L\max}$ and $v_{C\max}$, which is given in by

$$i_{L_1}(t_3) = i_{L\max} = \frac{v_{C\max}}{Z_r}. \tag{7}$$

Mode IV [$t_3 < t < t_4$] shown in Fig. 3(d): Starting this mode, the gate signal of S_1 is turned OFF, which results in both switches being OFF. Meanwhile, the current in L_2 is zero, and i_{L1} is experiencing its maximum in the switching cycle or $i_{L\max}$. Since the

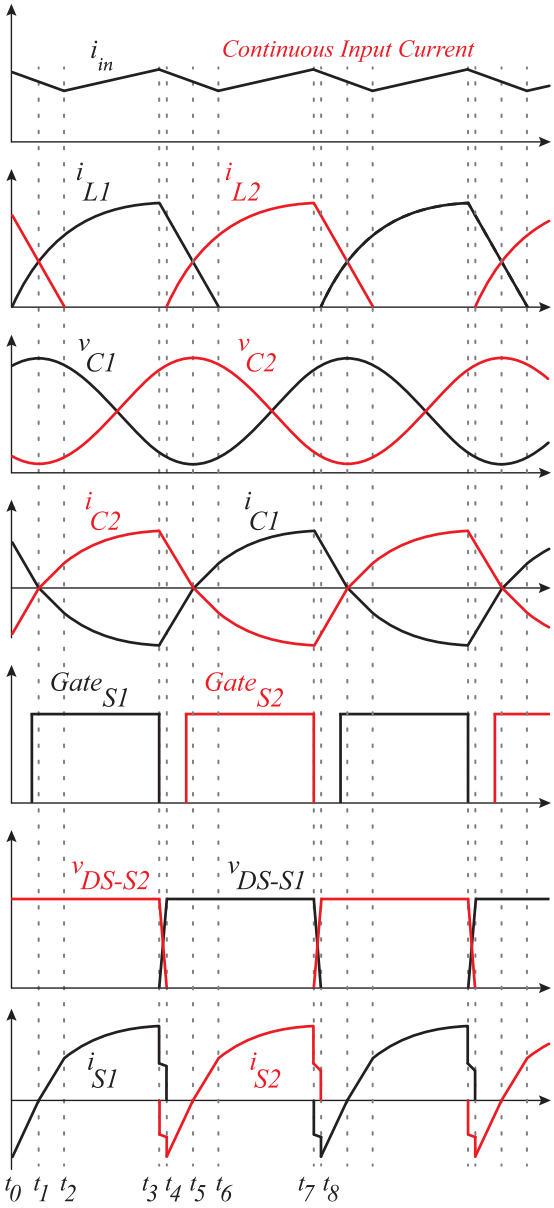


Fig. 4. Operating modes of the converter during switching cycle intervals. The circuit works with simple variable switching frequency modulation and complementary gate signals with 50% duty cycle. These waveforms are for the converter at positive half-line cycles. The operation of the converter is the same in the negative half-line cycles because of the symmetry in the topology.

current of an inductor cannot change suddenly, i_{L1} cannot reach zero instantaneously, and the only way it can close its path, is to flow through the drain–source capacitors in the MOSFETs. In other words, it is helping to charge the drain–source capacitance of S_1 and discharge the capacitance of S_2. If S_1 has a big capacitor across the drain–source, its voltage does not reach v_{out} suddenly, and this helps decrease the turn-OFF loss. This leads to the reduction in $\frac{dv}{dt}$ across the switches at turn-OFF moments. On the other hand, if the parallel capacitance of the switch is chosen larger, it takes more time and energy to discharge this capacitor prior to turn-ON of the switch, risking the ZVS condition at turn-ON. However, since the current for discharging the cap is the maximum current of each inductor ($i_{L\max}$), ZVS at turn-ON is achieved even under light loading conditions. At the end of this interval, the voltage across the drain–source capacitance of S_2 reaches zero, and from this moment on, the inductor current i_{L1} will flow through the anti-parallel diode of the switch S_2. During this interval, S_2 can be switched ON with discharged parallel capacitor or ZVS.

Because of the symmetry in the circuit, the next four modes of operation [see Fig. 3(e)–(h)] are similar to the first four intervals [see Fig. 3(a)–(d)] discussed in this section. In other words, as seen in the first four intervals, switch S_1 is going to be turned ON under soft-switching conditions, but in the next four intervals, S_2 can be switched ON under ZVS. Therefore, the same pattern is observed in terms of operation of the circuit in the second four intervals, and the discussion would be very similar to that of the first intervals. In Section III, mathematical equations of the proposed converter are analyzed and presented.

III. Proposed Converter's Analysis

In this section, the proposed converter is mathematically analyzed. The proposed converter has a simple and symmetrical structure, which makes the mathematical analysis easier. In this section, the line frequency characteristics of the proposed converter are investigated as well as the switching scale behaviour. In the line frequency analysis, it will be mathematically shown that the proposed converter has inherent PFC capability without any current loops. It will be also shown that the proposed converter draws continuous input current with low ripples, even with the small inductances with discontinuous currents. These characteristics happen with a simple variable frequency modulation technique with 50% duty cycles in complementary mode. In this section, the equations presented in Section II at each time interval are used to enhance the analytical description of the proposed structure. Switching cycle analysis is provided in Section III-A, and Section III-B represents the analysis in the line frequency cycles.

A. Converter's Analysis in a Switching Cycle

In this section, the voltages and currents of the proposed circuit are analyzed at different time intervals in a switching cycle. In order to have a better understanding about the behavior of the converter, input and output currents should be first studied in the switching cycle. In this section, some of the equations related to the input and output currents are given. It should be mentioned that at this part, all of the converter characteristics like $v_{\text{in}(t)}$ are assumed to be constant in a switching cycle, which is fairly a valid assumption, because the switching cycle is much smaller than a line frequency cycle. First, input capacitors' voltages are analyzed. As seen in Fig. 1(a), summation of v_{C1} and v_{C2} is equal to the input voltage, which is assumed to have a constant value in a switching cycle, while it is changing in a line frequency cycle. Therefore, the following can be considered:

$$v_{C1} + v_{C2} = v_{\text{in}(t)} \xrightarrow{i_C = C\frac{dv_C}{dt}, C_1 = C_2} i_{C1} = -i_{C2}. \quad (8)$$

By considering kirchhoff's current law (KCL) in the positive node of the input capacitor C_1 and the negative node of C_2, (9)

and (10) can be presented as

$$i_{C1} = \frac{i_{L2} - i_{L1}}{2},\ i_{C2} = \frac{i_{L1} - i_{L2}}{2}. \tag{9}$$

As can be seen in (10), input current (i_{in}) is the average of the two inductors' currents (i_{L1} and i_{L2}), which is the actual reason why the input current is continuous despite the inductors' currents being in discontinuous conduction mode

$$i_{\text{in}} = \frac{i_{L1} + i_{L2}}{2}. \tag{10}$$

Since the duration of the mode IV ($t_3 < t < t_4$) is shorter than the other intervals already discussed, it can be assumed that the voltages and the currents of the circuit remain constant, so as i_{L1} and i_{L2}. Utilizing (3), the maximum current of the inductors (which is the same for both, because of the symmetry in the circuit) can be calculated as

$$i_{L\max} \approx \frac{V_{\text{out}} - v_{\text{in}(t)} + v_{C\max(t)}}{L_2}(t_2 - t_0). \tag{11}$$

Moreover, i_{L1} at t_2 is given by

$$i_{L1}\ (t_2) = \frac{v_{C\max(t)}}{L_1}(t_2 - t_0). \tag{12}$$

Output current's average value in a switching cycle is calculated in (13) based on the average value of i_{L2} waveform. This is done during the first and second intervals from t_0 to t_2 shown in Fig. 4. Therefore, assuming (11), following can be written:

$$< i_O >_{f_{Sw}} = \frac{V_{\text{out}} - v_{\text{in}(t)} + v_{C\max(t)}}{L_2}\frac{(t_2 - t_0)^2}{T_{Sw.}}. \tag{13}$$

Based on the continuous behavior of i_{in} shown in Fig. 4, considering (10) and (11), and with the fact that $i_{\text{in\_max}}$ is half of $i_{L\max}$ at t_0, $i_{\text{in\_max}}$ is analyzed as follows:

$$i_{\text{in\_max}} = \frac{V_{\text{out}} - v_{\text{in}(t)} + v_{C\max(t)}}{2L}(t_2 - t_0). \tag{14}$$

In addition, based on Fig. 4 at t_2, and using (10) and (12), $i_{\text{in\_min}}$ is presented as

$$i_{\text{in\_min}} = \frac{v_{C\max(t)}}{2L}(t_2 - t_0). \tag{15}$$

As discussed, even with the discontinuous currents flowing through the inductors in the circuit, input current is continuous, which is one of the greatest benefits of this structure. The average and ripple of the input current in a single switching period can be calculated in (16) and (17) based on (14) and (15) as follows:

$$< i_{\text{in}} > (t) = \frac{V_{\text{out}} - v_{\text{in}(t)} + 2v_{C\max(t)}}{4L}(t_2 - t_0) \tag{16}$$

$$\Delta i_{\text{in}}(t) = \frac{V_{\text{out}} - v_{\text{in}(t)}}{2L}(t_2 - t_0). \tag{17}$$

Based on (7) and (11), $(t_2 - t_0)$ can be calculated based on a relationship between V_{out}, $v_{\text{in}(t)}$, and $v_{C\max(t)}$, given by

$$(t_2 - t_0) = 2LC\frac{v_{C\max(t)}\ \omega_{\text{res}}}{V_{\text{out}} - v_{\text{in}(t)} + v_{C\max(t)}}. \tag{18}$$

Replacing (18) in (13) and (16) eliminates the variables $(t_2 - t_0)$, resulting in the simpler equations (19) and (20) that describe the relationship for the average value of the output and input currents in a switching cycle, respectively, as the followings:

$$< i_O >_{f_{Sw}} = \frac{V_{\text{out}} - v_{\text{in}(t)} + v_{C\max(t)}}{LT_{Sw.}} \times \left(\frac{2LC\ v_{C\max(t)}\ \omega_{\text{res}}}{V_{\text{out}} - v_{\text{in}(t)} + v_{C\max(t)}}\right)^2 \tag{19}$$

$$< i_{\text{in}} >_{f_{Sw}} = \frac{V_{\text{out}} - v_{\text{in}(t)} + 2v_{C\max(t)}}{4L} \times \left(\frac{2LC\ v_{C\max(t)}\omega_{\text{res}}}{V_{\text{out}} - v_{\text{in}(t)} + v_{C\max(t)}}\right). \tag{20}$$

Output and input current averages over a switching cycle are given in (19) and (20). As seen in Fig. 1, $v_{C\max(t)}$ in a switching cycle is different from the absolute maximum of $v_{C\text{maxPeak}}$ in a line-frequency cycle. In other words, $v_{C\max(t)}$ is a sinusoidal function in the line cycles. Mathematical characteristics of $v_{C\max(t)}$ are analyzed in Section III-B along with the other characteristics of the converter in a line-frequency cycle. The maximum value of the input capacitors' voltages to the instantaneous value of the input voltage, or $\frac{v_{C\max(t)}}{v_{\text{in}(t)}}$, is a constant value in the line cycle if the value of the switching frequency and load remain constant. Since variable switching frequency modulation is used in the proposed circuit, $f_{Sw.}$ and load are kept constant in a line cycle. Therefore, $\frac{v_{C\max(t)}}{v_{\text{in}(t)}}$ remains constant during the line cycles. In other words, $\frac{v_{C\max(t)}}{v_{\text{in}(t)}}$ is kept constant, which results in $\frac{v_{C\max(t)}}{v_{\text{in}(t)}}$ being equal to $\frac{V_{C\text{maxPeak}}}{V_{\text{inPeak}}}$. $V_{C\text{maxPeak}}$ and V_{inPeak} are the maximum values of the functions $v_{C\max(t)}$ and $v_{\text{in}(t)}$ in a line cycle, respectively. In Section III-B, this simple characteristic will prove very helpful in interpreting the line frequency content of the input current in the proposed converter.

B. Converter Analysis in a Line Cycle

In this section, voltages and currents of the proposed converter are analyzed in the line frequency cycles. It is assumed that the input voltage is a pure sinusoidal waveform. At the very beginning, the equation for the input and output current will be analyzed. It will be shown that the input current follows the input voltage inherently with a simple constant frequency modulation. In other words, with a sinusoidal input voltage, the input current would be sinusoidal and continuous even with the DCM inductors being used. This also means that the power factor of the converter would be high with a simple frequency control without the need to have a current loop. As stated, with a constant switching frequency and load in a line cycle, $\frac{v_{C\max(t)}}{v_{\text{in}(t)}}$ remains constant. Using this characteristic, (20) can be made simpler as follows:

$$i_{\text{in}(t)} = v_{\text{in}(t)}\ \frac{C\ \left(\frac{V_{C\text{maxPeak}}}{V_{\text{inPeak}}}\right)\omega_{\text{res}}}{2} \times \left(1 + \frac{1}{\frac{V_{\text{out}}}{v_{C\max(t)}} + \left(1 - \frac{V_{\text{inPeak}}}{V_{C\text{maxPeak}}}\right)}\right). \tag{21}$$

As seen in (21), input current has two components in the parentheses. The first is the constant 1 and the other is an expression comprising some constant ratios and the variable ratio $\frac{V_{\text{out}}}{v_{C\max(t)}}$. If the second component appearing in (21) can be neglected most of the time during a line frequency cycle compared to the other component, it can be assumed with a relatively accurate approximation that the input current is very close to a sinusoidal waveform. The ratio $\frac{V_{\text{out}}}{v_{C\max(t)}}$ varies with an ac input voltage, and the circuit should be designed in such a way that the variable $v_{C\max(t)}$ is smaller than V_{out}. As seen in Fig. 1(b) and discussed in Section III-A, $v_{C\max(t)}$ is close to a sinusoidal function. Hence, if the circuit is designed in order to make $\frac{V_{\text{out}}}{v_{C\text{maxPeak}}}$ as low as possible, it can lead to $\frac{V_{\text{out}}}{v_{C\max(t)}}$ being a small value and thus negligible compared to $(1-\frac{V_{\text{inPeak}}}{V_{C\text{maxPeak}}})$. As a result, $i_{\text{in}(t)}$ can be close to a sinusoidal function. The proposed circuit is designed in Section IV to be compatible with the assumption that was made. Hence, if the converter is working with constant $f_{Sw.}$ for a particular amount of load in the whole line frequency cycle, the input current would be very close to sinusoidal, which results in a high power factor. This means that the input current loop is not needed in the structure in order to achieve a high power factor, and as a result the control circuit is very simple. As discussed, with a variable-frequency modulation in gate signals with 50% duty cycle, and sinusoidal input voltage, input current is automatically sinusoidal. Therefore, input current can be approximated to be a sinusoidal function in the equations in a line frequency cycle and it is hereafter assumed to be. In order to make the analysis simple, electrical variables of the circuit are going to be normalized. In the normalization process, there should be some reference values for the voltage, impedance, frequency, and current. These definitions have been given in the following:

$$v_{\text{ref}} = V_{\text{inRMS}} \tag{22}$$

$$Z_{\text{ref}} = Z_r = \sqrt{\frac{L}{2C}} \tag{23}$$

$$f_{\text{ref}} = f_{\text{res}} = \frac{1}{2\pi\sqrt{2LC}} \tag{24}$$

$$i_{\text{ref}} = \frac{v_{\text{ref}}}{Z_{\text{ref}}} = \frac{V_{\text{inRMS}}}{Z_r}. \tag{25}$$

Using the definitions in (22)–(25), the variables in the proposed circuit can be normalized as follows:

$$F_n = \frac{f_{Sw.}}{f_{\text{ref}}} = \frac{f_{Sw.}}{f_{\text{res}}} \tag{26}$$

$$Q = \frac{Z_r}{R_{\text{out}}} = \frac{\sqrt{\frac{L}{2C}}}{R_{\text{out}}} \tag{27}$$

$$m_v = \frac{V_{\text{out}}}{v_{\text{ref}}} = \frac{V_{\text{out}}}{V_{\text{inRMS}}} \tag{28}$$

$$v_{C\max n} = \frac{V_{C\text{maxPeak}}}{v_{\text{ref}}} = \frac{V_{C\text{maxPeak}}}{V_{\text{inRMS}}}. \tag{29}$$

Using the definitions in (26)–(29), the equations can be made simpler hereafter. The switching frequency has been normalized in (26). So F_n hereafter depicts the normalized switching frequency. Q in (27) is the normalized value of the output admittance or the quality factor. m_v is the gain of the converter defined in (28) as the ratio of the output voltage to the rms value of the input voltage. Also $v_{C\max n}$ is the representation of the normalized value of the maximum voltage of the input capacitors defined in (29). Considering the sinusoidal approximation for i_{in} and other parameters, and using the definitions in (26)–(29), (19) and (20) can be used to reach (30). Also, η represents the efficiency of the converter in (30) as

$$64F_n^2 Q \times m_v^3 - 12\sqrt{2}\pi^2 F_n\, Q\, \eta \times m_v^2 + (\pi^4\, Q\, \eta^2 - 4\pi\, F_n\, \eta^2) \times m_v + \sqrt{2}\, F_n\, \eta^2\, \pi^2 = 0. \tag{30}$$

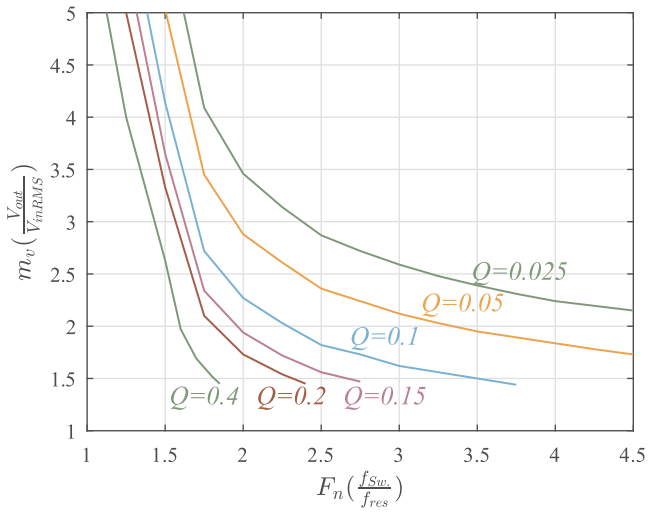
Equation (30) has been solved numerically in different values of F_n and Q. The solution for this equation has been drawn in Fig. 5(a) for different values of the quality factor (Q) and the normalized switching frequency (F_n). The definitions in (26)–(29), along with (19) and (20), can lead to (31) representing the equation for calculation of $v_{C\max n}$ in different values of F_n. This equation has also been drawn for different values of the quality factor (Q) and the normalized switching frequency (F_n) in Fig. 5(b)

$$v_{C\max n} = \frac{2Q\, m_v\left(16F_n\, m_v^2 - (2\sqrt{2}\eta\pi^2 + 4\sqrt{2}F_n\pi)\, m_v\, + \pi^3\eta\right)}{-8F_nQ\pi\, m_v^2 + \left(4\sqrt{2}F_n\eta + \pi^3Q\sqrt{2}\eta\right)\, m_v - 2F_n\eta\pi}. \tag{31}$$

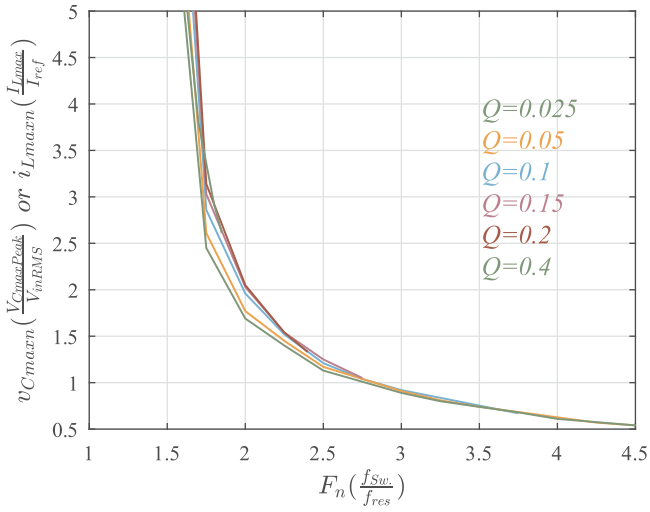
As stated, the proposed circuit works based on the resonance between the components in the circuit. Both of the input inductors (L_1 and L_2) and input capacitors (C_1 and C_2) participate in the resonance. The maximum current of the inductors ($i_{L\max}$) and maximum voltage of the capacitors ($v_{C\max}$) are important in selecting these components. The general relationship between these two parameters is given in (7). As stated, in order to make the analysis and design simple for the reader, variables are normalized based on the references defined in (22)–(25). As seen, I_{ref} is defined as the ratio of the voltage reference ($v_{\text{ref}} = V_{\text{inRMS}}$) to the reference of the impedance ($Z_{\text{ref}} = Z_r$). Therefore, based on (7), it is understood that the normalized value of the maximum current of the inductor would be equal to the maximum voltage of the capacitor. This expression is mathematically proved as

$$i_{L\max n} = \frac{I_{L\text{maxPeak}}}{i_{\text{ref}}} \overset{(7),(25)}{=\!=} \frac{\frac{V_{C\text{maxPeak}}}{Z_r}}{\frac{V_{\text{inRMS}}}{Z_{\text{ref}}}} = \frac{V_{C\text{maxPeak}}}{V_{\text{inRMS}}} = v_{C\max n}. \tag{32}$$

Based on (32), the maximum of the resonant inductor's current peak ($i_{L\max n}$) is equal to the value of the maximum voltage of the resonant capacitor's peak ($v_{C\max n}$). The value of $v_{C\max n}$ or $i_{L\max n}$ can be calculated using (31). In addition, this variable is depicted in Fig. 5(b) in different values of the normalized switching frequency and the quality factor. As seen in Fig. 5(b),



(a)



(b)

Fig. 5. (a) Voltage gain versus the normalized switching frequency in different values of the quality factor. (b) Normalized maximum value of the input capacitors' voltages and maximum value of inductors' currents in different values of the normalized switching frequency and the quality factor.

the maximum value of the capacitors' voltages and the maximum value of the inductors' currents do not vary in different quality factors. This shows that these values mostly depend on the normalized switching frequency. The average value of the inductor's current can be calculated by taking the average of (10). Since the average of inductors L_1 and L_2 currents are equal, their average value can be shown by $i_{L\text{aveg}}$. This parameter can be calculated by

$$< i_{\text{in}} > |_{@f_{Sw.}} = \frac{< i_{L1} > |_{@f_{Sw.}} + < i_{L2} > |_{@f_{Sw.}}}{2}. \quad (33)$$

Since the average value of the inductors' current are equal ($< i_{L1} > |_{@f_{Sw.}} =< i_{L2} > |_{@f_{Sw.}} = i_{L\text{aveg}}$), (34) can be assumed as

$$< i_{L\text{aveg}} > |_{@f_{Sw.}} =< i_{in} > |_{@f_{Sw.}} \quad (34)$$

Therefore, the average of the inductors' currents in the switching frequency are equal to the input current, which is considered a sinusoidal value. In addition, the voltage stress of the semiconductors are equal to the output voltage. For example, the maximum voltage of the switches are equal to the output voltage, once the other switch is conducting. The same scenario happens for the diodes. In other words, the voltages of the diodes are limited by the output voltage when they are OFF. Their voltages are restricted to V_{out} because of the conduction of the other diodes at the same time. The converter elements are designed in Section IV in a step-by-step process.

IV. Design Considerations

This section describes the practical design guidelines for the proposed resonant bridgeless PFC converter. There are two parts in this section. The first part of the section talks about the design procedure for selecting the components. The second part is about the control and modulation algorithm used in the proposed converter.

A. Selecting the Components

In this part, a prototype based on the analyzed equations is designed to prove the feasibility of the structure. The input voltage is considered 220 V ± 20% rms, with 400 V output dc voltage. The maximum load power is 400 W. The proposed converter should be designed with as low conduction losses as possible without sacrificing the gain variation versus the switching frequency. Since the switching losses in the converter are very low, the switching frequency can be increased without any problems. Based on the waveforms shown in Fig. 5(a), in order to decrease the switching frequency range, quality factor should be chosen to be high. However in this case, the maximum input capacitor voltage increases [shown in Fig. 5(b)]. As stated in Section III, in order to have higher power factors, the maximum voltage of the resonant capacitors ($V_{C\text{maxPeak}}$) should be limited. Therefore, Q_{max} should not be chosen to be high. The minimum and the maximum values of the gain can be calculated as

$$m_{v\_\text{min}} = \frac{V_{\text{out}}}{V_{\text{inRMS\_max}}} = 1.51$$
$$m_{v\_\text{max}} = \frac{V_{\text{out}}}{V_{\text{inRMS\_min}}} = 2.27. \quad (35)$$

The converter is designed such that it has minimal conduction losses while keeping the gain variation high with the small variations in the switching frequency. Since soft switching is provided for all the semiconductors, the switching frequency can be increased. Based on the waveforms illustrated in Fig. 5(a), if the quality factor is high, the difference between the maximum and minimum switching frequencies decreases, which is preferred. However, in that case, the ac voltage across the resonant capacitors increases as well, which requires special capacitors to be used. In addition, if $v_{C\text{max}}$ increases, based on (21), ratio $\frac{V_{\text{out}}}{V_{C\text{maxPeak}}}$ increases too, resulting in higher deviation of the input current from a sinusoidal waveform. This reduces the THD, which is undesirable. Moreover, since the time during which the current

of the inductor is being charged without transferring to the output is increasing, the conduction losses increase too. Therefore, it is not recommended to choose a high quality factor or Q. On the other hand, if Q is too small, the gain waveform flattens, increasing the frequency deviation with the same gain variation. Hence, a moderate value for Q should be selected in order to avoid these problems. Based on the description provided, maximum quality factor or $Q_{\max} = 0.1$ is selected to meet all of the requirements addressed earlier. The resonant frequency is selected to be 100 kHz. Therefore, the values of the input capacitors and the inductors can be calculated using (36) and (37). These equations are derived from (27) and (28) as

$$L = L_1 = L_2 = \frac{R_{\text{load}} Q_{\max}}{2\pi f_{\text{res}}} = 63.7\,\mu\text{H} \tag{36}$$

$$C = C_1 = C_2 = \frac{1}{4\pi R_{\text{load}} Q_{\max} f_{\text{res}}} = 19.9\,\text{nF}. \tag{37}$$

Three 5.6 nF capacitors from Epcos have been used as well as two 70 μH inductor with RM12 cores. Therefore, the real value of $Q_{\max}$ and f_{res} would be slightly different from those of (36) and (37). The real values can be calculated based on (5) and (27). The practical values of $Q_{\max}$ and f_{res} are 0.114 and 104 kHz, respectively. As seen in Fig. 5(a), the switching frequency of the converter at the nominal load when $Q_{\max} = 0.114$ and $f_{\text{res}} = 104$ kHz, is 230 kHz. In other words, the switching frequency of the proposed converter at full load ($v_{\text{in}} = 220$ V rms, $V_{\text{out}} = 400$ V, and $P_{\text{out}} = 400$ W) is 230 kHz. Also, the switching frequencies at v_{inMax} and v_{inMin} is 320 kHz and 190 kHz, respectively. As stated, because of soft switching in the proposed converter, increasing the switching frequency is not an issue; the efficiency does not drop significantly. The provided statement about the efficiency is checked in Section V in an experimental prototype. The characteristic impedance of the resonant tank can then be calculated as (38). This equation is based on the one given in (23) as

$$Z_{r\_\text{designed}} = \sqrt{\frac{L}{2C}} = 45.6\,\Omega. \tag{38}$$

Based on Fig. 5(b), the normalized maximum current of the inductor or maximum voltage of the capacitors are both equal to 1.2 at the nominal loading conditions. Based on (25), i_{ref} can be calculated using the input voltage and (38) as the references of the voltage and impedance, respectively. The maximum value of the inductor's current would be $1.2 \times \frac{v_{\text{inRMS}}}{Z_r} = 5.8$ A. Also, the maximum voltage of the capacitors would be equal to $1.2 \times v_{\text{inRMS}} = 264$ V. The core $RM12/I$ from Ferroxcube is selected with the material $3C95$. The number of the turns is selected to be 17 with AWG 12 Litz wire. Litz wire is chosen in order to have a low resistance in higher frequencies. The resistance of the core has been calculated at the nominal switching frequency. This value for the inductors is 0.65 Ω. TK20A60W and RURP1560 are selected as the switches and the diodes, respectively. All of the circuit elements are listed in Table I. TK20A60W is a low-cost switch with slightly higher drain–source parasitic capacitance. This capacitance helps the proposed converter to provide lower $\frac{dv}{dt}$, even at turn-OFF.

TABLE I
EXPERIMENTAL PARAMETERS

Parameter	Value	Description
$L_1,\ L_2$	70 μH	$RM12-3C95$
$C_1,\ C_2$	3×5.6 nF	$Epcos$
$S_1,\ S_2$	TK20A60W	–
$D_1 - D_4$	RURP1560	–

The only challenge with this method is discharging the bigger capacitance before turning ON the switch or providing ZVS at turn-ON. Fortunately, since in the proposed converter the parasitic capacitance of the switches is discharging with the maximum value of the inductors' currents, ZVS is achieved with no problem. Loss analysis of the selected components for the experimental prototype has been done in Section IV-B.

B. Loss Analysis

In this part of the paper, loss analysis is done for the selected components at the operating conditions. Loss breakdown in the proposed converter is done to give a better understanding about the different sources of losses in the circuit. Based on the presented analysis, the proposed converter can provide ZVS for the switches, and ZCS for the diodes in the circuit. Therefore, the switching losses in the proposed converter is reduced significantly. Since the proposed converter provides soft switching for the MOSFETs, switching losses can be neglected in comparison with other types of losses like conduction. Also, because of the ZCS turn-OFF in the diodes, reverse recovery losses are negligible and can be ignored as well. The different types of losses investigated in this part of the paper are—copper losses in the inductors, core losses in the inductors, conduction losses in the diodes, and conduction losses in the MOSFETs.

As seen in Section IV-A, $RM12/I$ from Ferroxcube is selected with the material $3C95$. Number of the turns in the designed inductors are 17. Since the currents of the inductors are discontinuous, the ac resistance of the inductors should be considered for the copper loss analysis. Resistances of the inductors are measured at 230 kHz to make the analysis more accurate. The measured resistance is 0.65 Ω at 230 kHz. First step to calculate the copper losses in the inductors, is to calculate the rms value of the inductors' currents. In order to make the analysis simpler, it can be assumed that the inductors' currents waveforms shown in Fig. 4 are triangular with a maximum value that is changing with a sinusoidal shape in the line cycles. The core losses are calculated based on the datasheet of the selected material for the cores ($3C95$).

As stated in Section IV-A, the average value of the diodes' or the inductors' currents are equal to the input current. In other words, the average value of the current going through D_1 and D_2 are equal to the half-line cycle average of the input current. The same scenario occurs for the other diodes in the circuit (D_3 and D_4). Moreover, the same approximation done for the inductors' currents can be made in calculation of the rms value

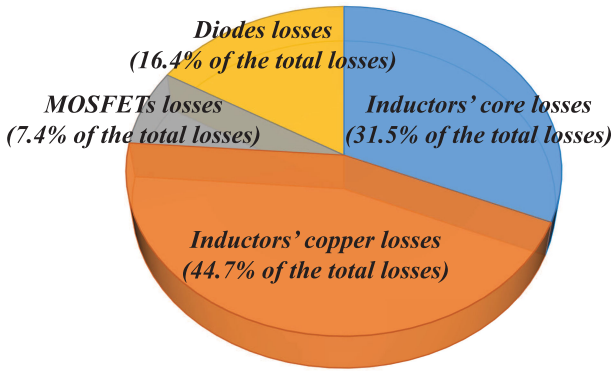


Fig. 6. Losses breakdown of the designed prototype at the nominal operating conditions.

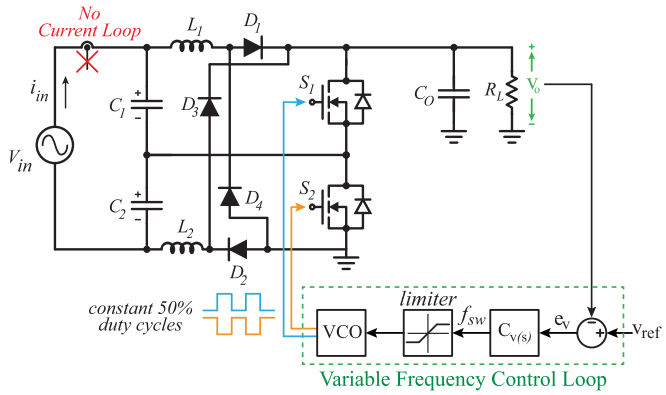


Fig. 7. Modulation and control block diagram of the proposed converter.

of the currents going through the switches. In other words, a triangular shape for the currents of the switches can be assumed with a maximum value that is changing like a sinusoidal waveform in the line cycle. This makes the analysis simple and also conservative in a sense that the calculated value would be the maximum possible point. Loss breakdown of the components in the presented prototype at the nominal conditions is shown in Fig. 6. The calculated efficiency at the nominal conditions at 400 W and 220 V_{RMS} is 94.96%. As seen in the figure, the majority of the losses in the proposed converter comes from the inductors. The efficiency of the converter is further analyzed in the experimental setup presented in Section V.

C. Control and Modulation Algorithm

The modulation and control scheme for the proposed bridgeless resonant PFC converter is presented in this part of the paper. The proposed converter has a simple modulation algorithm which requires only two complementary gate signals with constant $\approx$ 50% duty cycles with some deadtime. Because of the complimentary gate signals in the switch leg, a non-isolated gating strategy like bootstrap can be used, which makes the gate circuitry simple. The duty ratio of the gate signals are constant and equal to 50%. The switching frequency of the gate signals are constant during the whole line cycle. As shown in Section III the input current of the converter is inherently sinusoidal and continuous. Therefore, if the converter has a constant switching frequency in a whole line cycle with complementary gate signals with 50% duty cycles, the power factor of the proposed converter would be high. The switching frequency of the proposed converter can be used for the control purposes. In other words, the variable frequency method can be used only to control the output voltage of the converter in different loading and input voltage conditions. Hence, there is no need to have a current control loop in the proposed converter. The input current is inherently continuous and sinusoidal without using any current loop controllers.

The control block diagram of the proposed converter is shown in Fig. 7. As seen in Fig. 7, there is no current loop in the circuit and thus the power factor correction is inherent. Only a voltage loop is used to achieve regulations in the output voltage. After measurement of the output voltage, this value is subtracted from the reference value, which is 400 V in the studied prototype. The error in the output voltage or the output of the subtracter is shown with e_V in Fig. 7. This value is the input of the compensator block shown with C_V. The compensator produces an output, which is interpreted as the switching frequency of the converter. This value (f_{sw}) then feeds the input of the voltage controlled oscillator (VCO) after the limiter block. The VCO block generates two complementary pulsed signals with near 50% duty ratios with proper deadtime, with a frequency equal to the switching frequency (f_{sw}). With this method, the output voltage is regulated and the input current is inherently following the input voltage, which has a sinusoidal waveform. The main design consideration for the voltage compensator is to have a slow dynamic signal across one half-line cycle, so that it does not try to compensate the instantaneous variations of the input voltage. Therefore, the voltage controller is designed with a very slow bandwidth. However, if the voltage compensator is too slow, the converter does not react to the load variations fast enough and this could cause over stress in the components or a very slow response. A PI compensator is used in the presented prototype for the proposed converter. If the time constant of the PI compensator is at least five times higher than twice of the line frequency cycle, the compensator could skip the line frequency and regulate the output voltage mean value. Moreover, like other resonant converters, there should be a negative sign in the PI controller to support the negative slope of the gain versus the variation of the switching frequency shown in Fig. 5(a). The experimental prototype using the components in Table I, along with the results from testing, is presented in Section V.

V. Experimental Results

The proposed resonant bridgeless PFC converter has been tested in an experimental setup with 400 W nominal output power. The picture of the designed prototype is shown in Fig. 8. The experimental results of the proposed converter are presented in this section. It will be shown with the experimental waveforms that the proposed converter provides continuous input current even with the small inductances and input capacitors in the circuit. In addition, the operation of the proposed

Fig. 8. Picture of the designed prototype based on the proposed structure.

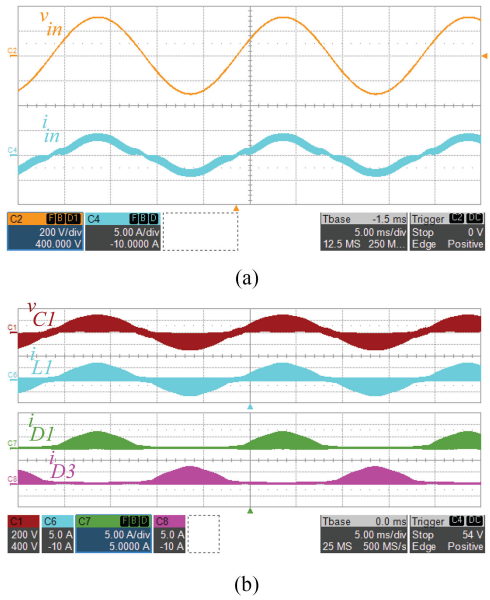


Fig. 9. (a) Input voltage and current with a near-unity measured power factor. (b) v_{C1}, i_{L1}, i_{D1}, and i_{D3}, in line-cycle scale at full load and the nominal input–output conditions.

bridgeless converter is compared with a conventional structure with the same components resulting in higher efficiencies, and lower THDs in the proposed structure. The proposed resonant PFC structure has a high efficiency due to the bridgeless structure, and also providing soft switching for all of the semiconductor elements. Components used for the experimental setup are designed in Section IV. The full list is given in Table I. As seen, the values of the input capacitors and the inductors are small. Even with these small values, the proposed circuit can guarantee the continuous input current behavior. Therefore, the power factor remains high at different load conditions. There are two parts in this section of the paper. The first part is dedicated to the function of the proposed converter in an experimental prototype with related waveforms. In the second one, the proposed converter is compared with a conventional interleaved boost PFC in terms of efficiency and power factor. The same components have been used for both of the converters to keep the comparison fair.

A. Operation of the Proposed Converter in the Experimental Setup

Experimental waveforms of the input voltage and current are shown in Fig. 9(a) in a line-frequency scale. In addition, voltage of the input capacitor C_1 and the inductor L_1 current are shown in Fig. 9(b). Diodes D_1 and D_3 currents are also shown in Fig. 9(b) in synchronous with the line voltage. As seen, the input current is sinusoidal even with the simple voltage loop control shown in Figs. 1(a) and 7. As shown in the experimental captures, input diodes do not conduct in all of the line cycle. This is an important characteristic for the proposed resonant bridgeless PFC converter. Fig. 9(a) shows that the input current is sinusoidal and in-phase with the input voltage. The measured input power factor is near unity without adding any extra filter. In other words, using only 70 μH inductors and 16.8 nF capacitors resulted in a near unity power factor without the need to add any other filter elements in the input. As seen in Fig. 9(a), input current remains continuous with low ripples, without adding extra filter at the input. This certifies the claim that the input current is continuous even with the low inductances in the circuit. As seen in Fig. 9, v_{C1} and i_{L1} are working in both half-line cycles of the input ac voltage, but the diodes D_1 and D_2 are just working in the positive half-line cycles along with the diodes D_2 and D_4 working only in the negative half-line cycles. Therefore, the operation of the converter is as discussed in the theoretical analysis section of this paper.

Waveforms of the proposed converter in a switching-cycle scale are shown in Fig. 10. This figure is captured at the peak of the input voltage at the nominal loading conditions. As seen in Fig. 10(a), the resonant capacitors' voltages (i.e., v_{C1} and v_{C2}) and inductors' currents (i_{L1} and i_{L2}) are alternating with the resonant frequency, which has the same characteristics as expected in the theoretical analysis. In addition, as shown in Fig. 10(b), switch S_2 is turned ON under ZVS conditions. As mentioned, this feature reduces the switching losses significantly. The same scenario happens for the other switch because of the symmetry in the circuit. Moreover, voltage and current waveforms of the diode D_1 are shown in Fig. 10(c), which shows that the diode turns OFF under zero current switching conditions. This feature reduces the switching losses in the circuit considerably. ZCS turn-OFF is provided for all of the diodes in the circuit, helping to decrease the switching losses and increase the efficiency in the circuit. These soft-switching characteristics enable the converter to be designed for higher switching frequencies.

As stated, the switching frequency operation of the presented prototype has been shown in Fig. 10. The voltage of the resonant capacitors (v_{C1} and v_{C2}) along with the resonant inductors' currents (i_{L1} and i_{L2}) are shown in Fig. 10(a) in the switching cycle at the peak of the input voltage. Resonance waveforms of the proposed converter shown in this figure are similar to the theoretical waveforms depicted in Fig. 4. In addition, the same behaviour is seen in Fig. 10(b) and (d) as the theoretical predictions made in Fig. 4. The only difference seen in the experimental waveforms, which is different from the theory is the small tail

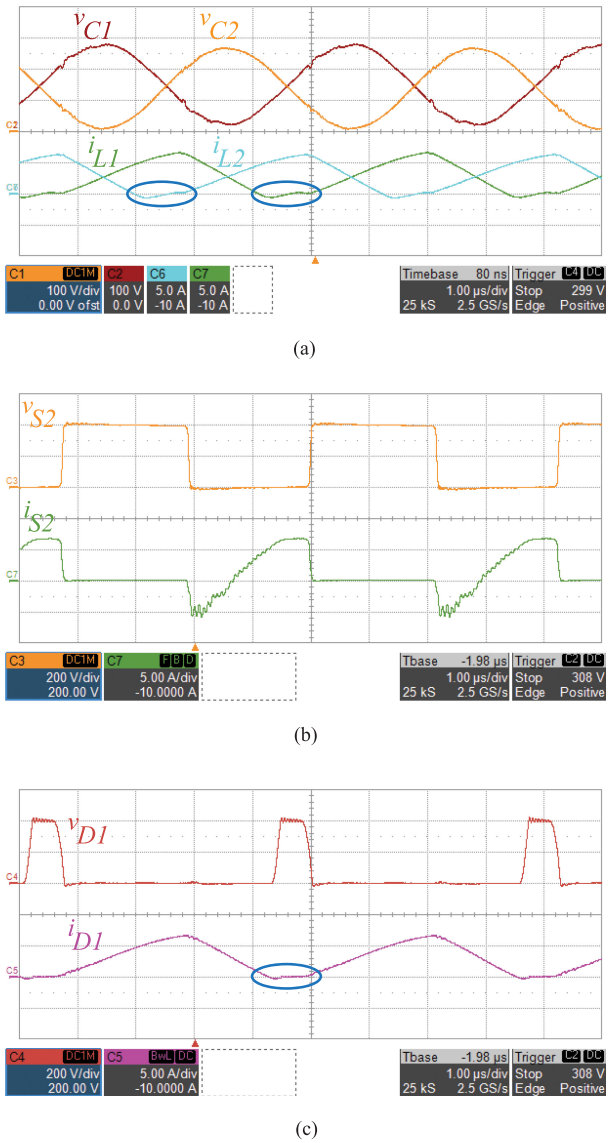


Fig. 10. (a) Resonant elements' voltages and currents alternating with the resonant frequency, (b) switching waveforms of the switch S_2 indicating ZVS turn-ON, and (c) switching waveforms of the diode D_1 with ZCS turn-OFF, all in a switching frequency cycle captured at peak of the input voltage at full load and nominal conditions.

in the inductors' and the diodes' currents in Fig. 10. This small current tail is shown in Fig. 10 for i_{L1}, i_{L2}, and i_{D1} with blue circles. This happens because of the small resonance between the inductors and the intrinsic capacitors of the diodes. This resonance occurs once the inductors' currents reach zero. This resonance is controlled with other diodes in the circuit acting like clamps to limit the voltage across the diodes. For example, once i_{L1} reaches zero at t_6, i_{L1} starts resonating with the capacitor across D_1 which is then controlled by the diode D_4. In this case, D_4 acts like a clamp avoiding the voltage across D_1 to exceed V_{out}. Therefore, the structure clamps the voltage across the diodes to the output voltage, which enables the designer to use 600 V diodes in the prototype.

B. Comparison of the Proposed Converter With the Conventional Interleaved Boost

To further analyze the behaviour of the proposed converter, the performance of the designed prototype has been compared with an interleaved boost converter with the same components and input–output specifications. Since the same components listed in Table I are used in the interleaved boost, with the same input–output characteristics and the nominal switching frequency, the inductors in the interleaved boost experience discontinuous currents. If the inductors in the traditional interleaved boost converter have discontinuous currents, the input current intrinsically can be approximately sinusoidal without any current loops [43]. This current can get more sinusoidal if the difference between the input voltage peak and the output voltage gets bigger. Therefore, this conventional circuit has many features that are close to the proposed converter including inherent PFC capability with DCM inductors' currents, and similar number of components with only two more diodes than the proposed structure. However, the only problem in the interleaved DCM boost would be the higher ripples in the input current, which gets completely discontinuous at medium to light load compared to the continuous input current in the proposed converter. This forces the designers to use big passive elements as filters in the traditional converter. Therefore, the overall volume of the proposed converter is less than that of the conventional DCM interleaved boost. Moreover, the proposed converter provides soft switching for all of the semiconductors in the circuit. It can provide ZVS for the switches and ZCS for the diodes, whereas the traditional DCM boost converter cannot provide ZVS for the MOSFETs. In other words, the traditional DCM boost converter cannot discharge the parasitic capacitor of the switches and the diodes prior to turning ON the switches. This causes the discharge of the parallel capacitors of the MOSFETs into the switches at turn-ON. This restricts the function of the traditional boost converter in higher frequencies.

The interleaved boost has the same components with a constant switching frequency equal to the nominal frequency (230 kHz) of the designed converter. This is helpful in keeping the efficiency of the interleaved boost high, because of the switching losses. Although the switching frequency of the interleaved boost converter is rather low compared to the proposed converter in lighter loads, the efficiency is not higher as shown in Fig. 11(a). Fig. 11(a) shows 2% improvement in the efficiency of the proposed converter at the nominal load compared to the traditional interleaved boost converter with the same components. As seen in Fig. 11(a), the efficiency of the proposed converter is always higher than the efficiency of the interleaved boost converter from light load to full loading conditions at the nominal input voltage. The efficiency of the proposed converter in different input voltages has been also compared with that of the traditional DCM boost converter in Fig. 11(b).

As stated, low inductances are used in the proposed converter. The same components listed in Table I have been used in both of the proposed converter and the interleaved boost. The traditional interleaved boost works with 70 μH inductors and 230 kHz switching frequency. With these values, each of the

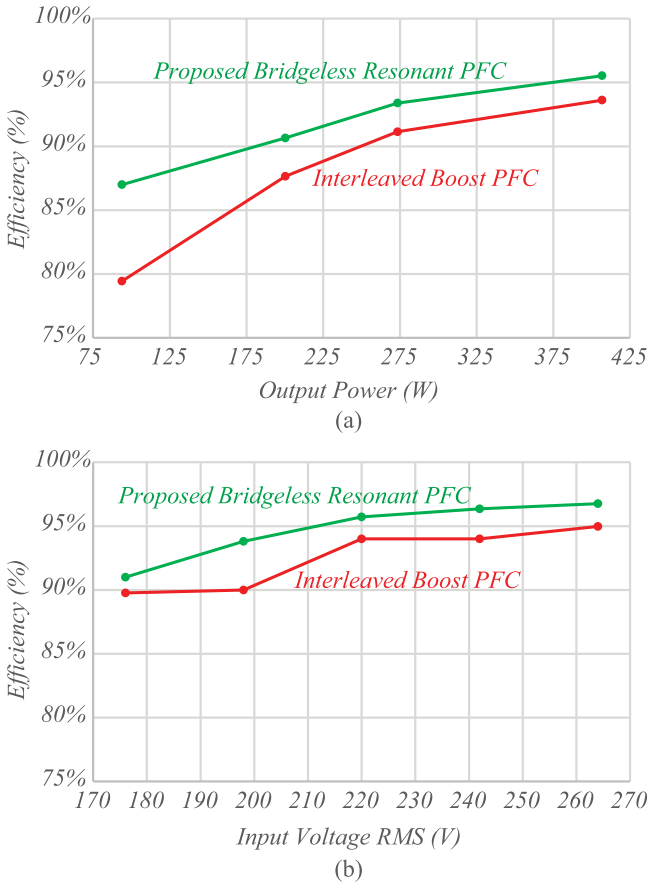


Fig. 11. Efficiency of the proposed converter compared with the conventional interleaved boost PFC converter with the same components in (a) different output power levels, and (b) at the nominal load in different input voltage levels.

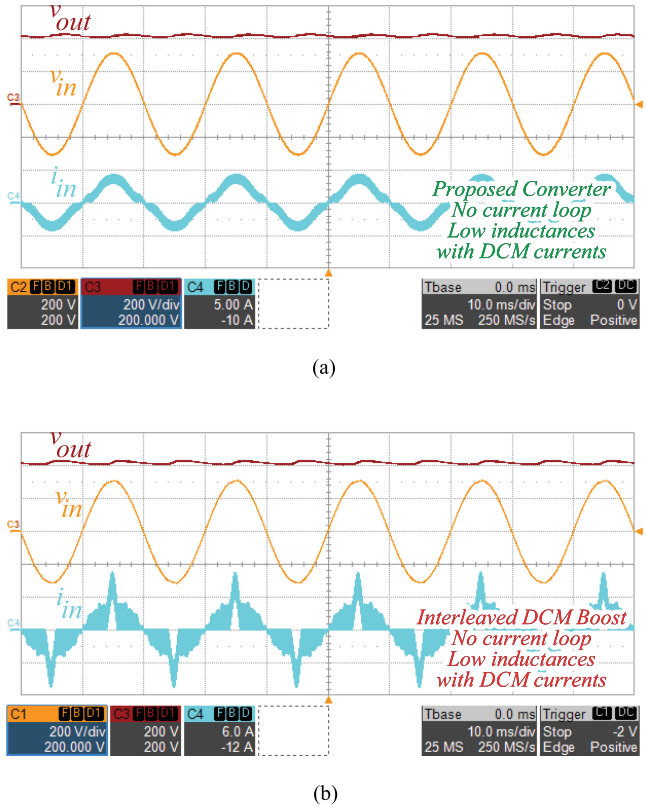


Fig. 12. (a) Input voltage and current, and output voltage of the proposed converter at full load. (b) Input voltage and current, and output voltage of the conventional interleaved boost converter with the same components at full load. The same components are used for both of the converters. No current loops have been used in any of the converters. The measured power factor for the proposed converter is near unity, and for the traditional interleaved boost converter is 0.74.

inductors' currents in the traditional interleaved boost are always discontinuous in the full operating conditions. This happens even at full load. Therefore, the interleaved boost converter with low inductances with discontinuous currents can have an intrinsic high power factor even without a current loop. This characteristic has been proved mathematically in [43]. The input current of interleaved boost converter, however, is the sum of the currents of the two inductors. In the specified operating conditions, the input current of the conventional converter is continuous in only a very small fraction of the line cycle. In other words, the average of the input current in the DCM interleaved boost is approximately sinusoidal. However, since bulky filtering elements are not used in the structures, the input current is discontinuous in most of the line cycle even at the nominal load. This reduces the power factor and increases the THD significantly. On the other hand, the input current of the proposed converter remains continuous with the same conditions. Input current, input voltage, and the output voltage of the proposed converter have been shown in Fig. 12(a), as well as those of the conventional interleaved boost in Fig. 12(b). Both of the converters are running at full load with 220 V rms input voltage. To have a better view of the converters' operations, these waveforms are measured without any filter elements in the input. This means that the input characteristics of the proposed converter is similar to a CCM converter, even with the small inductors used. The measured power factor for the proposed converter is near unity. Nonetheless, the interleaved boost converter has 0.74 input power factor with the same components. No additional filter is used in the input of the converters. This shows that the required input filter size in the proposed converter would be smaller than that of the conventional interleaved boost converter.

The power factor and THD of the proposed converter compared to the conventional interleaved boost structure are shown in Fig. 13(a) and (b), respectively. Fig. 13 shows that the power factor of the proposed converter is more than that of the conventional converter with the same components in different load levels. The input current waveform of the interleaved boost converter along with that of the proposed converter has been shown in Fig. 12. As seen, the input current of the interleaved boost is discontinuous in most of the line cycle. However, input current of the proposed converter is continuous with the same inductors at the same operating conditions. As the output power decreases, the input current of the interleaved boost gets more discontinuous, which results in the reduction of the PF and/or increase in the THD. This characteristic has been reflected in Fig. 13(a) and (b) in different output power levels.

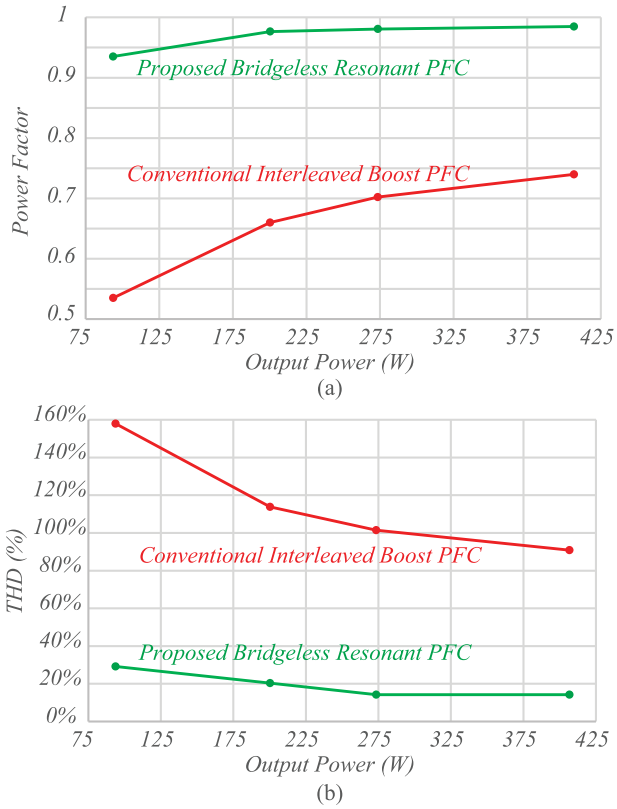


Fig. 13. (a) Power factor, and (b) total harmonic distortion (THD%) of the proposed converter compared to the conventional interleaved boost converter versus output power levels. The same components have been used in both of the converters.

VI. Conclusion

A resonant bridgeless PFC rectifier with high frequency and inherent power factor capabilities has been proposed in this paper with the related theoretical analysis and experimental results. The proposed converter can provide continuous input current with low THD, even with small inductances with discontinuous currents. The proposed structure is simple, symmetrical, and bridgeless. In addition, as shown in the experimental waveforms, the analyzed converter provides soft switching for all of the semiconductors in the structure, helping to further increase the efficiency at high frequencies. The simple variable frequency method has been used for the modulation with complementary gate signals with constant ≈50% duty cycles plus deadtime. The proposed converter has been compared with a conventional interleaved boost converter with the same components, resulting in 2% improvement in the efficiency at full load and more than 8% under light loading conditions. The proposed converter also provides a near-unity power factor at full load with no current loops and no extra filter elements.

References

[1] *Electromagnetic Compatibility (EMC) – Part 3-2: Limits – Limits for Harmonic Current Emissions (Equipment Input Current ≤16 A per Phase)*, IEC 61000-3-2:2018, International Electrotechnical Commission, Geneva, Switzerland, Jan. 2018.

[2] G. B. B. Singh and V. Garg, "An input current waveshaping ac-dc converter for rectifier loads," *J. Power Electron.*, vol. 8, no. 1, pp. 1–9, 2008.

[3] M. Kazerani, P. D. Ziogas, and G. Joos, "A novel active current waveshaping technique for solid-state input power factor conditioners," *IEEE Trans. Ind. Electron.*, vol. 38, no. 1, pp. 72–78, Feb. 1991.

[4] A. R. Prasad, P. D. Ziogas, and S. Manias, "An active power factor correction technique for three-phase diode rectifiers," *IEEE Trans. Power Electron.*, vol. 6, no. 1, pp. 83–92, Jan. 1991.

[5] M. Mahdavi and H. Farzanehfard, "Zero-voltage transition bridgeless single-ended primary inductance converter power factor correction rectifier," *IET Power Electron.*, vol. 7, no. 4, pp. 895–902, Apr. 2014.

[6] H. Valipour, G. Rezazadeh, and M. R. Zolghadri, "Flicker-free electrolytic capacitor-less universal input offline led driver with PFC," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6553–6561, Sep. 2016.

[7] H. Valipour, G. Rezazadeh, M. R. Zolghadri, and N. Noroozi, "Electrolytic capacitor-less ac-dc led driver with constant output current and PFC," in *Proc. 6th Power Electron. Drive Syst. Technol. Conf.*, Feb. 2015, pp. 107–112.

[8] M. A. Saket, M. Ordonez, and N. Shafiei, "Planar transformers with near-zero common-mode noise for flyback and forward converters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1554–1571, Feb. 2018.

[9] C. M. Wang, "Zero-current-switching PWM power-factor-correction converter," *IEE Proc. Elect. Power Appl.*, vol. 152, no. 5, pp. 1233–1238, Sep. 2005.

[10] H. Bodur and S. Yldrmaz, "A new ZVT snubber cell for PWM-PFC boost converter," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 300–309, Jan. 2017.

[11] M. M. Jovanovic and Y. Jang, "State-of-the-art, single-phase, active power-factor-correction techniques for high-power applications— An overview," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 701–708, Jun. 2005.

[12] M. A. Saket, M. Ordonez, M. Craciun, and C. Botting, "Improving planar transformers for LLC resonant converters: Paired layers interleaving," *IEEE Trans. Power Electron.*, to be published, doi: 10.1109/TPEL.2019.2903168.

[13] H. Valipour and M. Ordonez, "High efficiency LC resonant boost topology: Analysis and design," in *Proc. IEEE Energy Convers. Congr. Expo.*, Oct. 2017, pp. 3427–3432.

[14] H. Ma, Y. Li, J. S. Lai, C. Zheng, and J. Xu, "An improved bridgeless SEPIC converter without circulating losses and input voltage sensing," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1447–1455, Sep. 2018.

[15] B. Singh and R. Kushwaha, "A PFC based EV battery charger using a bridgeless SEPIC converter," in *Proc. IEEE 7th Power India Int. Conf.*, Nov. 2016, pp. 1–6.

[16] M. Mahdavi and H. Farzanehfard, "Bridgeless SEPIC PFC rectifier with reduced components and conduction losses," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4153–4160, Sep. 2011.

[17] M. Mahdavi and H. Farzaneh-Fard, "Bridgeless CUK power factor correction rectifier with reduced conduction losses," *IET Power Electron.*, vol. 5, no. 9, pp. 1733–1740, Nov. 2012.

[18] L. Huang, F. Chen, W. Yao, and Z. Lu, "Flexible mode bridgeless boost PFC rectifier with high efficiency over a wide range of input voltage," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3513–3524, May 2017.

[19] T.-F. Wu, J.-C. Hung, S.-Y. Tseng, and Y.-M. Chen, "A single-stage fast regulator with PFC based on an asymmetrical half-bridge topology," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 139–150, Feb. 2005.

[20] Y. Xiao, Z. Yan, H. Qin, J. Li, and Q. Zheng, "An LLC resonant ac-dc converter with PFC function based on a double inductor structure," in *Proc. 5th Int. Conf. Instrum. Meas. Comput. Commun. Control*, Sep. 2015, pp. 645–650.

[21] J. Leigh *et al.*, "Scalable resolution display walls," *Proc. IEEE*, vol. 101, no. 1, pp. 115–129, Jan. 2013.

[22] M. Dong and L. Zhong, "Power modeling and optimization for OLED displays," *IEEE Trans. Mobile Comput.*, vol. 11, no. 9, pp. 1587–1599, Sep. 2012.

[23] J. Turchi, "Key steps to design an interleaved PFC stage driven by the NCP1631," *Appl. Note AND8407/D*. [Online]. Available: http://www.onsemi.com/

[24] J. Moldaschl and M. Darwish, "An ultra flat profile natural interleaved power factor corrector with advanced power management," in *Proc. 24th Telecommun. Forum*, Nov. 2016, pp. 1–4.

[25] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode (TCM) single-phase PFC rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 873–882, Feb. 2014.

[26] F. Musavi, W. Eberle, and W. G. Dunford, "A high-performance single-phase bridgeless interleaved PFC converter for plug-in hybrid electric vehicle battery chargers," *IEEE Trans. Ind. Appl.*, vol. 47, no. 4, pp. 1833–1843, Jul. 2011.

[27] M. Mahdavi and H. Farzanehfard, "Zero-current-transition bridgeless PFC without extra voltage and current stress," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2540–2547, Jul. 2009.
[28] H. F. M. Mahdavi, "A new zero voltage transition bridgeless PFC with reduced conduction losses," *J. Power Electron.*, vol. 9, no. 5, pp. 708–717, Sep. 2009.
[29] M. Ramezani and S. M. Madani, "New zero-voltage-switching bridgeless P, using an improved auxiliary circuit," *IET Power Electron.*, vol. 4, no. 6, pp. 732–741, Jul. 2011.
[30] W. Y. Choi, J. M. Kwon, and B. H. Kwon, "Bridgeless dual-boost rectifier with reduced diode reverse-recovery problems for power-factor correction," *IET Power Electron.*, vol. 1, no. 2, pp. 194–202, Jun. 2008.
[31] C. M. Wang, "Zero-current-switching PWM power-factor-correction converter," *IEE Proc. Elect. Power Appl.*, vol. 152, no. 5, pp. 1233–1238, Sep. 2005.
[32] H. Valipour, M. Ordonez, and M. Mahdavi, "High efficiency interleaved LC resonant boost topology: Analysis and design," *IEEE Trans. Power Electron.*, to be published, doi: 10.1109/TPEL.2019.2898460.
[33] M. Mohammadi, E. Adib, and M. R. Yazdani, "Family of soft-switching single-switch PWM converters with lossless passive snubber," *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 3473–3481, Jun. 2015.
[34] S. W. Lee and H. L. Do, "Soft-switching two-switch resonant ac/dc converter with high power factor," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 2083–2091, Apr. 2016.
[35] D. L. O'Sullivan, M. G. Egan, and M. J. Willers, "A family of single-stage resonant ac/dc converters with PFC," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 398–408, Feb. 2009.
[36] A. A. Fardoun, E. H. Ismail, M. A. Al-Saffar, and A. J. Sabzali, "A bridgeless resonant pseudoboost PFC rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5949–5960, Nov. 2014.
[37] M. Alam, W. Eberle, D. S. Gautam, C. Botting, N. Dohmeier, and F. Musavi, "A hybrid resonant pulse-width modulation bridgeless ac/dc power factor correction converter," *IEEE Trans. Ind. Appl.*, vol. 53, no. 2, pp. 1406–1415, Mar. 2017.
[38] M. Alam, W. Eberle, D. S. Gautam, and C. Botting, "A soft-switching bridgeless ac/dc power factor correction converter," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7716–7726, Oct. 2017.
[39] E. A. A. Emrani, M. Mahdavi and E. Adib, "Soft Switching Bridgeless PFC Buck Converters," *J. Power Electron.*, vol. 12, no. 2, pp. 268–275, Mar. 2012.
[40] M. Alam, W. Eberle, and N. Dohmeier, "An inrush limited, surge tolerant hybrid resonant bridgeless PWM ac-dc PFC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2014, pp. 5647–5651.
[41] M. Alam, W. Eberle, C. Botting, and M. Edington, "A bridgeless hybrid-resonant PWM zero voltage switching boost ac-dc power factor corrected converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2014, pp. 606–610.
[42] A. Emrani, M. R. Amini, and H. Farzaneh-Fard, "Soft single switch resonant buck converter with inherent PFC feature," *IET Power Electron.*, vol. 6, no. 3, pp. 516–522, Mar. 2013.
[43] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. New York, NY, USA: Springer, 2001.

Hamed Valipour (S'14) was born in Tehran, Iran. He received the B.Sc. and M.Sc. degrees from the Sharif University of Technology, Tehran, Iran, in 2012 and 2014, respectively, both in electrical engineering. He is currently working toward the Ph.D. degree at the University of British Columbia (UBC), Vancouver, BC, Canada.

He has been involved in many research and industrial projects including design and implementation of power electronics circuits in renewable energies, electric vehicles, LED drivers, voltage monitoring relays, and firmware design for numerous applications. His research interests include design and implementation of power electronic circuits (soft-switching techniques, renewable energies, electric vehicles, high-frequency converters), and firmware development.

Mr. Valipour is the recipient of numerous awards and scholarships for his academic performance including the Four Year Fellowship (2016), and Graduate Support Initiative Scholarships (2018) from UBC.

Mohammad Mahdavi was born in Isfahan, Iran, in 1984. He received the B.S, M.S., and Ph.D. degrees in electrical engineering from the Isfahan University of Technology, Isfahan, Iran, in 2006, 2009, and 2013 respectively.

He joined Islamic Azad University, Isfahan, Iran, as an Assistant Professor. He is currently a Post-doctoral Fellow with the Department of Electrical and Computer Engineering, University of British Columbia, Vancouver, BC, Canada. His research interests include power electronics, power factor correction converters, soft-switching techniques, renewable energies, electric vehicles, and high frequency converters.

Martin Ordonez (S'02–M'09) was born in Neuquen, Argentina. He received the Ing. degree in electronics engineering from National Technological University, Cordoba, Argentina, in 2003, and the M.Eng. and Ph.D. degrees in electrical engineering from the Memorial University of Newfoundland (MUN), St. John's, NL, Canada, in 2006 and 2009, respectively.

He is currently a Professor and Canada Research Chair in power converters for renewable energy systems with the Department of Electrical and Computer Engineering, University of British Columbia (UBC), Vancouver, BC, Canada. He is also the holder of the Fred Kaiser Professorship in Power Conversion and Sustainability at UBC. He was an Adjunct Professor with Simon Fraser University, Burnaby, BC, Canada, and MUN. His industrial experience in power conversion includes research and development at Xantrex Technology Inc./Elgar Electronics Corp. (now AMETEK Programmable Power in San Diego, California). With the support of industrial funds and the Natural Sciences and Engineering Research Council, he has contributed to more than 150 publications and R&D reports.

Dr. Ordonez is a Guest Editor for the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, and Editor for the IEEE TRANSACTIONS ON SUSTAINABLE ENERGY. He is with several IEEE committees, and reviews widely for IEEE/IET journals and international conferences. He was the recipient of the David Dunsiger Award for Excellence in the Faculty of Engineering and Applied Science (2009) and the Chancellors Graduate Award/Birks Graduate Medal (2006), and became a Fellow of the School of Graduate Studies, MUN.