Noninverting Buck–Boost DC–DC Converter Using a Duobinary-Encoded Single-Bit Delta-Sigma Modulator

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***Abstract*—This paper presents a delta-sigma modulation (DSM) control scheme for noninverting buck–boost (NIBB) converter that features a duobinary encoding for four power switch controls. The proposed scheme converts the single-bit output of the modulator into a 1.5-b signal to enable a three-phase operation comprising the charging, bypassing, and discharging phases. This control method reduces both switching and conduction losses by changing only two switches in each period, thus, achieving high conversion efficiency. A smooth mode transition is provided by the DSM controller, which automatically and continuously determines the operating mode of the converter. Thus, the dead zone can be effectively released with improved transient responses. Furthermore, the spurious tones in the output are effectively eliminated by the robust noise shaping capability of the modulator. The proposed DSM-based NIBB converter was implemented on a 180-nm CMOS. It regulated the output in the range of 2.0–4.6 V with input voltage of 2.5–5.0 V, and the maximal load current was 500 mA. The converter showed a peak efficiency of 94.8% at 90-mA load and the output voltage ripples were maintained under 18 mV. A low noise floor with the first spurious peak located –92 dBc below the signal was achieved across all mode operations. In addition, the converter occupied a small chip area of 1.51 mm^2.**

***Index Terms*—Deadtime control, delta-sigma modulator, duobinary encoding, noninverting buck–boost converter, switching noise.**

I. Introduction

With increasing use of battery-powered portable electronics such as mobile phones and laptops, efficient power management techniques have become the most important design criteria to extend the battery life [1], [2]. Noninverting buck–boost converters (NIBBs) are appropriate solutions for using the full battery capacity more effectively due to their ability to provide wide operating ranges of input and output voltages [2]–[14]. These converters operate in the buck and boost modes or in the buck–boost (BB) mode depending on the magnitudes of the input and output voltages. Unlike buck and boost converters, which have two power switches, conventional NIBB converters consist of four power switches, and the two additional power switches cause higher switching and conduction losses. Several control methods have been proposed to improve its efficiency.

The NIBB converters based on the traditional two-phase BB mode operation in which all four switches are turned ON and OFF during the single switching period are presented in [2] and [3]. These control methods increase the switching loss and deteriorate the conversion efficiency, especially when the input voltage (V_{IN}) approaches the output voltage (V_{OUT}), as the average inductor current is twice the load current [4]. An improved three-phase switching method consisting of charging, discharging, and bypassing phases was proposed to improve the efficiency of the converter [4]–[7]. In this method, only two switches change their states in each period, rather than four switches, that reduce the switching and conduction losses. To further improve the efficiency, the converters are made to operate in the buck or boost mode only depending on whether V_{OUT} is higher or lower than V_{IN} [8]–[10]. These converters may be more efficient because they do not operate in the complicated BB mode. Although the efficiency of the NIBB converters can be improved through various control methods, these methods require additional comparators and circuits for dividing the submodes and complex control.

The dead zone arising from the mode change between the buck and boost operations continues to be a problem [2]–[8], [11]–[13]. The dead zone represents nonlinearity in the voltage transfer function and causes pulse skipping and random jumps of the output voltage, resulting in increased output voltage ripple and instability during mode transition. The simplest way is to control the converter solely by operating in the two-phase BB mode at the cost of decreased efficiency [2], [3]. The improved approach to mitigate the dead zone problem is to insert an intermediate region such as the BB mode between the buck and boost modes [4], [5], [11]. This approach reduces the discontinuity in the converter, but inevitably creates efficiency issues in the BB mode. Other results have been reported in [6], [8], [12], and [13], where the duty cycles of both the buck and boost modes are overlapped and clamped with the appropriate value. Consequently, the dead zone can be effectively released with high efficiency. However, these earlier works are based on

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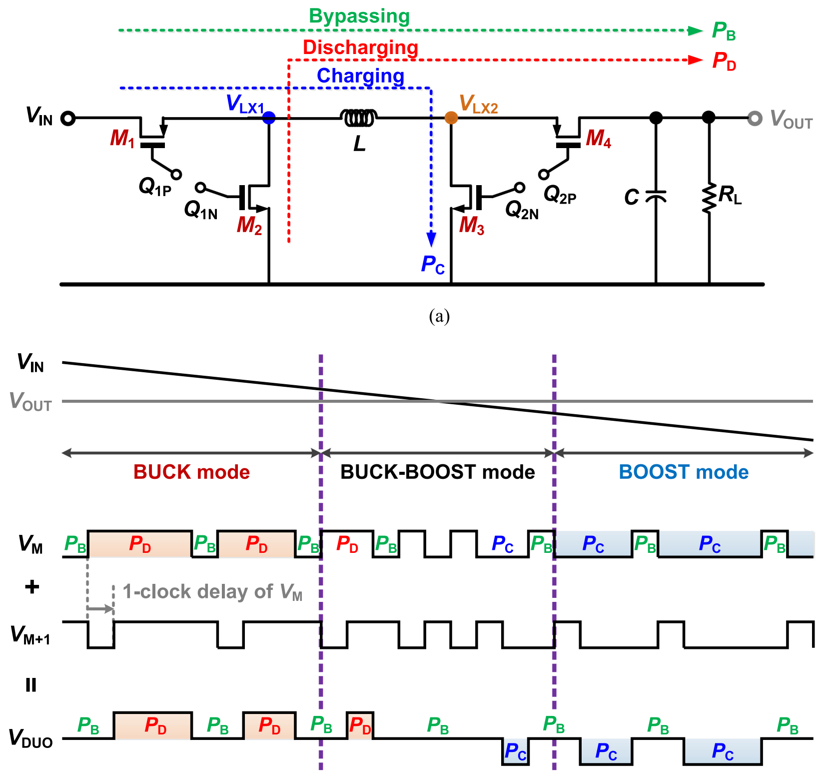


(a)

(b)

Fig. 1. Proposed control scheme of power switches using three-level signaling. (a) NIBB converter switches and three-phase operation. (b) Proposed control scheme with duobinary encoding.

complicated control algorithms, which are difficult to implement in a practical system.

A delta-sigma modulator (DSM) controller for dc–dc converters offer many advantages, such as reduction of output harmonics, alleviation of electromagnetic interferences (EMI), and high efficiency with scalable sampling frequency (f_S) [15]. Prior works on single-bit DSM controlled power converters are limited to only buck and boost converters [15]–[18]. Their control schemes are not directly applicable to NIBB converters because the single-bit output of the DSM cannot independently control four switches. A multibit DSM in combination with a digital pulsewidth modulation (PWM) is applied to the NIBB converter in [19] and [20]. It is possible to obtain a low output ripple through high resolution DSM, but the increased switching activity and higher inductor current leads to lower conversion efficiency. Therefore, it is necessary to produce a new control method to obtain low switching noise and high efficiency with low design complexity when applying single-bit DSM to a NIBB converter.

This paper presents a low switching noise NIBB dc–dc converter, which uses a single-bit DSM controller. The proposed converter improves the conversion efficiency by duobinary encoding, which transforms the single-bit modulator output to three-level output, thereby enabling three-phase operation with reduced switching and conduction losses. Moreover, a smooth mode transition is obtained because the operating mode of the NIBB converter is continuously and automatically determined by the modulator. The remainder of this paper is organized as follows. Section II introduces the proposed NIBB converter architecture. Section III describes the detailed circuit implementations. Section IV presents the experimental results of the prototype converter. Section V presents the conclusion.

II. Proposed DSM-Based NIBB Converter

A. Control Method of Power Switches

We propose a switching method of power transistors based on a single-bit DSM. Owing to the oversampling nature of the DSM, the modulator accurately estimates the input signal by averaging a number of samples even though the instantaneous output is very coarse [21]. Thus, if the DSM is used as a switch controller, the averaged ON duty duration of the modulator output (V_M) is proportional to the magnitude of V_{IN}, as shown in Fig. 1. V_M determines how the switches should operate in each mode. When V_{IN} is significantly higher than V_{OUT}, the converter may operate in the buck mode, where the duty of the discharging phase (P_D) is controlled by the ON duration of V_M. When V_{IN} is much lower than V_{OUT}, it may operate in the boost mode, where the duty of the charging phase (P_C) is controlled by the OFF duration of V_M. When V_{IN} is close to V_{OUT}, it may operate in the BB mode, where the three phases are operated successively to achieve high efficiency. However, the single-bit output of V_M is unable to directly control the four switches in the three-phase operation. The controller output should have a control signal of at least 1.5 b to perform this operation. Therefore, duobinary encoding technique is applied to the DSM output.

Although duobinary encoding has been widely used in data communications, it can be applied to a switching converter for efficient power switch control. This technique is an amplitude modulation scheme, where the bit stream is manipulated to reduce the bandwidth and certain phenomena that lead to inter symbol interference [22]. Using this method, the binary signal V_M is converted to a three-level duobinary-encoded signal $V_{\rm DUO}$, as shown in Fig. 1(b). $V_{\rm DUO}$ can be represented by

$$V_{\rm DUO} = V_M + V_{M+1} \tag{1}$$

where V_{M+1} is a one-clock delayed signal of V_M. Thus, $V_{\rm DUO}$ gives the output levels 0, 1, and 2. Note that the averaged pulse duration of $V_{\rm DUO}$ is proportional to the magnitude of $V_{\rm IN}$–$V_{\rm OUT}$ in the time domain. In addition, the noise shaping characteristic of the DSM is preserved while the spectral width is narrowed in the frequency domain. The detailed frequency spectrum is provided in Section III. Therefore, a modulator output with duobinary encoding can be directly used to control NIBB switches.

When $V_{\rm IN} \gg V_{\rm OUT}$, the converter operates in two-phase (P_D and bypassing phase (P_B)) buck mode because $V_{\rm DUO}$ produces only 1 and 2 output levels. $V_{\rm OUT}$ regulation is obtained by adjusting the discharging phase according to $V_{\rm IN}$. When $V_{\rm IN} \ll V_{\rm OUT}$, the converter operates in the two-phase (P_C and P_B) boost mode because $V_{\rm DUO}$ produces only 0 and 1 output levels. $V_{\rm OUT}$ regulation is obtained by adjusting the charging phase according to $V_{\rm IN}$. When $V_{\rm IN} \sim V_{\rm OUT}$, the converter operates in the three-phase (P_D, P_B, and P_C) BB mode. As $V_{\rm IN}$ approaches $V_{\rm OUT}$, V_M produces equal numbers of high and low outputs, and $V_{\rm DUO}$ mainly outputs the intermediate value of 1; therefore, the bypassing phase becomes a dominant operation in this mode. To enable discharging or charging operation in this mode, V_M should be maintained high or low, respectively, for more than two cycles, as shown in Fig. 1(b). It is worth noting that because the DSM controller outputs an average value of the input signal, the converter may perform different switching operations depending on the output data stream of the DSM even at the same input voltage. Thus, the operating mode cannot be clearly distinguished. Nonetheless, the converter can achieve robust performance through continuous and seamless switching operation of the DSM.

The proposed switching technique using a three-level signaling has several advantages when compared with conventional NIBB controllers. First, the proposed control scheme enables highly energy efficient operation in the BB mode because it performs a three-phase operation. Successively operated three-phase switching effectively reduces both the switching and conduction losses [9]. Second, the mode transition is automatically determined by the operation of the DSM rather than by a specific criterion; it is simple to design without a complicated mode change algorithm or additional circuitry. Furthermore, the continuous bit stream of the DSM suppresses the dead zone occurrence to enable smooth mode conversion and small voltage ripple even though the boundary of the mode cannot be clearly distinguished. Finally, replacing a conventional controller with a DSM can reduce the switching harmonics and EMI because a DSM has noise shaping capability and produces a variable output frequency through the pulse-density-modulated signal [15],

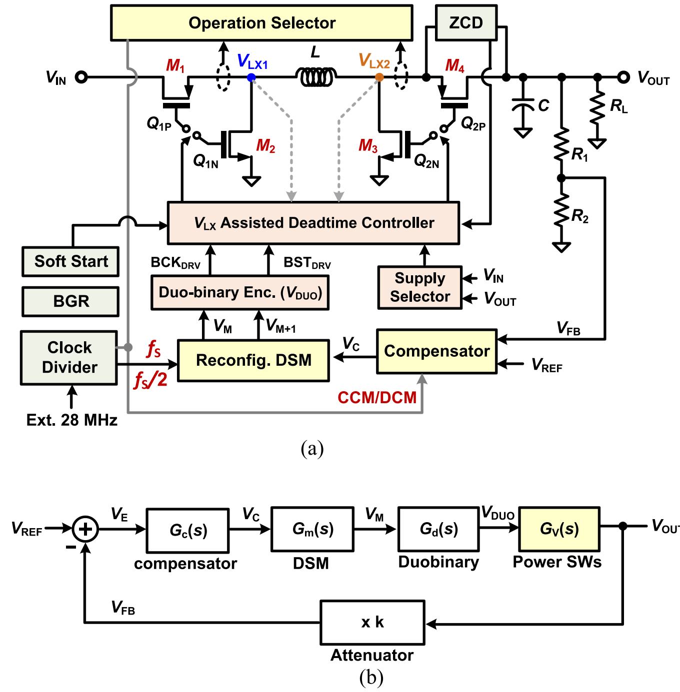


Fig. 2. Proposed DSM-based NIBB converter. (a) Block diagram. (b) Small signal model.

[16]. The implemented DSM also produces a wide-range sampling frequency and has low power consumption, resulting in improved conversion efficiency over the entire load range.

B. DSM-Based NIBB Converter Architecture

Fig. 2(a) shows the block diagram of the proposed DSM-based NIBB converter. This converter is composed of a power stage, a feedback network, and control blocks. The power stage contains four switches (M_1–M_4), an inductor L, and an output capacitor C. M_1–M_4 are integrated into the chip, whereas L and C are composed of external components consisting of a 3-μH inductor and 20-μF capacitor. The output voltage $V_{\rm OUT}$ is scaled down to $V_{\rm FB}$ by resistor dividers R_1 and R_2. The difference between $V_{\rm FB}$ and the reference voltage $V_{\rm REF}$ is processed by the compensator, which generates the compensation signal V_C and ensures the stability of the converter. The DSM reconfigures the loop filter (LF) structure according to the operating condition of the converter and converts V_C into the noise-shaped single-bit signal V_M [15]. The transformation of the LF structure is intended to obtain a scalable f_S operation with enhanced converter efficiency. Moreover, the switching noise of this converter can be effectively reduced by the noise-shaped and pulse-density modulated output signal of the DSM. The binary signal V_M is encoded into a duobinary signal $V_{\rm DUO}$ for efficient power switch control. Finally, $V_{\rm DUO}$ drives the power stage through switching nodes ($V_{\rm LX1}$ and $V_{\rm LX2}$) assisted deadtime controller. In addition, the operation selector detects the averaged inductor current and determines the operating conditions of the reconfigurable DSM and compensator. The operating conditions are simply divided into continuous-conduction mode (CCM) operation and discontinuous-conduction mode (DCM) operation.

TABLE I
OVERALL OPERATING CONDITIONS OF THE PROPOSED NIBB CONVERTER

Operating conditions		
Converter operation	**Reconfigurable DSM**	
	LF order	**f_S (MHz)**
CCM	3	14
DCM	2	7

The DSM changes the LF order and f_S for each operation. The clock signal is applied by an external 28-MHz signal source, which is reproduced as 14- and 7-MHz signals that are fed to the DSM through an internal divider circuit. Table I presents the detailed operating conditions of the proposed converter. A bandgap reference, soft start, and zero current detector (ZCD) are also included for more robust operation.

C. Loop Analysis

The small signal model of the proposed buck–boost converter is shown in Fig. 2(b). $G_c(s)$ is the transfer function (TF) of the loop compensator, $G_m(s)$ is the TF of the DSM, $G_d(s)$ is the TF of the duobinary encoder, and $G_v(s)$ is the control-to-output TF of the power stage. The overall loop TF of the converter is $G_{TF}(s) = \mathrm{k} \cdot G_c(s) \cdot G_m(s) \cdot G_d(s) \cdot G_v(s)$. All TFs should be determined to achieve an optimum phase margin and loop bandwidth. The TFs of the power switches are described here and those of the compensator, DSM, and duobinary encoder are described in the next section along with the loop compensation results.

The operating conditions of the proposed converter are categorized as CCM and DCM operations. In the DCM operation, the converter has a first-order response that simplifies the control loop design; hence, only the analysis of the CCM operation is described here for simplicity. The TFs of the buck and boost stages in CCM can be expressed as [23]

$$G_{V,\mathrm{buck}}(s) = \frac{V_{\mathrm{IN}} \cdot R_L}{s^2 \cdot LCR_L + s \cdot L + R_L} \tag{2}$$

$$G_{V,\mathrm{boost}}(s) = \frac{R_L(1-D)^2 - s \cdot L}{s^2 \cdot LCR_L + s \cdot L + R_L(1-D)^2} \cdot \frac{V_{\mathrm{IN}}}{(1-D)^2} \tag{3}$$

where $D = 1 - V_{\mathrm{IN}}/V_{\mathrm{OUT}}$. In the buck mode, one pole and two zeros are added at the dc and half the conjugate pole, respectively, to make the loop stable. The boost mode also has a conjugate pole at the resonant frequency, which changes with the input voltage. Moreover, a right-half-plane zero (RHPZ) exists that can make control difficult in this mode. Because the TFs of the power stage are changed with the operating mode and load current, the loop compensation should be carefully designed. Note that because the proposed converter operates in the buck, BB, and boost modes, the loop analysis in the BB mode is additionally required. However, because the BB mode is a combination of the buck and boost operations (the converter operates only in buck or boost mode in the refined range), a stable frequency response in the buck and boost conditions can ensure BB mode stability.

III. CIRCUIT IMPLEMENTATION

The proposed NIBB converter is designed for a supply of 2.5–5.0 V, output voltage of 2.0–4.6 V, and output current of 1–500 mA. It uses two different switching frequencies of 7 and 14 MHz with a reconfigurable DSM structure. This section provides a detailed circuit implementation of the DSM, duobinary encoder, compensator, and deadtime controller for the proposed NIBB converter.

A. Reconfigurable DSM

The DSM in the proposed NIBB converter is employed as a controller of the power switches and it determines the operating regions of the buck, BB, and boost modes automatically by adjusting the on-time duration of the output V_M according to the relationship between V_{IN} and V_{OUT}. This modulator does not require any additional circuitry such as dual-ramp generator and comparators, which are essential for independent mode operation [6], [9]. In addition to these features, the DSM is utilized to suppress the switching harmonics by means of its noise shaping capability. Generally, the quality of noise rejection is proportional to the order of DSM and f_S, but a higher order DSM leads to a lower stability and a faster f_S produces more switching losses. To cope with this problem, the proposed DSM changes f_S along with the LF structure depending on the load current [15], as shown in Fig. 3. In the CCM operation, where the CCM switches (S_C) are closed and DCM switches (S_D) are opened, the third-order LF and high f_S are adopted for effective harmonic rejection and improved output ripple characteristics. As the load current decreases, f_S scaling is required to reduce the switching losses, but this may cause the third-order DSM to become unstable. Therefore, in the DCM operation, the third-order LF is changed to the second-order LF with half f_S. Here, S_C are opened and S_D are closed. This ensures stable operation of the DSM and improves the conversion efficiency over a wide load range.

The proposed DSM adopts continuous-time architecture and reconfigures the LF structure with single op-amp resonators (SORs), as shown in Fig. 3. The SOR merges multiple integrators into a single op-amp while providing the same dynamic characteristics, resulting in improved power and area efficiency [24], [25]. The inverted buffer in Fig. 3 is easily implemented using a cross-coupled connection of the differential signal. The detailed circuit configuration, operation, and mathematical analysis are described in our previous work [15]. This approach has two main differences when compared with [15]. First, the operating conditions of the DSM are divided into CCM and DCM for simplicity. Although the subdivided operating conditions may show improved performance, these conditions are simplified to focus on the feasibility of the DSM-based NIBB converter. Second, the conventional buck or boost converter uses the DSM output V_M directly, but the NIBB converter requires a 1.5-b duobinary-encoded signal V_{DUO} obtained by converting V_M. As can be seen in Fig. 1, the fastest transition of V_{DUO} from the

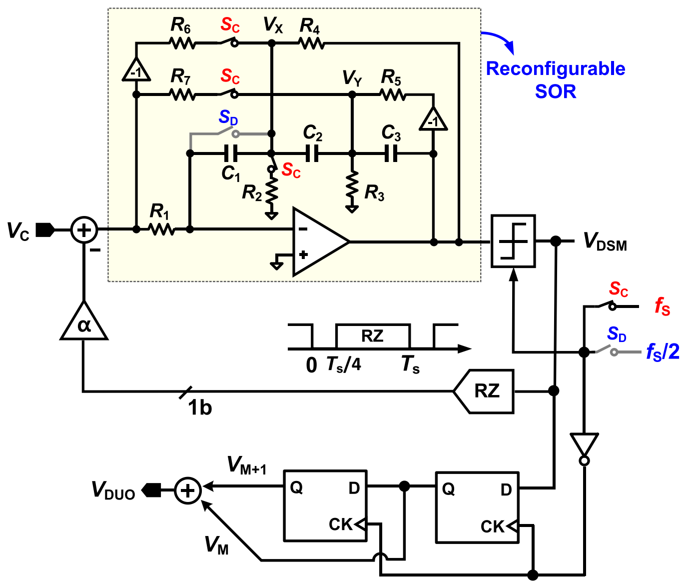


Fig. 3. Proposed reconfigurable DSM with duobinary output.

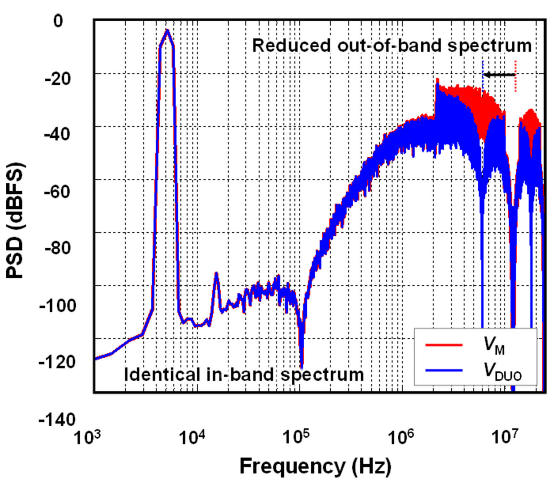
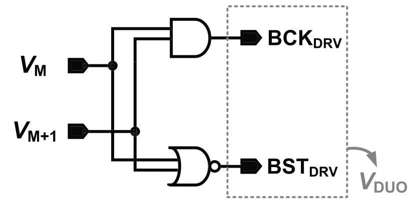


Fig. 4. Comparisons of output spectra of the single-bit DSM (V_M) and 1.5-b duobinary output (V_{DUO}).

highest level 2 to the lowest level 0 or vice versa needs at least two-bit intervals, which is twice the original binary sequence. This corresponds to a bandwidth reduction by a factor of two or doubling the rate of the binary sequence. Therefore, the spectral width of V_{DUO} is narrowed whereas the in-band noise shaping characteristic is maintained. Fig. 4 compares the power spectral densities of V_M and V_{DUO}. The reduced spectral power of V_{DUO} at half the sampling frequency is apparent and the two spectra are virtually the same at the in-band. With this duobinary interface, the DSM produces 1.5-b output data stream with reduced energy at high frequencies, thereby effectively maintaining its switching noise rejection capability.



(a)

V_M	V_{M+1}	V_{DUO}	BCK_{DRV}	BST_{DRV}	Switching Phase	On switches
0	0	0	0	1	P_C	M_1 & M_3
0	1	1	0	0	P_B	M_1 & M_4
1	0					
1	1	2	1	0	P_D	M_2 & M_4

(b)

Fig. 5. Duobinary encoder. (a) Circuit implementation. (b) Operations.

The TF of the third-order SOR in CCM is expressed as Eq. (4) shown at the bottom of this page, where $R_X\ (= R_2\|R_4\|R_6)$ and $R_Y\ (= R_3\|R_5\|R_7)$ are defined as the equivalent resistances of the parallel-connected resistors at the V_X and V_Y nodes, respectively. $C\ (= C_1 = 2C_2 = C_3)$ is the typical capacitance of the series-connected capacitors. The signal transfer function (STF) can be used to evaluate how the DSM affects the signal response from its input to the output [21]. The STF of the DSM is simply defined as

$$G_m(s) = \frac{H_{\mathrm{SOR,CCM}}(s)}{1 + \alpha \cdot H_{\mathrm{SOR,CCM}}(s)} \tag{5}$$

where α is a feedback coefficient of the DSM. The STF of the DSM exhibits a high-order low-pass characteristic. In our design, the -3 dB frequency of $G_m(s)$ is designed to be much higher than the system bandwidth; therefore, the low-pass nature of the DSM can be neglected.

B. Duobinary Encoder

Because the intermediate state of the duobinary output ($V_{\mathrm{DUO}} = 1$) operates as a bypassing phase, which is essential for both buck and boost modes, the operating mode of this state can be determined by the mode of the previous state. Thus, a finite state machine is suitable for implementation of the duobinary encoder because it can change from one state to another in response to an external input [26]. However, the duobinary outputs directly correspond to the switching phases in the proposed converter, and the duobinary encoder can be implemented more simply with logic gates instead of the complex finite state machine. Fig. 5(a) shows the schematic of the proposed encoding circuit.

$$H_{\mathrm{SOR,CCM}}(s) = \frac{s^2 \cdot \frac{1}{C}\left(\frac{4}{R_1} + \frac{1}{R_7} - \frac{3}{R_6}\right) + s \cdot \frac{1}{C^2}\left[\frac{3}{R_1}\left(\frac{1}{R_X} + \frac{1}{R_Y}\right) - \frac{2}{R_6 R_Y}\right] + \frac{2}{C^3 R_1}\left(\frac{1}{R_X} \cdot \frac{1}{R_Y}\right)}{s \cdot \left[s^2 + \frac{2}{C^2 R_4 R_Y}\right]} \tag{4}$$

Buck switches composed of M_1 and M_2 shown in Fig. 2(a) can be driven by an AND gate because M_2 is turned ON only when $V_M = 1$ and $V_{M+1} = 1$ ($V_{\mathrm{DUO}} = 2$, discharging phase). Boost switches composed of M_3 and M_4 can be driven by a NOR gate because M_3 is turned ON only when $V_M = 0$ and $V_{M+1} = 0$ ($V_{\mathrm{DUO}} = 0$, charging phase). In addition to these operations, the detailed encoder operations are described in Fig. 5(b). The duobinary encoder requires 1.5-b V_{DUO} output, but it generates simple encoder output signals of $\mathrm{BCK}_{\mathrm{DRV}}$ and $\mathrm{BST}_{\mathrm{DRV}}$ for driving the power switches through the AND and NOR gates, thus, enabling an efficient driving circuitry design. Moreover, the dedicated operations of the NIBB converter such as soft start, over-current or voltage protection, and zero-current control are realized by adding control signals to the proposed encoder circuit.

The Laplace transform of a delay element can be described as e^{-sT} [27], where T is the time delay ($=1/f_S$). Therefore, the complete TF of the duobinary encoder in (1) is written as

$$G_d(s) = 1 + e^{-sT}. \tag{6}$$

It can be seen that the TF of the duobinary encoder exhibits a low-pass characteristic, which has a passband frequency much higher than the crossover frequency. Thus, the effect of the duobinary encoder is also negligible in the overall loop analysis.

C. Compensator

The loop compensator should be carefully designed to accomplish the regulation of the DSM-based NIBB converter. The transfer function of the converter varies with the magnitude of the load current and the operating mode, i.e., the buck and the boost modes. In particular, the RHPZ in the boost mode causes reduced phase margin. As the load current increases, the RHPZ moves to a lower frequency, and the converter becomes more difficult to control [19].

A type-III compensator [17] is used, as shown in Fig. 6(a). The compensator is composed of the on-chip components of an error amplifier with feedback network and the off-chip components of R_1, R_3, and C_2 at the input stage. The TF of the compensator is expressed in the loop analysis as follows:

$$G_C(s) = \frac{(sC_1(R_2+R_H)+1)(sC_2(R_1+R_3)+1)}{s\cdot(sC_1C_3(R_2+R_H)+(C_1+C_3))(sC_2R_1R_3+R_1)}. \tag{7}$$

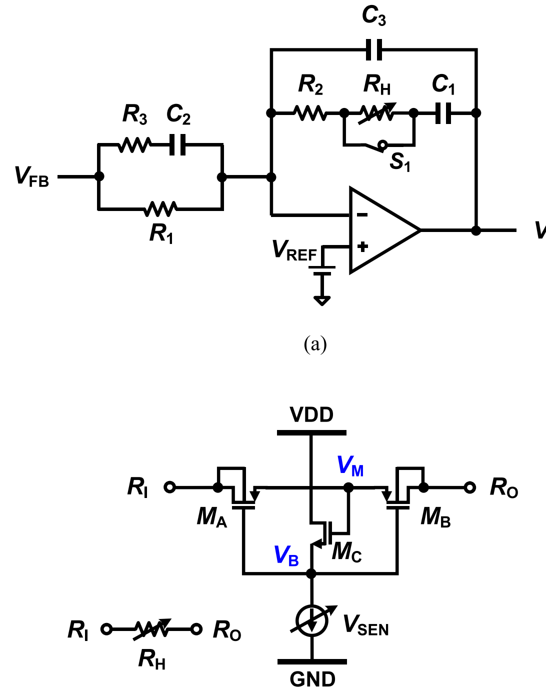


Fig. 6. Compensator. (a) Type-III compensator. (b) R_H.

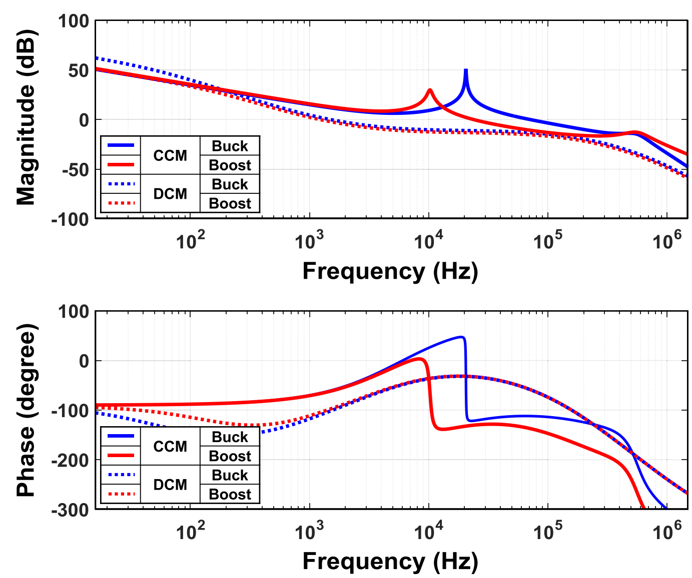


Fig. 7. Frequency responses of the compensated converter.

This compensator provides three poles and two zeros in the frequency domain. The first pole is placed at the origin and it produces high dc gain to minimize the dc regulation error. The double zeros are placed at 4.3 and 8.2 kHz around the power stage resonant frequency (f_0) to compensate the phase delay caused by the external inductor and capacitor. The second and third poles are placed at the coincidence of 1.6 and 0.6 MHz with the equivalent series resistance zero frequency and RHPZ frequencies, respectively. Although these parameters are optimized for frequency compensation in the boost mode, these can produce the appropriate compensation even in the buck mode. The influence of the DSM and duobinary encoder on the compensation loop is negligible because its poles are placed at a much higher frequency than that of the crossover frequency (f_C). Based on these criteria, Fig. 7 shows the frequency response of the compensated loop in the buck and boost modes of the CCM region. In CCM, only R_2 is considered in the series connection of R_2 and R_H. These simulations are performed under worst-case conditions, which means the buck mode occurs when $V_{\mathrm{IN}} = 5.0$ V and $V_{\mathrm{OUT}} = 2.0$ V at the CCM/DCM boundary (50 mA), and the

TABLE II
SUMMARY OF FREQUENCY RESPONSES OF THE COMPENSATED CONVERTER

Converter Operation	Mode	Switch S_1	V_{IN} (V)	V_{OUT} (V)	I_L (mA)	f_C (kHz)	PM (°)
CCM	Buck	ON	5	2	50	71	68
	Boost		2.5	5	500	24	50
DCM	Buck	OFF	5	2	5	1.5	78
	Boost		2.5	5	25	1.2	75

boost mode occurs when $V_{\mathrm{IN}} = 2.5$ V and $V_{\mathrm{OUT}} = 5.0$ V under the maximum load (500 mA). Table II summarizes the small signal loop gain responses for the DSM-based NIBB converter. The nominal f_C values for the buck and boost modes of CCM region are 71 and 24 kHz, respectively. Note that the proposed converter shows a significantly lower system bandwidth than the average switching frequency, and additional effort is needed to improve it.

In addition, when using voltage-mode control, the variation in f_C can generate problems at different operating points; therefore, the entire range of operation should be carefully checked. Especially in the DCM region, a low-frequency zero corresponding to the movable DCM pole is required. To achieve this, the control switch S_1 of the compensator is turned OFF and a large tunable resistor R_H is enabled in the DCM. The high-value resistor structure from [28] is adopted as R_H. The high resistance is provided by two small-size p-type transistors (M_A and M_B) with shorted bulk-drain terminals biased in the subthreshold regime as shown in Fig. 6(b). Moreover, R_H is tunable from 20 to 50 MΩ by controlling the bias voltage through the average inductor current value, thus, producing a scalable zero position according to the load current level. Fig. 7 additionally shows the results of the compensated converter loop in the DCM.

D. Switching Node Assisted Deadtime Controller

Fig. 8 shows the proposed switching node assisted deadtime controller for controlling the boost switches M_3 and M_4. The deadtime controller for the buck switches has been described in [15], and only the boost-mode controller is explained here. The proposed scheme is based on the fixed deadtime circuit but is designed to improve the excessive deadtime by using switching node voltage V_{LX2}.

When the boost clock ($\mathrm{BST_{DRV}}$) input signal moves from high to low, Q_{2N} follows this signal. Then, M_3 is turned OFF, and M_4 remains turned OFF from the previous state. This causes a deadtime status. During this time, the inductor current discharges the parasitic capacitor of V_{LX2}, the body diode of M_4 turns ON, and V_{LX2} is changed to a voltage above V_{OUT}. When $V_{\mathrm{LX2}} > 0$ and the enable signal remains low, the P-assist circuit is solely enabled. Thus, V_{EP} is set to high and N_4 is activated, resulting in deadtime termination by turning ON M_4 regardless of the fixed deadtime.

When the $\mathrm{BST_{DRV}}$ signal changes from low to high, Q_{2P} follows this signal. Then, M_4 is turned OFF, and M_3 remains turned OFF from the previous state. This is another deadtime status. During this time, $V_{\mathrm{LX2}} > 0$ and the enable signal remains high;

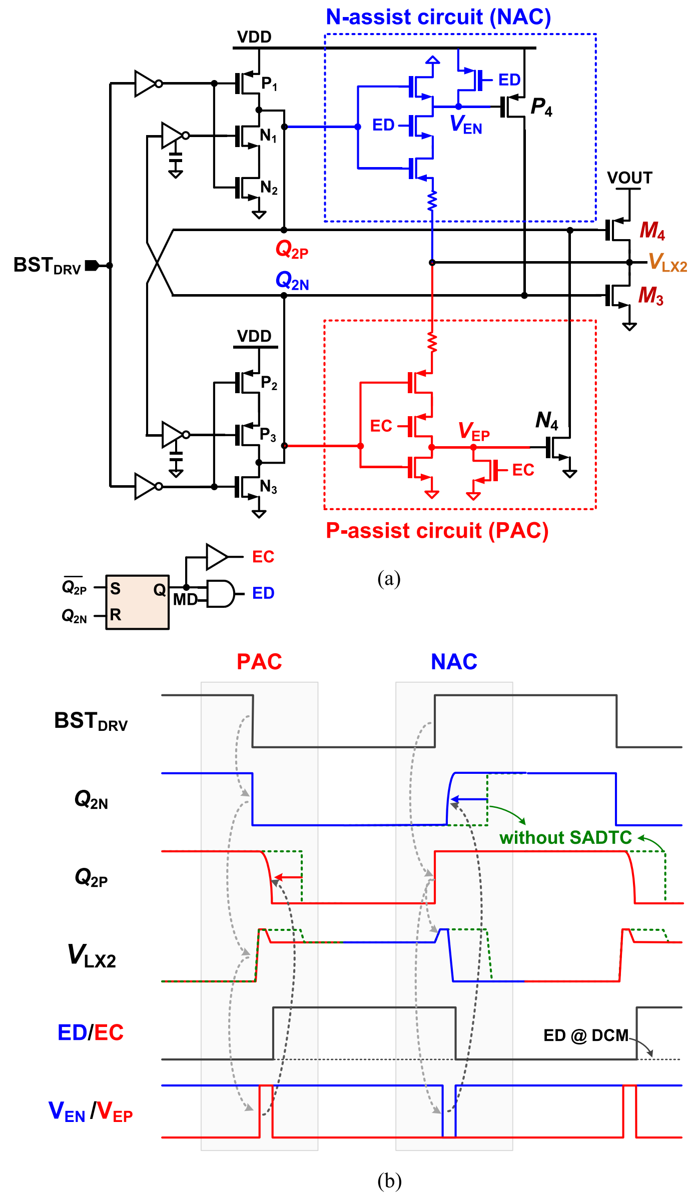


Fig. 8. Deadtime controller. (a) Schematic. (b) Timing diagram.

accordingly, the N-assist circuit (NAC) is enabled. Thus, V_{EN} is set to low and P_4 is activated, which turns on M_3. Because the falling time of V_{LX2} is very short, the turn ON operation of M_3 after M_4 is turned OFF requires only a fixed short delay. This may be accomplished by controlling the NAC design parameters. With these control schemes for the boost mode power transistors, the duration of body-diode conduction can be minimized. Fig. 9 compares the simulation results of the proposed deadtime controller with the conventional fixed deadtime control. It can be seen that the proposed approach can effectively reduce the body-diode conduction time by approximately 60%.

IV. MEASUREMENT RESULTS

The proposed DSM-based NIBB converter was implemented in a 180-nm CMOS process and the die photograph is shown in

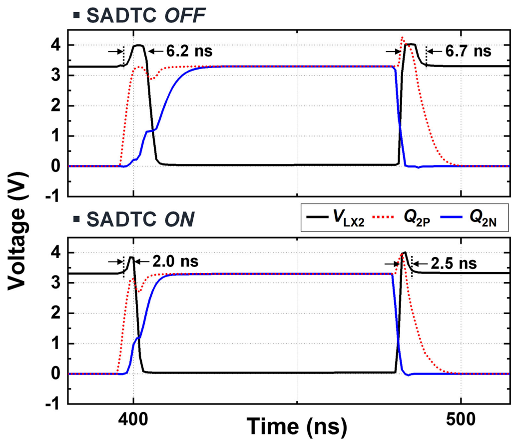


Fig. 9. Simulated transient waveforms. (a) Fixed deadtime control. (b) Proposed deadtime control.

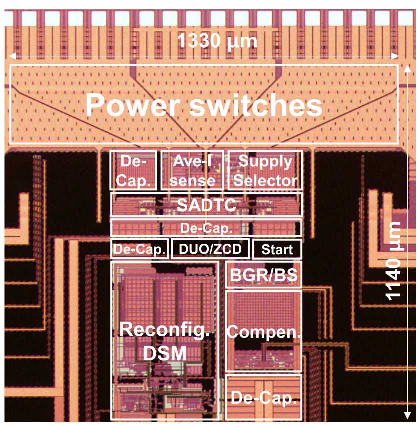


Fig. 10. Die micrograph of the proposed DSM-based NIBB converter.

Fig. 10. The chip area of the prototype was 1.33 × 1.14 mm^2. The NIBB converter regulates supply voltages of $V_{\rm IN} = 2.5$–5.0 V. The converter output is regulated to $V_{\rm OUT} = 2.0$–4.6 V and the load current range is $I_L = 1$–500 mA. The sampling frequencies of the modulator in the CCM and DCM regions are 14 and 7 MHz, respectively.

The line transient response was measured to verify the behavior based on a duobinary encoding and the feature of smooth mode transition of the proposed DSM-based NIBB converter, and the results are shown in Fig. 11. The $V_{\rm IN}$ steps are between 2.5 and 5 V, and $V_{\rm OUT}$ is maintained at 3.3 V with I_L of 1 mA; hence, the converter operates in different modes depending on $V_{\rm IN}$. When $V_{\rm IN} \gg V_{\rm OUT}$, the converter operates in the two-phase buck mode and thus, only the buck switch node $V_{\rm LX1}$ is employed. When $V_{\rm IN}$ approaches $V_{\rm OUT}$, the dominant operation, which is the $V_{\rm LX1}$ switching, is reduced, and the switching of the boost switch node $V_{\rm LX2}$ is gradually increased. The simultaneous operation of $V_{\rm LX1}$ and $V_{\rm LX2}$ indicates a three-phase operation; thus, the converter operates in the BB mode. When $V_{\rm IN} \ll V_{\rm OUT}$, the dominant switching operation is handled by $V_{\rm LX2}$; thus, the converter operates close to the boost mode.

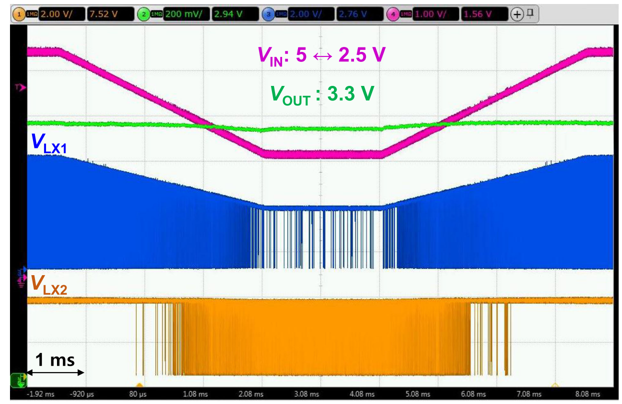
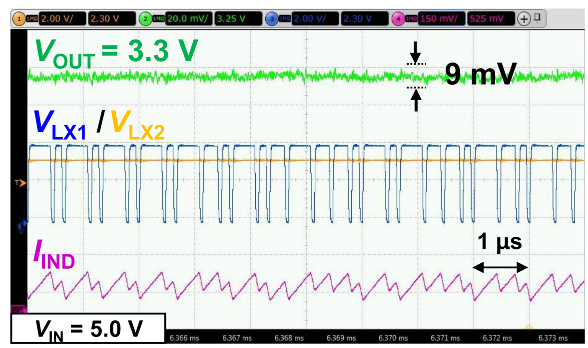
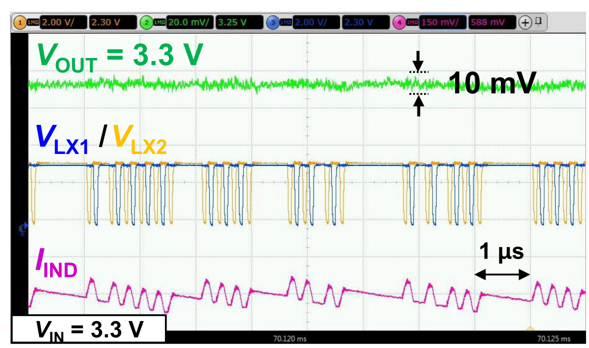


Fig. 11. Measured operation of proposed DSM-based NIBB converter.



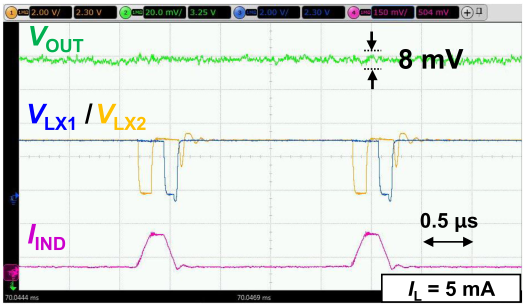
(a)



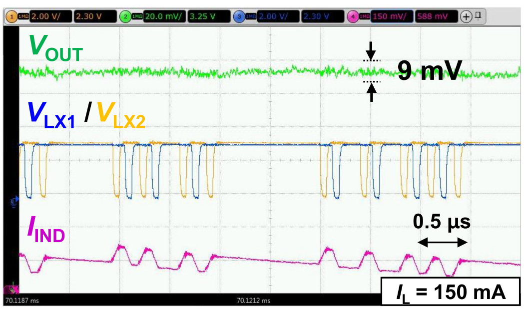
(b)

(c)

Fig. 12. Detailed operating modes. (a) Buck mode. (b) BB mode. (c) Boost mode.



(a)



(b)

(c)

Fig. 13. Transient waveform in BB mode. (a) DCM region, $I_L = 5$ mA. (b) CCM region, $I_L = 150$ mA. (c) CCM region, $I_L = 450$ mA.

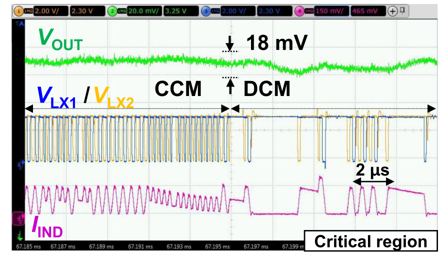
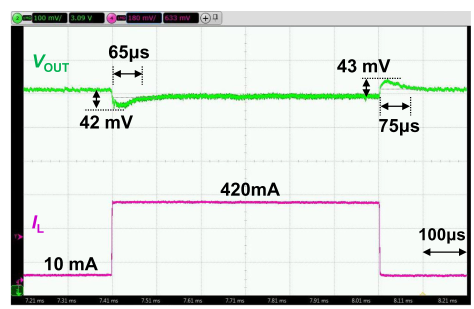
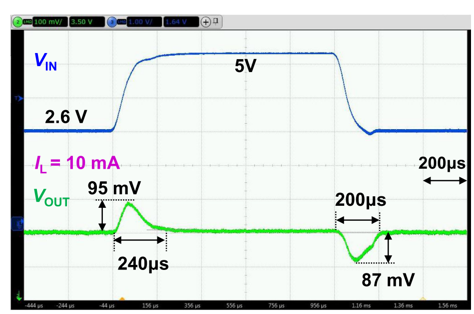


Fig. 14. Transient waveform in the DCM and CCM boundary region.

Fig. 15. Dynamic output voltage scaling.



(a)



(b)

Fig. 16. Transient responses of the converter. (a) Load regulation. (b) Line regulation.

When $V_{IN} = 2.5$ V, the converter does not operate fully in the boost mode but in a mixed mode with partial buck operation due to the nonideal effects of the converter, such as offset voltages and device mismatches. Although the mode conversion is not symmetrical and the boundary of the operating mode is not clearly distinguished, the proposed converter can produce a robust operation through the continuous and seamless output properties of the DSM. Moreover, this controller suppresses the dead zone occurrence to enable smooth mode conversion, resulting in a relatively small output voltage ripple. The highest output voltage ripples during mode transition under all operating conditions are measured to be within 18 mV.

The detailed operation of each mode with I_L of 90 mA is shown in Fig. 12. For V_{OUT} of 3.3 V, the input voltages were 5.0, 3.3, and 2.5 V in the buck, BB, and boost modes, respectively. As shown in Fig. 12(a) and (c), V_{LX1} and V_{LX2} nodes are switched solely in the buck and boost modes, respectively, because of which the inductor current I_{IND} has a sawtooth shape. On the other hand, I_{IND} has a quadrangular shape in the BB mode because V_{LX1} and V_{LX2} switch simultaneously [see Fig. 12(b)]. Fig. 12 also shows that the body-diode conduction is effectively controlled in all modes due to the proposed deadtime control. This restricts the V_{OUT} ripple to a small value.

Fig. 13 shows the transient waveforms depending on the load current I_L in the BB mode ($V_{IN} = 3.3$ V and $V_{OUT} = 3.3$ V). When $I_L = 5$ mA [see Fig. 13(a)], the converter operates in the DCM region. During this time, the reverse inductor current does not flow by the ZCD, which effectively controls the power

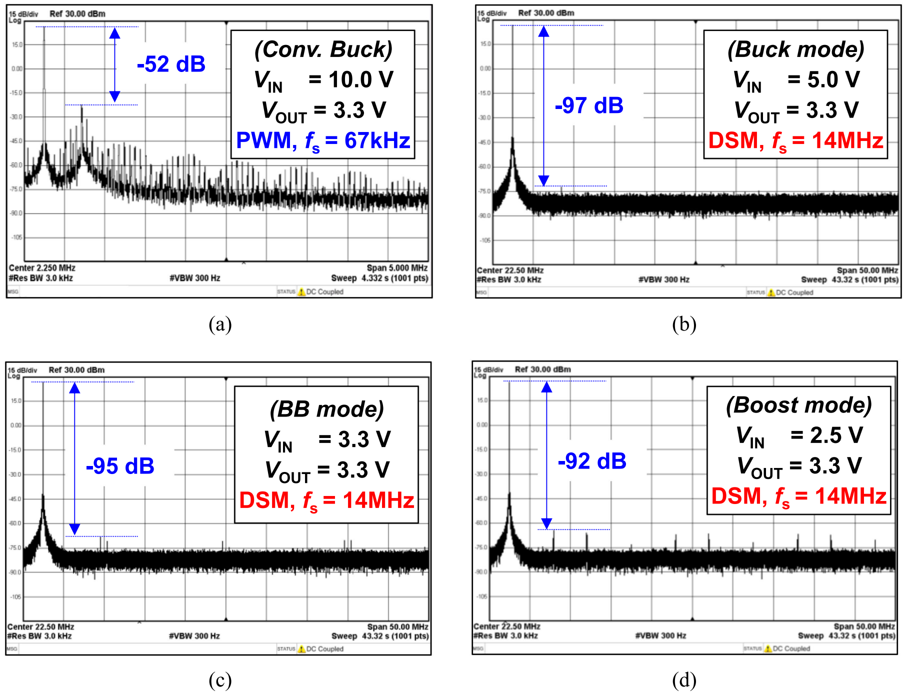


Fig. 17. Measured output spectra. (a) Traditional PWM buck converter [29]. (b) Proposed DSM-based converter in buck mode. (c) Proposed DSM-based converter in BB mode. (d) Proposed DSM-based converter in boost mode.

transistors of M_2 and M_4. When $I_L \gg 50$ mA [see Fig. 13(b) and (c)], the converter operates in the CCM region. Although the $V_{\rm OUT}$ ripple gradually worsens as the load current increases, it can be controlled within 16 mV at 450-mA load. The measured waveform of the DCM and CCM transition region is shown in Fig. 14. The converter switches from CCM to DCM when the load current is close to 50 mA. In this boundary region, the DSM order, f_S, and compensator coefficients are fully reconfigured, but stability is maintained concretely and the $V_{\rm OUT}$ ripple can be restricted within 18 mV.

As shown in Fig. 15, the proposed converter can dynamically adjust $V_{\rm OUT}$ by changing the reference voltage $V_{\rm REF}$ applied to the compensator. For $V_{\rm IN}$ of 3.3 V, $V_{\rm OUT}$ varies between 2.0 and 4.6 V. In addition, $V_{\rm IN}$ regulation may allow the converter to achieve a different range of $V_{\rm OUT}$.

Fig. 16(a) illustrates the load transient response with $V_{\rm IN} =$ 3.3 V and $V_{\rm OUT} = 3.3$ V when I_L varies between 10 and 420 mA. The transient recovery time under undershoot and overshoot conditions were 65 and 75 μs, respectively, and the corresponding voltages were less than 43 mV. The converter has a small voltage fluctuation and a fast settling time when the load current changes rapidly. Fig. 16(b) shows the line transient response with a 3.3-V output and 10-mA load. When $V_{\rm IN}$ was varied from 2.6 to 5.0 V, the overshoot and undershoot voltages were 95 and 87 mV, respectively. The output voltage could be recovered within 240 μs with changes in $V_{\rm IN}$. These results show that the proposed DSM-based NIBB converter can produce robust transient responses with good stability.

In addition to these time domain responses, the proposed converter produces high switching noise rejection characteristics in the frequency domain. Fig. 17 shows the measured output

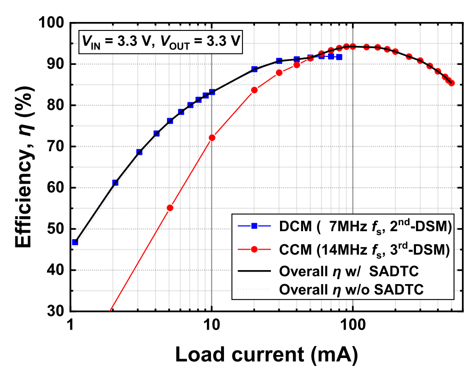


Fig. 18. Measured efficiency in BB mode.

spectra of a fixed frequency PWM voltage mode buck converter [29] and the proposed DSM-based converter under the three different modes. Compared with the traditional PWM mode converter, the first harmonic peak has been reduced by –45 dB in the buck mode. The proposed technique effectively suppresses the switching harmonics in each mode. The spurious free signal range of 97, 95, and 92 dB were achieved in the buck, BB, and boost modes, respectively. With a resolution bandwidth of 3 kHz, the noise floor was maintained below –76 dBm across all modes and frequencies. Although the boost mode exhibited slightly reduced noise rejection capability because the *LC* filter was disconnected from the load in the charging phase, the proposed DSM-based NIBB converter demonstrated dramatically reduced switching noise and harmonics.

Fig. 18 shows the measured efficiency as a function of the load current in the BB mode ($V_{\rm IN} = 3.3$ V and $V_{\rm OUT} = 3.3$ V).

TABLE III
PERFORMANCE COMPARISON TO PRIOR WORKS

Reference		This work	[10]	[6]	[11]	[9]	[5]
V_{IN} (V)		2.5~5.0	2.5~5.0	2.7~5.5	2.5~5.0	2.3~5.0	3.0~5.5
V_{OUT} (V)		2.0~4.6	3.3	2.0~5.0	3.3	3.3	3.6
Controller	f_S (MHz)	7, 14	1.66	2.5	0.5	0.5	2
	type	R-DSM w/ duobinary	Hysteretic current mode	Two sawtooth PWM	Mode select PWM	ACM w/ dual ramp	Error-avg. sense FET
L (μH)		3	1	1	18	4.7	2.2
C (μF)		20	10	10	47	22	10
Load current (mA)	min	1	10	100	50	50	600
	max	500	400	2000	330	400	1200
Efficiency, η (%)	light load η	83 @10mA	80.4 @10mA	88 @400mA	34 @50mA	76 @50mA	78 @600mA*
	peak η	94.8	98.1	91	91.6	92	90.7
Max ripple V_{OUT} (mV)		18 @500mA	20 @10mA	10 @1.9A	-	40	-
Noise floor (dBm)		–76	-	-	-	-	-
Process (nm)		180	350	180	350	350	500
Required hardware for mode transitions		DSM	Hysteresis window circuit & Hysteresis current logic	2 Saw-tooth gen. & Automatic mode selector	Dynamic ramp gen. & Mode selector	Dual ramp gen. & Mode selector	Current estimator, Mode switching & Duty cycle gen.
Mode boundary conditions		-	V_{IT}, V_{IM}, V_{IB}	$V_{bound,bst}$ $V_{bound,bck}$	V_{boost} V_{buck}	Boost ramp Buck ramp	D_{Boost} D_{Buck}
Size (mm^2)		1.51	3.86	4.13	4.75	4.11	7.50

*Extracted from graph.

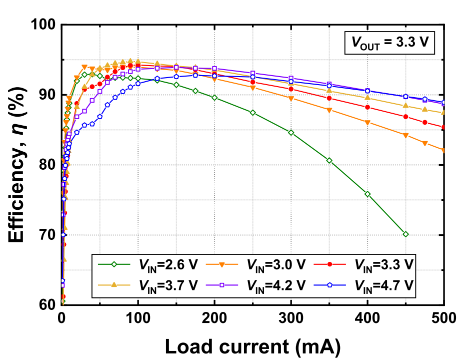


Fig. 19. Measured efficiency for different V_{IN}.

By virtue of the three-phase operation based on duobinary encoding, the proposed converter produced a peak efficiency of 94.2% in the CCM operation. The converter showed high conversion efficiency over a wide load range because of the reconfigurable operation of the DSM controller and compensator. Moreover, the proposed deadtime controller effectively reduced the conduction losses, which further enhanced the conversion efficiency by up to 1.6%.

Fig. 19 demonstrates the measured efficiency versus the load current for different values of V_{IN}. The maximum efficiency is 94.8%, which is achieved when V_{IN} is 3.7 V and I_L is 90 mA. In the CCM, the conduction loss is proportional to I_L, and the efficiency increases with decreasing I_L. In the DCM, the efficiency drops drastically because the current consumption of the control circuits is relatively high when compared with the small load current. For load current from 10 to 500 mA, the efficiency of the proposed converter was maintained at nearly 80% regardless of the operating modes. Table III summarizes the performance of the proposed NIBB converter and compares this work with prior studies. The prototype exhibited a higher conversion efficiency over a wide input and load range with a switching noise-free output by using a duobinary-encoded reconfigurable DSM. In addition, the proposed converter employed the smallest chip size when compared with previous NIBB converters.

V. CONCLUSION

A DSM-based NIBB converter with improved conversion efficiency and transient responses was presented. Implemented in a 180-nm CMOS, the proposed converter achieved a peak efficiency of 94.8%, and the efficiency was maintained at almost 80% for a 10 to 500-mA load regardless of the operating modes. Three-phase operation by duobinary encoding reduced both switching and conduction losses, thereby improving the power efficiency. The DSM controller, which continuously and automatically determines the operating mode of the converter, provided a smooth mode transition and improved the transient responses. Moreover, the spurious tones were effectively eliminated by the noise-shaped controller with a noise floor below –76 dBm, and output voltage ripples were maintained below

18 mV. The converter occupied a chip area of 1.51 mm^2, which is one of the smallest among the reported NIBB converters. The proposed duobinary-encoded NIBB dc–dc converter is expected to be a potential solution for battery-powered portable electronics.

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