

# Manitoba Rectifier—Bridgeless Buck–Boost PFC

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**Abstract**—This paper presents a new bridgeless buck–boost power factor corrector with the use of the active virtual ground technique, which is named as the Manitoba Rectifier. The proposed topology can convert the grid ac voltage into a wide range of voltage outputs within a single-stage circuit. It is in a bridgeless structure and simple in design. During the operation, an *LC* filter is generated at the system input, where continuous grid current is guaranteed in a buck–boost characteristic topology. In addition, the filter capacitor helps to clamp the voltage ripple between the grid and the output bus terminal. Both leakage current and common mode noise are kept in a relatively small value. Thus, a single-stage and low common-mode buck–boost converter system is built. The proposed topology is successfully implemented on an 800 W prototype, and the performance is experimentally verified, which shows good agreement with the theoretical findings.

**Index Terms**—AC–DC, bridgeless buck–boost, *LC* filter, power factor corrector (PFC).

## I. INTRODUCTION

IN most grid-connected power converter applications, a dual-stage system is usually adopted to support the power conversion between the ac grid and the low-voltage dc. For example, a low dc output voltage is required in a battery charger system [2]–[3]; a wide range of dc output voltages are required in brushless dc (BLDC) motor application for the speed control [4], in lighting systems for the dimming control [5] and in induction heating cooker for the loading control [6]. The implementation of a dual-stage system is simple and straight forward in the design. In a typical design, an ac–dc stage is adopted to correct the power factor and step up the input voltage to a higher level bus voltage. Meanwhile, it is followed by a dc–dc stage to step down the bus voltage to the required low output voltage. Several semiconductors are involved in the main current flowing path, therefore, the conduction loss in the system becomes critical. Also, a large number of components count are involved in a traditional dual-stage system. Hence, the system efficiency is restricted and the platform power density is also limited.

In order to simplify the dual-stage structure, some cascade solutions [7]–[11] and some single-stage solutions [4], [12]–

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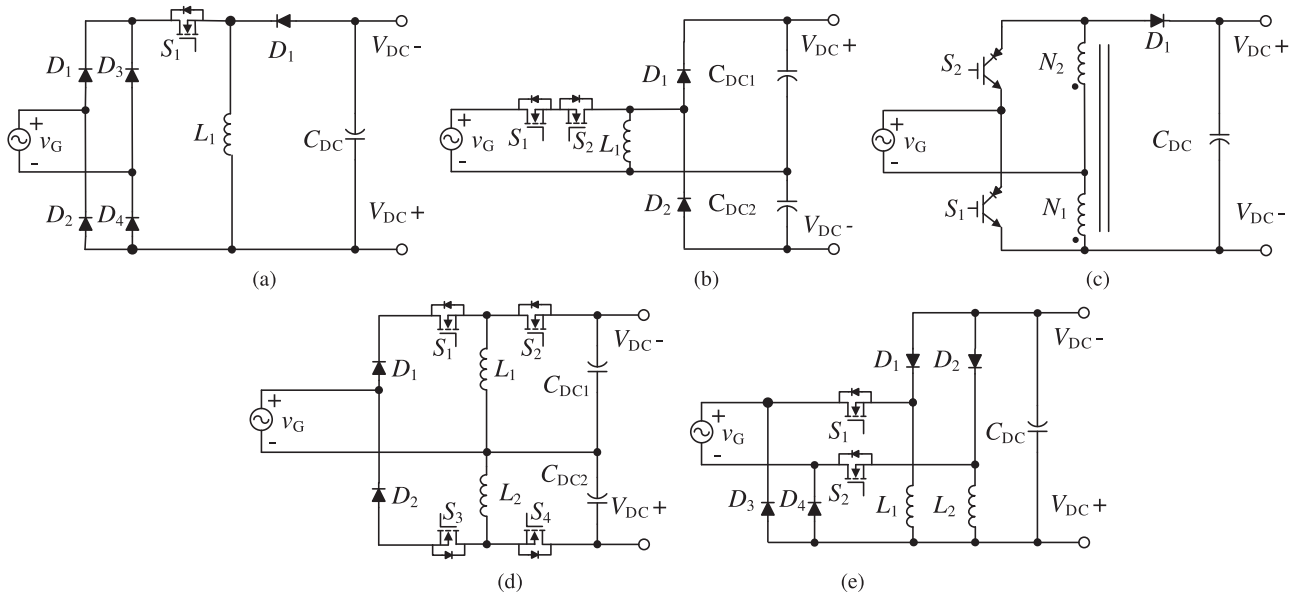


Fig. 1. Types of buck-boost PFC topology. (a) [15]. (b) [12]. (c) [13]. (d) [14]. (e) [4].

TABLE I  
SUMMARY OF NUMBER OF SEMICONDUCTOR DEVICES AND PASSIVE COMPONENTS INVOLVED IN THE TOPOLOGIES

Topology	No. of switches		No. of diodes	No. of passive components			No. of components in the main current path		Type of input filter
	LF	HF		Inductor	Dc Cap.	Filter Cap.	Turn-on	Turn-off	
Fig. 1a	0	1	5	1	1	0	3	3	No
Fig. 1b	0	2	2	1	2	0	2	1	No
Fig. 1c	0	2	1	2	1	0	1	1	No
Fig. 1d	0	2	4	2	2	0	2	1	No
Fig. 1e	0	2	4	2	1	0	2	2	No
Fig. 2 (proposed)	2	2	2	2	1	1	2	2	LC

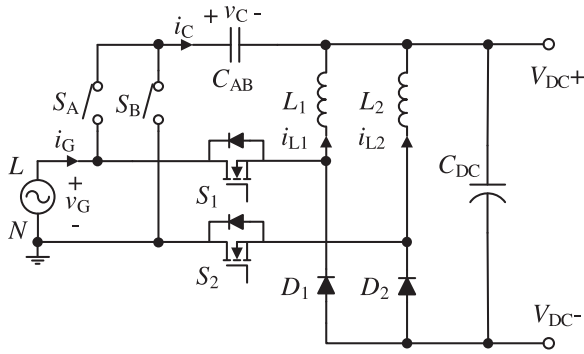


Fig. 2. Proposed bridgeless buck-boost PFC.

is generated at the system front stage. In the main current path of the proposed system, the conduction loss of semiconductors is always less than the traditional dual-stage system. Only two semiconductors are conducting during the inductor charging period, and only one semiconductor is involved for the power transfer during the inductor discharging period. Therefore, the system loss in the conduction path is minimized. The design of

the reconfigurable  $LC$  filter is based on the recently proposed active virtual ground concept, [17], [18]. In each half line cycle operation, an  $LC$  filter is generated at the input to solve the discontinuous current problem that appeared at the grid inductor. Meanwhile, the common mode (CM) noise of the system is reduced due to the filter capacitor clamping the voltage between the grid and the bus terminals. As a result, low system noise and high system efficiency are guaranteed by the proposed topology. Both system operation principles and steady-state characteristics of the proposed topology are described in detail in this paper. Also, an 800 W prototype is successfully implemented to verify the performance of the proposed topology. All the experimental results show good agreement with the theoretical knowledge.

## II. PRINCIPLE OF OPERATION

The bridgeless buck-boost circuit is formed by two identical switching cells together with two bidirectional switches ( $S_A$  and  $S_B$ ) and one filter capacitor ( $C_{AB}$ ). The bidirectional switches are synchronized with the input line frequency (LF) to form a reconfigurable  $LC$  filter at the PFC input. They can be realized by connecting two MOSFETs back-to-back in series or other configurations, which is shown in Fig. 3. The circuit structures

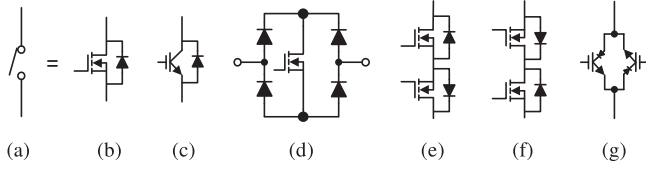


Fig. 3. Bidirectional switch arrangements. (a) Ideal switch. (b) MOSFET. (c) IGBT. (d) Diode bridge. (e) Common emitter back-to-back. (f) Common drain back-to-back. (g) Anti-parallel reverse blocking IGBTs.

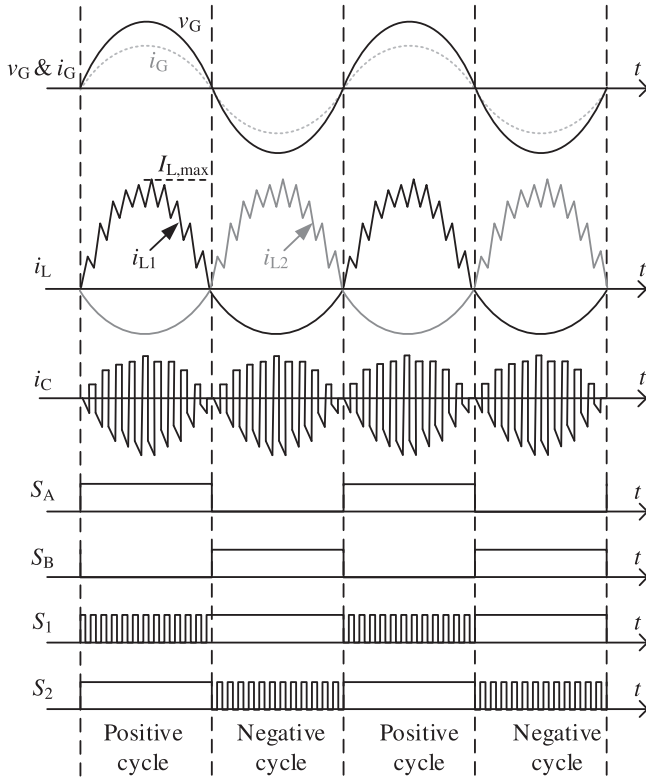


Fig. 4. Switching pattern of the proposed topology.

of the proposed rectifier in the positive and negative half line cycles are different where the corresponding switching pattern is shown in Fig. 4. Accordingly, a reconfigurable  $LC$  filter is always generated at the system input. It helps to filter out the discontinuous current of the buck–boost converter so that the current ripple in the grid side is reduced and the size of additional input filter is reduced. In addition, due to the capacitor clamps, the potential difference between the ac power source and the dc bus terminal, CM noise voltage on between is able to be minimized and the leakage current generated from the PFC circuit can also be reduced. Based on the system noise reduction, the overall noise filter can be maintained in a small size and can be further optimized on the system performance.

#### A. States of System Operation

The switching states of the proposed topology in the positive half cycle are shown in Fig. 5(a), and the corresponding buck–boost equivalent circuits are shown in Fig. 6(a). During

the positive half line cycle, switch  $S_2$  is continuously ON to provide a current return path to the circuit. Switch  $S_1$  is with high frequency (HF) ON–OFF as a converter switch and forms a switching cell together with diode  $D_1$ . Inductor  $L_1$  becomes a converter-side inductor to support the energy conversion in the buck–boost operation. During the turn-ON state, two semiconductors are conducting in the main current path to charge up  $L_1$ . During the turn-OFF state, only one semiconductor is conducting in the power transformation. The corresponding current waveform is shown in Fig. 4.

During the positive half line cycle, switch  $S_A$  is always ON and builds up the connection between  $C_{AB}$  and line terminal ( $L$ ) of the grid. Together with  $L_1$ , an  $LC$  filter is configured at the input.  $L_2$  becomes the grid-side inductor in this half line cycle. Benefiting from the filter capacitor, the HF switching current is looping inside the converter through  $C_{AB}$ , as shown in Fig. 6(a). The input  $LC$  filter helps to filter the discontinuous current generated from the buck–boost circuit. Thus, the grid current maintains in a continuous sinusoidal waveform and only a relatively small ripple appears on top of it. In addition,  $C_{AB}$  is coupling the voltage between line and positive bus terminal. Only a small voltage ripple appears in  $C_{AB}$ , therefore, the CM noise that appears between the grid and the dc bus terminal will be smaller, and the induced leakage current can be minimized to a small value.

The switching states of the proposed topology in the negative half cycle are shown in Fig. 5(b), and the corresponding buck–boost equivalent circuits are shown in Fig. 6(b). During the negative half line cycle, switch  $S_1$  is continuously ON to provide a current return path to the circuit.  $S_2$  is with HF ON–OFF as the converter switch and forms a switching cell with diode  $D_2$ .  $L_2$  acts as a converter-side inductor to support the energy conversion in the buck–boost operation. During the turn-ON state, two semiconductors are conducting in the main current path to charge up  $L_2$ . During the turn-OFF state, only one semiconductor is conducting in the power transformation path.

As switch  $S_B$  is always ON in the negative half line cycle, it helps to build up the connection between  $C_{AB}$  and neutral terminal ( $N$ ) of the grid. Together with  $L_1$ , another  $LC$  filter is configured at the input.  $L_1$  becomes a grid-side inductor in this half line cycle. Benefiting from the filter capacitor, the HF switching current is looping inside the converter through  $C_{AB}$ , as shown in Fig. 6(b), the HF switching current is looping inside the converter through  $C_{AB}$ . Also, the input  $LC$  filter helps to filter the discontinuous current generated from the buck–boost circuit. Thus, the grid current can maintain in a continuous sinusoidal waveform and only with a relatively small ripple appears on top of it. In addition,  $C_{AB}$  is coupling the voltage between the neutral and positive bus terminal. Only small voltage ripple appears in  $C_{AB}$ , therefore, low CM noise and small leakage current result from the system.

#### B. Control Scheme

The control diagram of the proposed topology is shown in Fig. 7. In the control architecture, a proportional integral (PI) controller is implemented in the outer loop to regulate the recti-

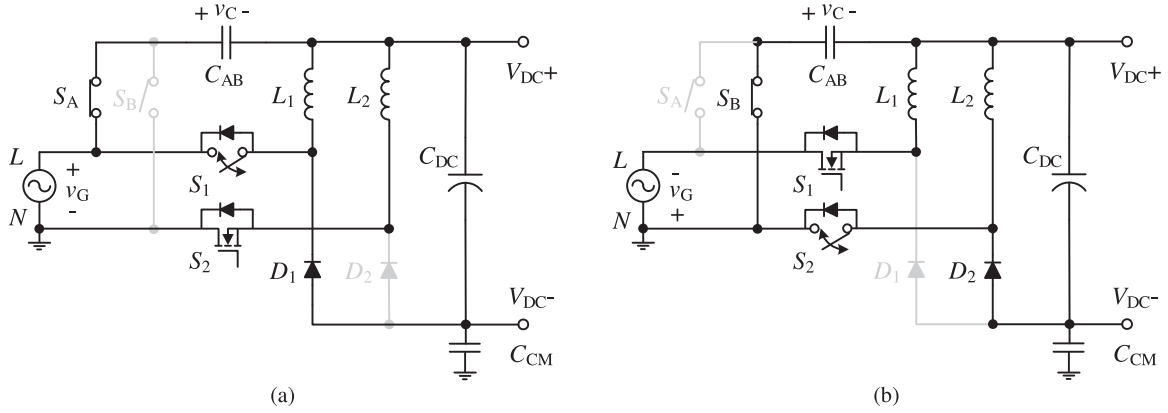


Fig. 5. Switching action in (a) positive and (b) negative half line cycles.

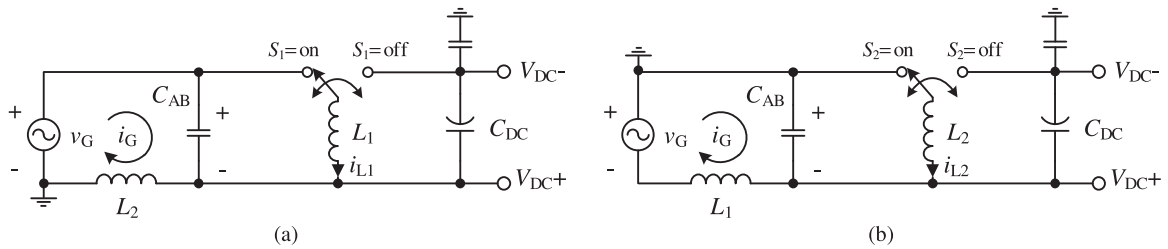


Fig. 6. Equivalent circuit in (a) positive and (b) negative half line cycles.

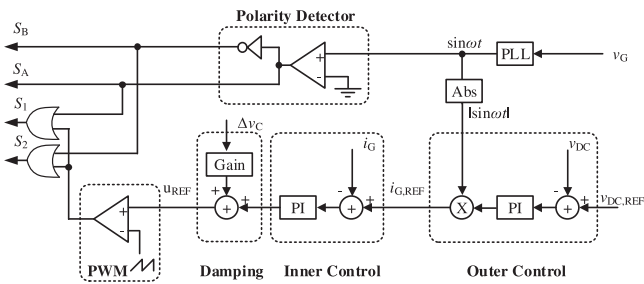


Fig. 7. Control diagram of the proposed topology.

fier output voltage  $v_{DC}$  and to limit the voltage fluctuation during any possible transient situations. Output of the outer loop is a grid current reference  $i_{G,REF}$ . The inner loop is a grid current control loop, which is implemented by another PI controller to maximize the system power factor by tracking the grid current  $i_G$  in sinusoidal. Output of the inner loop is a duty reference  $u_{REF}$ , which is used to generate the PWM switching signals of the rectifier. An active damping circuit [19] is implemented into the controller with the use of HF capacitor ripple  $\Delta v_C$ . It can help to stabilize the circuit operation and to damp any possible resonant harmonic current in the grid. By combining with the polarity signal, the switching signal of  $S_1$  and  $S_2$  are obtained.

As shown in Fig. 4, switching signals of  $S_A$  and  $S_B$  are controlled by the polar of the grid voltage  $v_G$ . Under the polarity detector,  $S_A$  stays ON at the positive half line cycle and  $S_B$  is ON at the negative half line cycle. Under unipolar switching method, only either one of the main switches,  $S_1$  or  $S_2$ , is operated at HF

ON-OFF in each half line cycle.  $S_1$  is under HF switching during the positive half line cycle and keeps ON during the negative half line cycle. On contract,  $S_2$  is kept as HF switching during the negative half line cycle and is kept ON at the positive half line cycle.

### III. STEADY-STATE CHARACTERISTICS

According to the operation diagram in Fig. 6, system steady-state characteristics are able to be found. Due to the symmetrical structure of the proposed topology, only the positive half line cycle is taken for the following analysis. In the design, the inductances of  $L_1$  and  $L_2$  are identical and with the same values. Thus, an equivalent inductance  $L_X$  is used to represent all the inductances in the proposed circuit, i.e.,  $L_X = L_1 = L_2$ .

#### A. Duty Cycle

In the positive half line cycle,  $L_1$  acts a converter-side inductor and  $L_2$  acts a grid-side inductor. With the use of the reconfigurable  $LC$  filter, all the time the filter capacitor voltage is always a positive sign. By neglecting the small voltage drop on the grid-side inductor, the capacitor voltage  $v_C$  is close to the rectified grid voltage,  $|v_G|$ , as

$$v_C(t) \approx |v_G(t)| = V_G |\sin \omega t| \quad (1)$$

where  $V_G$  is the peak amplitude of grid voltage, and  $\omega$  is the angular LF.

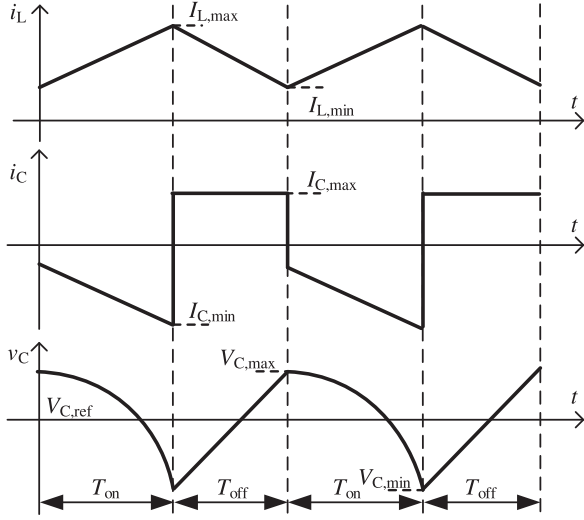


Fig. 8. Switching waveforms of filter capacitor.

Same as a general buck–boost converter, duty cycle of the proposed rectifier  $D$ , is expressed as

$$D(t) = \frac{V_{DC}}{V_{DC} + V_G |\sin\omega t|} \quad (2)$$

where  $V_{DC}$  is the dc value of the system output voltage.

All the time, the duty cycle is time varying and is following the change of grid voltage as shown in (2).

### B. Converter-Side Inductor Fundamental Current and HF Current Ripple

In a buck–boost circuit, the converter-side inductor current is all the time larger than or equal to the grid-side inductor current. As a large amount of energy is required to support the buck–boost operation. The fundamental current value of converter-side inductor  $i_L$  is dependent on the input current value and the duty cycle information, where  $i_L$  is expressed as

$$i_L(t) = \frac{2 \cdot P_O \cdot \sin\omega t \cdot (V_{DC} + V_G |\sin\omega t|)}{V_G \cdot V_{DC}} \quad (3)$$

where  $P_O$  is the output power.

The ripple current on the converter-side inductor is related to the energy conversion process. Under fixed frequency switching and continuous-conduction mode (CCM) operation, the converter-side inductor current ripple  $\Delta i_L$  is developed from the ON-state characteristic as

$$\Delta i_L(t) = \frac{V_{DC} \cdot V_G |\sin\omega t|}{(V_{DC} + V_G |\sin\omega t|) \cdot L_X \cdot f_{SW}} \quad (4)$$

where  $f_{SW}$  is the switching frequency.

A detailed derivation of (3) and (4) are given in the appendix.

### C. Filter Capacitor HF Voltage Ripple

As shown in Fig. 8, a discontinuous current is appeared on the filter capacitor, which is generated from the buck–boost circuit operation. An  $LC$  filter is always configured at the grid side,

thus, the converter-side HF current is expected to be filtered out and circulates in the converter side through the  $C_{AB}$ . The HF current results a voltage ripple in the filter capacitor  $\Delta v_C$ , which is calculated as

$$\Delta v_C(t) = \frac{2 \cdot P_O \cdot |\sin\omega t|^2}{(V_{DC} + V_G |\sin\omega t|) \cdot C_{AB} \cdot f_{SW}}. \quad (5)$$

A detailed derivation of (5) is given in the appendix.

### D. Grid-Side Inductor HF Current Ripple

Due to the  $LC$  filter characteristic, the grid-side inductor current ripple is much smaller than the converter-side current ripple. From the circuit characteristic, the grid current ripple is mainly contributed from the capacitor voltage ripple. Under CCM operation, continuous current is present in the grid. The voltage ripple appeared in the filter capacitor is the same as the HF voltage ripple that appeared in the grid-side inductor. To simplify the calculation, a small approximation is taken. The inductor voltage ripple is approximating to the triangle waveform, therefore, the grid current ripple  $\Delta i_G$  is formed as

$$\Delta i_G(t) \approx \frac{P_O \cdot |\sin\omega t|^2}{4 \cdot (V_{DC} + V_G |\sin\omega t|) \cdot L_X \cdot C_{AB} \cdot f_{SW}^2}. \quad (6)$$

A detailed derivation of (6) is given in the appendix.

### E. Output Capacitor Voltage Ripple

Output capacitor is used to hold the dc-link output voltage and to filter the HF current in the output. In the proposed topology, power decoupling function, [20], [21], is not included. Thus, in a single-stage rectifier design, a double LF voltage ripple is always been found at the rectifier output. The magnitude of the output voltage ripple is dependent on the size of the capacitor and the rated power of the system. The double LF voltage ripple of the output capacitor  $\Delta V_{DC}$  is calculated as

$$\Delta V_{DC} = \frac{P_O}{\omega \cdot C_{DC} \cdot V_{DC}}. \quad (7)$$

A detailed derivation of (7) is given in the appendix.

From (7), it shows that when power increases, the output ripple is increased. In order to maintain the capacitor ripple voltage into a small value, generally, a larger scale dc-link capacitor is needed for an application with a higher power rating.

### F. HF CM Noise Voltage Between AC Grid and DC Bus

As shown in Figs. 5 and 6, a parasitic capacitor  $C_{CM}$  is used to represent the coupling between the grid and the dc bus terminal. In the positive cycle, the coupling voltage is equal to the sum of the output voltage, filter capacitor voltage, and the negative input voltage. In the negative cycle, the coupling voltage is equal to the sum of the output voltage and filter capacitor voltage. In the HF analysis, the input voltage source and the dc output capacitor are always equivalent to short circuit. Thus,  $C_{CM}$  is virtually parallel to the filter capacitor in the Manitoba Rectifier circuit and has the same HF voltage ripple as the filter capacitor ripple. By modifying (5), the HF CM voltage ripple  $\Delta v_{CM}$  is

obtained

$$\Delta v_{CM}(t) = \frac{2 \cdot P_O \cdot |\sin\omega t|^2}{(V_{DC} + V_G |\sin\omega t|) \cdot (C_{AB} + C_{CM}) \cdot f_{SW}}. \quad (8)$$

### G. HF Leakage Current Between AC Grid and DC Bus

In the system design, the HF current is circulating inside the rectifier through the filter capacitor. Thus, the magnitude of the filter capacitor ripple current is close to or equal to the maximum inductor current during each switching period. An HF switching current is inducted in the coupling path and causes leakage current generated the system. Accordingly, the HF leakage current in the coupling path  $\Delta i_{CM}(t)$  can be found as

$$\Delta i_{CM}(t) = \frac{C_{CM}}{C_{AB} + C_{CM}} \cdot \left( i_L(t) + \frac{\Delta i_L(t)}{2} \right). \quad (9)$$

By combining (3) and (4) into (9), the expression of the HF leakage current is rearranged to

$$\begin{aligned} \Delta i_{CM}(t) &= \frac{C_{CM}}{(C_{AB} + C_{CM})} \cdot \left( \frac{2 \cdot P_O \cdot \sin\omega t \cdot (V_{DC} + V_G |\sin\omega t|)}{V_G \cdot V_{DC}} \right. \\ &\quad \left. + \frac{V_{DC} \cdot V_G |\sin\omega t|}{2 \cdot (V_{DC} + V_G |\sin\omega t|) \cdot L_X \cdot f_{SW}} \right). \end{aligned} \quad (10)$$

According to (10), the magnitude of the leakage current is directly proportional to maximum converter-side inductor current and the capacitance ratio between  $C_{CM}$  and  $C_{AB}$ . It means the leakage current can be adjusted by turning the value of  $C_{AB}$ . The positive sign magnitude of  $i_{CM}$  is following to inversed duty cycle  $\delta$ , which is calculated as

$$\delta = \frac{V_G |\sin\omega t|}{V_{DC} + V_G |\sin\omega t|}. \quad (11)$$

## IV. DESIGN AND IMPLEMENTATION

### A. Options in Implementation

The proposed circuit can have two types of circuit structure, which are the positive cell and negative cell structures. The positive cell structure is shown in Fig. 9(a), which is the same as Fig. 2. The negative bus voltage is connected to the anodes of each diode and the positive bus voltage is connected to those inductors. The negative cell structure is shown in Fig. 9(b). Both switch and diode positions are in opposite directions when comparing to the positive cell structure. The polarity of the output voltage is also revised. The negative bus terminal is connected to both inductors and the positive bus terminal is connected to the cathodes of each diode. Switching signals of all the switches are exchanged, but the same switching pattern is kept as shown in Fig. 4. There is no change in the system performance.

There are two types of reconfigurable filter circuit, which are shown in Fig. 10. Based on the design requirements and application needs, different filter structures are selected and different connection methods are considered. In Fig. 10(a), a single capacitor circuit is demonstrated, which is the one that appears in Fig. 2. In Fig. 10(b), a spitted capacitor circuit is demonstrated,

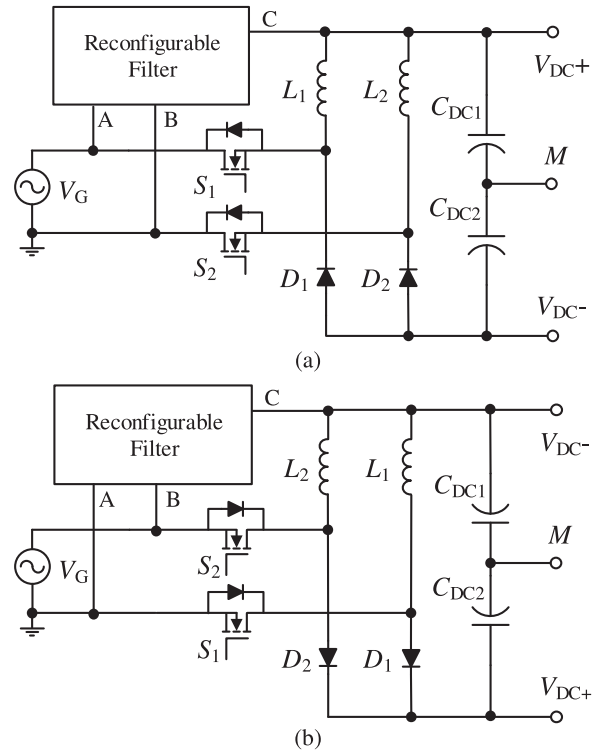


Fig. 9. Implementation of the proposed topology with the use of (a) positive cell and (b) negative cell structures.

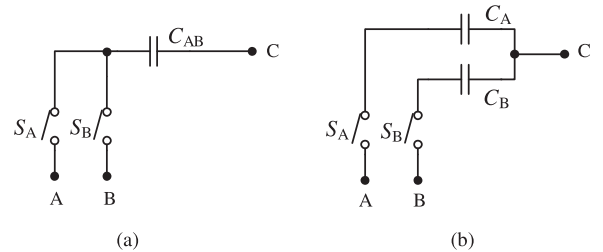


Fig. 10. Implementation of the reconfigurable filter circuit. (a) Single capacitor. (b) Spitted capacitor methods.

which is used to avoid any short-circuit possibility at the input. Each branch is formed by a separated filter capacitor and one bidirectional switch. Each of them handles half line cycle. Even a failed signal appears in both switch  $S_A$  and  $S_B$  at the same time, there would not have any short circuit happened. The corresponding operation diagrams and the equivalent circuits of the spitted capacitor method are the same as Figs. 4 and 6, respectively. Meanwhile, at the voltage zero crossing point, a relatively small dead time can be set. Thus, the power quality of the system can be further improved.

Also variants of connection method are offered. The terminal C of the reconfigurable filtering circuit is possible to connect either the positive bus terminal, negative bus terminal, or the middle point of the dc-link capacitor M. The advantage of middle point connection is when a large surge current appears in the input, the output capacitor can help to handle the large current

TABLE II  
VALUE OF THE SYSTEM CONDITION USED IN THE DESIGN

Parameter	Value	Parameter	Value
$V_{AC}$	120–220 Vac	$V_{DC}$	50–200 Vdc
Input Frequency	60 Hz	$P_O$	800W
$f_{sw}$	50 kHz	$I_{L,MAX}$	25A

flow. The drawback is that there is a dc voltage offset in the filter capacitor, therefore, a higher voltage margin is required in the filter capacitor.

### B. Selection of Filter Components

For the Manitoba Rectifier prototype, the maximum power is set to 800 W and with a wide input and output voltage ranges. The target system specification is shown in Table II. Universal input voltage is considered, which covers from 120 to 220 Vac. The output voltage range is dependent on the application needs. The maximum output voltage is related to the device breakdown voltage and the minimum output voltage is related to the maximum available inductor current. In the design, the output voltage range is set to 50 to 200 V<sub>dc</sub>. Meanwhile, the specified inductance current ripple is set to 15%. Based on (4) and all the testing conditions, the minimum required inductance is calculated as 0.7 mH. Finally, 0.78 mH is designed for both of the inductor  $L_1$  and  $L_2$ . They are implemented by two 77.8-mm high flux cores, 58 907, and are routed with 76 turns on top. The selection of  $C_{AB}$  is based on the following two criteria:

- 1) Maximum resonance frequency, to avoid the interaction between the LC filter resonance frequency and the switching frequency, there should be a big ratio different on between, such as ten-times different. The relationship is expressed as

$$C_{AB} \geq \frac{1}{L_X} \left( \frac{10}{2\pi f_{sw}} \right)^2. \quad (12)$$

Based on the specification in Table II, the minimum capacitance value is calculated 1.3  $\mu$ F.

- 2) Maximum leakage current  $\Delta I_{CM,MAX}$ , BLDC is taken as an example, the leakage current amplitudes are limited to 3.5 A and 3.5 mA, as shown in [20] and [23], respectively. Refer to [24] and [25], 0.47 nF is selected as a reference of the system  $C_{CM}$  value to fulfill the requirement of 3.5 mA leakage current. From (8), the equation related to the maximum leakage current can be rearranged as

$$C_{AB} \geq C_{CM} \cdot \left( \frac{I_{L,MAX}}{\delta \cdot \Delta I_{CM,MAX}} - 1 \right). \quad (13)$$

Based on the specification in Table II, the minimum capacitance value is calculated as 1.97  $\mu$ F. Finally, a 3.3  $\mu$ F capacitor is selected for  $C_{AB}$  of the designed prototype.

The value selection of  $C_{DC}$  is based on the following two criteria:

- 1) Hold-up time  $t_{hold}$  is used to ensure that the design circuit can maintain function properly when the input power is

TABLE III  
LIST OF SEMICONDUCTORS

Device	Type	Part Number	Voltage Stress
Switches $S_A$ and $S_B$	Si MOSFET	IPW60R070C6	$V_G$
Switches $S_1$ and $S_2$	Si MOSFET	IPW60R080P7	$V_G + V_{DC}$
Diodes $D_1$ and $D_2$	SiC Diode	GP2D020A060B	$V_G + V_{DC}$

suddenly stopped for a short period of time. The corresponding equation is expressed as follows:

$$C_{DC} \geq \frac{2P_O \cdot t_{hold}}{V_{DC}^2 - V_{DC,MIN}^2}. \quad (14)$$

If 5 ms is required for the hold-up time, and the minimum output voltage  $V_{DC,MIN}$  is set to 60% of the maximum rated output. The minimum output capacitance is calculated as 0.87 mF.

- 2) Output voltage ripple  $\Delta V_{DC}$ , the maximum output ripple is set to 20 V of the target design. Based on (4) and all the targeted testing conditions, the minimum output capacitance is calculated as 0.88 mF.

Finally, a 0.94-mF capacitor is selected for  $C_{DC}$  in the prototype design.

### C. Selection of Semiconductors

Semiconductors are required in the system to form the switching cells and to generate the reconfigurable LC input filter.  $S_1$  and  $S_2$  are the main switches of the circuit, which handle the charging period of the buck–boost operation. They act as the converter switches and operate under HF switching.  $D_1$  and  $D_2$  are the converter diodes, which handle the discharging period of the buck–boost operation. The voltage stress that appears in the switching cell is equal to the sum of the input voltage and the output voltage. According to the voltage specifications shown in Table II, 600 V devices are required. Based on HF and high voltage requirement, Si MOSFETs are selected for the converter switches and SiC diodes are selected for the converter diodes.  $S_A$  and  $S_B$  are the LF bidirectional switches, which are used to configure different structural input LC filters during each half line cycle. Only HF ripple current passes through the LF switches and the voltage stress on top is from the grid only. Therefore, low ON-state resistance MOSFETs are selected and are connected in a back-to-back configuration to support the required bidirectional blocking function. The selected semiconductors are summarized in Table III.

A loss breakdown of light load (200 W) and full load (800 W) under 120 Vac–120 V<sub>dc</sub> test conditions are given in Fig. 11(a) and (b), respectively [26], [27]. It can be seen that the highest converter loss is coming from the converter-side inductor where the HF current ripple induces the core loss, and the high-level buck–boost inductor current induces the conduction loss. The lowest converter loss appears on the grid-side inductor, where the core loss of itself is close to zero and only LF current conduction loss is left. In the switching cells, the major losses appear on top are switching loss and conduction loss. For the LF switches,

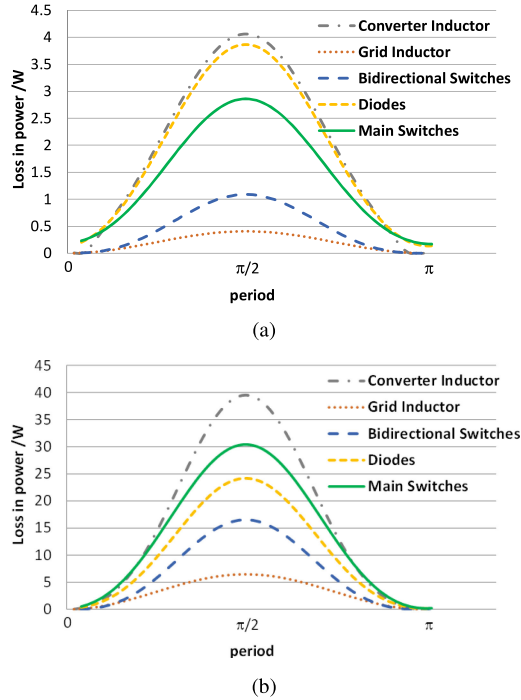


Fig. 11. Loss breakdown at  $120 V_{ac}$ - $120 V_{dc}$  with (a) 200-W power delivery and (b) 800 W power delivery.

all the time the conduction loss is on top. Also, they are only carrying the HF ripple, thus, the loss is far lower than the main switches. In the light load condition, the current value is low, therefore, the conduction loss generated from those devices is less and is close to or less than the HF switching loss portion. In the full-load condition, the conduction loss generated from those devices become more obvious as the current level is increased. The system conduction loss portion dominates the overall system loss. Based on the system loss estimation, a corresponding system efficiency figure is generated and is shown in Fig. 12(a). Significantly, in the middle to full-load range, when the output voltage is lower, the system efficiency is lower. It is because the converter-side inductor current is higher when the output voltage is dropped. In the light load condition, the change of system efficiency depends on the balance between the switching loss and conduction loss.

For efficiency evaluation, a two-stage solution is used as a reference for comparison, which is the combination of a traditional boost-type converter and a buck-type converter. The corresponding system efficiency is estimated and is shown in Fig. 12(a). The applied system parameters and the type of the considered devices are the same as the proposed topology. In  $200 V_{dc}$  test case, the proposed method is always more efficient than the two-stage system. In 50 and  $120 V_{dc}$  test cases, in most of the power ranges, the proposed topology obtains a better performance than the two-stage system. Only when the power is larger than 80% of the loading, the two-stage system has its benefits. In the low output voltage but with high-power rating situation, the inductor current produced in the buck-boost type rectifier is relatively higher than the current in the two-stage

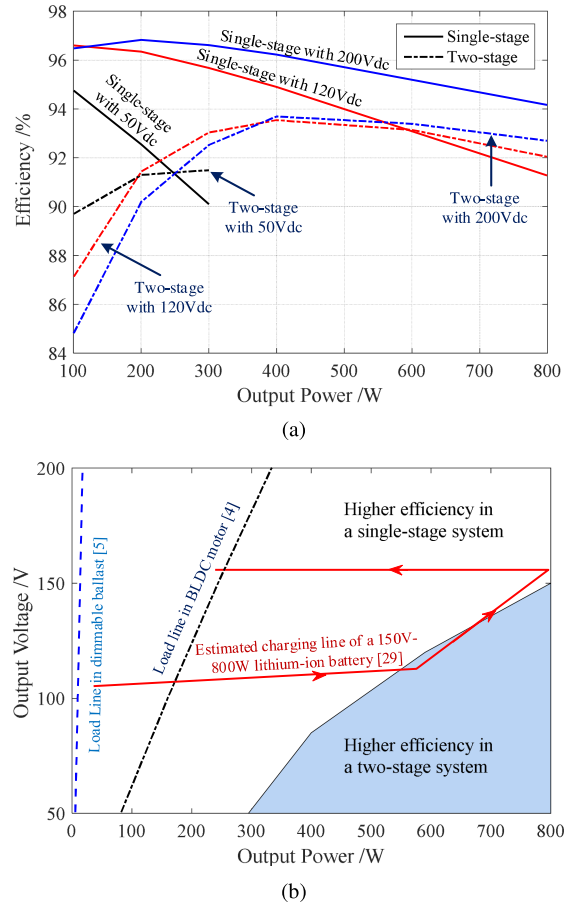


Fig. 12. System estimation with (a) efficiency prediction different power rating and (b) performance tradeoff between the proposed rectifier and a two-stage system.

system. Thus, the benefit of a single-stage buck-boost rectifier will be reduced accordingly. The performance tradeoff between the proposed rectifier and the two-stage system is shown in Fig. 12(b). However, in those systems that require a variable dc voltage, the output voltages are usually proportional to the output power, such as in BLDC motor system [4] and lighting dimming system [5]. Also, in the battery charging system, [2] and [28], similar behavior can be found in a constant current charging period of a lithium-ion battery pack [29]. Thus, the design of a single-stage buck-boost type rectifier can have the biggest advantage on it. Meanwhile, there is a method to enhance the benefits of the proposed rectifier at higher power rating, which is to choose a lower ON-state resistance device. However, the tradeoff is that the light load efficiency will be reduced.

## V. EXPERIMENTAL VERIFICATIONS

An 800 W Manitoba Rectifier prototype is implemented, which is based on the design guideline that is provided in Section IV. In Fig. 13(a), it demonstrates the operating principle of the LF switches. By switching  $S_A$  and  $S_B$  alternatively, an LC filter was always formed in the front stage, and the filter capacitor voltage was maintained close to the rectified grid

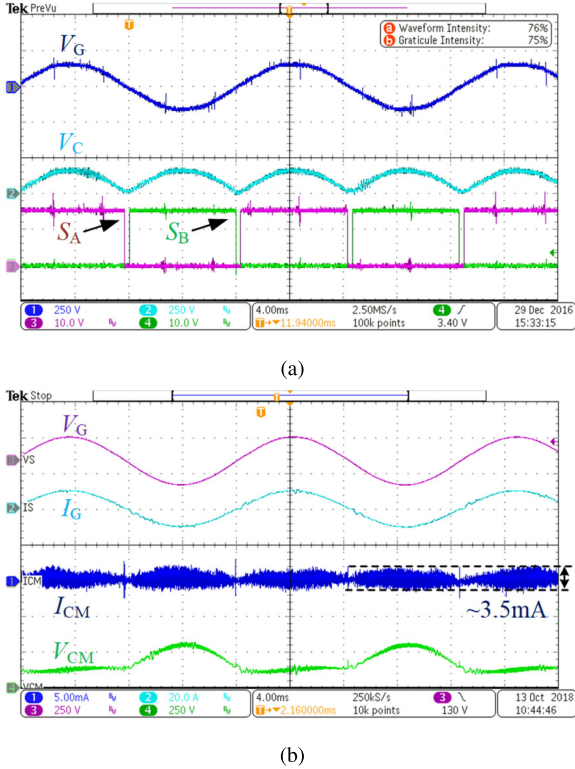


Fig. 13. Experimental waveform at  $120 V_{ac}$ – $120 V_{dc}$ –800 W. (a) Filter capacitor waveform. (b) Parasitic capacitor waveform.

voltage. The filter capacitor helped to maintain the ripple voltage between the grid and the bus terminal into a small value. Thus, low CM voltage and low leakage current were expected. In Fig. 13(b), a 470-pF capacitor is added into the system to simulate the effect of the parasitic capacitor. The voltage between the neutral of the grid and the negative bus voltage was measured and used to represent the CM noise voltage of the system. The current that flowed through the capacitor was used to represent the leakage current. The result proved that the HF noise voltage was in a relatively small value and close to the ripple on the filter capacitor. Also, the resulted leakage current was able to minimize into the mA range, which was accepted by the industrial standard.

Fig. 14 demonstrates the steady-state performance of the system at varying system conditions, which includes both step-up and step-down case situations. In Fig. 14(a)–(c), the platform is tested under  $120 V_{ac}$  input with 50, 120, and 200  $V_{dc}$  output, respectively. In Fig. 14(d), the platform is tested under  $220 V_{ac}$  input and 120  $V_{dc}$  output. All of them demonstrated a stable performance at the steady-state conditions. During each half line cycle, the inductor role was interchanged. At the positive half line cycle,  $L_1$  acted as a converter-side inductor to handle the power conversion. The negative half line cycle acted as a grid-side inductor and had the same current magnitude as the grid current. The magnitude of the inductor current and the current ripple on top were matched with the theoretical concepts, which are calculated in (6) and (7). Under different output voltage conditions, the ratio between the converter-side inductor current and

TABLE IV  
SUMMARY OF THE TEST RESULTS

$V_G / V$	$V_{Dc} / V$	Fig. 14	$P_o / W$	$\eta / \%$	$V_G$ THD $/ \%$	$I_G$ THD $/ \%$	PF
120	50	(a)	196	93.1	0.30	4.93	0.993
120	120	(b)	780	91.6	0.34	2.91	0.998
120	200	(c)	773	94.0	0.35	3.16	0.997
220	120	(d)	779	94.4	0.33	3.63	0.997

the grid-side current was varied. Smaller in the output voltage, higher in the inductor current magnitude was obtained. Because an  $LC$  input filter was configured at the input, the discontinuous buck–boost input current was filtered out and an LF continuous current was given in the grid side. Under the same power rating, lower in the output voltage, higher output capacitor voltage ripple was obtained.

The power factor of the system were higher than 0.99. In the 120  $V_{ac}$  input measurement, the best efficiency point was 96.8%, which was located at 200  $V_{dc}$  output and with 200 W loading. In detail, at full loading condition of 200 V output, voltage total harmonic distortion (THD) was 0.351% and the current THD was 3.16% where the system efficiency was 94.4%. At full loading condition of 120-V output, the voltage THD was 0.34% and the current THD was 2.91% where the system efficiency was 91.6%. Similar performance was obtained in the 120  $V_{ac}$ –50  $V_{dc}$  and 220  $V_{ac}$ –120  $V_{dc}$  testing conditions. All the time, the system THD in both voltage and current were also kept lower than 5% [30]. Meanwhile, the detailed system efficiency is provided in Fig. 15 and is summarized in Table IV.

The performance of the proposed rectifier was competitive to another single-stage buck–boost rectifiers. In [8], under a similar  $R_{dson}$  device, STY60NM50, the simulation efficiency of the bridgeless Sepic rectifier was around 92.4% at 120  $V_{ac}$ –48  $V_{dc}$ –200 W. In a similar test case, 120  $V_{ac}$ –50  $V_{dc}$ –200W, the achieved efficiency of the proposed rectifier is 93.1%. The result was close. As shown in Fig. 1(c) [13] and (d) [14], two different types of bridgeless buck–boost rectifier were proposed. One was operated at hard-switching and the other one was worked at soft-switching control. The given measured efficiencies were 87.7% at 110  $V_{ac}$ –48  $V_{dc}$ –100 W and 97.6% at 240  $V_{ac}$ –100  $V_{dc}$ –150 W, respectively. Under similar testing conditions, 120  $V_{ac}$ –50  $V_{dc}$ –100 W and 220  $V_{ac}$ –120  $V_{dc}$ –220 W, the measured system efficiency was 94.76% and 96.47%, respectively. The performance of the proposed converter was better than [13] but lower than [14]. The difference mainly came from the difference between soft-switching and hard-switching control. Even though there is better performance in soft-switching control, it relies more on the system parameters, and more precise control is required. Meanwhile, in those reference topologies, input filter is not included in their design. It implies that the loss in the filter circuit is not included in their corresponding measurement. In proposed topology, a reconfigurable  $LC$  filter is always located at the input and helps to filter out the high-frequency current ripple. In summary, the overall performance of the proposed topology was always comparable with others.

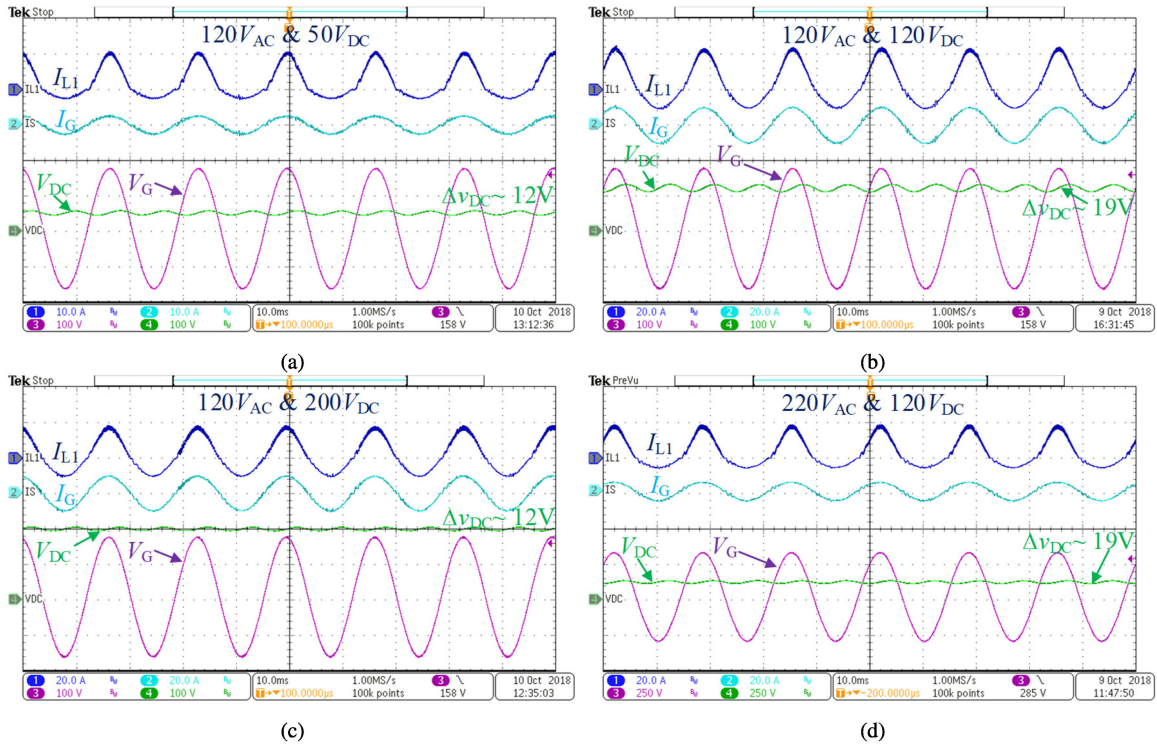


Fig. 14. Experimental waveform. (a)  $120 V_{ac}$ - $50 V_{dc}$ -200 W. (b)  $120 V_{ac}$ - $120 V_{dc}$ -800 W. (c)  $120 V_{ac}$ - $200 V_{dc}$ -800 W. (d)  $220 V_{ac}$ - $120 V_{dc}$ -800 W.

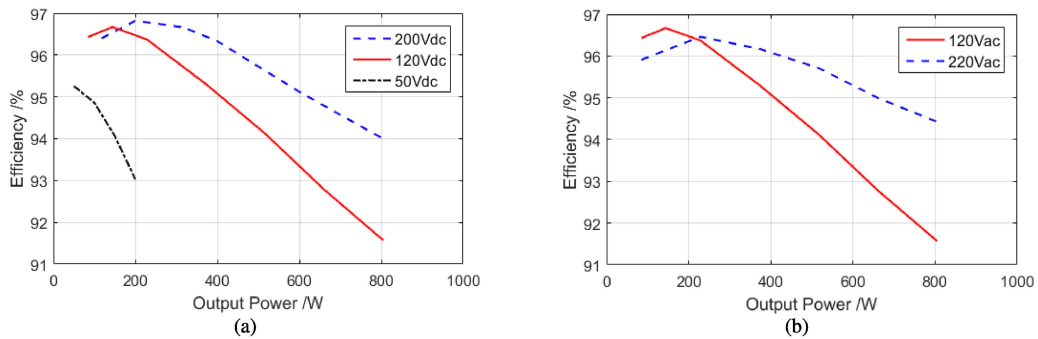


Fig. 15. Measured system efficiency (a) under a fixed input voltage ( $120 V_{ac}$ ) and (b) under a fixed output voltage ( $120 V_{dc}$ ).

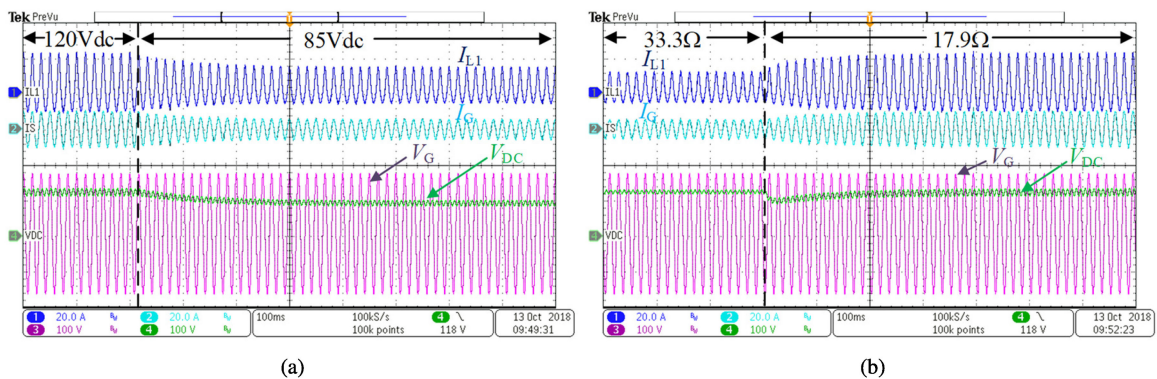


Fig. 16. Transient waveform during (a) an output voltage change and (b) a load change.

Apart from the steady-state, the system also achieves a stable performance under transient operations. Two transient tests were done. One is output voltage change, as shown in Fig. 16(a). In the test, the input voltage was kept at  $120 V_{ac}$  meanwhile the output voltage was dropped from 120 to  $85 V_{dc}$ . The consuming power was a half of the previous one. Another transient test case is load change. The performance is shown in Fig. 16(b). In the  $120 V_{ac}$ – $120 V_{dc}$  test case, the output loading was changed from  $33.3$  to  $17.9\Omega$ . As the loading resistance dropped, the output power was rapidly increased at a short period of time. In both cases, the system was stable. The grid current was sinusoidal and was able to convert into the steady state in a short moment of time after the change appeared. The performance of the designed prototype was always able to fulfill the industrial standard requirements and had good alignment with the topology concept.

## VI. CONCLUSION

This paper presented a new bridgeless buck–boost PFC rectifier. It can convert the grid voltage into a wide range of output voltages in both step-up and step-down conditions. Benefiting from the single-stage structure, the proposed PFC is simpler than other dual-stage topologies with fewer components required and all the components are fully utilized. Moreover, since an  $LC$  filter is built in the front stage, a continuous grid current and low CM noise system is also guaranteed. The operating principle and the steady-state characteristics of the proposed topology were explained. An  $800 W$  prototype has been implemented in order to verify the presented concept. The performance of the proposed bridgeless buck–boost PFC was demonstrated on it with the experimental results. A good agreement is achieved between theoretical concepts and experimental results.

## APPENDIX

### A. Derivation of (3) and (4)

The fundamental current of the converter-side inductor can be found from the grid-side inductor current and system duty cycle. The grid-side inductor current and the relationship with the converter-inductor current are expressed as

$$i_G(t) = \frac{2 \cdot P_O \cdot \sin\omega t}{V_G} \quad (A1)$$

$$i_L(t) = \frac{i_G(t)}{D(t)}. \quad (A2)$$

By putting (A1) and (2) into (A2), (3) can be calculated.

The ripple current of the converter-side inductor is related to the energy conversion process. It can be developed from the inductor ON-state characteristic as

$$v_{L,ON} = V_G |\sin\omega t| = L_X \cdot \frac{\Delta i_L(t)}{D(t) \cdot T} \quad (A3)$$

where  $T$  is the time period.

By putting (2) into (A3), (4) can be calculated.

### B. Derivation of (5)

As shown in Fig. 8, the capacitor current is equal to the grid current during the OFF-state. Therefore, the state equation can be formulated as

$$i_{C,ON}(t) = i_G(t) = C_{AB} \cdot \frac{\Delta v_C(t)}{(1-D(t)) \cdot T}. \quad (A4)$$

By putting (2) into (A4), (5) can be calculated.

### C. Derivation of (6)

As an  $LC$  filter structure is formed at the front stage, the capacitor voltage ripple is equal to the grid-side inductor voltage ripple. By approximating the ripple to the triangle waveform, the grid current ripple expression can be formed as

$$\Delta i_G(t) = \frac{\Delta v_C(t)}{8 \cdot L_X \cdot f_{SW}}. \quad (A5)$$

By putting (A4) into (A5), (6) can be calculated.

### D. Derivation of (7)

The output capacitor voltage ripple can be determined from the system power equation. The input power and the output power equations are as follows:

$$P_{IN}(t) = V_G \sin\omega t \cdot I_G \sin\omega t \quad (A6)$$

$$P_O(t) = \frac{V_{DC}^2}{R} + \frac{1}{2} \cdot C_{DC} \cdot \frac{d}{dt} \left[ V_{DC} + \frac{\Delta V_{DC}}{2} \sin(2\omega t) \right]^2 \quad (A7)$$

where  $R$  is the output resistance.

During the steady state, power at the input and output must be equalized. By solving the double LF term in (A6) and (A7), (7) can be obtained.

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