Analysis and Design of a Single-Switch High Step-Up Coupled-Inductor Boost Converter

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***Abstract*—Analysis and design of a single-switch high step-up coupled-inductor boost converter are presented in this paper. With the aid of the coupled inductor, the proposed converter can achieve high-voltage gain without extreme duty cycle. Also, low switch voltage stress can be achieved, thus low-voltage-rating MOSFET is allowed to lower the conduction loss. Moreover, the proposed converter features continuous input current, which is desirable and friendly to the battery, fuel cell, and photovoltaic applications. In addition, the reverse recovery problem of the diodes can be alleviated and leakage energy can be recycled. The operation principles and characteristics of the proposed converter are discussed. Experimental results are provided to verify the theoretical analysis.**

***Index Terms*—Boost converter, continuous input current, coupled inductor, high step-up converter.**

I. Introduction

In RECENT years, high step-up dc–dc conversion has attracted substantial attentions in many application areas. For example, in renewable energy systems, the renewable sources, such as fuel cells and photovoltaic (PV) modules, generate a low voltage. The low-level voltage has to be boosted to a high bus voltage in order to satisfy the requirement of the grid-connected inverters [1]. Also, in uninterrupted power supplies and high-intensity-discharge lamp ballast for automobiles, high step-up converters are required to convert the low voltage of the battery to a high dc link voltage [2]. The conventional boost converter is not suitable for high step-up applications because extreme duty cycle has to be used, which results in high power losses. Therefore, high step-up converters with high efficiency are needed.

Various boosting techniques have been proposed to achieve high step-up conversion [3]. Switched capacitor, switched inductor, voltage multipliers, and voltage lift techniques have been reported to extend the voltage gain [4]–[8]. Unfortunately, under very high gain applications, a large number of diodes and capacitors may be needed, which increases the cost and degrades the efficiency. Also, these topologies may suffer from diode reverse recovery and electromagnetic interference problems, thus additional snubbers may be needed [8]. Utilizing magnetic coupling is an attractive approach for high conversion ratio applications. With the aid of coupled inductor, large voltage gain can be achieved without extreme duty cycle. However, the leakage inductance may result in large voltage spike across the switch, which causes high-voltage stress and decreased efficiency. In order to handle the leakage problem, coupled-inductor converters with passive or active clamp circuit were proposed [9]–[14]. Converters integrating coupled inductor with switched-capacitor or voltage-multiplier cells were also proposed in the literature [15]–[18] to recover the leakage energy and further increase the voltage gain. These coupled-inductor topologies feature a pulsating input current. The peak-to-peak current ripple depends on the current level and the turns ratio. If the current level is increased or the turns ratio is increased for higher voltage gain, the input current ripple becomes even larger. The large current ripple results in high rms current stress, causing high conduction losses. Moreover, the pulsating input current is detrimental to the lifetime of the low-voltage sources like batteries and fuel cells [19]–[20]. Also, in PV applications, the pulsating input current makes it hard to precisely track the true maximum power point (MPP), which can cause a severe drop in energy extraction [21]. Therefore, in practice, additional *LC* (or *C*) input filter is required. Due to the high current stress at the input side, large electrolytic capacitor has to be employed, which is not only bulky and costly, but also has a short lifetime, hampering the reliability of the system [22]–[24].

Converters with continuous input current are advantageous for battery, fuel cell, and PV applications [25], [26]. The feature of continuous input current can significantly reduce the input capacitor or even save the input filter, which increases the power density and reliability. Interleaving technique has been employed in coupled-inductor converters to achieve low input current ripple [27]–[30]. They are more suitable for high power and ultra-high gain applications. Sepic derived converter have been proposed in [31] and [32] to obtain continuous input current. In [33] and [34], two-switch high step-up converters were proposed. Zero-voltage-switching of the switches are achieved. But the additional switch and gate driver lead to increased cost and complexity. In [35] and [36], boost converter integrated with voltage multiplier cells were proposed. In [37] and [38], quadratic boost based coupled-inductor converters were proposed. These topologies achieve high-voltage gain and continuous input current with high component count.

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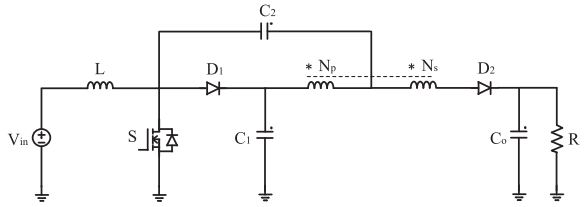

Fig. 1. Proposed converter.

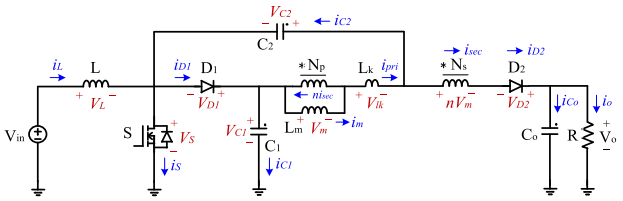

Fig. 2. Equivalent circuit.

This paper proposes a single-switch high step-up coupled-inductor boost converter. The analysis and design are presented. The proposed converter has the following features.

1) Turns ratio of the coupled inductor is employed as an extra degree of freedom to achieve high-voltage gain.
2) Low switch voltage stress is achieved, thus low-voltage-rating MOSFET with small ON-resistance is allowed to lower the conduction loss.
3) With a discrete inductor at the input side, continuous input current can be obtained, which is desirable and friendly to the battery, fuel cell, and PV applications.
4) Reverse recovery problem of the diodes is alleviated and leakage energy can be recycled.

The rest of this paper is organized as follows. The proposed converter and its operation principles are described in Section II. Characteristics are analyzed in Section III. Design considerations are discussed in Section IV. Experimental results are presented in Section V. Conclusions are given in Section VI.

II. Proposed Converter and Operation Principles

The proposed single-switch high step-up coupled-inductor boost converter is shown in Fig. 1. It is composed of one input inductor, one coupled inductor, one switch, two diodes, two energy transfer capacitors, and one output capacitor. Fig. 2 shows the equivalent circuit. The coupled inductor is modeled as an ideal transformer with magnetizing inductance (L_m) and leakage inductance (L_k) [43].

In order to simplify the analysis, the following assumptions are made: first, all semiconductor devices are considered ideal; second, all the capacitors are large enough so that the voltages across them are constant without ripples.

When the input inductor current (i_L) is above zero throughout the switching cycle and the output diode current (i_{D2}) is above zero throughout the switch OFF time, the converter is operating in continuous conduction mode (CCM). Discontinuous conduction mode (DCM) occurs when the input current ripple is large so that

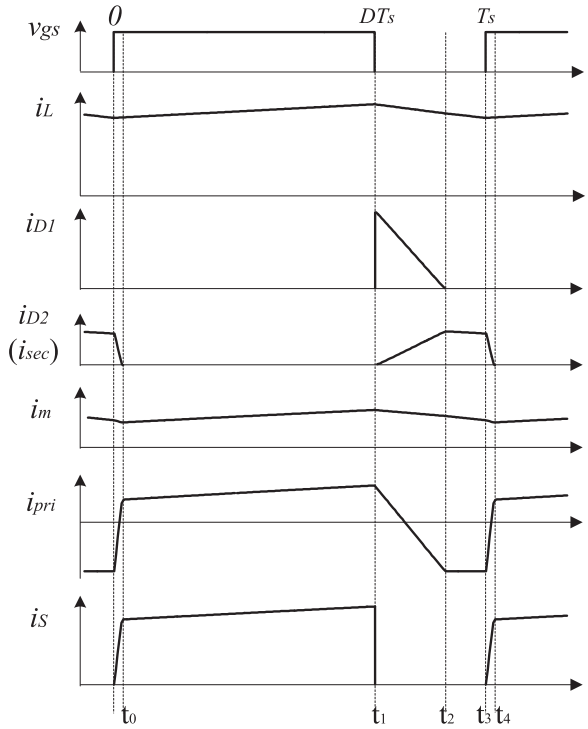

Fig. 3. Key waveforms of the proposed converter in CCM.

i_L reaches zero, or the magnetizing current ripple is large, which makes diode D_2 reverse-biased before the end of the switching period. As one main feature of the proposed converter is continuous input current, DCM operation with i_L reaching zero is not desired. Only DCM operation with D_2 reverse-biased before the end of the switching period is discussed in this paper.

A. CCM Operation

Fig. 3 shows the key waveforms of the proposed converter in CCM. Four modes are observed during one switching period. The corresponding circuits of each mode are shown in Fig. 4.

Mode 1 $[t_0 - t_1]$*:* The switch is ON, and all diodes are reverse-biased, as shown in Fig. 4(a). The input inductor is charged linearly by the input source. The capacitor C_1 is delivering energy to the coupled inductor and capacitor C_2. The primary voltage of the coupled inductor is $V_{C1} - V_{C2}$, and the coupled inductor is magnetized. The output capacitor supports the load. As the leakage inductance is negligible compared to the magnetizing inductance, the following equations are obtained:

$$v_L = V_{\text{in}} \tag{1}$$

$$v_m = V_{C1} - V_{C2} \tag{2}$$

$$i_{Co} = -I_o \tag{3}$$

$$-i_{C1} = i_{C2} = i_{\text{pri}} = i_m\,. \tag{4}$$

Mode 2 $[t_1 - t_2]$*:* At t_1, the switch is turned OFF, which makes diodes D_1 and D_2 turned ON, as shown in Fig. 4(b). The input inductor starts releasing energy. The capacitor C_1 is being charged. The primary voltage of the coupled inductor is clamped to $-V_{C2}$,

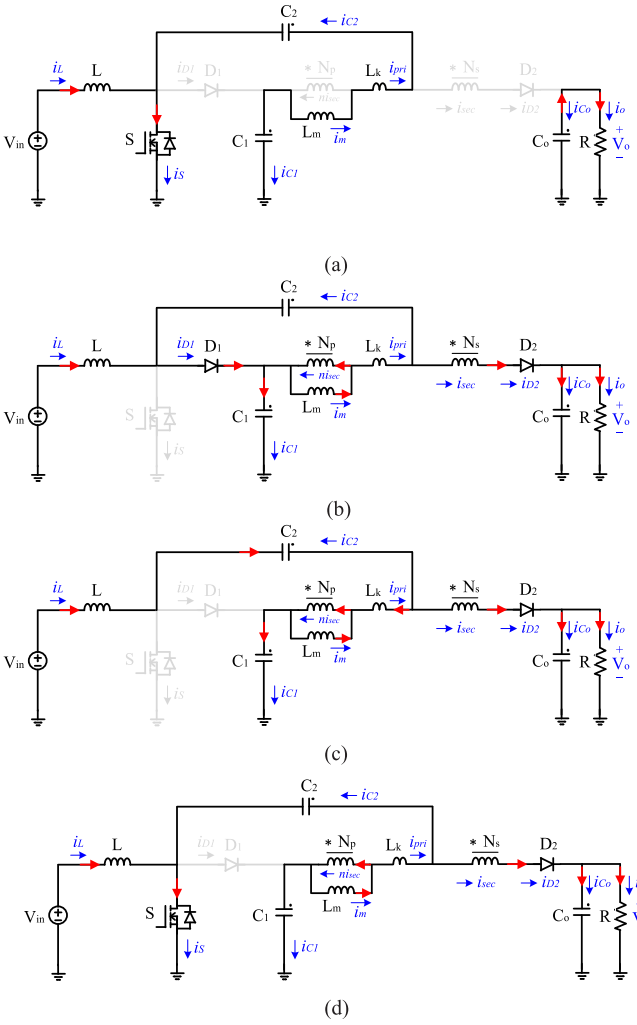

Fig. 4. Operation modes of the proposed converter in CCM. (a) Mode 1 $[t_0 - t_1]$. (b) Mode 2 $[t_1 - t_2]$. (c) Mode 3 $[t_2 - t_3]$. (d) Mode 4 $[t_3 - t_4]$.

and thus the coupled inductor is demagnetized. The secondary current of the coupled inductor $i_{\rm sec}$ is increasing linearly, and the current through D_1 is decreasing linearly. The equations in this mode are obtained as follows:

$$v_m = -V_{C2} \tag{5}$$

$$V_{\rm in} = v_L - V_{C2} - v_m + V_{C1} \tag{6}$$

$$V_{C1} = (n+1)\, v_m + V_o \tag{7}$$

$$i_{\rm pri} = i_m - n i_{\rm sec} \tag{8}$$

$$i_{D2} = i_{\rm sec} = \frac{V_{C1} + (n+1)\, V_{C2} - V_o}{n^2 L_k}\ (t - t_1) \tag{9}$$

$$i_{Co} = i_{\rm sec} - I_o \tag{10}$$

$$i_{C2} = i_{\rm pri} - i_{\rm sec} = i_m - (n+1)\, i_{\rm sec} \tag{11}$$

$$i_{D1} = i_L + i_{C2} = i_L + i_m - (n+1)\, i_{\rm sec} \tag{12}$$

$$i_{C1} = i_{D1} - i_{\rm pri} = i_L - i_{\rm sec}. \tag{13}$$

Solving (6) and (7), the following can be obtained:

$$v_L = V_{\rm in} + V_{C2} - \frac{n}{n+1} V_{C1} - \frac{1}{n+1} V_o \tag{14}$$

$$v_m = \frac{1}{n+1}\ (V_{C1} - V_o)\,. \tag{15}$$

Mode 3 $[t_2 - t_3]$*:* At t_2, the current through D_1 decreases to zero and D_1 is naturally turned OFF. Therefore, D_1 has no reverse recovery problem. As shown in Fig. 4(c), the inductor current i_L discharges C_2, and the primary current of the coupled inductor $i_{\rm pri}$ charges C_1. The difference of i_L and $i_{\rm pri}$ is delivered to the load. Equation (6)–(8) and (14)–(15) still hold in this mode, and the following equations are obtained:

$$i_{C2} = -i_L \tag{16}$$

$$i_L + i_{\rm pri} = i_{\rm sec}\,. \tag{17}$$

Substituting (8) to (17), $i_{\rm sec}$ is evaluated as

$$i_{\rm sec} = \frac{1}{n+1}\ (i_L + i_m)\,. \tag{18}$$

Then

$$i_{D2} = \frac{1}{n+1}\ (i_L + i_m) \tag{19}$$

$$i_{C1} = -i_m + n\, i_{\rm sec} = \frac{n}{n+1}\, i_L - \frac{1}{n+1} i_m \tag{20}$$

$$i_{Co} = i_{\rm sec} - I_o = \frac{1}{n+1}\ (i_L + i_m) - I_o. \tag{21}$$

Mode 4 $[t_3 - t_4]$*:* At t_3, the switch is turned ON, as shown in Fig. 4(d). As the leakage inductance limits the current changing rate, the switch current is increasing gradually after the switch is turned ON, which helps reduce the switching loss. The current of diode D_2 is decreasing, and the falling rate is determined by the leakage inductance. Thus, the reverse recovery problem of D_2 is alleviated. This mode ends when the current through D_2 becomes zero and then turned OFF. The falling rate of D_2 is given by

$$\frac{di_{D2}}{dt} = -\frac{V_o + nV_{C1} - (n+1)\, V_{C2}}{n^2 L_k}. \tag{22}$$

B. DCM Operation

Fig. 5 shows the key waveforms of the proposed converter in DCM. Four modes are observed during one switching period.

Mode 1 $[t_0 - t_1]$*:* The switch is ON, and all diodes are reverse-biased. The corresponding circuit is the same as in Fig. 4(a). The input current is increasing linearly. The primary voltage of the coupled inductor is clamped at $V_{C1} - V_{C2}$, and thus the magnetizing current is increasing linearly.

Mode 2 $[t_1 - t_2]$*:* The switch is turned OFF, and diodes D_1 and D_2 are forward-biased. The corresponding circuit is the same as in Fig. 4(b). The input current is decreasing linearly. The primary voltage of the coupled inductor is clamped to $-V_{C2}$, and thus the magnetizing current is decreasing linearly. The secondary current is increasing, and the current through D_1 is decreasing.

Mode 3 $[t_2 - t_3]$*:* At t_2, the current through D_1 decreases to zero and D_1 is naturally turned OFF. The corresponding circuit

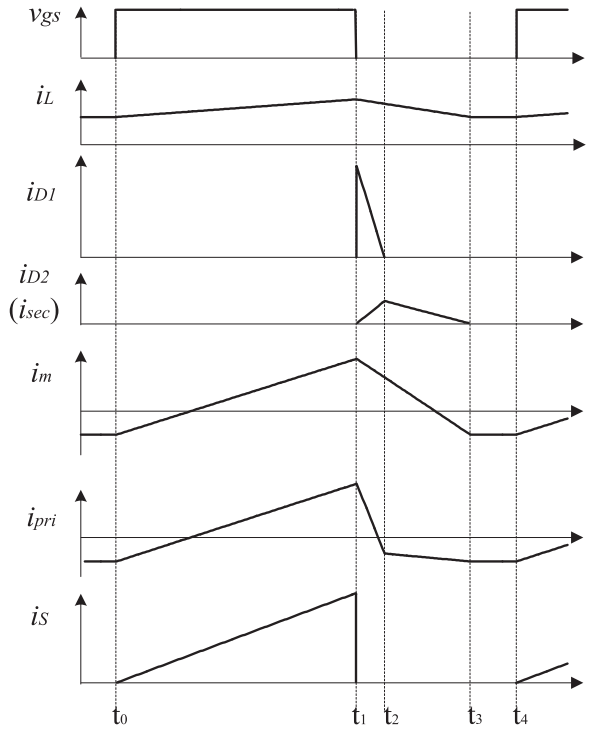

Fig. 5. Key waveforms of the proposed converter in DCM.

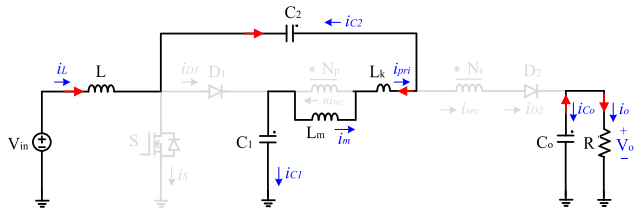

Fig. 6. Mode 4 of the proposed converter in DCM.

is the same as in Fig. 4(c). The input current and the magnetizing current keep decreasing. The current through D_2 in this mode can be expressed as in (19). It is a fraction of the sum of the input current and magnetizing current. As the magnetizing inductance is small under DCM, the magnetizing current has large ripple. Small ripple assumption cannot be applied. Thus, the current through D_2 is decreasing as well.

Mode 4 $[t_3 - t_4]$*:* At t_3, the current through D_2 decreases to zero and D_2 is naturally turned OFF. The corresponding circuit in this mode is shown in Fig. 6. All the switch and diodes are in the OFF state. The input current becomes equal to the magnetizing current in magnitude but opposite in direction. At t_4, the switch is turned ON, and mode 1 starts again.

Similar to flyback converter, the voltage gain of the proposed converter in DCM is dependent to the load, and the peak and rms currents in the windings and switches become higher compared to the CCM operation. This is not favorable for high-current applications. In this paper, only analysis and design of the proposed converter in CCM will be discussed.

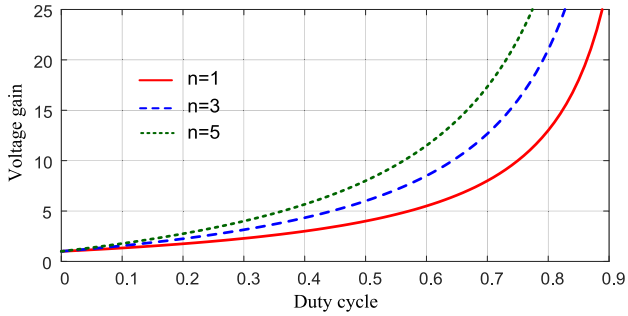

Fig. 7. Voltage gain versus duty cycle under different turns ratios.

III. Performance Analysis

A. Voltage Gain

By applying the voltage-second balance principle to L and L_m, the following equations are obtained:

$$V_{\text{in}} D + \left(V_{\text{in}} + V_{C2} - \frac{n}{n+1} V_{C1} - \frac{1}{n+1} V_o \right) (1 - D) = 0 \tag{23}$$

$$(V_{C1} - V_{C2})\, D + \frac{1}{n+1} (V_{C1} - V_o)\, (1 - D) = 0. \tag{24}$$

Solving (5) to (7), the following relationship is derived:

$$V_{C1} + (n+1)\ V_{C2} = V_o\ . \tag{25}$$

Solving (23)–(25), the voltage gain of the proposed converter is derived as

$$M = \frac{V_o}{V_{\text{in}}} = \frac{1 + (n+1)\, D}{1 - D}\ . \tag{26}$$

The voltages of C_1 and C_2 are derived as

$$V_{C1} = \frac{V_{\text{in}}}{1 - D} = \frac{V_o}{1 + (n+1)\, D} \tag{27}$$

$$V_{C2} = \frac{D V_{\text{in}}}{1 - D} = \frac{D V_o}{1 + (n+1)\, D}\ . \tag{28}$$

Fig. 7 shows the curves of the voltage gain versus duty cycle under different turns ratios. It can be seen that the proposed converter can achieve a high-voltage gain by adjusting the duty cycle and turns ratio.

B. Voltage Stress

The voltage stresses of the capacitors are given by (27) and (28). The voltage stress of the switch can be derived as

$$V_S = \frac{1}{1 + (\text{n} + 1)\, D}\ V_o. \tag{29}$$

It can be seen that the switch voltage stress is much lower than the output voltage. It decreases as the voltage gain is extended by either increasing the duty cycle or the turns ratio. Therefore, low-voltage-rating MOSFETs with small ON-resistance can be adopted to reduce the conduction loss.

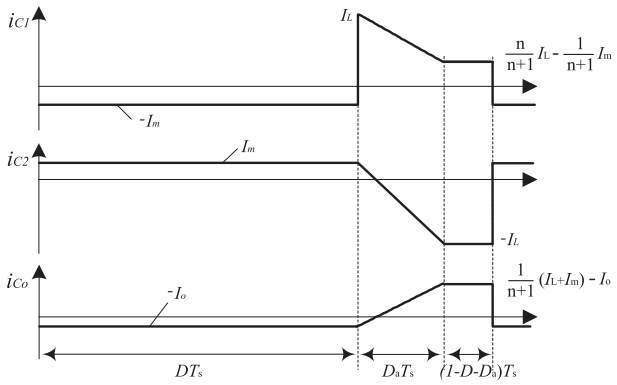

Fig. 8. Simplified current waveforms of the capacitors.

The voltage stresses of the diodes are obtained as

$$V_{D1} = \frac{1}{1+(\mathrm{n}+1)\,D}\,V_o \tag{30}$$

$$V_{D2} = \frac{n+1}{1+(\mathrm{n}+1)\,D}\,V_o. \tag{31}$$

By applying small-ripple approximation, the input inductor current is assumed to be I_L and the magnetizing current of the coupled inductor is assumed to be I_m. Let $t_2 - t_1 = D_a\,T_s$, and then $t_3 - t_2 = (1-D-D_a)T_s$. Ignoring the transitional mode, the simplified current waveforms of the capacitors is shown in Fig. 8.

According to the charge balance of C_1, C_2, and C_o, the following equations are obtained:

$$-I_m\,D + \frac{1}{2}\left(I_L + \frac{nI_L}{n+1} - \frac{I_m}{n+1}\right)D_a + \left(\frac{nI_L}{n+1} - \frac{I_m}{n+1}\right)(1-D-D_a) = 0 \tag{32}$$

$$I_m\,D + \frac{1}{2}\,(I_m - I_L)\,D_a - I_L)(1-D-D_a) = 0) \tag{33}$$

$$-I_o\,D + \frac{1}{2}\left(-I_o + \frac{I_m + I_L}{n+1} - I_o\right)D_a + \left(\frac{I_m + I_L}{n+1} - I_o\right)(1-D-D_a) = 0. \tag{34}$$

Solving (32)–(34), the following is derived:

$$I_L = \frac{1+(n+1)\,D}{1-D}\,I_o \tag{35}$$

$$I_m = \frac{(n+1)\,(1-D)}{1+(n+1)\,D}\;\; I_L = (n+1)\,I_o \tag{36}$$

$$D_a = \frac{2}{n+2}\;(1-D)\,. \tag{37}$$

Since the average currents of capacitors in one switching period are zero, according to the operation principles, the average current of the diodes can be evaluated as

$$I_{D2\_\mathrm{avg}} = I_{Co\_\mathrm{avg}} + I_o = I_o \tag{38}$$

$$I_{D1\_\mathrm{avg}} = I_{C1\_\mathrm{avg}} + I_{C2\_\mathrm{avg}} + I_{D2\_\mathrm{avg}} = I_o\,. \tag{39}$$

The rms current stress of the switch can be expressed as

$$I_{S\_\mathrm{rms}} = (I_L + I_m)\;\;\sqrt{D} = \frac{(n+2)\,\sqrt{D}}{1-D}\;I_o. \tag{40}$$

The rms current of the primary winding of the coupled inductor is given by

$$I_{pri\_\mathrm{rms}} = \mathrm{sqrt}\left(DI_m{}^2 + \frac{(1-D)}{(n+2)\,(n+1)}\left(\frac{2}{3}I_m\,((n+2)\,I_m - nI_L) + \frac{n+\frac{2}{3}}{n+1}(I_m - nI_L)^2\right)\right). \tag{41}$$

The rms current of the secondary winding of the coupled inductor is given by

$$I_{\mathrm{sec\_rms}} = \frac{n+2}{n+1}\,\sqrt{\frac{n+\frac{2}{3}}{(n+2)\,(1-D)}}\,I_o. \tag{42}$$

The current stresses of the capacitors are given by

$$I_{C1\_\mathrm{rms}} = \mathrm{sqrt}\left(DI_m{}^2 + \frac{1-D}{n+2}\left(\frac{2}{3}I_L\left(\frac{2n+1}{n+1}I_L - I_o\right) + \left(n+\frac{2}{3}\right)\left(\frac{n}{n+1}I_L - I_o\right)^2\right)\right) \tag{43}$$

$$I_{C2\_\mathrm{rms}} = \mathrm{sqrt}\left(DI_m{}^2 + \frac{1-D}{n+2}\cdot\left(\frac{2}{3}I_m\,(I_m - I_L) + \left(n+\frac{2}{3}\right)I_L{}^2\right)\right) \tag{44}$$

$$I_{Co\_\mathrm{rms}} = \mathrm{sqrt}\left(DI_o{}^2 + \frac{1-D}{n+2}\left(\frac{2}{3}I_o\left(I_o - \frac{I_L}{n+1}\right) + \frac{\left(n+\frac{2}{3}\right)I_L{}^2}{(n+1)^2}\right)\right). \tag{45}$$

C. Input Current Ripple

Due to the presence of a discrete inductor at the input side, the input current of the proposed converter is continuous. The current ripple can be evaluated as

$$\Delta i_L = \frac{V_{\mathrm{in}}D}{Lf_s} = \frac{V_oD\,(1-D)}{Lf_s\,(1+(n+1)\,D)}\,. \tag{46}$$

The continuous input current makes the proposed converter beneficial to extend the lifetime of the low-voltage sources like batteries and fuel cells. Also in PV applications, the feature of the continuous input current can significantly reduce the input capacitor, which helps increase the power density and reliability.

D. Influence of the Leakage Inductance

As can be seen from the operation principles, the current of the leakage inductance partly goes through the capacitor C_2 and partly goes to the load when the switch is turned OFF. Thus, the leakage energy can be recycled and no additional components are needed.

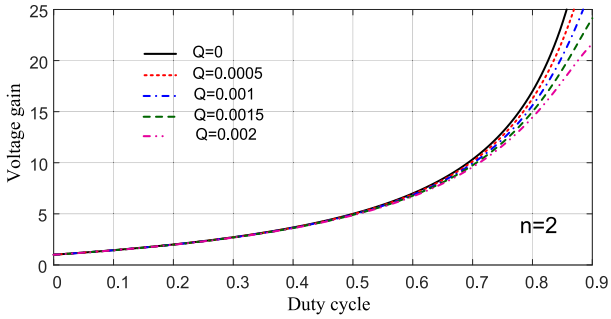

Fig. 9. Voltage gain considering the effect of the leakage inductance.

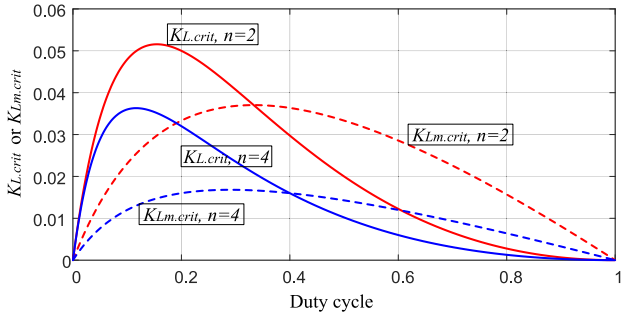

Fig. 10. Boundary condition of the proposed converter.

During mode 2, due to the presence of the leakage inductance, the current of the diode D_1 decreases linearly and then naturally turns OFF. Thus, D_1 has no reverse recovery problem. During mode 4, the current falling rate of the diode D_2 is limited by the leakage inductance, which can significantly alleviate the reverse recovery of D_2. Also, with the aid of the leakage inductance, the switch current rises gradually when the switch is turned ON, which helps reduce the switching loss.

The leakage inductance can also have an effect on the voltage gain. Considering the rising slope of the secondary current $i_{\rm sec}$, the following equation can be written:

$$\frac{V_{C1}+(n+1)\,V_{C2}-V_o}{n^2 L_k}=\frac{i_L+i_m}{(n+1)\,D_a T_s}\,. \tag{47}$$

Substituting (35)–(37) to (47), the following equation is obtained:

$$V_{C1}+(n+1)\;V_{C2}=\left(\frac{n^2(n+2)^2}{2\,(n+1)\,(1-D)^2}Q+1\right)V_o \tag{48}$$

where $\mathrm{Q}\;=L_k\;/(RT_s)$.

As the average voltages of the inductances are zero during steady state, the following equation can be obtained according to KVL:

$$V_{\rm in}=\;-V_{C2}+V_{C1}. \tag{49}$$

Due to the voltage-second principle of the input inductor, the following equation can be written:

$$V_{\rm in}D+\;(V_{\rm in}-V_{C1})\,D_a+\left(V_{\rm in}+V_{C2}-V_{C1}+\frac{V_{C1}-V_o}{n+1}\right)(1-D-D_a)=0. \tag{50}$$

Solving (48)–(50), the voltage gain with the effect of the leakage inductance is expressed as

$$M\;=\frac{V_o}{V_{\rm in}}\;=\frac{1+(n+1)\,D}{(1-D)\left(1+\frac{n^2(n+2)^2}{2(n+1)^2(1-D)^2}Q\right)}\,. \tag{51}$$

The voltage gain with the effect of the leakage inductance is plotted in Fig. 9. It can be seen that the voltage gain is not very sensitive to the leakage inductance. If the leakage inductance is ignored, (51) will be equal to (26).

E. Boundary Condition

The aforementioned analysis is under CCM condition. In order to ensure CCM condition, the input inductor current must be above zero throughout the switching cycle and the diode current of D_2 must be above zero throughout the switch OFF time, which yields

$$i_{L.\min}=I_L\;-\;\frac{\Delta i_L}{2}=\frac{1+(n+1)\,D}{1-D}\,I_o-\frac{V_{\rm in}D}{2Lf_s}>0 \tag{52}$$

$$i_{D2.\min}=\frac{1}{n+1}\left(I_L-\frac{\Delta i_L}{2}+I_m-\frac{\Delta i_m}{2}\right)=\frac{1}{n+1}\left(\frac{n+2}{1-D}I_o-\frac{V_{\rm in}D}{2Lf_s}-\frac{(V_{C1}-V_{C2})D}{2L_m f_s}\right)>0. \tag{53}$$

Define $k_L=\;2Lf_s/R$ and $k_{Lm}=\;2L_m f_s/R$. By solving (52) and (53), the CCM criteria are obtained as follows:

$$k_L>K_{L.\rm crit}=\frac{D(1-D)^2}{(1+(n+1)\,D)^2} \tag{54}$$

$$k_{Lm}>\;K_{Lm.\rm crit}=\frac{D(1-D)^2}{(1+(n+1)\,D)\,(n+1)\,(1-D)}\,. \tag{55}$$

The dependence of $K_{L.\rm crit}$ and $K_{Lm.\rm crit}$ on the duty cycle and turns ratio are plotted in Fig. 10. It can be seen that when the turns ratio increases, it is easier to achieve CCM condition.

F. Voltage Gain Considering Parasitic Elements

Similar to the conventional boost converter, the voltage gain of the proposed converter would deviate from the ideal value if parasitic elements are considered, especially under extreme duty cycles. The equivalent circuit including parasitic elements is illustrated in Fig. 11, where $r_{\rm on}$ is the ON-resistance of the switch, r_L is the resistance of the input inductor, $r_{\rm pri}$ and $r_{\rm sec}$ are the resistances of the primary winding and secondary winding of the coupled inductor, respectively, and V_d is the forward voltage drop of all diodes. The leakage inductance and the equivalent series resistance of the capacitors are ignored in order to simplify calculation.

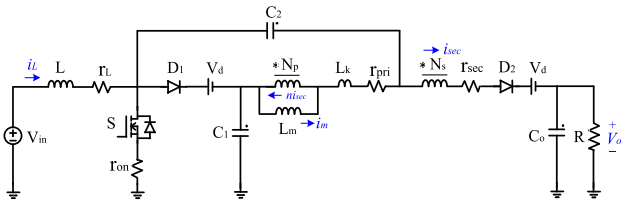

Fig. 11. Equivalent circuit including parasitic elements.

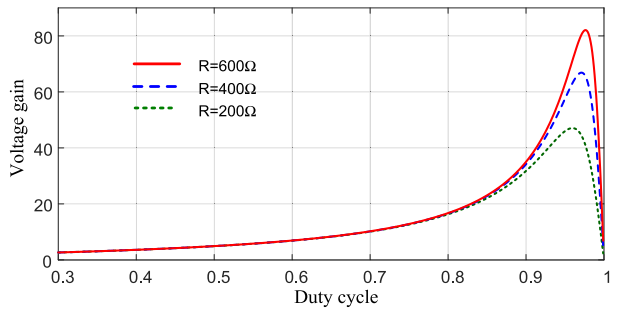

Fig. 12. Voltage gain with parasitic elements ($r_{\rm on} = 7.5$ mΩ, $r_L = 20$ mΩ, $r_{\rm pri} = 20$ mΩ, $r_{\rm sec} = 100$ mΩ, $V_d = 0.7$ V, $n = 2$, $V_{\rm in} = 20$ V).

TABLE I
COMPARISON OF THE PROPOSED CONVERTER WITH [31]

Topologies	[31]	Proposed
Switch/Diode/Core/Winding /Capacitor	1/2/2/3/3	1/2/2/3/3
Voltage gain	$\frac{1+nD}{1-D}$	$\frac{1+(n+1)D}{1-D}$
Switch voltage stress	$\frac{(n+M)V_o}{(n+1)M}$	$\frac{(n+1+M)V_o}{(n+2)M}$
Output diode voltage stress	$\frac{n(n+M)V_o}{(n+1)M}$	$\frac{(n+1)(n+1+M)V_o}{(n+2)M}$

By using KVL and voltage-second balance of the input inductance and magnetizing inductance, the voltage gain considering parasitic elements can be derived as

$$\frac{V_o}{V_{\rm in}} = \frac{\frac{1+(n+1)D}{1-D} - 2\frac{V_d}{V_{\rm in}}}{1+\frac{1}{1-D}\left(A\frac{r_{\rm on}}{R}+B\frac{r_L}{R}+C\frac{r_{\rm pri}}{R}+\frac{r_{\rm sec}}{R}\right)} \tag{56}$$

where $A=(n+2)(n+1+1/(1-D))$, $B=(1+(n+1)D)^2/(1-D)$, and $C=(n+2)(n+1)(1-D)$.

The voltage gain considering parasitic elements at different loads is shown in Fig. 12. Under given parasitic parameters, the voltage gain would decrease as the load increases. Also the voltage gain with parasitic elements would collapse under extreme duty cycles.

G. Comparison

In this section, the proposed converter is compared with the converter in [31]. The component count, voltage gain, switch voltage stress, and maximum diode voltage stress are listed in Table I. The comparison curves are illustrated in Fig. 13. It can be seen that the proposed converter achieves higher voltage gain under the same duty cycle and turns ratio. Also the proposed converter has lower switch voltage stress, thus low-voltage-rating MOSFET with small ON-resistance can be used to lower conduction loss.

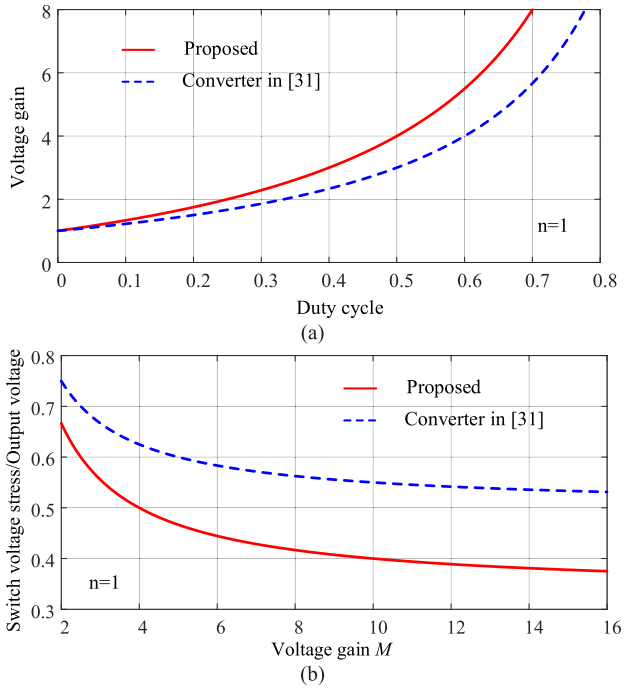

Fig. 13. Comparison. (a) Voltage gain. (b) Normalized switch voltage stress.

IV. DESIGN CONSIDERATIONS

In this section, design considerations of the key components will be discussed. As a design example, a 200 W 20 V-input 200 V-output converter is to be considered. The switching frequency is set to 100 kHz.

A. Coupled-Inductor Design

The voltage gain is determined by the duty cycle and the turns ratio. A larger duty cycle would result in larger current ripple and increased switch voltage stress. A smaller duty cycle leads to high turns ratio, which increases the size of the coupled inductor. Hence, a compromise should be considered. In this design example, $D = 0.693$ and $n = 2$ are selected based on (26).

The magnetizing inductance of the coupled inductor can be designed based on the ripple $(\delta_m\%)$ of the magnetizing current. The average magnetizing current I_m is calculated as 3 A according to (36). Considering a peak-to-peak magnetizing current ripple to be less than 50% of the magnetizing current, the magnetizing inductance can be calculated as

$$L_m = \frac{V_{in}D}{\delta_m\%I_m\ f_s} > 92\,u\text{H}. \tag{57}$$

Finally, the value of the magnetizing inductance is selected as 100 uH.

The peak magnetizing current is calculated by

$$I_{m\_pk} = I_m + \frac{1}{2}\,\delta_m\%I_m = 4.5\text{ A}. \tag{58}$$

The leakage inductance of the coupled inductor helps limit the current falling rate and thus alleviate the diode reverse recovery problem. In order to effectively reduce the reverse recovery, di/dt of the diode should be less than 100 A/*u*s [39]. Therefore, the minimum leakage inductance for alleviating the reverse recovery is given by

$$L_k = \frac{(n+1)\,V_o}{(1+(n+1)\,D)\,n^2\frac{di_{D2}}{dt}} > 0.49\ u\text{H}. \tag{59}$$

On the other hand, if the leakage inductance is too large, the voltage gain becomes lower, hence the duty cycle has to be increased for compensation, which increases conduction losses. Therefore, a compromise should be considered when choosing the leakage inductance.

The design procedure of the coupled inductor follows the flyback transformer design method [40]–[42], as they both have a two-winding structure and store dc energy. Powder cores are made of materials with evenly distributed air gap, which offers advantages of soft saturation, better temperature stability, and lower fringing losses compared to ferrite cores with discrete air gap [40]. Therefore, powder cores are used in the design. MPP core C055089A2 is chosen. The primary number of turns is selected as 25 and the secondary number of turns is 50.

B. Input Inductor Design

The input inductor is designed based on the required input current ripple ($\delta_{\text{in}}\%$). Considering the peak-to-peak input current ripple to be less than 15% of the input current, the input inductor can be calculated by

$$L = \frac{V_{\text{in}}D}{\delta_{\text{in}}\%I_{\text{in}}\,f_s} > 92\ u\text{H}. \tag{60}$$

Finally, the value of the input inductance is selected as 100 *u*H.

C. Semiconductor Selection

The switches and diodes are selected according to their voltage and current stresses. The voltage stresses of the switch and diodes can be calculated from (29)–(31). The current stresses of the switch and diodes are given by (38)–(40). Considering the voltage overshoot and ringing in real applications, the voltage ratings of the selected devices should be higher than the calculated values.

TABLE II
KEY PARAMETERS OF THE PROTOTYPE

Parameters	Value/Description
Switch	IPA075N15N3
Diodes D_1	STPS20200CT
Diodes D_2	STTH20L03C
Coupled inductors	Turns ratio = 25:50 Magnetizing inductance = 100 uH Leakage inductance = 2.2 uH
Input inductor	100 uH
Capacitor C_1, C_2	22 uF Film capacitor
Capacitor C_o	56 uF electrolytic capacitor

D. Capacitor Design

The capacitors can be designed based on the voltage ripple ($\delta_c\%$) and the output power P_o. Considering the voltage ripple to be less than 3% of the capacitor voltage. The calculations of the capacitors are given by (eq. 61, 62, 63) shown at the bottom of this page.

The voltage stresses of the energy transfer capacitors ($C_1 - C_2$) can be calculated by (27)–(28), which are 65 and 45 V, respectively. The voltage stress of the output capacitor is equal to the output voltage. The ripple currents of the capacitors can be calculated by (43)–(45), which are 4.5, 5.0, and 1.6 A, respectively.

Finally, 22 μF film capacitors are selected for the energy transfer capacitors C_1 and C_2. In practice, considering the voltage overshoot during the load transient, larger output capacitor may be needed. In this design example, 56 *u*F electrolytic capacitor is selected for the output capacitor C_o.

V. EXPERIMENTAL RESULTS

In order to verify the performance of the proposed converter, a 200 W 20 V-input 200 V-output prototype is built and tested. The switching frequency is set to 100 kHz. The duty cycle of the switch is around 0.69. The key parameters of the prototype are listed as in Table II. A picture of the prototype is shown in Fig. 14.

Fig. 15 shows the driving signal and the drain-to-source voltage of the switch. It can be seen that extreme duty cycle is avoided. The voltage stress of the switch is at around 68 V, which matches the calculation from (29). Fig. 16 shows the voltages of the diodes. As can be seen, the blocking voltages of D_1 and D_2 are around 68 and 200 V, respectively, which match the calculations from (30) and (31). Fig. 17 shows that the input voltage

$$C_1 = \frac{(1+(n+1)\,D)\,(n+1)\,DP_o}{\delta_c\%{V_o}^2 f_s} > 10.7\ u\text{F} \tag{61}$$

$$C_2 = \frac{(1+(n+1)\,D)\,(n+1)\left((n+2)^2D+(n+1)\,(1-D)^2\right)P_o}{\delta_c\%(n+2)^2D{V_o}^2 f_s} > 17.4\ u\text{F} \tag{62}$$

$$C_o = \frac{(n+2)^2\left((n+2)^2D+(n+1)\,(1-D)^2\right)P_o}{\delta_c\%{V_o}^2 f_s} > 1.3\ u\text{F} \tag{63}$$

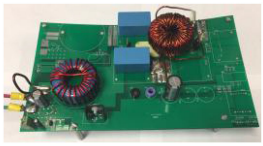

Fig. 14. Picture of the prototype.

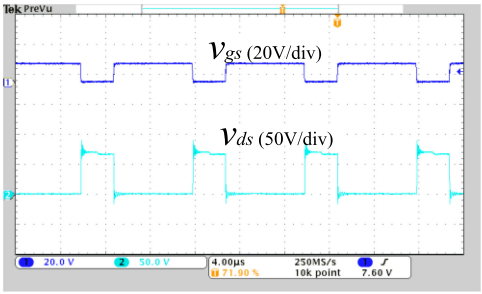

Fig. 15. Driving signal and drain-to-source voltage of the switch.

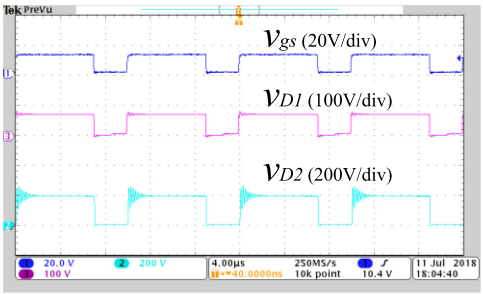

Fig. 16. Voltages across the diodes.

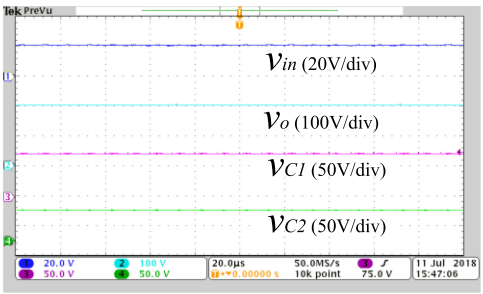

Fig. 17. Input and output voltages and the capacitor voltages.

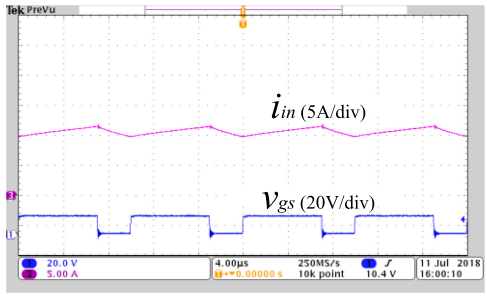

Fig. 18. Input current.

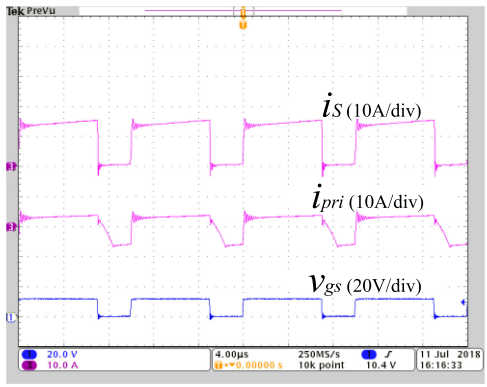

Fig. 19. Switch current and the primary current of the coupled inductor.

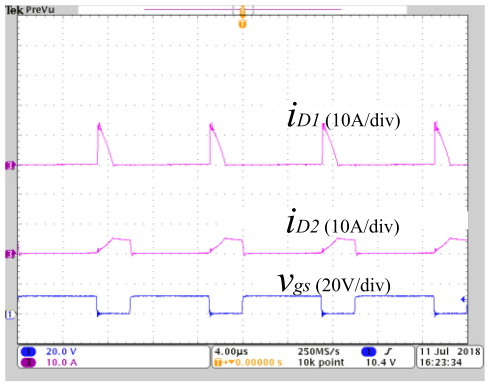

Fig. 20. Diode currents.

is 20 V and the output voltage is 200 V. The capacitor voltages V_{C1} and V_{C2} are around 68 and 48 V, respectively, which are consistent with the calculations from (27) and (28). Fig. 18 shows the input current. It can be seen that continuous input current is achieved. Fig. 19 shows the switch current and the primary current of the coupled inductor, which are consistent with the theoretical analysis. Fig. 20 shows the currents through the diodes. It can be seen that reverse recovery problems of the diodes are alleviated.

A theoretical loss analysis is performed based on the selected components of the hardware prototype. The loss breakdown of the proposed converter at full load is shown in Fig. 21. It can be seen that the loss of the input inductor accounts for the highest percentage as it carries high current. Better-graded wires can be used in the inductor to further improve the efficiency.

The calculated efficiency and the measured efficiency under different output power are shown in Fig. 22(a). The discrepancy is caused by ignoring the leakage inductance, small-ripple assumption, and measurement error. The measured peak efficiency is 94.1%, which is achieved at 125 W. At the full load, the measured efficiency is 93.8%.

The efficiency of the proposed converter is compared to that of the sepic-integrated boost (SIB) converter in [31]. The comparison is made under the same specifications, as given in

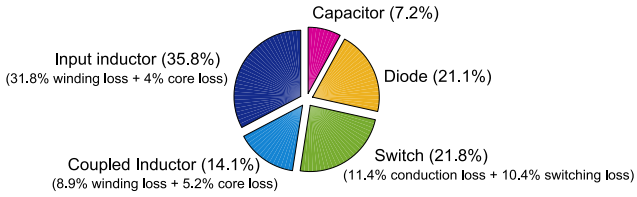

Fig. 21. Loss breakdown.

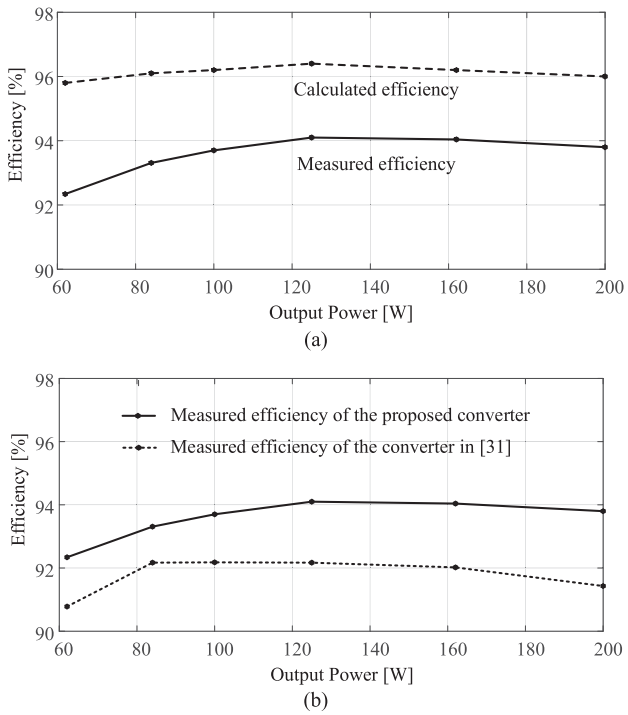

Fig. 22. Efficiency versus output power. (a) Calculated and measured efficiency. (b) Efficiency comparison of the proposed converter and the converter in [31].

Table II. The duty cycles of the two converters are selected to be the same, and then the same switch and the same diodes can be employed in the two implementations. In order to achieve the same voltage gain, the turns ratio of the coupled inductor in the SIB converter is 25:75. The measured efficiency curves are provided in Fig. 22(b). As can be seen, the proposed converter achieves higher efficiency than the SIB converter. This is because the coupled inductor in the proposed converter carries lower current, leading to lower winding loss. Also, due to the higher step-up capability of the proposed converter, the turns ratio is lower. Hence, less copper is used, which further reduces the winding loss. Besides, lower turns ratio of the coupled inductor results in smaller leakage inductance, which also contributes to lower conduction loss.

The power density of the converters largely depends on the size of the magnetic components, as they contribute to a significant portion of the total volume. The input inductors in the two converters have the same size under the same specifications. The coupled inductor in the proposed converter has lower current stress and lower number of turns under given conditions, leading to a smaller core geometrical constant K_g [42]. Hence, the proposed converter has a smaller coupled-inductor size compared to the SIB converter, leading to higher power density.

VI. Conclusion

A single-switch high step-up coupled-inductor boost converter has been proposed. The proposed converter has advantages such as high-voltage gain, low switch voltage stress, and continuous input current, which makes it suitable in battery, fuel cell, and PV applications. The performance analysis and design considerations have been presented. Experimental results have verified the theoretical analysis.

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