Analysis and Design of *LLC* Converter Considering Output Voltage Regulation Under No-Load Condition

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***Abstract*—In the no-load condition, *LLC* converter usually fails to regulate its output voltage although it operates at a high switching frequency. Till now, it is hard to obtain the exact relationship between design parameters and the maximum switching frequency for no-load regulation capability. In this paper, a specific criterion for no-load regulation of *LLC* converter is provided, without using active components or other modulation schemes. By analyzing the macroscopic switching period and microscopic switching transition in the no-load condition, it is shown that not only the peaking resonant current during the switching transition, but also the resonant tank design affect the no-load regulation of the *LLC* converter, which affects the no-load regulation capability. Furthermore, the relationship among design parameters is analyzed and the design guideline is also provided to achieve no-load regulation at the specified maximum switching frequency. To verify the effectiveness of the proposed design, 400 V input and 50 V/200 W output prototype is built and tested.**

***Index Terms*—DC-DC power converter, LLC converter, no load regulation.**

I. Introduction

NOWADAYS, *LLC* converter in Fig. 1 is one of the most promising dc-dc converter topologies in various applications [1]–[22]. This is because *LLC* converter has soft switching characteristics and small number of components. Usually, the voltage gain of *LLC* converter is determined by the turns ratio of the transformer in a nominal input voltage condition, because *LLC* converter is designed to operate at the resonant frequency maximizing its efficiency. However, the voltage gain usually increases in a light load condition resulting in a high switching frequency, high switching turnoff losses, and incapability of output voltage regulation. Since the importance of the light/no-load operation is increasing nowadays, the research on *LLC* converter in the no-load condition is also essential.

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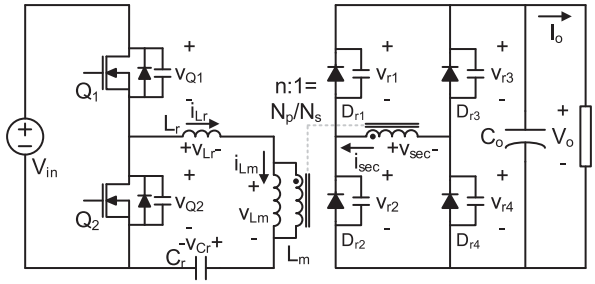

Fig. 1. *LLC* resonant converter.

In a light/no-load condition, the peaking resonant current during the switching transition is well known as the main cause of regulation problem [12], [13]. In order to beat this problem, many researchers proposed various solutions. Solutions for the light-load condition can be divided into modifying modulation [14]–[17] and utilizing additional components [18], [19]. Modifying modulation utilized phase-shifted [14]–[16] or modified synchronous rectifier signals [17] to achieve light-load regulation. Adding components utilized to suppress the peaking resonant current [18] or to provide discharging path of excessive output charges from the switching transition [19]. From these, it can be noted that the no-load regulation of *LLC* converter is an important issue to be solved.

However, it is still difficult to obtain exact analysis and design criterion till now. The explicit solution for the maximum switching frequency and the design procedure are not investigated. Additionally, there was no research on the effect of the resonant tank design in the no-load condition. In this paper, a specific criterion for no-load regulation of *LLC* converter is provided. By analyzing the macroscopic switching period and microscopic switching transition in the no-load condition, it is shown that not only the peaking resonant current during the switching transition, but also the resonant tank design affects the no-load regulation of *LLC* converter. The relationship between design parameters is analyzed and the design guideline is also provided to achieve no-load regulation at the specified maximum switching frequency, without using active components or other modulation schemes. It is shown that the switching frequency, magnetizing and resonant inductance, resonant capacitor, output capacitors of main switches, junction capacitors of rectifier diodes, and also other parasitic capacitors in *LLC* converter are all related to the no-load regulation requirement. Finally, an explicit condition for no-load regulation has been derived and verified.

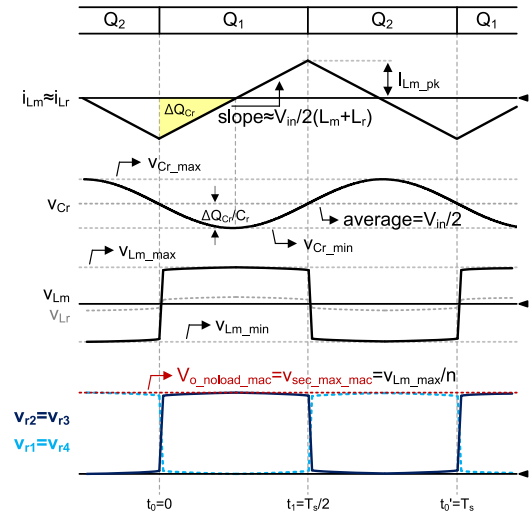

Fig. 2. Macroscopic switching period waveforms without parasitic capacitors at no-load condition.

II. Analysis in No-Load Condition

A. Macroscopic Switching Period Analysis

Fig. 2 represents the switching period waveforms of *LLC* resonant converter at no-load condition. In order to focus on the effect of the ripple voltage of the resonant capacitor, the effect of parasitic capacitors of the main switches and rectifier diodes is neglected in this section. Additionally, the leakage inductance is ignored in this paper to provide simple intuition. In order to analyze macroscopically, the switching period is divided into two modes where the main switches Q_1 and Q_2 are turned ON for a half switching period $T_s/2$ alternately. Effects of the output and junction capacitors of main switches and rectifier diodes will be studied in the next section. Since two modes are symmetric, only one mode where Q_1 is turned ON is analyzed. In the no-load condition, the currents on the magnetizing and resonant inductor i_{Lm} and i_{Lr} become same to each other because the output current is not delivered to the secondary side. In this case, the voltage across the primary side inductors becomes the half of the input voltage V_{in}. Therefore, the current can be regarded as a linearly increasing waveform and its slope becomes $V_{\text{in}}/2(L_m + L_r)$, where L_m and L_r represent the magnetizing and resonant inductance, respectively. In this case, the peak value of the magnetizing current I_{Lm_pk} can be expressed as follows:

$$I_{Lm\_pk} = \frac{V_{in} T_s}{8\,(L_m + L_r)}. \tag{1}$$

The voltage across the resonant capacitor v_{Cr} increases while i_{Lm} is positive, and decreases while i_{Lm} is negative. The minimum voltage on the resonant capacitor $v_{Cr\_\min}$ occurs when i_{Lm} is 0 at $t = T_s/4$, since the current waveform is symmetric. $v_{Cr\_\min}$ can be obtained by integrating i_{Lm} as follows:

$$\begin{aligned} v_{Cr\_\min} &= \frac{V_{\text{in}}}{2} - \frac{1}{C_r}\int_0^{T_s/4} \frac{V_{\text{in}}}{2\,(L_m + L_r)}\, t\, dt \\ &= \frac{V_{\text{in}}}{2} - \frac{V_{\text{in}} {T_s}^2}{64 C_r\,(L_m + L_r)}. \end{aligned} \tag{2}$$

Since the voltage across the magnetizing inductor v_{Lm} becomes $(V_{\text{in}} - v_{Cr})L_m/(L_m + L_r)$, the maximum v_{Lm} occurs when v_{Cr} is the minimum. Additionally, the voltage applied to the secondary side of the transformer v_{sec} becomes the maximum at $t = T_s/4$ [20], [21] as follows:

$$v_{\text{sec}\_\text{max}\_\text{mac}} = v_{\text{sec}}\left(t = \frac{T_s}{4}\right) \tag{3}$$

where $v_{\text{sec}\_\text{max}\_\text{mac}}$ represents the maximum v_{sec} considering the macroscopic switching period analysis. At this point, it can be noted that the output voltage V_o becomes $v_{\text{sec}\_\text{max}\_\text{mac}}$. When $v_{\text{sec}\_\text{max}\_\text{mac}}$ is larger than V_o at $t = T_s/4$, the rectifier diodes D_{r1} and D_{r4} are conducted so that V_o increases to $v_{\text{sec}\_\text{max}\_\text{mac}}$. Therefore, from the macroscopic switching period analysis, the output voltage can be obtained as follows:

$$\begin{aligned} V_{o\_\text{noload}\_\text{mac}} &= v_{\text{sec}\_\text{max}\_\text{mac}} \\ &= \frac{V_{\text{in}}}{2n}\left(1 + \frac{{T_s}^2}{32 C_r\,(L_m + L_r)}\right)\frac{L_m}{L_m + L_r} \end{aligned} \tag{4}$$

where $V_{o\_\text{noload}\_\text{mac}}$ represents the output voltage considering the macroscopic switching period analysis under the no-load condition. Considering that the *LLC* converter is usually designed to operate at the resonant frequency in a nominal state, we can assume the output voltage is designed as $V_o = V_{\text{in}}/2n$. Additionally, in order to achieve the no-load regulation, $V_{o\_\text{noload}\_\text{mac}}$ needs to be smaller than V_o. In this case, rearranging (4) leads to a very simple condition for no-load regulation

$$C_r L_r\left(1 + \frac{L_r}{L_m}\right) > \frac{{T_s}^2}{32}. \tag{5}$$

Furthermore, assuming the switching frequency $f_s(= 1/T_s)$ is equal to α times the resonant frequency $f_r(= 1/2\pi\sqrt{L_r C_r})$, (5) can be further simplified as follows:

$$\alpha > \sqrt{\frac{\pi^2}{8}\left(\frac{1}{1 + L_r/L_m}\right)} \cong 1.11\sqrt{\frac{1}{1 + L_r/L_m}}. \tag{6}$$

At this point, αf_r can be regarded as the switching frequency of the *LLC* converter for no-load regulation according to the macroscopic switching period analysis. From (6), α should be larger than $1.11\sqrt{1/(1 + L_r/L_m)}$. This means that with a given $L_m/L_r(= K)$ value, the switching frequency should be higher than αf_r for no-load regulation considering the macroscopic switching period analysis. However, α cannot be higher than 1.11 because α converges to 1.11 as *K* increases to the infinity.

Therefore, when we set the maximum switching frequency αf_r larger than $1.11 f_r$, the no-load regulation can be achieved regardless of the *K* value, considering only the macroscopic switching period analysis.

B. Microscopic Switching Transition Analysis

In previous research works, it is reported that the junction capacitors of the rectifier diodes cause a peaking current on L_r during the switching transition at $t = 0$ and $T_s/2$. In the no-load condition, this peaking current is delivered to the output capacitor causing the regulation problem. To verify further, the

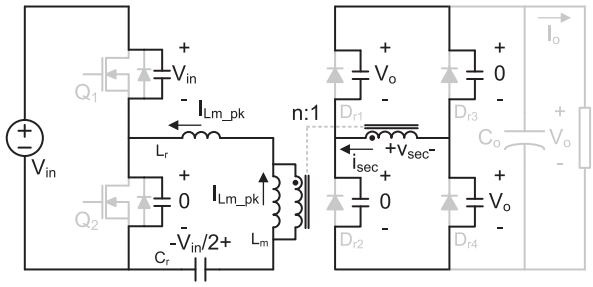

Fig. 3. Initial condition of the switching transition at $t = 0$.

switching transition in Fig. 2 at $t = 0$ is analyzed in detail. To avoid complexity, assumptions are made as follows.

A1) The output capacitances of main switches are identical as $C_{\rm oss}$.

A2) The junction capacitances of rectifier diodes are also identical as C_j.

A3) $i_{Lm}(0)$ and $i_{Lr}(0)$ are equal each other as I_{Lm_pk} at $t = 0$. $i_{Lm}(0)$ remains constant during the switching transition.

A4) C_r is much larger than $C_{\rm oss}$ or C_j so that it can be regarded as a voltage source of $V_{\rm in}/2$ during the switching transition.

A5) Voltage across rectifier diodes D_{r2} and D_{r3} (v_{r2} and v_{r3}) is 0 at $t = 0$, assuming that the ripple voltage on the resonant capacitor C_r is small to be neglected. Accordingly, voltage across the other rectifier diodes D_{r1} and D_{r4} (v_{r1} and v_{r4}) can be regarded as V_o at $t = 0$. Additionally, by making C_r infinity in (4), V_o can be simplified as follows:

$$V_o = \frac{L_m V_{\rm in}}{2n\left(L_m + L_r\right)}. \tag{7}$$

In the case $L_m >> L_r, V_o$ becomes $V_{\rm in}/2n$ in (7), and $nV_o = V_{\rm in}/2$.

A6) During the switching transition, the difference between i_{Lm} and i_{Lr} is much smaller than I_{Lm_pk}. i_{Lm} is constant during the switching transition.

Figs. 3 and 4 represent the initial condition of the switching transition at $t = 0$ and its equivalent circuits. From A1 to A5, the initial condition can be presented with the circuit in Figs. 3 and 4(a). The equivalent circuit in Fig. 4(a) can be expressed as Fig. 4(b) with independent voltage/current sources. From A3, the current sources can be merged into one current source as shown in Fig. 4(c). From A6, it can be assumed that most current from the current source flows into $2C_{\rm oss}$, so that the left-hand side of the circuit can be virtually separated from the right-hand side as shown in Fig. 4(d). In this case, $2C_{\rm oss}$ can be approximated as a ramp voltage source, which increases from zero to $V_{\rm in}$ during the switching transition as shown in Fig. 4(e). When we assume $L_m >> L_r$ and i_{Lm} is not varying during the switching transition according to A5 and A6, the voltage sources $V_{\rm in}/2$ and nV_o in Fig. 4(e) can be canceled out and the simplified equivalent circuit can be obtained as shown in Fig. 4(f). Considering nV_o dc source in Fig. 4(e), the voltage across the junction capacitor C_j/n^2 will increase from zero to $2nV_o$. Then, $v_{\rm sec}$ becomes V_o so that D_{r1} and D_{r4} are conducted and the switching transition

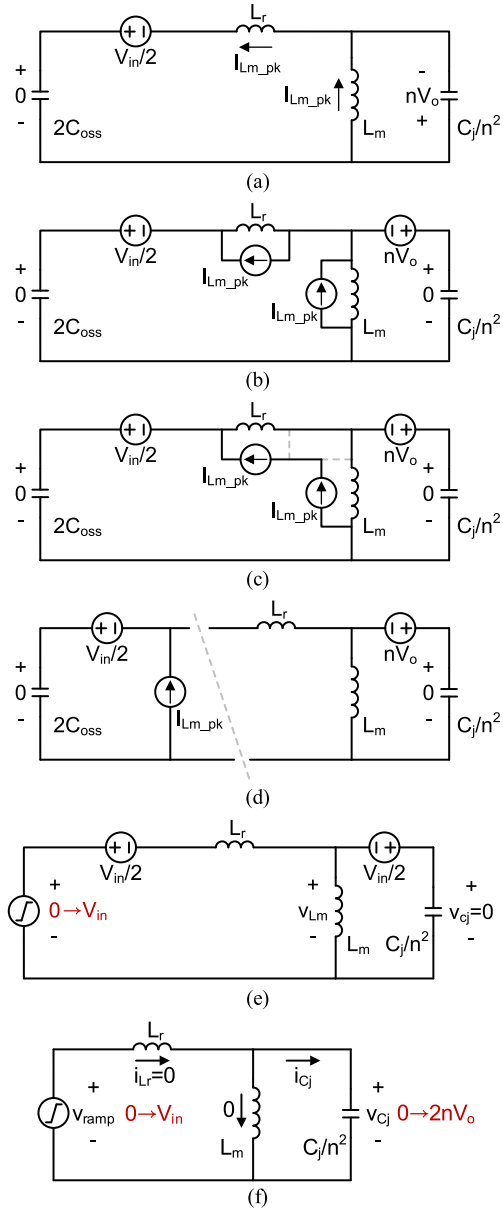

Fig. 4. Equivalent circuits for the initial condition of the switching transition at $t = 0$. (a) Initial condition. (b) Expression with independent sources. (c) Current source merging. (d) Current source separation. (e) Substituting current source to a ramp voltage source. (f) Simplified equivalent circuit.

ends at this moment. During the transition, v_{r1} and v_{r4} decrease from V_o to zero and v_{r2} and v_{r3} increase from zero to V_o. The general relationship between v_{Cj} and $v_{\rm sec}$ can be obtained from Fig. 4(e) as follows:

$$v_{\rm sec} = \frac{v_{Lm}}{n} = \frac{1}{n}\left(v_{Cj} - nV_o\right). \tag{8}$$

From the ac equivalent circuit, we can reach several understandings about the peaking L_r current during the switching transition.

1) The switching transition begins with the voltage transition in the primary side, and the voltage transition can be regarded as a ramp voltage source.

2) Although the voltage varies in the primary side, the voltage across the junction capacitors remain the same because the primary side current flows into $2C_{\rm oss}$ as shown in Fig. 4(c).
3) This makes the voltage difference between the primary side and the secondary side, and the voltage difference is applied to L_r, resulting in the peaking current during the switching transition.
4) By the ramp voltage source, the junction capacitors are charged and discharged according to *LC* resonant circuit in Fig. 4(f). The peaking current on L_r is produced by the resonance.
5) At the moment the voltage across the junction capacitors reaches $2nV_o$, when the rectifier diodes conduct, the peaking current on L_r will be delivered to the output capacitor, increasing the output voltage.
6) In the no-load condition, the output voltage will increase until the output current is not delivered to the output capacitor.
7) The voltage and current of the junction capacitor v_{Cj} and i_{Cj} can be obtained from the *LC* resonant circuit in Fig. 4(f). First, the ramp voltage source $v_{\rm ramp}$ can be expressed as follows:

$$v_{\rm ramp}(t) = \frac{1}{2C_{\rm oss}} \int_0^t I_{Lm\_pk} dt = \frac{I_{Lm\_pk}}{2C_{\rm oss}} t. \quad (9)$$

The duration of the ramp voltage source $T_{\rm ramp}$ can be expressed by $v_{\rm ramp}(T_{\rm ramp}) = V_{\rm in}$ as follows:

$$T_{\rm ramp} = \frac{2V_{\rm in}C_{\rm oss}}{I_{Lm\_pk}}. \quad (10)$$

Additionally, v_{Cj} and i_{Cj} can be expressed from Figs. 4(f) and (9) as follows:

$$v_{Cj}(t) = v_{r2} = v_{r3} = \frac{L_m}{L_m + L_r} \frac{I_{Lm\_pk}}{2C_{\rm oss}} \left[t - \frac{1}{\omega} \sin(\omega t) \right] \quad (11)$$

$$i_{Cj}(t) = \frac{L_m}{L_m + L_r} \frac{C_j/n^2}{2C_{\rm oss}} I_{Lm\_pk} \left[1 - \cos(\omega t) \right] \quad (12)$$

where $I_{Lm\_pk} = V_{\rm in}T_s/8(L_m + L_r), L_m//L_r = L_mL_r/(L_m + L_r)$, and $\omega = 1/\sqrt{(L_m//L_r)C_j/n^2}$. v_{Cj} and i_{Cj} at $T_{\rm ramp}$ can be obtained by substituting $t = T_{\rm ramp}$, (8), and (10) into (11) and (12) as follows:

$$v_{Cj}(T_{\rm ramp}) = 2nV_o - \frac{L_m}{L_m + L_r} \frac{1}{\omega} \sin(\omega T_{\rm ramp}) \quad (13)$$

$$i_{Cj}(T_{\rm ramp}) = \frac{L_m}{L_m + L_r} \frac{C_j/n^2}{2C_{oss}} I_{Lm\_pk} \left[1 - \cos(\omega T_{\rm ramp}) \right]. \quad (14)$$

At this point, when $T_{\rm ramp} = 2\pi/\omega = T_{\rm res}$, which means $T_{\rm ramp}$ is equal to the resonant period of C_j during the switching transition, (13) and (14) become as follows:

$$v_{Cj}(T_{\rm ramp})|_{T_{\rm ramp}=2\pi/\omega} = 2nV_o \quad (15)$$

$$i_{Cj}(T_{\rm ramp})|_{T_{\rm ramp}=2\pi/\omega} = 0. \quad (16)$$

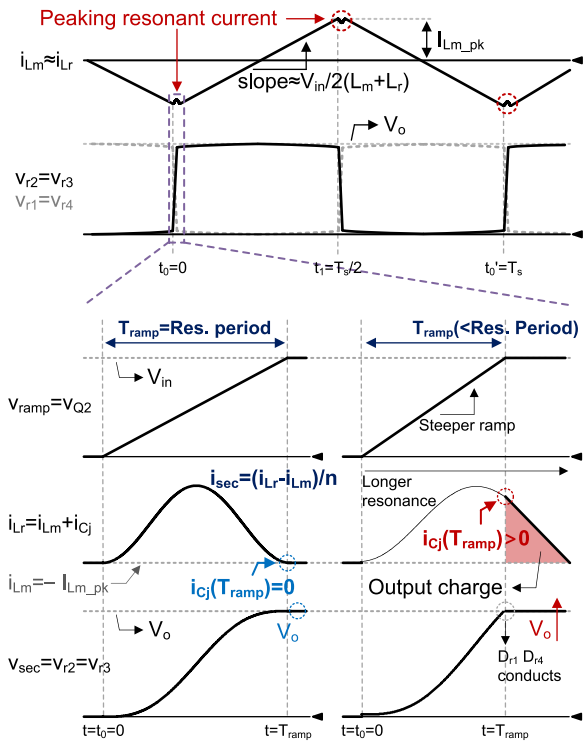

Fig. 5. Comparative zoomed in waveforms of the peaking current on L_r during the switching transition in the case of $T_{\rm ramp} = T_{\rm res}$ (left) and $T_{\rm ramp} < T_{\rm res}$ (right).

Equations (15) and (16) indicate that the peaking resonant current during the switching transition becomes *zero* when the voltage across C_j/n^2 and D_{r2} reach $2nV_o$ and V_o, respectively. From now, the resonant period of the peaking resonant current during the switching transition is called $T_{\rm res}$.

On the other hand, when $T_{\rm ramp} \neq T_{res}$, $i_{Cj}(T_{\rm ramp})$ becomes larger than zero since $1 - \cos(\omega T_{\rm ramp})$ term in (14) is always larger than zero except the case $T_{\rm ramp} = T_{\rm res}$.$v_{Cj}(T_{\rm ramp})$ still can be assumed as $2nV_o$ in the case $\omega >> 1$ in (11) as follows:

$$v_{Cj}(T_{\rm ramp})|_{T_{\rm ramp} \neq T_{\rm res}} \sim 2nV_o = \frac{L_m}{L_m + L_r} V_{\rm in} \quad (17)$$

$$i_{Cj}(T_{\rm ramp})|_{T_{\rm ramp} \neq T_{\rm res}} > 0. \quad (18)$$

Fig. 5 represents comparative zoomed in waveforms at the switching transition in the case of $T_{\rm ramp} = T_{\rm res}$ and $T_{\rm ramp} < T_{\rm res}$ according to (11) and (12). From Fig. 5, $v_{\rm ramp}$ is the ramp voltage, which is equal to v_{Q2}, the voltage across switch Q_2. i_{Lr} becomes $i_{Lm} + i_{Cj}$. Considering (12), i_{Cj} is proportional to 1–cos(ωt). Additionally in (11), v_{Cj} is proportional to t–sin(ωt)/ω. As mentioned before, while v_{Cj} increases from zero to $2nV_o$, v_{r2} and v_{r3} increase from zero to V_o. On the left-hand side of Fig. 5, in the case of $T_{\rm ramp} = T_{\rm res}$, i_{Cj} becomes zero and i_{Lr} becomes equal to i_{Lm} at the moment v_{r2} and v_{r3} reaches V_o. Therefore, the output current is not delivered to the secondary side, and the output voltage does not increase in this condition. The right-hand side of Fig. 5 represents the case of $T_{\rm ramp} < T_{\rm res}$. In this case, i_{Cj} still remains although v_{r2} reaches V_o due to either a steeper v_{Q2} or a longer resonant period of C_j. The remained

i_{Cj} is delivered to the output capacitor increasing V_o. The output voltage will be increased up to the peak voltage of the resonance, till the output charge cannot be delivered to the output capacitor. In the case of $T_{\rm ramp} > T_{\rm res}$, the same phenomena can be found since $i_{Cj}(T_{\rm ramp}) > 0$.

For these reasons, when *the duration of the primary side voltage transition is equal to the resonant period of the junction capacitor, the output voltage does not increase* and remains at $V_o = V_{\rm in}/2n$. At this point, the condition for the no-load regulation can be obtained according to the switching transition analysis. Substituting $t = 2\pi/\omega$ and $\omega = 1/\sqrt{(L_m//L_r)C_j/n^2}$ into (8) and (11) leads to the condition for the no-load regulation capability as follows:

$$16C_{\rm oss}\left(L_m + L_r\right) f_{s\_\max\_\rm mic} = 16C_{\rm oss}\left(L_m + L_r\right)\beta f_r = 2\pi\sqrt{\left(L_m//L_r\right)C_j/n^2} \quad (19)$$

where $f_{s\_\max\_\rm mic} = \beta f_r$ represents the maximum switching frequency of *LLC* converter considering the microscopic switching period analysis under the no-load condition.

C. Further Considerations on the Case $T_{\rm ramp} \neq T_{\rm res}$

In real situations, there are many cases of $T_{\rm ramp} \neq T_{\rm res}$. According to (19), it can occur when $C_{\rm oss}, (L_m + L_r)$, and f_s are smaller resulting in a steeper slope of $v_{\rm ramp}$, and/or when $(L_r//L_m)$ and C_j are larger resulting in a longer resonant period.

Fig. 6 represents more detailed zoomed in waveforms when $T_{\rm ramp} = T_{\rm res}$ and $T_{\rm ramp} < T_{\rm res}$. As shown in Fig. 6(a) in the case $T_{\rm ramp} = T_{\rm res}, i_{Lm}(T_{\rm ramp})$ and $i_{Lr}(T_{\rm ramp})$ become equal each other and increasing linearly together so that the assumption A3 holds at the next switching transition. On the other hand, as shown in Fig. 6(b), in the case $T_{\rm ramp} < T_{\rm res}, i_{Lr}(T_{\rm ramp})$ and $i_{Lm}(T_{\rm ramp})$ are not equal and the output voltage is determined according to the peak of the resonance. Since the resonance is still remained after the switching transition, $i_{Lr}(0)$ at the next switching transition is determined according to the resonance and A3 does not hold. The case $T_{\rm ramp} > T_{\rm res}$ is omitted because it shows the same operation with the case $T_{\rm ramp} < T_{\rm res}$ in that $i_{Cj}(T_{\rm ramp}) > 0$. In these cases, it is extremely complicated to obtain the output voltage since all the initial conditions are not zero. One thing we can predict is that the output voltage would be the maximum when $i_{Cr}(T_{\rm ramp})$ is the peak of the resonance.

D. Effect of Other Parasitic Components

Since there are more parasitic capacitors in the *LLC* converter such as winding capacitors of the resonant inductor, transformer, and printed circuit board (PCB), it is required to understand their effects and maximize design accuracy. Fig. 7 represents circuits in the initial condition of the switching transition at $t = 0$ considering other parasitic capacitors. Fig. 7(a) represents connection of parasitic capacitors in the *LLC* resonant converter. C_{Lr}, C_{T_P}, C_{T_S}, and C_P represent the winding capacitor of the resonant inductor, primary side of the transformer, secondary side of the transformer, and primary side PCB winding, respectively. The parasitic capacitance of the secondary side PCB is added parallel to C_j, and it is omitted for simplicity. As shown

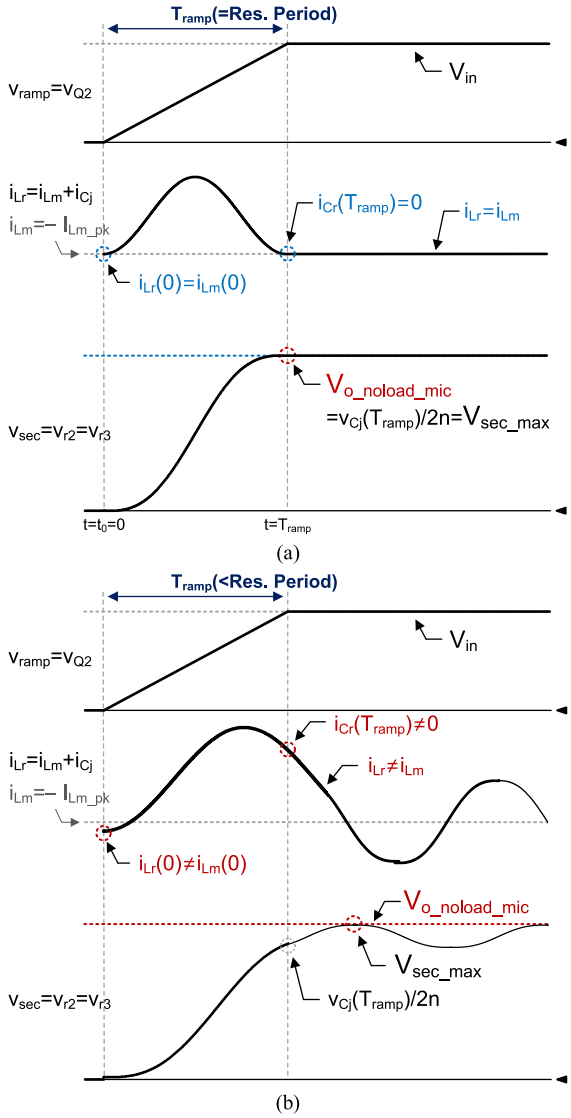

Fig. 6. More detailed zoomed in waveforms of the peaking current on L_r in the case of (a) $T_{\rm ramp} = T_{\rm res}$ (A3 holds) and (b) $T_{\rm ramp} < T_{\rm res}$ (A3 does not hold).

in Fig. 7(a), C_{Lr} is connected to L_r in parallel, C_{T_P} is connected to L_m in parallel, C_{T_S} is connected to the secondary side of the transformer in parallel, and C_P is connected to $C_{\rm oss}$ in parallel. The parasitic capacitance across Q_1 and Q_2 because of PCB layout can be different according to the layout strategy, but they are connected in parallel in ac equivalent circuit so only C_P is presented as the total parasitic capacitor from PCB in this paper. In a similar manner, the parasitic PCB capacitance across the rectifier diodes is also added to C_j, but it is omitted for simplicity. In the experiment, there was no overlapped region in the secondary side rectifier so that the capacitance of secondary side PCB becomes zero.

Fig. 7(b) represents the equivalent circuit at the beginning of the switching transition. Since C_j, C_{T_P}, and C_{T_S} are all connected in parallel and their initial voltages are all the same, they can be represented similarly with Fig. 4(d). It can be noted that C_j/n^2 in Fig. 4(d) is increased to $C_{T\_P} + (C_{T\_S} + C_j)/n^2$

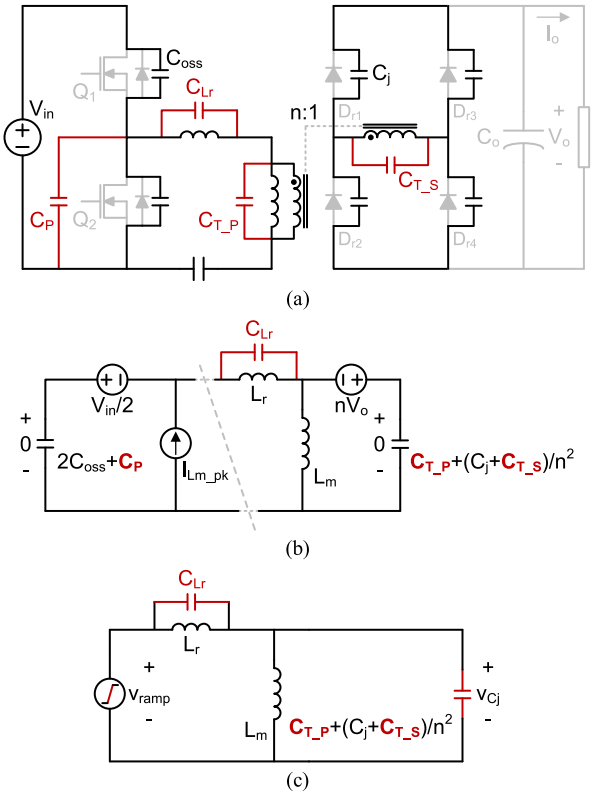

Fig. 7. Circuits in the initial condition of the switching transition at $t = 0$ considering parasitic capacitors. (a) Connection of parasitic capacitors, (b) equivalent circuit, and (c) its simplified equivalent circuit.

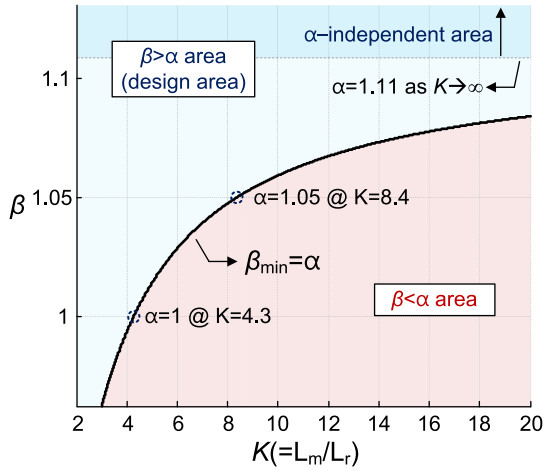

Fig. 8. β design considering $K(= L_m/L_r)$.

in Fig. 6(b). On the other hand, $2C_{\rm oss}$ in Fig. 4(d) is increased to $2C_{\rm oss} + C_P$ since C_P is connected with the output capacitor of Q_2.

Fig. 7(c) represents the simplified equivalent circuit for the initial condition of the switching transition considering C_j, C_{T_P}, C_{T_S}, and C_P. It can be noted that C_{T_P} and C_{T_S} increase the resonant period, and C_P reduce the slope of the ramp voltage, increasing $T_{\rm ramp}$.

The condition for the no-load regulation shown in (19) can be modified considering all aforementioned parasitic capacitors as follows:

$$8\left(2C_{\rm oss}+C_P\right)\left(L_m+L_r\right)f_{s\_\max\_\rm mic} = 2\pi\sqrt{\left(L_m//L_r\right)\left[C_{Lr}+C_{T\_P}+\left(C_{T\_S}+C_j\right)/n^2\right]}. \quad (20)$$

In (20), it should be noted that the left-hand side indicates $T_{\rm ramp}$ and the right-hand side indicates $T_{\rm res}$.

In this paper, the effect of the leakage inductors of the transformer is ignored in order to provide a simple intuition and avoid complexity in the resonant circuit. In some cases, since the leakage inductor plays the role of the resonant inductor, the leakage inductor is designed to be larger using a separate winding technique. In this case, the resonant circuit used in the analysis becomes different since the leakage inductor in the secondary side is unneglectable. However, even in this case, the no-load regulation can also be achieved with the same criterion that the output current is not delivered to the output capacitor, if the resonant current becomes zero when $v_{\rm sec}$ reaches $V_{\rm out}$.

D. No-Load Regulation Criteria With the Specified Maximum Switching Frequency

The output voltage under the no-load condition $V_{o\_\rm noload}$ is determined as a larger value between $V_{o\_\rm noload\_mac}$ and $V_{o\_\rm noload\_mic}$, where $V_{o\_\rm noload\_mic}$ represents the maximum v_{r2} value during the switching transition. Therefore, both (6) and (20) should be satisfied at the maximum switching frequency $f_{s\_\max}$. In order to satisfy both conditions, $f_{s\_\max}$ needs to be larger than αf_r considering the macroscopic switching period analysis. Additionally, the switching frequency should be βf_r exactly, considering the microscopic switching transition analysis. Therefore, in order to satisfy both conditions, β should be larger than α, and α becomes the minimum β ($\beta_{\rm min}$). The switching frequency in the no load condition will be βf_r.

Fig. 8 represents β design considering $K(= L_m/L_r)$. The black solid line represents α according to K from (6). The blue and red shaded areas represent $\beta > \alpha$ and $\beta < \alpha$ area, respectively. β should be selected in the blue-shaded area. Additionally, according to (6), α converges to 1.11 as K increases to infinity. Therefore, if β is larger than 1.11, then α does not need to be considered in the design criteria. Finally, the analysis can be concluded with the no-load regulation criteria.

When β is larger than α and (20) holds, $V_{o\_\rm noload}$ can be remained as $V_{\rm in}/2n$ at $f_s = \beta f_r$. If β is larger than 1.11, then $\beta > \alpha$ always holds, and α does not need to be considered.

III. Design Guidelines and Examples

A. Turns Ratio of the Transformer, n

In order to verify the effectiveness of the analysis, two design examples are provided in this paper. The prototype I converter has an LED TV specification with 400∼330-V input voltage, 50-V output voltage, and 200-W output power. The converter

TABLE I
DESIGN STEPS AND ACTIONS FOR TWO PROTOTYPES

Steps	Actions	
	Prototype I V_{in}=400~330V with hold up time	***Prototype II*** V_{in}=400V constant input voltage
A. Design n	$n=V_{in}/2V_o=4$	
B. Design f_r, L_r, and C_r	f_r=100kHz, L_r=115μH, and C_r=22nF	
C. Design L_m and calculate α	Wide gain range → small L_m L_m=610μH, α=1.01	Constant gain → large L_m L_m=1430μH, α=1.07
D. Design switching/magnetic components and extract parasitics	SCT3120AL (C_{oss}=84pF), STPS10H100CG (C_j=185pF) C_P=100pF, C_{Lr}=21.2pF, C_{T_P}=20.3pF, C_{T_S}=70.7pF	
E. Calculate T_{res}	$\boldsymbol{T_{res}}=2\pi\sqrt{\left(L_m//L_r\right)\left[C_{Lr}+C_{T\_P}+\left(C_{T\_S}+C_j\right)/n^2\right]}$	
	T_{res}=469ns	**T_{res}=492ns**
F. Select $\beta\sim\beta_{min}(=\alpha)$, calculate T_{ramp}	β=1.1 (>α=1.01) **T_{ramp}=234ns(<<T_{res})**	β=1.2(>α=1.07) **T_{ramp}=546ns(>T_{res})**
G. Approaches for timing matching	For a longer T_{ramp}: (1) increase L_m (2) increase β (3) add C_{oss} For a shorter T_{ramp}: (4) decrease L_m For a longer T_{res}: (5) add C_j/C_{Lr}/C_{T_P}/C_{T_S}	
G. Timing matching: T_{ramp} and T_{res}	**Longer T_{ramp}**/Shorter T_{res} is required. (1) Cannot be used due to the gain range (2) **Increase β**=1.3 (3) **Add C_{oss}** by 141pF **→ T_{ramp}=490ns(~T_{res})**	**Shorter T_{ramp}**/Longer T_{res} is required (4) **Decrease L_m**=1220μH (5) Add C_j/C_{Lr}/C_{T_P}/C_{T_S} **→ T_{res}=489ns(~T_{ramp}=472ns)**
Iteration from C and finalize the design		

operates at 400 V input voltage in the nominal state and operates at 330 V only during the hold-up time when the input line is missed. Therefore, no-load regulation capability of the *LLC* converter is considered only when the input voltage is 400 V. The prototype II converter has fixed 400-V input voltage without hold-up time requirement, 50-V output voltage, and 200-W output power. Table I represents the design steps and actions considering the no-load regulation. The design procedure is provided in following paragraphs. Additionally, Table II represents the design results of two prototype converters.

B. Resonant Frequency, L_r and C_r

The selection of the resonant frequency, L_r, and C_r is the same for two prototypes. The resonant frequency can be selected considering a tradeoff between the size of the magnetic components and switching turn-off losses. When the resonant frequency becomes higher, the size of transformer and L_r can be reduced, whereas switching turn-off losses increase. $f_r = 100\,\text{kHz}, C_r = 22\,\text{nF}$, and $L_r = 115\,\mu\text{H}$ are selected in this example.

C. L_m and α

The most important factor in design of the LLC converter is the range of the gain according to the switching frequency. In this example, the range of gain ($= V_{\text{out}}/V_{\text{in}}$) needs to be from $0.125(= 50/400)$ to $0.152(= 50/330)$. The gain graph of the *LLC* converter can be obtained by the first harmonics approximation as follows:

$$\frac{V_o}{V_{\text{in}}} = \frac{1}{2n\sqrt{\left[1+\frac{1}{K}\left\{1-\left(\frac{f_r}{f_s}\right)^2\right\}\right]^2+\left[\frac{\pi^2}{8n^2}Q\left(\frac{f_s}{f_r}-\frac{f_r}{f_s}\right)\right]^2}} \tag{21}$$

TABLE II
DESIGN RESULT OF THE PROTOTYPE CONVERTERS

Component	Design result	
	Prototype I	***Prototype II***
Transformer	PQ2620, N_p:N_s = 40 (AWG26) : 10 (AWG18 Litz) C_{T_P}=20.3pF, C_{T_S}=70.7pF	
	$\boldsymbol{L_m}$**=610μH**	$\boldsymbol{L_m}$**=1220μH**
L_r	115μH (PQ2016, 25turn, AWG26 2 strands), C_{Lr}=21.2pF	
C_r	22nF/1kV film capacitor	
Q_1, Q_2	SCT3120AL, C_{oss}=84pF	
D_{r1}~D_{r4}	STPS10H100CG, C_j=185pF	
C_{add}	47pF MLCC **3EA** for each main switch	N/A

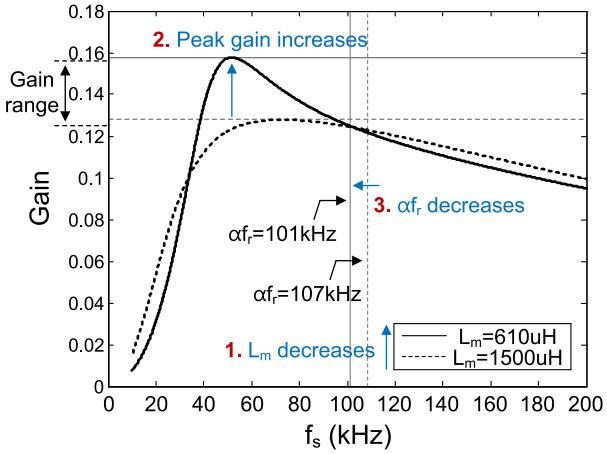

Fig. 9. Gain graph, required gain range at the full-load condition, and αf_r according to different L_m values.

where Q represents $\sqrt{L_r/C_r}/R_o = I_o\sqrt{L_r/C_r}/V_o$ in Fig. 1. From (21), the maximum gain increases as L_m decreases. Fig. 9 represents the gain graph, required gain range, peak gain, and αf_r at the full-load condition according to different L_m values, 610 and 1500 μH. Solid lines represent the case of $L_m = 610\,\mu$H, and dotted lines represent the case of $L_m = 1500\,\mu$H. Two horizontal lines represent the peak gains of the *LLC* converter, and two vertical lines represent αf_r for each L_m values, which was the switching frequency for the no-load regulation considering the macroscopic switching period analysis in (6).

For the first prototype, $L_m = 610\,\mu$H, $L_r = 115\,\mu$H, $C_r = 22$ nF, and $\alpha = 1.01$ are selected to satisfy the gain rage. Here, it can be noted that when the input voltage has a wide range, α is close to the resonant frequency.

When the input voltage range of the *LLC* converter becomes narrow, L_m can be larger to maximize the efficiency with a smaller circulating current. In this case, α increases, and the largest L_m would be limited by the designer's choice on α. This example limits α to 1.07, $L_m = 1500\,\mu$H.

D. Select Switching Components

In order to fix $C_{\rm oss}$ and C_j, the next step is the selection of switching components. In terms of efficiency optimization, $C_{\rm oss}$ and C_j will be changed according to switching components. Accordingly, design steps for no-load condition need to be considered again every time the switching components are changed. In this example, SCT3120AL and STPS10H100CG are selected as the main switches and rectifier diodes for both cases. Since $C_{\rm oss}$ and C_j show nonlinearity according to the voltage across them, total charge related $C_{\rm oss}$ and C_j value can be obtained based on their datasheets as follows:

$$C_{\rm oss}V_{\rm in} = \int_0^{V_{\rm in}} C_{\rm oss\_SCT3120AL}(v)\,dv \tag{22}$$

$$C_jV_o = \int_0^{V_o} C_{j\_\rm STPS10H100CG}(v)\,dv \tag{23}$$

where $C_{\rm oss\_SCT3120AL}(v)$ and $C_{\rm j\_STPS10H100CG}(v)$ represent the output capacitance of SCT3120AL and the junction capacitance according to the voltage across them. In this case, $C_{\rm oss}$ and C_j become 84 and 185 pF, respectively.

E. Obtain Other Parasitic Components and the Resonant Period

After the components design, the next step is to obtain other parasitic components and $T_{\rm res}$. Table II represents the design result and their parasitic components. Parasitic capacitance of magnetic components can be obtained by the self-resonant frequency using a frequency response analyzer. Parasitic capacitance of the PCB can be obtained using a general equation for a capacitance C = εA/d. In this example, $C_P = 100$ pF ($\varepsilon = 4.8$*8.854 pF/m with FR4, A = 7.5 cm^2, and d = 0.32 mm), $C_{Lr} = 21.2$ pF, $C_{T\_P} = 20.3$ pF, and $C_{T\_S} = 70.7$ pF. From the right-hand side of (20), $T_{\rm res}$ for two prototypes are different as 469 and 523 ns due to different L_m values.

F. β and $T_{\rm ramp}$ Calculation

For prototypes I and II, $\beta = 1.1$ and 1.2 are selected to be slightly larger than $\beta_{\min} = \alpha$. For prototype I, $T_{\rm ramp}$ can be calculated as 234 ns according to the left-hand side of (20), and it is much shorter than $T_{\rm res} = 469$ ns. On the other hand, for prototype II, $T_{\rm ramp}$ becomes 546 ns and it is longer than $T_{\rm res} = 492$ ns.

G. Timing Matching: $T_{\rm ramp}$ and $T_{\rm res}$

In order to match $T_{\rm ramp}$ and $T_{\rm res}$, several approaches can be used. For a longer $T_{\rm ramp}$, we can 1) increase L_m, 2) increase β, and 3) add external $C_{\rm oss}$. For a shorter $T_{\rm ramp}$, we can 4) decrease L_m. For a longer $T_{\rm res}$, we can 5) add $C_j/C_{Lr}/C_{T\_P}/C_{T\_S}$. We cannot use smaller β since it is set to its minimum value in Section III-F.

In prototype I, a longer $T_{\rm ramp}$ is required. 1), 2), and 3) can be considered. However, 1) using larger L_m is impossible, because it decreases the peak gain of the *LLC* converter. In this paper, since $T_{\rm ramp}$ is much shorter than $T_{\rm res}$, both (2) and (3) are selected. β is increased to 1.3 and 141 pF $C_{\rm oss}$ is added for each main switch. By doing so, $T_{\rm ramp}$ and $T_{\rm res}$ are matched near 500 ns.

In prototype II, a shorter $T_{\rm ramp}$ or a longer $T_{\rm res}$ is required. 4) and 5) can be considered. Rather than adding additional capacitors, L_m is slightly reduced to 1220 μH. By doing so, $T_{\rm ramp}$ and $T_{\rm res}$ are matched near 500 ns, similar with the prototype I.

The design procedure repeats from Section III-C and it can be finalized as presented in Table II. At this point, we can compare the design results of two cases. In prototype I, when the input voltage range is wide, α becomes smaller so that we can start the design with a small $\beta_{\min}$ value. However, due to a small L_m value for a wide gain range, $T_{\rm ramp}$ becomes too short and it is inevitable to set β larger. When we want to set β smaller value, a large additional $C_{\rm oss}$ needs to be used.

On the other hand, in prototype II, when the input voltage is fixed, α becomes larger and we need to start the design with a larger $\beta_{\min}$ value. However, due to a large L_m value for a high efficiency, $T_{\rm ramp}$ becomes too long and it is inevitable to limit the maximum L_m value.

IV. Experimental Results

A. Experimental Results With the Design

Fig. 10 represents the operating waveforms of prototype I in the no-load condition. Fig. 10(a) represents the switching period waveform. The output voltage is well regulated as 50 V at 130-kHz switching frequency. Although the maximum value of v_{Cj} is 51.2 V, the output voltage is lowered by the forward voltage drop of the circuit. It can be noted that the overall waveforms are well in accordance with the analysis. Assumption A3 holds as i_{Lr} is almost same with i_{Lm}. Since $\alpha = 1.11$, it can be seen that $V_{o\_noload\_mac}$ is lower than the output voltage, because there is no diode conduction at the zero crossing of i_{Lr}. Fig. 10(b) represents microscopic switching transition. As analyzed in (9), the voltage across main switch increases as a ramp function. Additionally, it can be seen that the shape of v_{r2} is a ramp minus sine

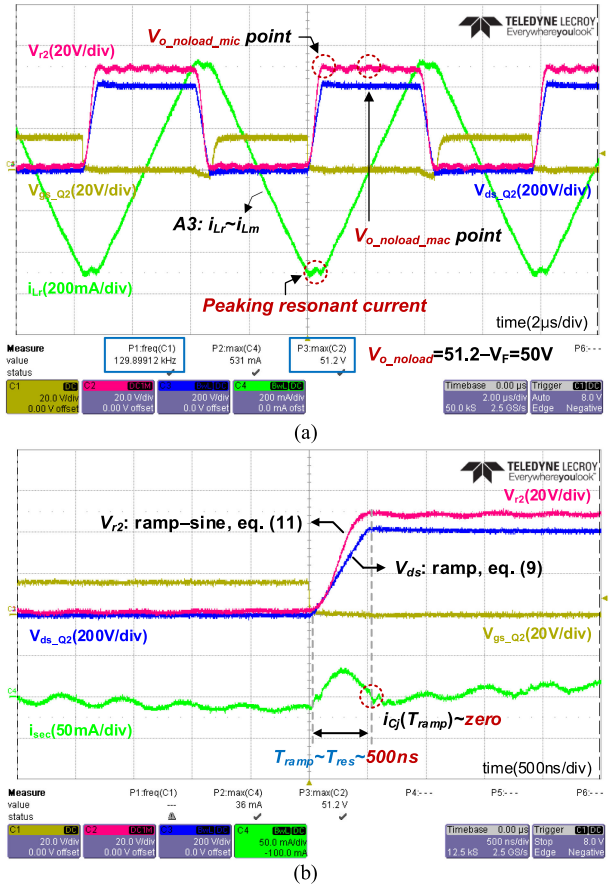

Fig. 10. Operating waveforms of prototype I in the no-load condition. (a) Macroscopic switching period. (b) Microscopic switching transition.

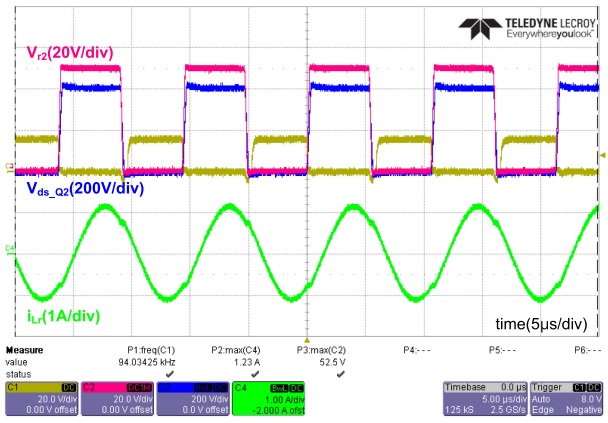

Fig. 11. Operating waveforms of prototype I in 50% (50 V/2 A) load condition.

function as shown in (11). Furthermore, the resonant period of the parasitic components is also well matched with the analysis: about 500 ns resonant period. $T_{\rm ramp}$ and $T_{\rm res}$ are almost same to each other so that the no-load regulation can be achieved at βf_r switching frequency. Therefore, it can be seen that the analysis in this paper is well matched with the experimental results. Fig. 11 represents operating waveforms of prototype I in 50% load condition. As shown here, the prototype is a general *LLC* converter with the resonant point operation.

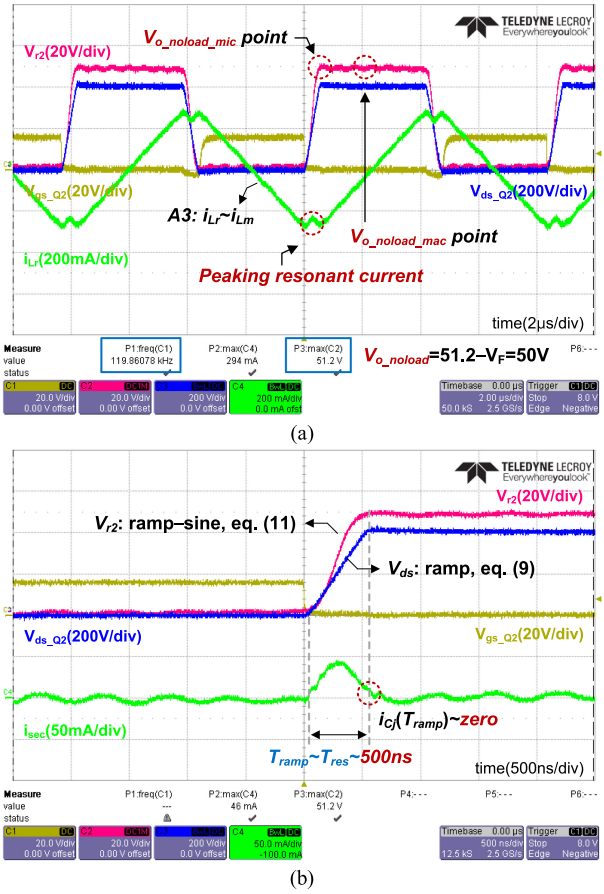

Fig. 12. Operating waveforms of prototype II in the no-load condition. (a) Macroscopic switching period. (b) Microscopic switching transition.

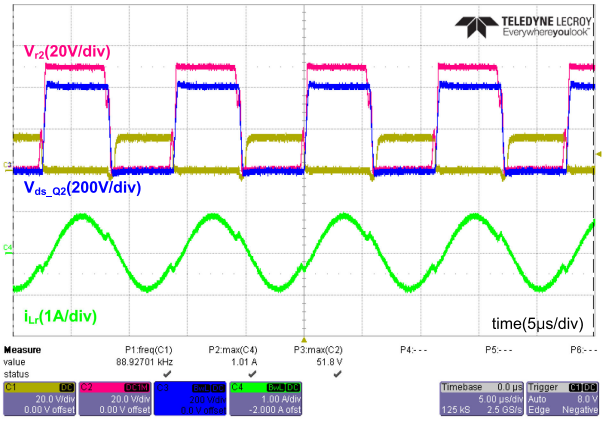

Fig. 13. Operating waveforms of prototype II in 50% (50 V/2 A) load condition.

Figs. 12 and 13 represent the operating waveforms of prototype II. Prototype II does not utilize any additional component. Only design parameters are changed. As shown in Fig. 12(a), since L_m is increased compared to prototype I, circulating current at the no-load condition is decreased. In Fig. 12(b), it can be noted that the resonant period of the parasitic components is also similar to 500 ns as analyzed. The output voltage is also

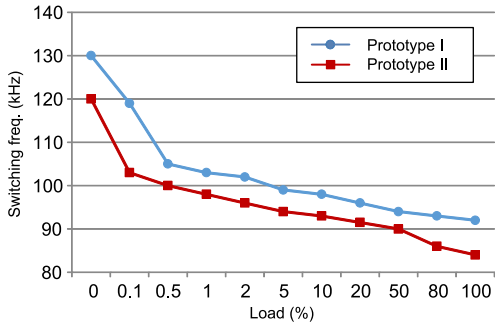

Fig. 14. Switching frequency according to the load condition.

well regulated at a designed maximum switching frequency. Additionally, $T_{\rm ramp}$ is still well matched with $T_{\rm res}$ because L_m is adjusted to satisfy the no-load regulation criterion. Fig. 13 represents operating waveforms of prototype II in 50% load condition. As shown here, the prototype is also a general *LLC* converter with the resonant point operation. Peak-to-peak current swing is decreased in prototype II compared to prototype I, because of a larger L_m.

Fig. 14 represents the switching frequency according to the load condition. As shown here, prototype converters operate near resonant frequency when the output current is large enough. When the load becomes less than 0.5% (1 W), switching frequency increases abruptly. The output voltage is well regulated at 50 V from 100% to zero load condition.

From the design example, it can be seen that, although prototype I has a smaller α than prototype II, β is set to be higher because $T_{\rm ramp}$ is much smaller because of a smaller L_m. With a wide input voltage range, it is hard to match $T_{\rm ramp}$ and $T_{\rm res}$ without using additional components or control methods. However, when the input voltage is fixed, the no load regulation can be achieved without using additional components. Just adjusting L_m can match $T_{\rm ramp}$ and $T_{\rm res}$. The maximum L_m value is limited by the no-load regulation capability.

B. Waveforms in the Case of $T_{\rm ramp} \neq T_{\rm res}$

Fig. 15 represents the operating waveforms of prototype I without timing matching. As shown in Fig. 15(a), when the no load regulation is not achieved, $i_{Lm}(0) \neq i_{Lr}(0)$ and A3 does not hold. In this case, the output voltage is arbitrarily determined according to the resonance of parasitic components, and $V_o > 70$ V in this case. Fig. 15(b) represents the waveforms of microscopic switching transition. $T_{\rm ramp}$ is decreased because the additional capacitors across the main switches are removed, and $T_{\rm ramp} < T_{\rm res}$ in both cases. Therefore, $i_{Cj}(T_{\rm ramp})$ is larger than zero so that the output voltage increases.

Fig. 16 represents the operating waveforms of prototype with $L_m = 1500\,\mu$H at f_s= 130 kHz without additional capacitors. The other parameters are all the same with the prototypes I and II. As shown in Fig. 16(a), A3 does not hold when the no-load condition is not achieved, and $V_o > 60$ V. Additionally, as shown in Fig. 16(b), $T_{\rm ramp}$ is increased to 700 ns, and $T_{\rm ramp} > T_{\rm res}$ in this case. Since we analyzed that i_{Cj} is proportional to $1 - \cos(\omega t)$ in the previous chapter, i_{Cj} increases again after the

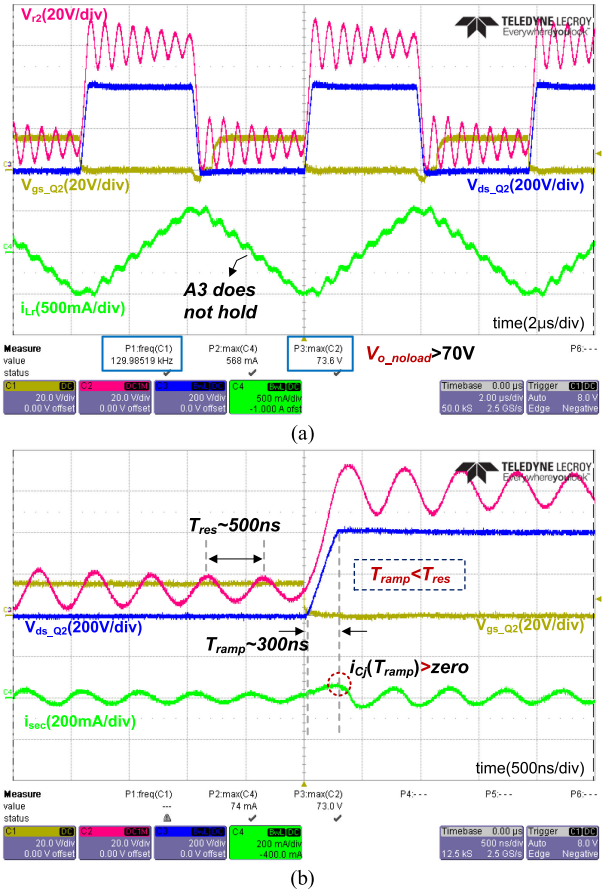

Fig. 15. Operating waveforms of prototype I in the no-load condition WITHOUT timing matching ($\boldsymbol{T}_{\rm ramp} < T_{res}$). (a) Macroscopic switching period. (b) Microscopic switching transition.

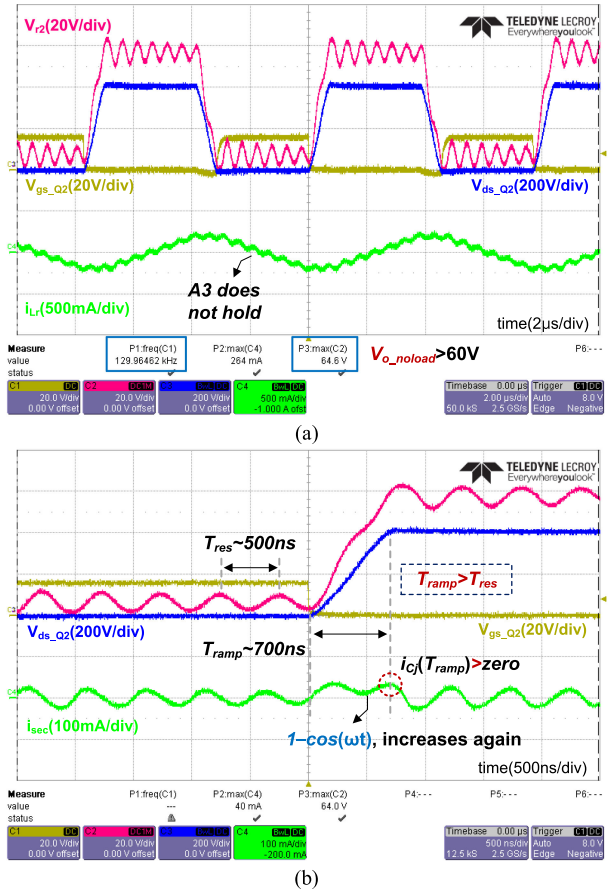

Fig. 16. Operating waveforms of prototype with $L_m = 1500$ μH at $f_r = 130$ kHz ($\boldsymbol{T}_{\rm ramp} > T_{res}$). (a) Macroscopic switching period. (b) Microscopic switching transition.

resonant period. Therefore, $i_{Cj}(T_{\rm ramp})$ is also larger than 0. v_{r2} and the output voltage increases. In this case, in order to match $T_{\rm ramp}$ and $T_{\rm res}$, it is required to add capacitors to the rectifier diodes, not the main switches in order to obtain a longer $T_{\rm res}$ as mentioned in the previous chapter.

At this point, it should be also noted that when the maximum switching frequency is set to be larger than βf_r, the output voltage will increase again. Therefore, the switching frequency from the controller needs to be limited to $f_{s\_\max} = \beta f_r$ exactly.

V. Considerations on Practical Issues

A. Ripple Voltage of Power Factor Correction (PFC) Circuit

In many applications, the *LLC* converter utilizes the output of PFC circuit as the input voltage source and the link capacitor is designed according to the ripple voltage on it. From [23], the peak-to-peak voltage on the link capacitor can be obtained as follows:

$$V_{\rm link\_ptop} = \frac{P_{\rm out}}{2\pi f_L C_{\rm link} V_{\rm link}} \tag{24}$$

where $V_{\rm link\_ptop}, P_{\rm out}, f_L, C_{\rm link}$, and $V_{\rm link}$ represent the peak-to-peak voltage on the link capacitor, output power, input line frequency, link capacitance, and the link voltage, respectively. As shown in (24), $V_{\rm link\_ptop}$ is directly proportional to $P_{\rm out}$, and it can be noted that $V_{\rm link\_ptop}$ becomes zero in the no-load condition. Therefore, although PFC is taken into consideration, the input voltage of the *LLC* converter becomes constant in the no-load condition in accordance with the assumption in the paper.

B. Tolerance of Resonant Tank Components

In this paper, 5% tolerance for C_r and 2% for L_m and L_r are chosen. A 5% tolerance for C_r can increase α by 2.6%. Therefore, since β needs to be larger than α, if we choose β larger than 1.026α, the maximum switching frequency considering the macroscopic switching waveforms is not affected by a 5% tolerance of C_r.

In microscopic switching transition analysis, the voltage across C_r becomes always $V_{\rm in}/2$ regardless of the resonant capacitance. Therefore, tolerance for C_r does not affect the microscopic switching transition. Tolerance for only L_m and L_r affects the macroscopic switching transition causing the mismatch between $T_{\rm ramp}$ and $T_{\rm res}$. From (1) and (10), $T_{\rm ramp} = 16C_{\rm oss}f_s(L_m + L_r) \sim 16C_{\rm oss}f_sL_m$ assuming $L_m >> L_r$. Additionally, from (19), $T_{\rm res} = 2\pi\sqrt{(L_m//L_r)C_j/n^2} \sim 2\pi\sqrt{L_rC_j/n^2}$ assuming $L_m >> L_r$. Therefore, the mismatch becomes the

maximum when L_m is 2% smaller and L_r is 2% larger. In this case, $T_{\rm ramp}{}' = 16C_{\rm oss}f_s 0.98L_m = 0.98T_{\rm ramp}$ and $T_{\rm res}{}' = 2\pi\sqrt{1.02L_rC_j/n^2} \sim 1.01T_{\rm res}$, where $T_{\rm ramp}$ and $T_{\rm res}$ represent ideal ramp and resonant periods, and $T_{\rm ramp}{}'$ and $T_{\rm res}{}'$ represent the ramp and resonant periods in the worst case.

Considering Figs. 4(f) and 5, the excessive charge delivered to C_j/n^2 ($Q_{\rm exc}$) in the worst condition can be approximately expressed from (14) as follows:

$$Q_{\rm exc} = \int_{T_{\rm ramp}{}'}^{T_{\rm res}{}'} i_{Cj}(t)dt = \int_{(1-T_{\rm ramp}{}'/T_{\rm res}{}')2\pi}^{2\pi} i_{Cj}(\theta)d\theta$$
$$\sim \frac{C_j/n^2}{2C_{\rm oss}} I_{Lm\_pk}{}' \int_{1.94\pi}^{2\pi} [1-\cos(\theta)]\, d\theta \qquad (25)$$

where apostrophe represents the actual value considering the tolerance. At this point, it should be noted that the timing mismatch becomes only (2–1.94)$\pi = 0.06\pi$ in radian considering 2% tolerance.

On the other hand, the total amount of charge delivered to C_j/n^2 with zero tolerance ($Q_{\rm ideal}$) can be expressed as follows:

$$Q_{\rm ideal} = \int_0^{T_{\rm res}} i_{Cj}(t)dt = \int_0^{2\pi} i_{Cj}(\theta)d\theta$$
$$\sim \frac{C_j/n^2}{2C_{\rm oss}} I_{Lm\_pk} \int_0^{2\pi} [1-\cos(\theta)]\, d\theta. \qquad (26)$$

It can be noted that the ratio $Q_{\rm exc}/Q_{\rm ideal}$ determines the output voltage variation (ΔV_o) as follows:

$$\Delta V_o = \frac{Q_{\rm exc}}{Q_{\rm ideal}} V_o = \frac{I_{Lm\_pk}{}'}{I_{Lm\_pk}} \frac{\int_{1.94\pi}^{2\pi} [1-\cos(\theta)]\, d\theta}{\int_0^{2\pi} [1-\cos(\theta)]\, d\theta} V_o$$
$$= 1.02 \times 0.03\ {\rm V}_o = 0.031\ {\rm V}_o. \qquad (27)$$

Therefore, it can be noted that 3.1% of output voltage variation, which is an acceptable value, can exist in the case of 2% tolerance on L_m and L_r. When the resonant tank values have tolerance, it is hard to precisely estimate the output voltage because assumption A3 does not holds. However, it can be noted that small tolerance does not affect the regulation capability severely.

C. No-Load Regulation in Lower $V_{\rm in}$ Condition

In many applications, it is required to regulate the output voltage when the input voltage is lower than the nominal value. For example, in prototype I, it is required to regulate the output voltage at 41.25 V when the input voltage is the minimum at 330 V. As analyzed before, the timing matching between $T_{\rm ramp}$ and $T_{\rm res}$ need to be considered. It can be easily noted that $T_{\rm res}$ does not vary according to the input voltage because $T_{\rm res}$ is only related to the parasitic components. Additionally, from the left-hand side of (20), it can be noted that $T_{\rm ramp}$ is also independent to the input voltage. This is because $V_{\rm in}$ is canceled out when (1) and (10) are combined into (20). As a conclusion, the no-load regulation criterion still holds with a lower input voltage condition since both $T_{\rm ramp}$ and $T_{\rm res}$ are independent to the input voltage.

D. Tradeoff for No-Load Regulation

Since the proposed design changes the design of the *LLC* converter, it is required to consider the tradeoff for no-load regulation. It can be found from approaches for timing matching in Table I. There are five actions for timing matching, and they are closely related to the efficiency and the cost of the *LLC* converter. Usually, increasing L_m leads to a smaller circulating current so that the *LLC* converter achieves a higher efficiency. On the other hand, the other methods all increase the losses or cost of the *LLC* converter. Increasing β leads to a higher switching frequency in a very light load condition resulting in larger gate driving and turn-off losses, decreasing L_m leads to large circulating current, and adding additional capacitors increases cost and complexity. In our prototypes, we increased β, added capacitors, and decreased L_m. Therefore, it can be noted that the no-load regulation capability usually decreases the efficiency or increases the cost and complexity of the system. However, since the modification is not so huge, the negative effects of the no-load regulation are usually negligible.

VI. Conclusion

This paper presents analysis and design of *LLC* resonant converter considering no load regulation capability. Considering parasitic components, a specific criterion on the no-load regulation has been derived and verified. As a result, two prototype *LLC* converters were able to achieve no load regulation at the specified/designed maximum switching frequency. It is shown that the "resonant tank design" considering the ripple voltage of resonant capacitor and the "timing matching" considering parasitic components are essential to achieve no-load regulation. $T_{\rm res}$, $T_{\rm ramp}$, and the maximum switching frequency are precisely predicted with the simplified equivalent circuit and parasitic component extraction. The authors wish the analysis and design guideline in this paper would be a help to *LLC* converter design when an engineer needs to set the switching frequency range, resonant tank, and switching components considering no-load regulation.

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